# HMC983LP5E

v02.0112

## DC - 7 GHz FRACTIONAL-N DIVIDER AND FREQUENCY SWEEPER

### Typical Applications

The DC - 7 GHz FRACTIONAL-N DIVIDER is suitable for:

- Test Equipment
- Portable Instruments
- High Performance Fractional-N Frequency Synthesizers with Ultra Low Spurious
- Stand-Alone Divider and/or Delta-Sigma Modulator

### Features

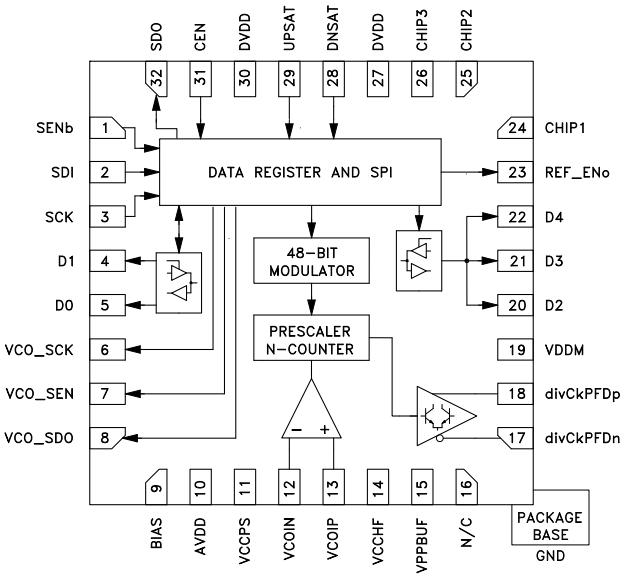
Wideband: DC - 7 GHz Input
-20-bit Frequency Divider

Low Noise: -160 dBc/Hz

Low Spurious: Largest Spurious - 95 dBc

48-bit 100 MHz Delta-Sigma Modulator (DSM)
- Configurable DSM Size
- Programmable Seed
- Phase Step

### Functional Diagram




Product covered by US and Foreign Patents including US Pat. No. 8,531,217.

### Features *(Continued)*

Integrated Frequency Sweeper
- Linear, Coherent Sweeps
- 2-Way, 1-Way, & User Defined Sweep Modes
- Automatic or Triggered
- Programmable Seed
-SPI & External Triggering

5-GPIO's, can be used for External DSM

Cycle Slip Prevention Support with PFD Chip (HMC984LP4E)

Differential VCO Input & Divider Output

Programmable Output Current Control:
-5 mA to 17.5 mA Open Collector Output Driver

32 pin, 5 x 5 mm, LP5 Package

### General Description

DC - 7 GHz FRACTIONAL-N DIVIDER is a fractional frequency divider targeted for fractional-N frequency synthesis, and stand-alone low noise frequency divider applications that require exceptional spurious performance.

Although the DC - 7 GHz FRACTIONAL-N DIVIDER can work with any VCO and/or compatible Phase Detector, best performance and features will be achieved when paired with the companion part, the HMC984LP4E.

Fabricated in SiGe BiCMOS process, the DC - 7 GHz FRACTIONAL-N DIVIDER features a 48-bit Delta Sigma Fractional Modulator (DSM) with programmable phase accumulator size, enabling precise control of frequency step size and resolution. Integrated DSM can generate frequencies with nearly 0 Hz frequency error. The DSM also includes a built-in programmable frequency sweep capability, with various automatic and user defined sweep modes and triggering options, including hardware trigger pin, or SPI trigger with optional delayed trigger.

DC - 7 GHz FRACTIONAL-N DIVIDER is a versatile part capable of various configurations. It has 5 general purpose I/Os (GPIOs). DSM outputs are made available from the GPIO port, enabling the DC - 7 GHz FRACTIONAL-N DIVIDER to import and/or export DSM sequences for various configuration options.

DC - 7 GHz FRACTIONAL-N DIVIDER divider outputs are differential, open collector with programmable current to accommodate different off-chip loads.

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## Table 1. Electrical Specifications

TA = +25 °C, AVDD, VCCPS, VCCHF, VDDM, DVDD = 3 V ± 10%; VPPBUF = 5 V ± 10%; GND = 0 V

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **RF Input Characteristics** | | | | | |
| RF Input Frequency range | | DC | | 7 | GHz |
| RF Input Sensitivity | | -15 | -10 | 0 | dBm |
| RF Input Capacitance | External Match Recommended | | | 3 | pF |
| Divider Range (20-bit) | | | | | |
| Integer Mode | | 32 | | 1,048,575 | |
| Fractional Mode | | 36 | | 1,048,571 | |
| **Divider Output Characteristics** | | | | | |
| Output Buffer Current | Programmable in 2.5 mA Steps | 5 | 12.5 | 17.5 | mA |
| Output Voltage Swing | Single- Ended, Vpullup = 5 V | 0.75 | 1 | 2 | V |
| Output Frequency Range<br>Integer Mode<br>Fractional Mode | Mode A and Mode B | <br>DC<br>DC | | <br>150<br>125 | MHz |
| Phase Noise | 50 MHz PFD, 6 GHz Input, Integer Mode | | -160 | | dBc/Hz |
| Fractional Spurious | Largest observed at 10 kHz Fractional Offset from Integer Boundary | | -95 | -85 | dBc |
| **Logic Inputs** | | | | | |
| Input High Voltage (VIH) | | | | DVDD-0.4 | V |
| Input Low Voltage (VIL) | | 0.4 | | | V |
| **Logic Outputs** | | | | | |
| Output High Voltage (VOH) | | | | DVDD-0.4 | V |
| Output Low Voltage (VOL) | | 0.4 | | | V |
| DC Load | | | | 1.5 | mA |
| Serial Port Clock Frequency | Main SPI and AUXSPI | | | 30 | MHz |
| **Power Supplies** | | | | | |
| AVDD, VCCPS, VCCHF | Analog Supplies. AVDD should be equal to DVDD. | 2.7 | 3 | 3.3 | V |
| VPPBUF | Output Buffer Supply. | 4.5 | 5 | 5.5 | V |
| VDDM, DVDD | Digital Supplies | 2.7 | 3 | 3.3 | V |
| **Current Consumption** | | | | | |
| IDD - Total Current Consumption | Integer Mode / Fractional Mode (50 MHz Divider Output) | | 104 / 122 | | mA |
| I - AVDD (AVDD Current, 3 V) | Integer Mode / Fractional Mode | | 5 / 5 | | mA |
| I - VCCPS (VCCPS Current, 3 V) | Integer Mode / Fractional Mode | | 79 / 79 | | mA |
| I - VCCHF (VCCHF Current, 3 V) | Integer Mode / Fractional Mode | | 8 / 8 | | mA |
| I - VDDM (VDDM Current, 3 V) | Integer Mode / Fractional Mode | | 11 / 11 | | mA |
| I - DVDD (Total DVDD Current, 3 V) | Integer Mode / Fractional Mode | | 1 / 19 | | mA |
| I - VPPBUF (Total VPPBUF Current, 5 V) | | | 5 | | uA |

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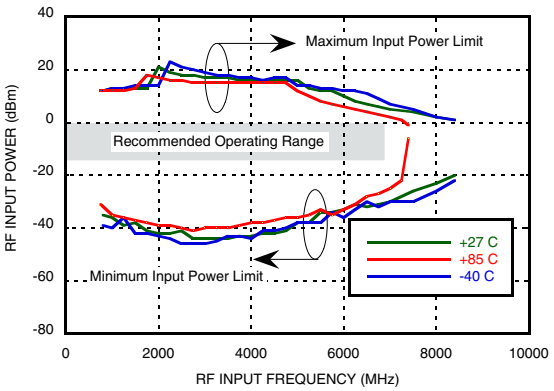
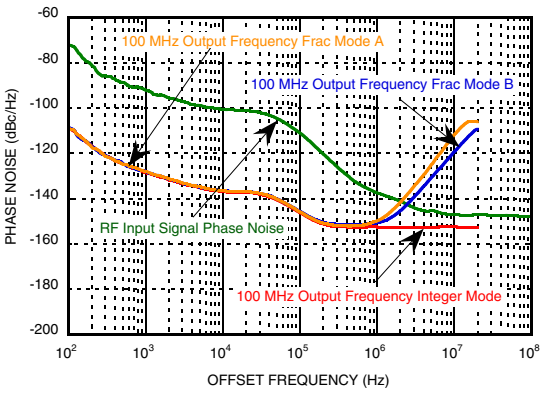
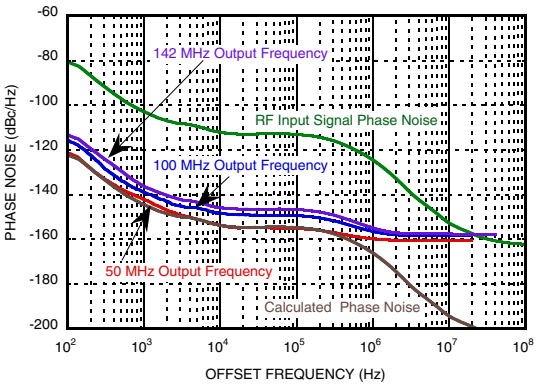
### Figure 1. RF Input Sensitivity [1]



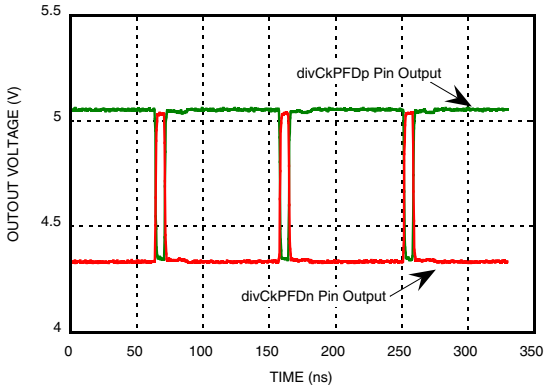

### Figure 2. Output Phase Noise, 6 GHz Input Frequency [2]



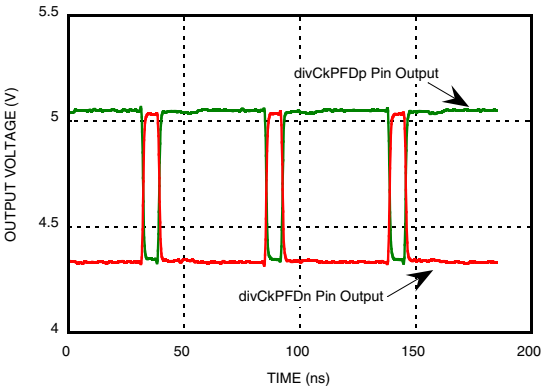

### Figure 3. Output Phase Noise with 6 GHz Input in Integer Mode [3]



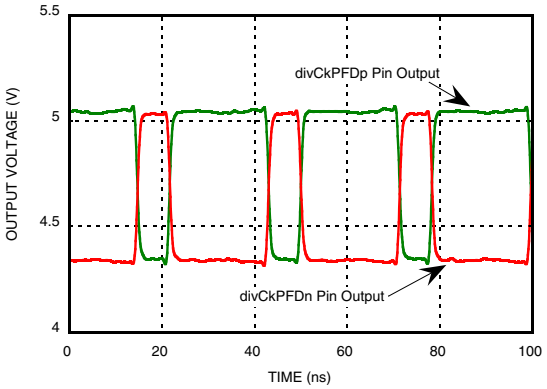

### Figure 4. Time Domain 10 MHz Output, 6.5 GHz Input [4]




### Figure 5. Time Domain 18 MHz Output, 6.5 GHz Input [4]




### Figure 6. Time Domain 35 MHz Output, 6.5 GHz Input [4]




[1] The maximum and minimum levels indicate operational limits of the DC - 7 GHz FRACTIONAL-N DIVIDER. Performance may degrade with input power greater than 0 dBm for frequencies higher than 6500 MHz.

[2] Due to Delta Sigma modulation in fractional mode, the output phase noise peaks at frequency offset of fout/2 from the output. Agilent MXG N5182A used as a signal source.

[3] Rohde & Schwarz SMBV100A used as a signal source.

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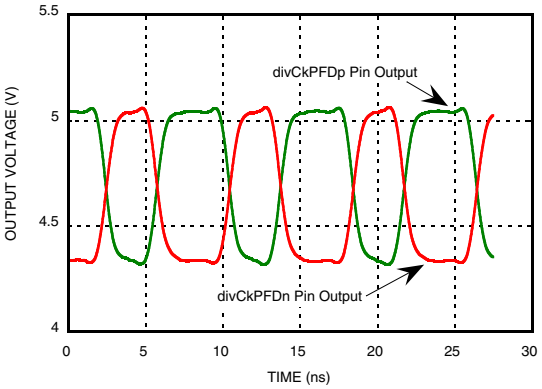
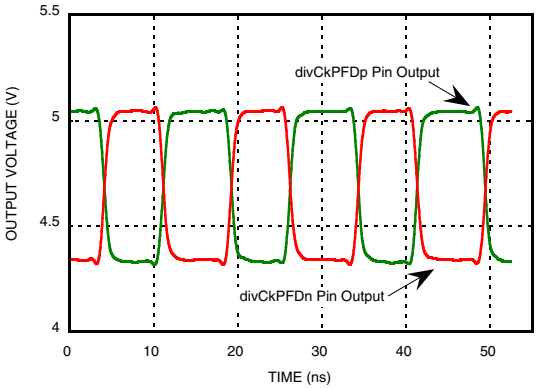
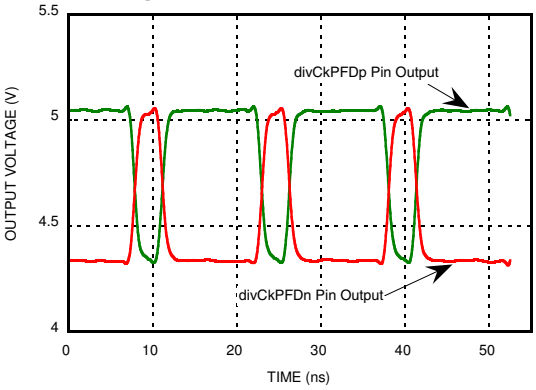
### Figure 7. Time Domain 124 MHz Output, 6.5 GHz Input [5]



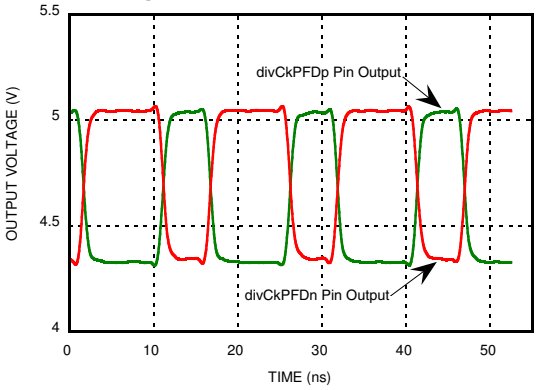

### Figure 8. Time Domain 66 MHz Output, 6.5 GHz Input [5]



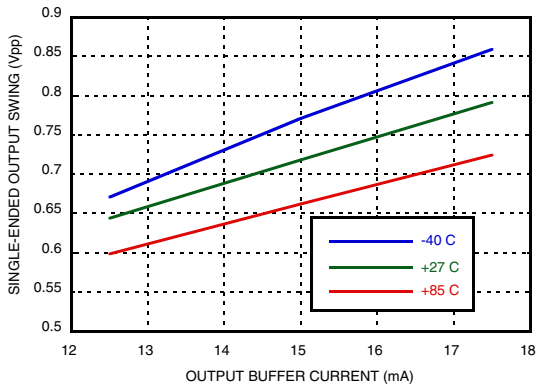

### Figure 9. Time Domain 61 MHz Output, 6.5 GHz Input [5]



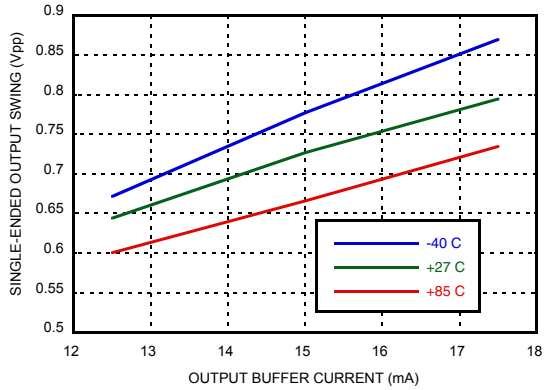

### Figure 10. Time Domain 66 MHz Output, 6.5 GHz Input [5]




### Figure 11. 10 MHz Output Swing vs Buffer Current [6]




### Figure 12. 50 MHz Output Swing vs Buffer Current [6]




[4] Measured with 50 Ω impedance per line, integer Mode, 15 mA Output Buffer Current (Reg 0Fh[4:2]) selected
[5] Measured with 50 Ω impedance per line, integer Mode, 15 mA Output Buffer Current (Reg 0Fh[4:2]) selected

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**Figure 13. 100 MHz Output Swing vs Buffer Current** [7]

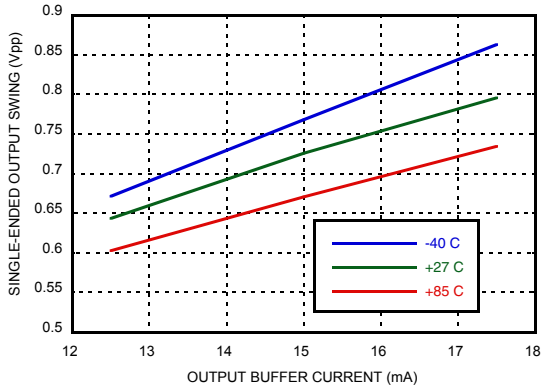



**Figure 14. Input Return Loss**

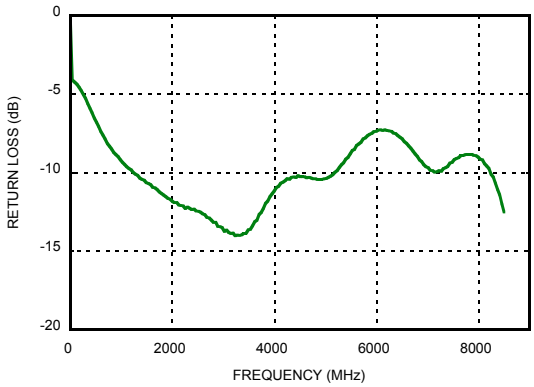



**Figure 15. Two Way Frequency Sweep, 50 MHz PFD** [8]

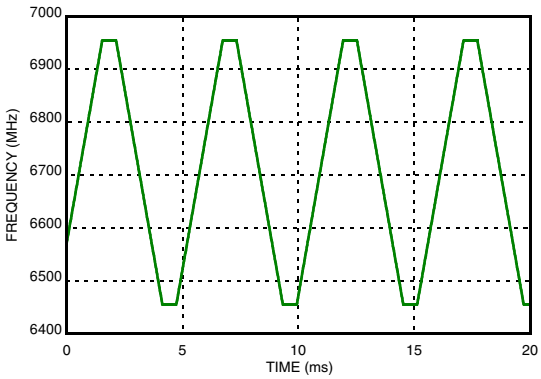



**Figure 16. One Way Frequency Sweep, 10 MHz PFD and 10 Hz external trigger** [8]

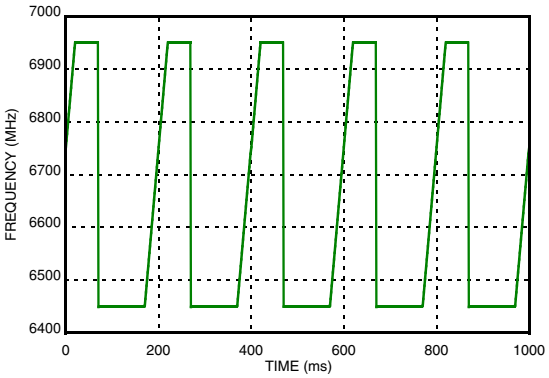



**Figure 17. PLL Cycle Slip Prevention, 100 MHz PFD** [8]

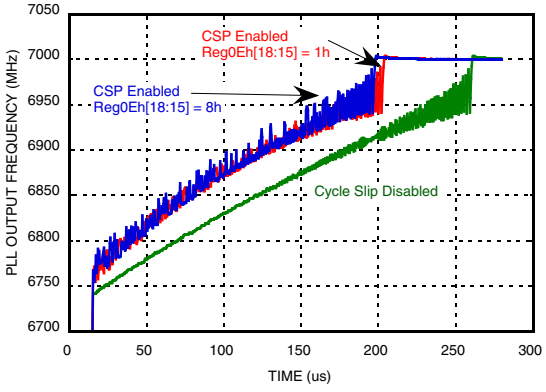
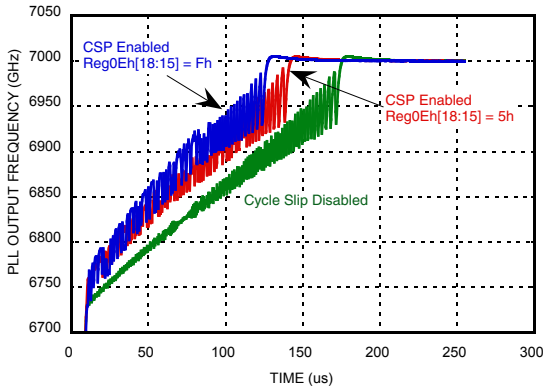



**Figure 18. PLL Cycle Slip Prevention, 50 MHz PFD** [8]




[6] Measured with 50 Ω impedance per line. Buffer current is controled via Reg 0Fh[4:2].

[7] Measured with 50 Ω impedance per line. Buffer current is controled via Reg 0Fh[4:2].

[8] Measured with HMC983LP5E/HMC984LP4E chip set as fractional-N synthesizer. Crystal input frequency = 100 MHz, CP current = 2.5 mA, CP offset current = 245 uA, Loop filter bandwidth = 87 KHz, DSM Mode B selected. Cycle Slip Prevention (CSP) is disabled in HMC984LP4E by setting Reg 01h [4] = 0. Setting Reg 01h [4] = 1 enables CSP in the two chip PLL.

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### Table 2. Pin Descriptions

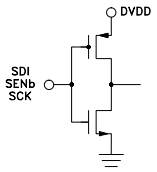
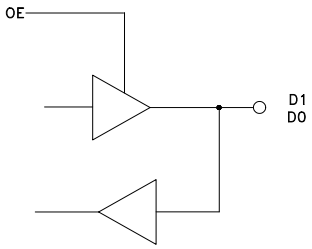
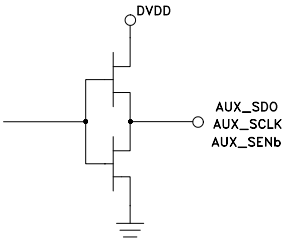
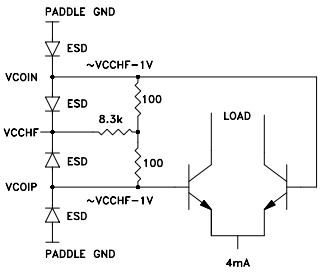
| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 1,<br>2,<br>3 | SENb<br>SDI<br>SCK | Main SPI Data Input |  |
| 4,<br>5 | D1<br>D0 | GPIO bit 1<br>GPIO bit 0 |  |
| 6,<br>7,<br>8 | AUX_SCLK<br>AUX_SENb<br>AUX_SDO | Auxiliary SPI Clock Output<br>Auxiliary SPI Enable<br>Auxiliary SPI Data Output |  |
| 9 | BIAS | External Decoupling for Analog Bias Circuits | |
| 10 | AVDD | 3 Volt Power Supply Pin for Internal Reference Current Sources | |
| 11 | VCCPS | 3 Volt Power Supply Pin for Prescaler | |
| 12,<br>13 | VCOIN,<br>VCIOP | Negative Pin for Prescaler Differential Input, AC-Coupled<br>Positive Pin for Prescaler Differential Input, AC-Coupled |  |
| 14 | VCCHF | 3 Volt Power Supply Pin for Prescaler Input Buffer | |
| 15 | VPPBUF | 5 Volt Power Supply Pin for Divider Output Buffer | |
| 16 | N/C | No Connect Pin | |

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**Table 2. Pin Descriptions** *(Continued)*

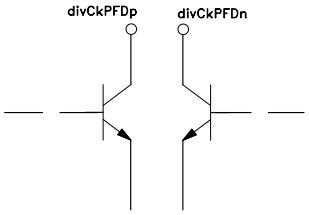
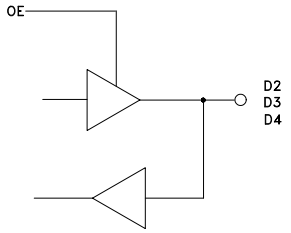
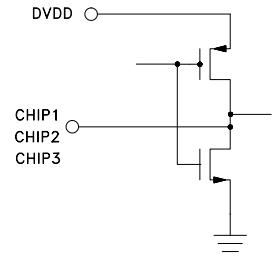
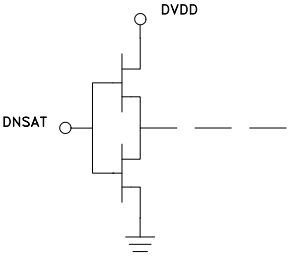
| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 17, 18 | divCkPFDn, divCkPFDp | Negative Pin for Open Collector Divider Output Driver<br>Positive Pin for Open Collector Divider Output Driver |  |
| 19 | VDDM | 3V Supply Pin for Digital Section of the Frequency Divider | |
| 20, 21, 22 | D2, D3, D4 | GPIO bit 2,<br>GPIO bit 3,<br>GPIO bit 4 |  |
| 23 | REF_Eno | Gate Control (Output) to request TCXO Clock Export from HMC984LP4E | |
| 24, 25, 26 | CHIP1, CHIP2, CHIP3 | Chip Address Pin 1,<br>Chip Address Pin 2,<br>Chip Address Pin 3 |  |
| 27, 30 | DVDD | 3V Power Supply for Digital | |
| 28, | DNSAT, | VCO Saturation Input flag from HMC984LP4E Chip |  |

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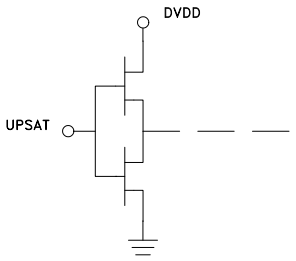
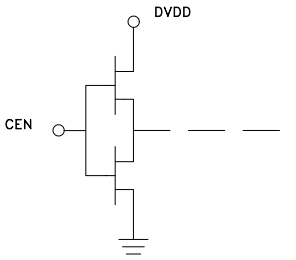
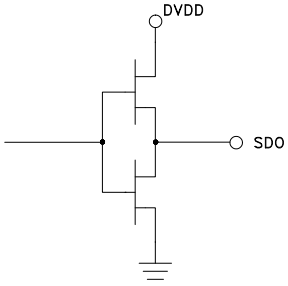
**Table 2. Pin Descriptions** *(Continued)*

| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 29 | UPSAT | Reference Saturation Input flag from HMC984LP4E Chip |   |
| 31 | CEN | Chip Enable |   |
| 32 | SDO | Main SPI Data Output |   |



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## Table 3. Absolute Maximum Ratings

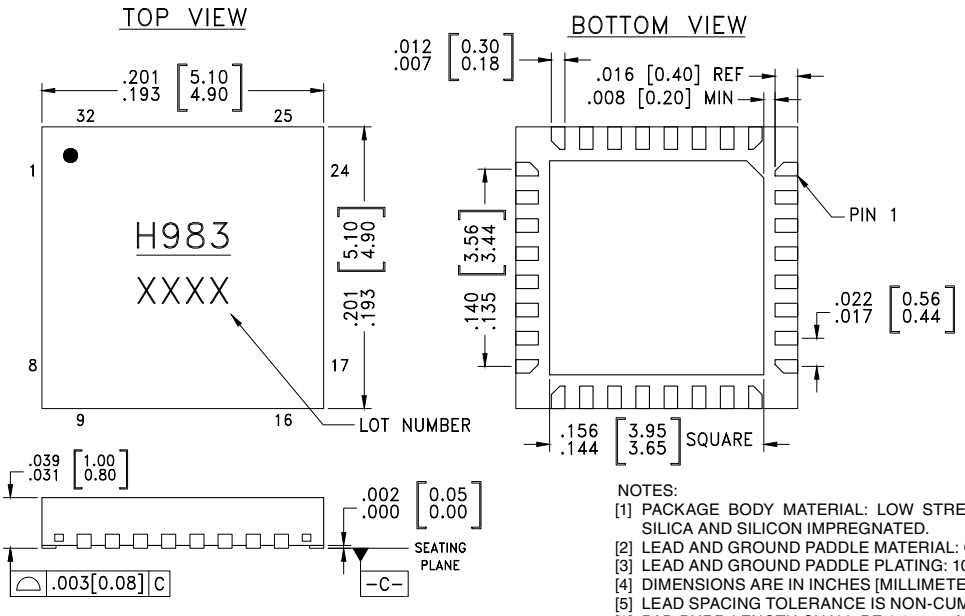
| | |
|---|---|
| Nominal 3V Supplies to GND | -0.3 to 3.6 V |
| Nominal 3V Digital Supply to 3V Analog Supply | -0.3 to +0.3 V |
| Nominal 5V Supply to GND (VPPBUF) | -0.3 to 5.5 V |
| divCkp, divCkn common mode DC | VCCPS + 0.5 V min |
| VCOIP, VCOIN Single Ended AC 50 Ω Source | + 7 dBm |
| VCOIP, VCOIN Differential AC 50 Ω Source | + 13 dBm |
| Digital Input Voltage Range | -0.25 to DVDD + 0.5 V |
| Minimum Digital Load | 1 kΩ |
| Operating Temperature Range | -40 °C to +85 °C |
| Maximum Junction Temperature | 125 °C |
| Storage Temperature | -65 to +125 °C |

| | |
|---|---|
| Thermal Resistance (Rth) (junction to ground paddle) | 40 °C/W |
| Reflow Soldering<br>Peak Temperature<br>Time at Peak Temperature | <br>260 °C<br>40 s |
| ESD Sensitivity (HBM) | Class 1B |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

## Outline Drawing




NOTES:
[1] PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
[2] LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
[3] LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
[4] DIMENSIONS ARE IN INCHES [MILLIMETERS].
[5] LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
[6] PAD BURR LENGTH SHALL BE 0.15 mm MAX. PAD BURR HEIGHT SHALL BE 0.25 m MAX.
[7] PACKAGE WARP SHALL NOT EXCEED 0.05 mm
[8] ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
[9] REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

## Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating [2] | Package Marking [1] |
|---|---|---|---|---|
| DGHERACTONALNDMDER | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 | H983<br>XXXX |

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

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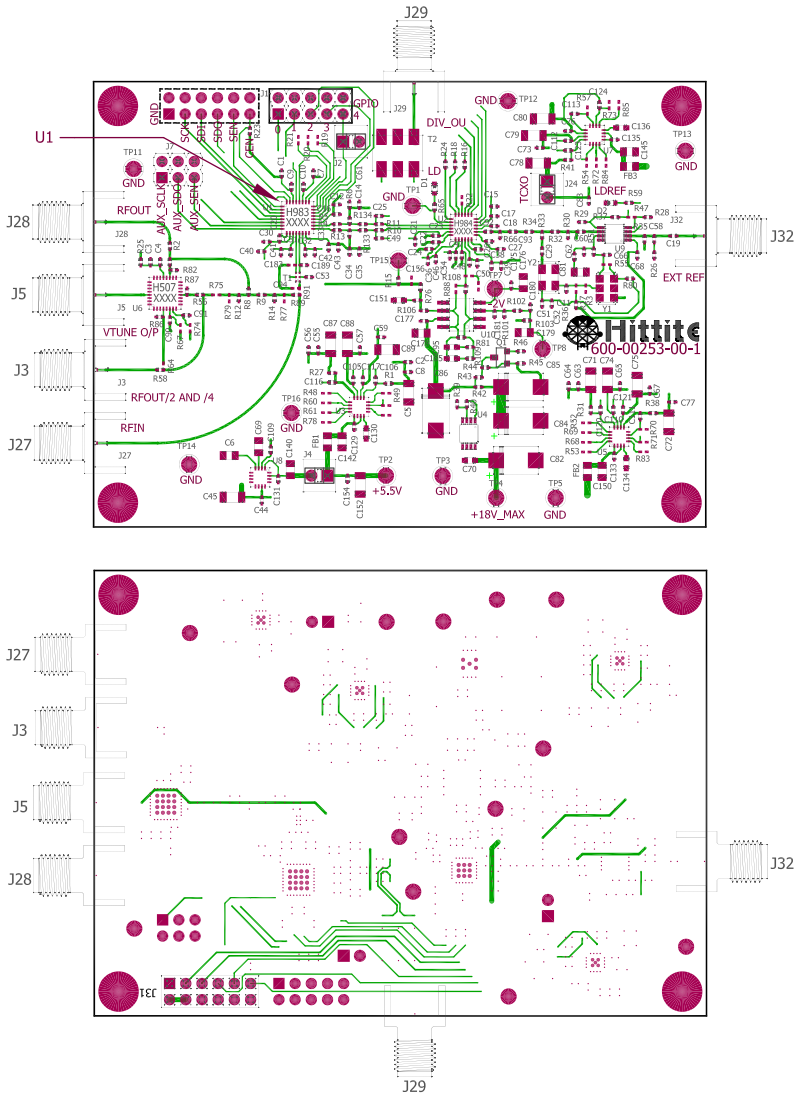
### Evaluation PCB




The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohms impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown unless mentioned otherwise. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

### Table 4. Evaluation Order Information

| Item | Contents | Part Number |
|---|---|---|
| Evaluation Kit | DC - 7 GHz FRACTIONAL-N DIVIDER and HMC984LP4E PLL Chipset Evaluation PCB<br>USB Interface Board<br>6' USB A Male to USB B Female Cable<br>CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software) | EKIT01-DC7GHzFRACTIONAL-NDIVIDER |

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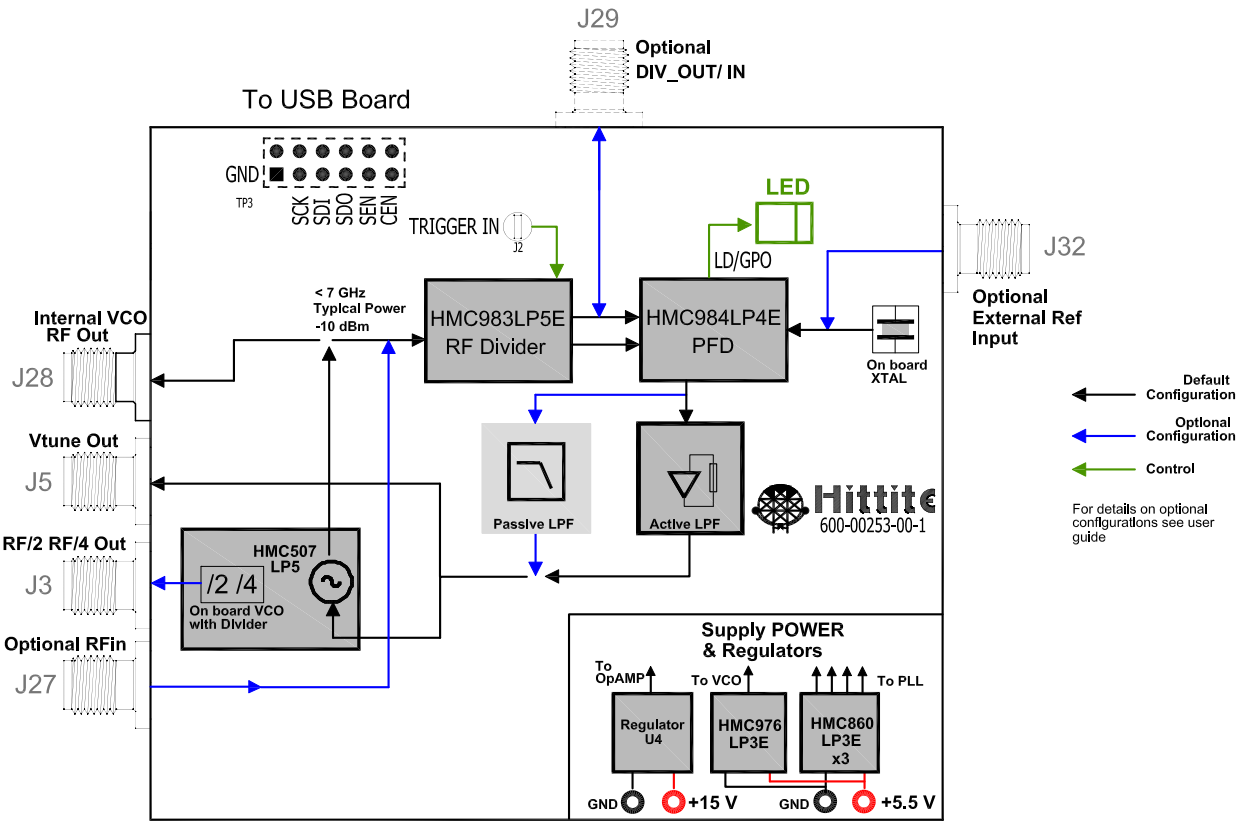
## DC - 7 GHz FRACTIONAL-N DIVIDER AND FREQUENCY SWEEPER



### Evaluation PCB Block Diagram

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## Theory of Operation

The DC - 7 GHz FRACTIONAL-N DIVIDER can be used in following configurations:

1. Fractional-N or Integer Mode RF Frequency Divider or Prescaler
2. Fractional-N Frequency Synthesizer with an appropriate Phase Detector and VCO

Primary target application of the DC - 7 GHz FRACTIONAL-N DIVIDER is to be used in conjunction with the AND FREQUENCY SWEEPER as shown in Figure 19. Together these two components form a high performance, low noise, ultra low spurious emissions fractional-N frequency synthesizer.

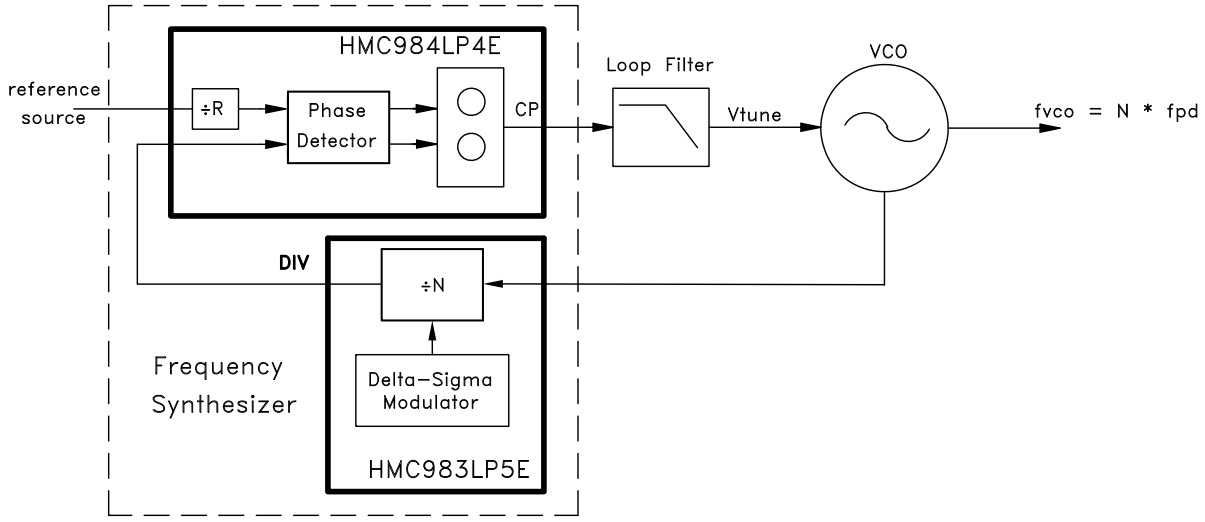


*Figure 19. Typical Application of HMC984LP4E with HMC983LP5E to Form a Frequency Synthesizer*

The DC - 7 GHz FRACTIONAL-N DIVIDER consists of the following functional blocks

1. RF Input Buffer
2. 7 GHz Frequency Prescaler and Multi Modulus Divider
3. 48-bit Configurable Fractional Delta Sigma Modulator
4. Bias Circuit
5. Differential Output Driver
6. Frequency Sweeper
7. Main Serial Port Interface
8. Auxiliary Serial Port Interface (Output Only)
9. General Purpose Digital IO
10. Power On Reset Circuit

### RF Input Buffer

The RF input stage provides the path from the external VCO to the fractional RF Divider. The RF input path is rated to operate nominally from DC to 7 GHz. The DC - 7 GHz FRACTIONAL-N DIVIDER RF input stage is a differential common emitter stage with DC coupling, and is protected by ESD diodes as shown in Figure 20. RF input is not matched to 50 Ω due to wide input frequency range. At low frequencies, a simple shunt 50 Ω resistor can be used external to the package to provide a 50 Ω match. For better performance it is recommended to match the RF inputs externally and provide differential drive from the VCO. In most applications the input is used single-ended into either the VCOIP or VCOIN pin with the other input connected to ground through a DC blocking capacitor. The preferred input level for best spectral performance is -10 dBm.

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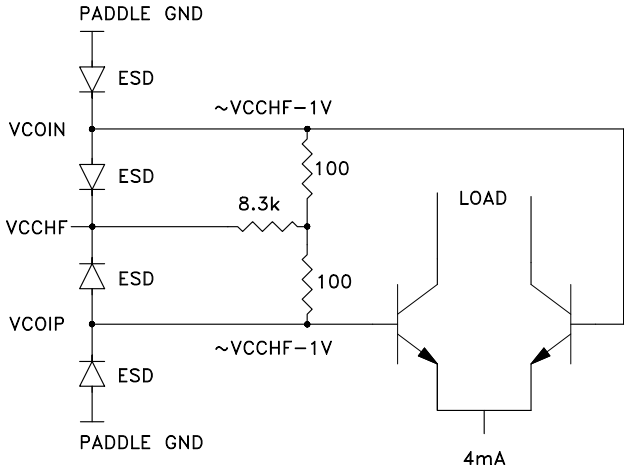


*Figure 20. RF Input Stage*

### *RF Path Fractional-N Divider*

The RF input buffer is followed by a high frequency prescaler and a multi modulus divider. The divider has been designed for the best output phase noise and spurious performance in both fractional and integer mode. The fractional-N divider can divide input frequencies from 32 to $2^{20}$-1 (1048575) in integer mode and from 36 to $2^{20}$-5 (1048571) in fractional-N mode. The divider output pulse width depends on the RF input period and is adjustable via SPI setting (refer to Duty Cycle Setting in register Reg 00h Chip ID, Soft Reset, Read Register[14:12]). The output pulse width recommended setting is 40% to 60% where possible. At low output frequencies it may not be possible to set 50% duty cycle. In such cases the maximum pulse width setting is recommended.

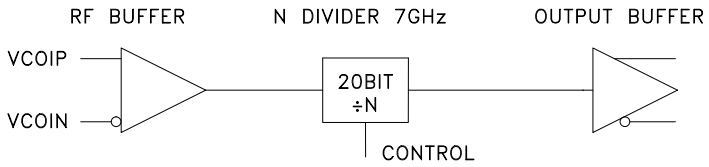


*Figure 21. Divider Path*

### *Divider Output Buffer*

The divider output is differential and the output buffer stage is an open collector amplifier with off-chip pull-up resistors. Due to sharp rise and fall times at the divider output, the external path should be designed differentially using RF techniques.

When DC - 7 GHz FRACTIONAL-N DIVIDER and AND FREQUENCY SWEEPER are operating together as a frequency synthesizer, 50 Ω pull-up resistors are provided in AND FREQUENCY SWEEPER.

VPPBUF pin should be connected to 5 V power supply. This pin does not sink DC current and is only used to bias the internal ESD diodes and to provide an appropriate voltage level for the phase detector chip (AND FREQUENCY SWEEPER). The two possible interface configurations are shown in Figure 22 and Figure 23 below.

The rising edge of the HMC983LP5E divider output divCkPFDp and falling edge of divCkPFDn are conditioned and re-synchronized for best spectral performance. The alternative edges are not This means for best spectral performance the HMC983LP5E must be used with a PFD, not an analog mixer.

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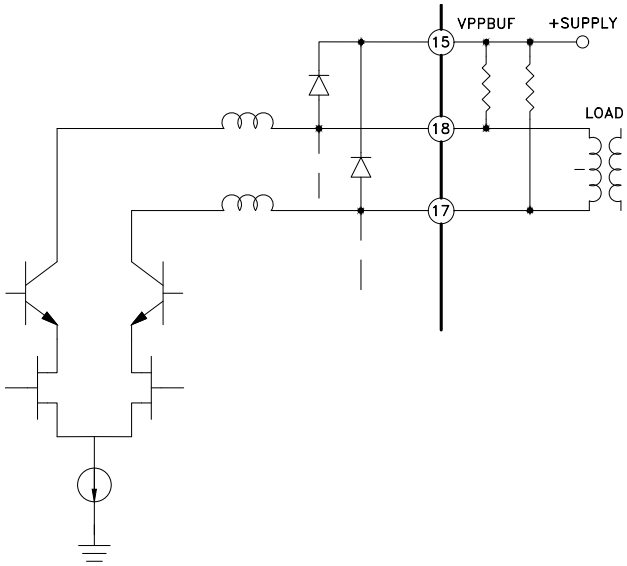


*Figure 22. Generic Divider Output Interface*

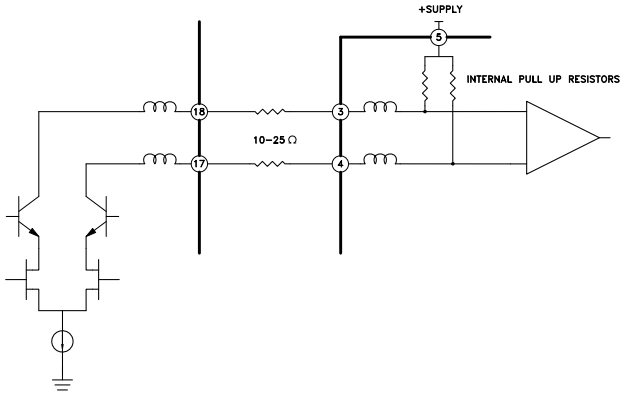


*Figure 23. Divider Interface with AND FREQUENCY SWEEPER*

### *Chip Address Pins*

The DC - 7 GHz FRACTIONAL-N DIVIDER has three SPI chip address pins (SPI address [2:0] = 'CHIP3, CHIP2, CHIP1'), which enable multiple DC - 7 GHz FRACTIONAL-N DIVIDER devices to use the same SPI bus. SPI chip address bits are read at power up, or every time DC - 7 GHz FRACTIONAL-N DIVIDER is reset. By default, all three pins are internally pulled to DVDD, thus there is no need to connect the pins to DVDD to set them to logic high. To assign a '0' to any chip address bit, the corresponding pin should be connected to ground.

When used on the same SPI bus together with the companion part (the AND FREQUENCY SWEEPER), to form a frequency synthesizer, some SPI commands, such as changing the reference division ratio to the AND FREQUENCY SWEEPER may also require an action by the DC - 7 GHz FRACTIONAL-N DIVIDER. In order to avoid the necessity to write two separate SPI transfers to implement one command (one to configure AND FREQUENCY SWEEPER, and the other one to configure the DC - 7 GHz FRACTIONAL-N DIVIDER), it is possible to write the SPI address of the companion part (AND FREQUENCY SWEEPER) into Reg 09h of the DC - 7 GHz FRACTIONAL-N DIVIDER. In such cases, the DC - 7 GHz FRACTIONAL-N DIVIDER is able to recognize an SPI command to the companion part (the AND FREQUENCY SWEEPER) that requires its own action, and act accordingly to update its own corresponding

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registers. Writing DC - 7 GHz FRACTIONAL-N DIVIDER's own chip address to the companion chip address register Reg 09h will disable this feature.

### *Saturation Detection Input Pins DNSAT, UPSAT*

When the DC - 7 GHz FRACTIONAL-N DIVIDER is operating with its companion chip the AND FREQUENCY SWEEPER as a frequency synthesizer, it automatically detects large phase errors and tries to tune the VCO faster by using its algorithm for cycle-slip prevention (CSP). The UPSAT and DNSAT provide indication which frequency is higher (VCO or Reference) from the counterpart Phase Detector/Charge Pump (the AND FREQUENCY SWEEPER). The CSP algorithm manipulates the RF Divider and the Phase Detector at appropriate intervals to lock faster. See AND FREQUENCY SWEEPER data sheet for more details. These pins should be connected to ground if not used.

### *REF_Eno Pin*

REF_Eno pin is a digital output pin that is used by the DC - 7 GHz FRACTIONAL-N DIVIDER to request crystal oscillator clock from the Phase Detector / Charge Pump chip (the AND FREQUENCY SWEEPER).

The crystal oscillator clock is multiplexed on the DC - 7 GHz FRACTIONAL-N DIVIDER's DNSAT pin. The internal frequency divider, programmed in Reg 02h, is used to generate the actual reference frequency present at the phase detector. The imported clock is only used to communicate through the AUXSPI. At all other times, the clock and the local reference dividers are turned off.

In stand-alone applications, if the DC - 7 GHz FRACTIONAL-N DIVIDER is required to communicate through the auxiliary SPI, the DC - 7 GHz FRACTIONAL-N DIVIDER will expect to receive the auxiliary SPI clock on DNSAT pin. Setting Reg 04h[15] = 1 keeps the auxiliary SPI clock enabled on the DNSAT pin.

### *Multi Purpose Digital IO Pins D0, D1, D2, D3, D4 (GPIO Pins)*

The five general purpose digital input/outputs can be used for various modes of operation as well as test/debugging purposes. GPIO pins are enabled by writing Reg 01h[4] = 1 (GPIO master enable). Setting Reg 01h[4] = 0 places the GPIO pins in tri-state high impedance mode.

GPIO pins are configured in Reg 08h[13:0]. All of the pins can configured to be either inputs or outputs by writing to Reg 08h[13:9]. In frequency sweep mode, pin D4 can be used as an external trigger pin, by writing Reg 08h[13] = 0.

Writing to Reg 08h[3:0] selects DC - 7 GHz FRACTIONAL-N DIVIDER's internal signals to be multiplexed out on the GPIO pins, as shown in Table 5. Signals include:

1. The output of the Delta-Sigma Modulator Reg 08h[3:0] = '0010'b.
2. GPIO test signals Reg 08h[3:0] = '0000'b, which outputs data written to Reg 08h[8:4] to test the GPIO pins.
3. Sweep status flags, when the DC - 7 GHz FRACTIONAL-N DIVIDER is configured to be in sweep mode Reg 08h[3:0] = '1000'b.

**Table 5. GPIO Pin Assignment and Output Signals**

| Reg 08h[3:0] | DC - 7 GHz FRACTIONAL-N DIVIDER GPIO Pins | | | | |
|---|---|---|---|---|---|
| | D4 | D3 | D2 | D1 | D0 |
| 0000 | gpo_test_out[4] | gpo_test_out[3] | gpo_test_out[2] | gpo_test_out[1] | gpo_test_out[0] |
| 0001 | reserved | reserved | reserved | reserved | reserved |
| 0010 | DSM_OUT[4] | DSM_OUT[3] | DSM_OUT[2] | DSM_OUT[1] | DSM_OUT[0] |
| 0011 | reserved | reserved | reserved | reserved | reserved |
| 0100 | reserved | reserved | reserved | reserved | reserved |
| 0101 | reserved | reserved | reserved | reserved | reserved |

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### Table 5. GPIO Pin Assignment and Output Signals

| Reg 08h[3:0] | DC - 7 GHz FRACTIONAL-N DIVIDER GPIO Pins | | | | |
|---|---|---|---|---|---|
| | D4 | D3 | D2 | D1 | D0 |
| 0110 | reserved | reserved | reserved | 0 | 0 |
| 0111 | reserved | reserved | reserved | reserved | reserved |
| 1000 | ramp_ready_flag | ramp_start_flag | ramp_stop_flag | ramp_busy_falg | reserved |
| 1001-1111 | 0 | 0 | 0 | 0 | 0 |

### Fractional Mode of Operation

In addition to providing simple integer division ratios, the DC - 7 GHz FRACTIONAL-N DIVIDER has a sophisticated, configurable 48-bit Delta Sigma Modulator (DSM), that allows fractional division of the input frequency in ultra fine steps. The DSM's size can be configured to 16/24/32/48 bits (Reg 16h[5:0]). DC - 7 GHz FRACTIONAL-N DIVIDER's auto-seed mode allows coherent frequency sweeps.

The DC - 7 GHz FRACTIONAL-N DIVIDER with its counterpart (the AND FREQUENCY SWEEPER), together with an external VCO comprise a fully functional fractional-N synthesizer. In that case, the output frequency of the external VCO is given by:

$$f_{vco} = \frac{f_{xtal}}{R} \cdot N_{\text{int}} + \frac{f_{xtal}}{R \cdot 2^{L}} \cdot N_{frac} = f_{\text{int}} + f_{frac} \quad \text{(Eq 1)}$$

When the DC - 7 GHz FRACTIONAL-N DIVIDER is being used as frequency divider, the output frequency is given by;

$$f_{out} = \frac{f_{vco}}{N_{\text{int}} + \frac{N_{frac}}{2^{L}}} \quad \text{(Eq 2)}$$

Where

$f_{vco}$ is the VCO frequency in Hz;

$f_{xtal}$ is the crystal oscillator frequency in Hz;

$N_{int}$ is the integer part of frequency division ratio (set in Reg 05h[19:0]);

$N_{frac}$ is the fractional part of frequency division ratio ($N_{frac}$[47:18] = Reg 06h[29:0], $N_{frac}$[17:0] = Reg 07h[17:0])

R is the reference frequency division ratio;

L is the size of the DSM accumulators (set in Reg 16h[5:0])

**Example 1:** Calculate the VCO frequency with the following parameters;

$f_{xtal}$ = 50 MHz; $f_{pfd}$ = 25 MHz

$N_{int}$ = 25; $N_{frac}$ = 1; L = 24

Where $f_{PFD}$ is the frequency at the phase detector, thus R = 2. According to (Eq 1), the VCO frequency with the above parameters will be;

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$$f_{vco} = \frac{50MHz}{2} \cdot 25 + \frac{50MHz}{2 \cdot 2^{24}} \cdot 1 = 2500MHz + 1.49Hz$$

If accumulator width (L) is changed to 48-bit, then the frequency resolution will improve and the fractional resolution of the VCO frequency will be 88.8178 nano-Hz.

**Example 2:** Set the VCO frequency to 4600.025 MHz using 100 MHz Crystal, R = 2 and L = 16. Compare if L = 32.

For this example the $f_{PFD}$ = 100 MHz/2 = 50 MHz,

The overall division ratio is 4600.025 MHz/50 MHz = 92.0005

The nearest integer would be 92, thus $N_{int}$ = Reg 05h[19:0] = 92d = 5Ch.

For L = 16, $N_{frac}$ = 32.768 or 33d rounded up. Thus $N_{frac}$ = 33d or 21h (Reg 06h[29:0] = 0, Reg 07h[17:0] = 21h).

For L = 32, $N_{frac}$ = 2147483.648 or 2147484d rounded up. Thus $N_{frac}$ = 20C49Ch (Reg 06h[29:0] = 8h, Reg 07h[17:0] = '001100010010011100'd).

Since $N_{frac}$ must be an integer, the actual frequencies in the two cases will have an error of + 177.02 Hz for L = 16 and only +0.004098 Hz for L = 32.

### *Phase Noise in Integer and Fractional Modes*

In a normal integer frequency divider the in-band phase noise is scaled from the input phase noise by 20Log10(N), where N is the divider value. In HMC983LP5E fractional mode, the frequency divider is modulated by the Delta Sigma Modulator to generate output frequencies that are fractional multiple of the input frequency. Delta Sigma Modulator shapes the quantization noise such that quantization noise density has a high pass shape which peaks at Fs/2, where Fs is the sampling frequency (the divider output frequency in case of HMC983LP5E). In fractional mode this quantization noise peak appears at an offset frequency of Fout/2. In the PLL, this peak is attenuated by the loop filter. However, when the HMC983LP5E is used stand-alone in fractional mode its output will exhibit the quantization noise as shown in Figure 2 and Figure 3. As a result, it is not possible to achieve the same noise floor in fractional mode as in integer mode without further filtering.

### *CW Frequency Sweeper*

The DC - 7 GHz FRACTIONAL-N DIVIDER features a built-in frequency sweeper function that supports automatic or externally triggered sweeps. External triggering can be executed via an external trigger pin D4 or the SPI interface.

DC - 7 GHz FRACTIONAL-N DIVIDER sweep function can be configured to operate in the following modes:

- 2-Way sweep mode
  - Repeating alternating positive and negative frequency sweep ramps
  - Frequency increments swept with automatic sequencer
  - Automatic or triggered
  - Symmetric or asymmetric (the positive ramp can have a different slope from that of the negative ramp)
- 1-Way Sweep Mode
  - Repeating one directional frequency sweeps followed by a reset to the starting frequency
  - Frequency increments swept with automatic sequencer
  - Triggered

User defined sweep mode

- Manually programmed user defined sweep patterns
- Triggered
- Symmetric or asymmetric (the positive ramp can have a different slope from that of the negative ramp)

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In all sweep modes, the starting sweep direction can be set to positive (increasing) or negative (decreasing). The trigger can be applied instantaneously or delayed by a programmable time delay.

DC - 7 GHz FRACTIONAL-N DIVIDER's sweep function is illustrated in Figure 24. The DC - 7 GHz FRACTIONAL-N DIVIDER generates a frequency sweep by implementing automatic, or triggered in User Defined Mode, discrete miniature frequency increments in time. A smooth and continuous sweep is then generated, at the output of the VCO, after the stepped signal is filtered by the loop filter, as shown in Figure 24. The stepped sweep approach enables the frequency synthesizer (comprising of DC - 7 GHz FRACTIONAL-N DIVIDER together with its counterpart, the HMC984LP4E) to be in lock for the entire duration of the sweep. This approach results in a number of advantages over conventional methods including:

- The ability to generate a linear sweep.
- The ability to have phase coherence between different sweep ramps, so that the phase profile of each sweep is identical.
- The ability to generate user defined sweeps in User Defined Sweep Mode.

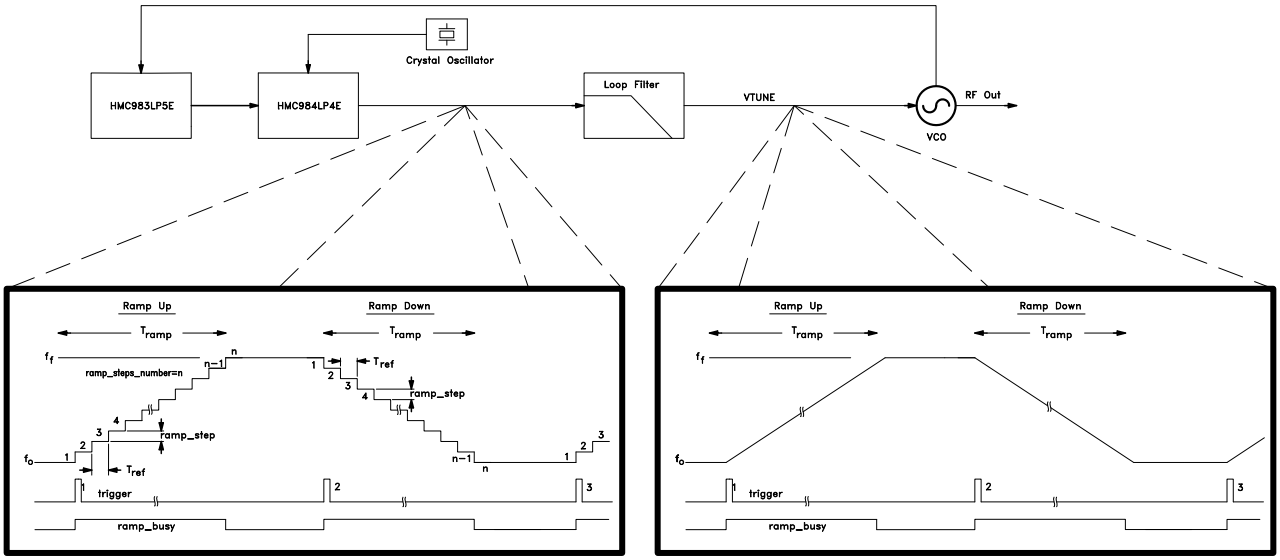


*Figure 24. DC - 7 GHz FRACTIONAL-N DIVIDER Sweep Function*

It is important to note that the synthesized ramp is subject to normal phase locked loop dynamics. If the loop bandwidth in use is much wider than the rate of frequency increments then the locking will be fast and the ramp will have a staircase shape. If the update rate is higher than the loop bandwidth, as is normally the case, the loop will not fully settle before a new frequency step is received. Hence the swept output will have a lag and will sweep in a near continuous fashion.

In all sweep modes, ramp_busy flag indicates an active sweep and will stay high between the 1st and nth ramp increment. ramp_busy may be monitored on pin D1 by setting Reg 08h[3:0] = 8h.

### *Triggering*

In sweep mode, the DC - 7 GHz FRACTIONAL-N DIVIDER can be triggered via one of two methods

- SPI trigger by setting Reg 0Eh[12]=1. This triggering method is asynchronous to the reference clock. To enable SPI trigger write Reg 0Eh[13] = 0.
- or applying an external trigger on pin D4. Setting Reg 0Eh[13] = 1 and Reg 08h[13] = 0h configures DC - 7 GHz FRACTIONAL-N DIVIDER's pin D4 as external trigger input. External trigger on pin D4 is triggered on the rising edge of the trigger. GPIO master enable (Reg 01h[4] = 1) is also required.

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- External triggering method can be synchronized with the reference clock, by enabling trigger delay (Reg 0Eh [7] = 1), and programming a trigger delay in Reg 05h[20:0] = number of delayed reference periods. Writing Reg 05h[20:0] = 1 for example ensures that the trigger is applied at the instant of the rising edge of the next reference rising edge. To disable trigger delay write Reg 0Eh [7] = 0.

### *2-Way Sweep Mode*

DC - 7 GHz FRACTIONAL-N DIVIDER's 2-Way sweep mode is shown in Figure 25. The 2-Way sweep mode can be automatic or triggered. In automatic 2-way sweep, the trigger is generated internally based on user defined 2-way sweep mode configuration. In a triggered 2-way sweep, frequency ramps are triggered either by external pin D4, or SPI trigger.

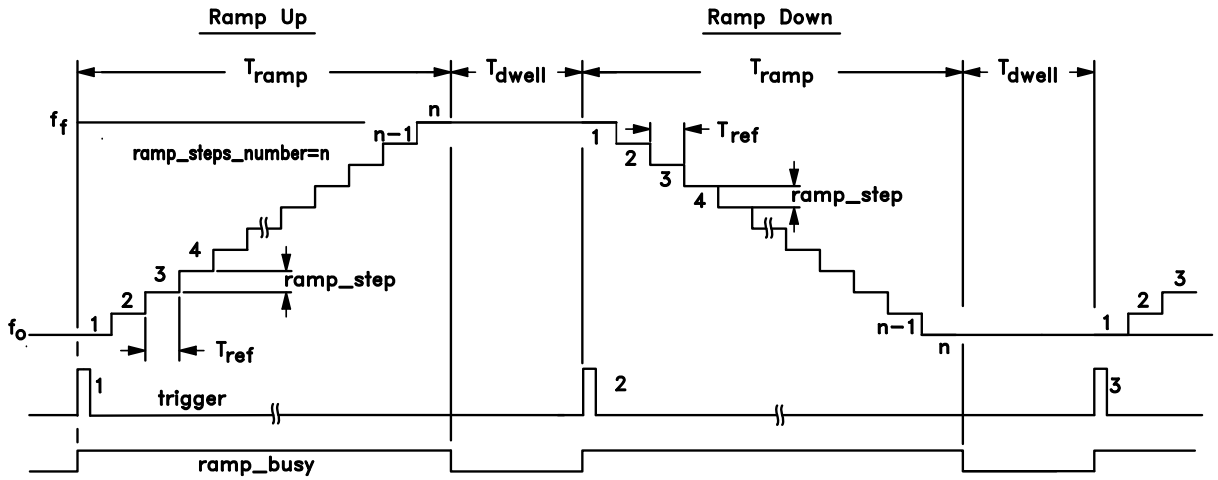


*Figure 25. DC - 7 GHz FRACTIONAL-N DIVIDER 2-Way Triggered Sweep*

### *Triggered 1-Way Sweeps*

DC - 7 GHz FRACTIONAL-N DIVIDER's 1-Way sweeps is shown in Figure 26. Unlike 2-Way sweeps, 1-Way sweeps require that the VCO hop back to the start frequency after the dwell period. Triggered 1-Way sweeps also require a 3rd trigger to start the new sweep. The 3rd trigger must be timed appropriately to allow the VCO to settle after the large frequency hop back to the start frequency. Subsequent odd numbered triggers will start each sweep and repeat the process.

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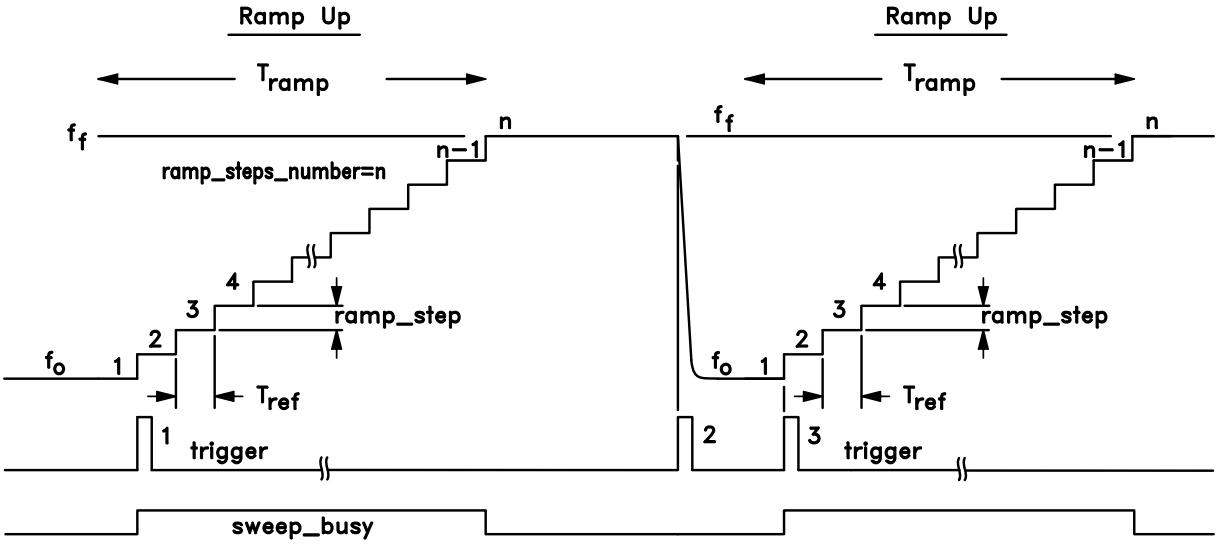


*Figure 26. DC - 7 GHz FRACTIONAL-N DIVIDER 1-Way Triggered Sweep*

1-Way sweeps are not recommended in auto-sweep mode since in auto-sweep the new sweep will start immediately after the 2nd trigger, as it does in 2-Way mode.

### *User Defined Sweep Mode*

In User Defined Sweep mode, the DC - 7 GHz FRACTIONAL-N DIVIDER is able to generate various user-defined sweep patterns by adjusting the time interval between adjacent frequency increments, which are executed by trigger events. DC - 7 GHz FRACTIONAL-N DIVIDER's User Defined Sweep Mode is shown in Figure 27. In this mode, an external trigger is required for each frequency increment of the sweep.



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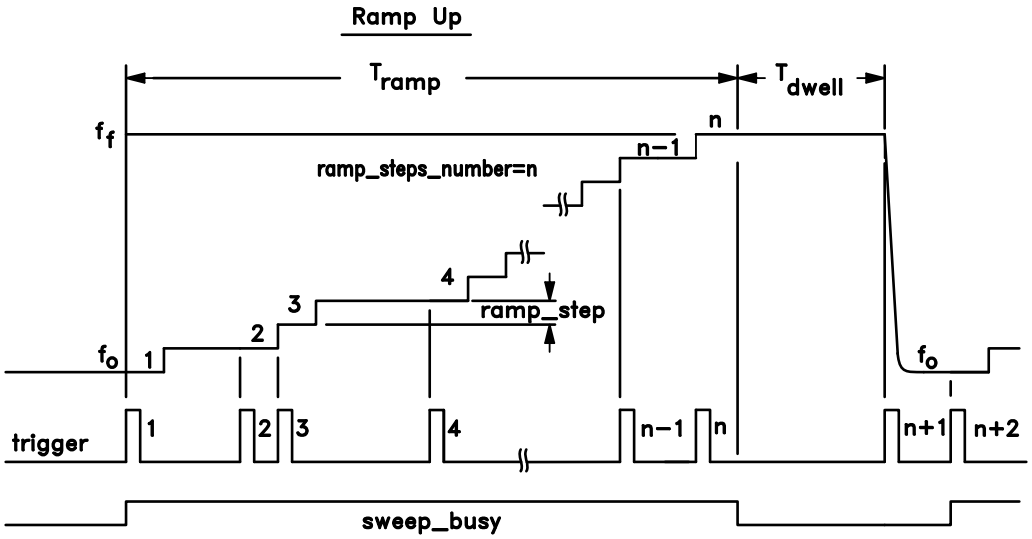


*Figure 27. DC - 7 GHz FRACTIONAL-N DIVIDER User Defined Sweep*

User defined sweep can function in both 1-Way or 2-Way sweep mode. In 1-Way sweep mode, the n+1 trigger will cause the ramp to jump to the start frequency, and the n+2 trigger will restart the 1-way sweep.

### *Detailed Sweeper Configuration*

Recommended procedure for configuring DC - 7 GHz FRACTIONAL-N DIVIDER sweeper in all three modes is shown in Table 6.

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### Table 6. DC - 7 GHz FRACTIONAL-N DIVIDER Sweeper Configuration Sequence

| Steps | Description | Sweeper Modes | | |
|---|---|---|---|---|
| | | 2-Way Sweep Mode | User Defined Sweep Mode | 1-Way Sweep Mode |
| 1 | Lock to start frequency ($f_o$) | • set the integer (Reg 05h) and fractional (Reg 06h and Reg 07h) divider values.<br>• Optionally, if required the seed (Reg 0Ah and Reg 0Bh) can also be programmed | | |
| 2 | Place the DSM in sweep mode | • Write Reg 0Eh[11] = 1 | | |
| 3 | Configure sweep mode | • Disable single step ramp mode (Reg 0Eh[24] = 0), so that each frequency increment will be incremented automatically<br>• Enable 2-way sweep mode (Disable 1-way sweep mode (Reg 0Eh[25] = 0))<br>• To place the DC-7GHz FRACTIONAL-N DIVIDER in automatic sweep mode write Reg 0Eh[2:3] = '11'. To place the DC-7GHz FRACTIONAL-N DIVIDER in triggered mode write Reg 0Eh[2:3] = '00'. | • Enable the single step ramp mode (Reg 0Eh[24] = 1), so that each frequency increment will require a trigger<br>• Enable 1-way sweep mode (Reg 0Eh[25] = 1), or enable 2-Way sweep mode (Reg 0Eh[25] = 1)<br>• To place the DC-7GHz FRACTIONAL-N DIVIDER in triggered mode write Reg 0Eh[2:3] = '00'. Automatic User Defined Sweep mode is not supported. | • Disable single step ramp mode (Reg 0Eh[24] = 0), so that each frequency increment will be incremented automatically<br>• Enable 1-way sweep mode (Reg 0Eh[25] = 1)<br>• To place the DC-7GHz FRACTIONAL-N DIVIDER in triggered mode write Reg 0Eh[2:3] = '00'. Automatic 1-Way Sweep mode is not supported. |
| 4 | Program Sweep Direction | • Reg 0Eh[26] = 1 begin sweep in positive direction, Reg 0Eh[26] = 0 begin sweep in negative direction | | |
| 5 | Configure symmetrical/ asymmetrical sweep | • Program ramp mode (symmetrical - Reg 0Eh[22] = 1, asymmetrical - Reg 0Eh[22] = 0). If symmetrical ramp mode is selected (Reg 0Eh[22] = 1), only Up sweep parameters will be used for both positive and negative sweeps, and hence down sweep parameters don't need to be programmed. In symmetrical ramp mode the positive and negative ramps are identical and opposite in direction. | | • Program Reg 0Eh[22] = 1. Asymmetrical sweep is not defined in 1-Way Sweep mode |
| 6 | Program Up Sweep Parameters | • Set dwell time(dwell time[47:0] = Reg 10h[29:0], dwell time[17:0] = Reg 11h[17:0])<br>• Set step size (step size[47:18] = Reg 12h[29:0], step size[17:0] = Reg 13h[17:0])<br>• Set the number of steps in a sweep (number of steps[47:18] = Reg 14h[29:0], number of steps[17:0] = Reg 15h[17:0]) | | |
| 7 | Program Down Sweep Parameters (Only if using asymmetrical sweep (if Reg 0Eh[22] = 0) in Step 5) | • Set dwell time (dwell time[47:0] = Reg 06h[47:18], dwell time[17:0] = Reg 07h[17:0])<br>• Set step size (step size[47:18] = Reg 19h[29:0], step size[17:0] = Reg 1Ah[17:0])<br>• Set the number of steps in a sweep (number of steps[47:18] = Reg 0Ch[29:0], number of steps[17:0] = Reg 0Dh[17:0]) | | • Asymmetrical sweep is not defined in 1-Way Sweep mode |
| 8 | Configure and apply trigger | • To use SPI trigger write Reg 0Eh[13] = 0 to select SPI trigger. SPI trigger is executed by writing to Reg 0Eh[12] = 1.<br>• To use external trigger on pin D4 write Reg 0Eh[13] = 1 to configure pin D4 as an external trigger. Write Reg 08h[13] = 0h to configure pin D4 to be an input. Applying master enable to GPIO pins (Reg 01h[4] = 1 ) is required.<br>• Enable trigger delay (Reg 0Eh[7] = 1), or disable trigger delay (Reg 0Eh[7] = 0).<br>• If using trigger delay, write delay value to Reg 05h[20:0], where Reg 05h[20:0] = number of delayed reference periods. Writing Reg 05h[20:0] = 1 for example ensures that the trigger is applied at the instant of the rising edge of the next reference rising edge. | | |

DC - 7 GHz FRACTIONAL-N DIVIDER sweep parameters are defined in the following way:

| | |
|---|---|
| $f_o$ | Initial frequency of the synthesizer |
| $f_f$ | Frequency of the synthesizer at the end of the sweep |
| R | Reference divider value(Reg 02h[13:0]) |

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| | |
|---|---|
| stepsize | frequency increment step size. In case of symmetric and UP sweeps, stepsize[47:18] = Reg 12h[29:0], stepsize[17:0] = Reg 13h[17:0]). In case of asymmetric sweeps, (downsweep stepsize[47:18] = Reg 12h[29:0], down sweep stepsize[17:0] = Reg 13h[17:0]) |
| $\Delta f_{step}$ | Frequency step size $= stepsize \cdot \frac{f_{xtal}}{2^L \cdot R}$, |
| L | Size of the DSM (set in Reg 16h[5:0]) |
| $T_{ref}$ | Period of the divided reference ($f_{PFD}$) at the phase detector. $T_{ref} = \frac{R}{f_{xtal}}$ |
| N | Total number of frequency step increments in a single sweep. N [47:18] = Reg 14h[29:0], N[17:0] = Reg 15h[17:0] |
| $T_{ramp}$ | Total time of one frequency sweep from $f_o$ to $f_f$. $T_{ramp} = T_{ref}$ x N |

Then final frequency $f_f$ is given by: $f_f = f_o + (\Delta f_{step}$ x N)

Setting autoseed (Reg 0Eh[8] = 1) ensures that different sweeps have identical phase profile. This is achieved by loading the seed (seed[47:18] = Reg 0Ah[29:0], seed[17:0] = Reg 0Bh[17:0]) into the phase accumulator at the beginning of each ramp.

*Example: Calculate sweep parameters for an asymmetric 2-Way sweep from $f_0$ = 3000 MHz to $f_f$ = 3105 MHz with positive $T_{ramp}$ ≈ 2 ms, and negative $T_{ramp}$ ≈ 4 ms, and positive dwell time = negative dwell time = 2 µs, with $f_{PD}$ = 50 MHz, and a 48-bit delta-sigma modulator size. Assuming R = 1.*

1. *Calculate the integer and fractional divider values for initial start frequency $f_0$*
   - *Start Nint = Reg 05h = 60d*
   - *Start Nfrac = Reg 06h = Reg 07h = 0d*
2. *Calculate the number of divided (R = 1) reference periods in the sweep = number of frequency increments N*
   - *Nup = 2 ms/(1/50 MHz) = 100000*
   - *Ndown = 4 ms/(1/50 MHz) = 200000*
3. *Calculate stepsize (size of frequency increments)*
   - *stepssize up = abs($f_f$ - $f_0$)/Nup = abs(3000 MHz - 3105 MHz)/100000 = 1050 Hz. Then as per Table 6, Reg 12h[29:0] = 0h, Reg 13h[17:0] = 1050d = 41Ah*
   - *stepsize down = abs(ff - f0)/Ndown = abs(3000 MHz - 3105 MHz)/200000 = 525 Hz Then as per Table 6, Reg 19h[29:0] = 0h, Reg 1Ah[17:0] = 1050d = 41Ah*

   *Note that it is possible to have a case where the frequency $f_f$* cannot be generated exactly. In that case it is required to approximate the final frequency to $f_f = f_o + (\Delta f_{step}$ x N) ≈ desired final frequency.
4. *Calculate number of divided (R = 1) reference periods in required dwell time*
   - *Up dwell time (Reg 10h[29:0], Reg 11h[17:0]) = down dwell time (Reg 06h[29:0], Reg 07h[17:0]) = dwell time/ (1/ 50 MHz) = 2 µs/(1/50 MHz) = 100. Then as per Table 6, Reg 10h[29:0] = Reg 06h[29:0] = 0h, and Reg 11h[17:0] = Reg 07h[17:0] = 100d = 64h.*

*Then proceed to configure the sweep according to the steps outlined in Table 6.*

### Serial Port Interface

The DC - 7 GHz FRACTIONAL-N DIVIDER features a four wire serial port for simple communication with the host controller. Typical serial port operation can be run with SCK at speeds up to 30 MHz.

The details of SPI access for the DC - 7 GHz FRACTIONAL-N DIVIDER is provided in the following sections. Note that the READ operation below is always preceded by a WRITE operation to Register 0 to define the register to be queried. Also note that every READ cycle is also a WRITE cycle in that data sent to the SPI while reading the data will also be stored by the DC - 7 GHz FRACTIONAL-N DIVIDER when SENb goes high. If this is not desired then it is suggested to write to Register 0 during the READ operation so that the status of the device will be unaffected.

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### Power on Reset and Soft Reset

The DC - 7 GHz FRACTIONAL-N DIVIDER has a built in Power On Reset (POR) and a serial port accessible Soft Reset (SR). POR is accomplished when power is cycled for the DC - 7 GHz FRACTIONAL-N DIVIDER while SR is accomplished via the SPI by writing Reg 00h = 80h, followed by writing Reg 00h =00h. All chip registers will be reset to default states approximately 250 us after power up.

#### Serial Port WRITE Operation

The host changes the data on the falling edge of SCK and the DC - 7 GHz FRACTIONAL-N DIVIDER reads the data on the rising edge.

A typical WRITE cycle is shown in Figure 28. It is 40 clock cycles long.

1. The host both asserts SENb (active low Serial Port Enable) and places the MSB of the data on SDI followed by a rising edge on SCK.
2. DC - 7 GHz FRACTIONAL-N DIVIDER reads SDI (the MSB) on the 1st rising edge of SCK after SENb.
3. DC - 7 GHz FRACTIONAL-N DIVIDER registers the data bits, D29:D0, in the next 29 rising edges of SCK (total of 30 data bits).
4. Host places the 5 register address bits, A6:A0, on the next 7 falling edges of SCK (MSB to LSB) while the DC - 7 GHz FRACTIONAL-N DIVIDER reads the address bits on the corresponding rising edge of SCK.
5. Host places the 3 chip address bits, CA2:CA0=[110], on the next 3 falling edges of SCK (MSB to LSB). Note the DC - 7 GHz FRACTIONAL-N DIVIDER chip address is fixed as “7d” or “111b”.
6. SENb goes from low to high after the 40th rising edge of SCK. This completes the WRITE cycle.
7. DC - 7 GHz FRACTIONAL-N DIVIDER also exports data back on the SDO line. For details see the section on READ operation.

#### Serial Port READ Operation

The SPI can read from the internal registers in the chip. The data is available on SDO pin. This pin itself is tri-stated when the device is not being addressed. However when the device is active and has been addressed by the SPI master, the DC - 7 GHz FRACTIONAL-N DIVIDER controls the SDO pin and exports data on this pin during the next SPI cycle.

DC - 7 GHz FRACTIONAL-N DIVIDER changes the data to the host on the rising edge of SCK and the host reads the data from DC - 7 GHz FRACTIONAL-N DIVIDER on the falling edge.

A typical READ cycle is shown in Figure 28. Read cycle is 40 clock cycles long. To specifically read a register, **the address of that register must be written to dedicated Reg 0h**. This requires two full cycles, one to write the required address, and a 2nd to retrieve the data. A read cycle can then be initiated as follows;

1. The host asserts SENb (active low Serial Port Enable) followed by a rising edge SCK.
2. DC - 7 GHz FRACTIONAL-N DIVIDER reads SDI (the MSB) on the 1st rising edge of SCK after SENb.
3. DC - 7 GHz FRACTIONAL-N DIVIDER registers the data bits in the next 29 rising edges of SCK (total of 30 data bits). **The LSBs of the data bits represent the address of the register that is intended to be read.**
4. Host places the 7 register address bits on the next7 falling edges of SCK (MSB to LSB) while the DC - 7 GHz FRACTIONAL-N DIVIDER reads the address bits on the corresponding rising edge of SCK. **For a read operation this is “0000000”.**
5. Host places the 3 chip address bits [111] on the next 3 falling edges of SCK (MSB to LSB).
6. SENb goes from low to high after the 40th rising edge of SCK. This completes the first portion of the READ cycle.
7. The host asserts SENb (active low Serial Port Enable) followed by a rising edge SCK.

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8. DC - 7 GHz FRACTIONAL-N DIVIDER places the 30 data bits, 7 address bits, and 3 chip id bits, on the SDO, on each rising edge of the SCK, commencing with the first rising edge beginning with MSB.
9. The host de-asserts SENb (i.e. sets SENb high) after reading the 40 bits from the SDO output. The 40 bits consists of 30 data bits, 7 address bits, and the 3 chip id bits. This completes the read cycle.

   Note that the data sent to the DC - 7 GHz FRACTIONAL-N DIVIDER SPI during this portion of the READ operation is stored in the SPI when SENb is de-asserted. It is recommended that during the second phase of the READ operation that Reg 00h is addressed with either the same address or the address of another register to be read during the next cycle.

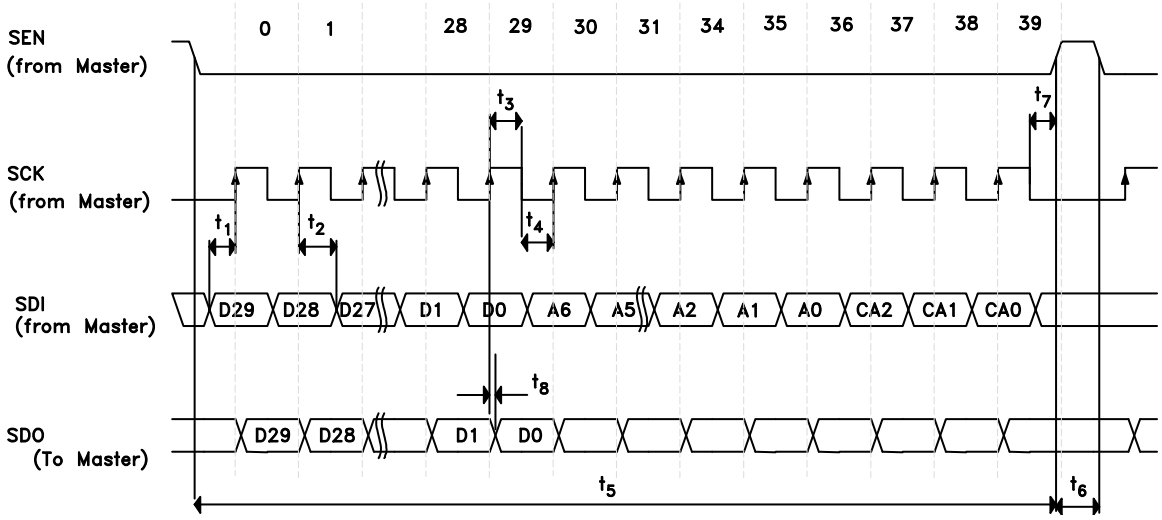


*Figure 28. SPI Timing Diagram*

DVDD = 5 V ±10%, GND = 0 V

### Table 7. Main SPI Timing Characteristics

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_1$ | SDI to SCK Setup Time | 8 | | | nsec |
| $t_2$ | SDI to SCK Hold Time | 8 | | | nsec |
| $t_3$ | SCK High Duration [1] | 10 | | | nsec |
| $t_4$ | SCK Low Duration | 10 | | | nsec |
| $t_5$ | SENb Low Duration | 20 | | | nsec |
| $t_6$ | SENb High Duration | 20 | | | nsec |
| $t_7$ | SCK to SENb [2] | 8 | | | nsec |
| $t_8$ | SCK to SDO out [3] | | | 8 | nsec |

[1] The SPI is relatively insensitive to the duty cycle of SCK.
[2] SENb must rise after the 32nd falling edge of SCK but before the next rising SCK edge. If SCK is shared amongst several devices this timing must be respected.
[3] Typical load to SDO is 10 pF, maximum 20 pF

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## Register Map

### Table 8. Reg 00h Chip ID, Soft Reset, Read Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [6:0] | R/W | Read Register Address | 7 | 0 | Address of the register to be read in the next cycle. |
| [7] | R/W | Soft Reset | 1 | 0 | Soft Reset. Writing 1 generates soft reset. Resets all the digital and registers to default states. Writing 0 resumes normal chip operation. |
| [31:8] | R/W | Chip ID | 24 | 97330h | Part Number, Description. Read reg00h returns chip ID. |

### Table 9. Reg 01h - Settings Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [0] | R/W | VCO Buffer Enable | 1 | 1 | Enables VCO input RF buffer. |
| [1] | R/W | Reserved | 1 | 1 | Write 0 to this bit. |
| [2] | R/W | AUXSPI Enable | 1 | 1 | Enables Auxiliary SPI. |
| [3] | R/W | Sigma Delta Enable | 1 | 1 | Enables Sigma Delta Function. |
| [4] | R/W | GPIO Enable | 1 | 1 | Enables output from all GPIO pins. |
| [5] | R/W | RF Divider Enable | 1 | 1 | Enables RF Divider. |
| [6] | R/W | Output Buffer Enable | 1 | 1 | Enables Divider Output Driver. |
| [7] | R/W | Bias Enable | 1 | 1 | Enables bias generator for all blocks. |
| [8] | R/W | PSCLK to Digital Enable | 1 | 1 | Enable Prescaler clock going to digital counters. |
| [9] | R/W | Unused | 1 | 1 | |

### Table 10. Reg 02h R-Divider Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [13:0] | R/W | R Divider Ratio | 14 | 1h | Local value for reference division ratio. |

#### Auxiliary SPI Registers

The following two registers define the communication through the AUXSPI. If the AUXSPI is enabled (Reg 04h[4] = 0), writes to AUXSPI are executed via Reg 03h. The auxiliary device address is expected in Reg 04h[2:0]. If DC - 7 GHz FRACTIONAL-N DIVIDER is working as a standalone frequency divider the AUXSPI clock is expected on the DNSAT pin, and Reg 04h[15] must be set to 1. It is recommended to disable AUXSPI when not used.

### Table 11. Reg 03h AUX. VCO Data Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [3:0] | R/W | AUXSPI Register Address | 4 | 0h | 4-bit Register address for the auxiliary device SPI. |
| [12:4] | R/W | AUXSPI Data | 9 | 000h | 9-bit long Register Data for the auxiliary device SPI. |



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### Table 12. Reg 04h - AUX. VCO Settings Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [2:0] | R/W | Auxiliary Device Address | 3 | 000h | Chip address used by AUXSPI. |
| [3] | R/W | Divide Clock by 4 for AUXSPI | 1 | 0 | 0 = Use XTAL for AUXSPI clock.<br>1 = Use XTAL divided by 4 for AUXSPI clock. |
| [4] | R/W | Start AUXSPI | 1 | 0 | 0 = Start AUXSPI when data is written to Reg03h.<br>1 = reserved. |
| [7:5] | R/W | Reserved | 3 | 4h | |
| [9:8] | R/W | Reserved | 2 | 2h | |
| [13:10] | R/W | Reserved | 4 | 8h | |
| [14] | R/W | Reserved | 1 | 0 | |
| [15] | R/W | Keep Xtal Gate Open | 1 | 0 | When 1, keeps the XTAL gate open to get XTAL from the companion PFD/CP chip HMC984LP4E. |
| [18:16] | R/W | Reserved | 3 | 0h | |

### Table 13. Reg 05h Integer Set-Point, Trigger Delay Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [19:0] | R/W | Integer Division Ratio | 20 | 200d | Sigma-Delta Modulator integer set point. Specifies the integer part of the division ratio for the RF Divider in fractional mode or the integer division ration in integer mode. |
| | | Ramp Trigger Delay | | | Also used as delay counter for hardware ramp trigger (Pin D4) in ramp mode. This value is valid when Reg 0Eh [11] = 1. |

### Table 14. Reg 06h Fractional Set-Point, Down Dwell Register (MSB)

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [29:0] | R/W | Fractional Division Ratio (MSB) | 30 | 0 | Most significant 30 bits to specify fractional set point for Sigma-Delta Modulator. Total Fractional bits are 48. |
| | | Down Dwell for Asymmetric Frequency. Ramp (MSB) | | | Defines the MSB portion of the dwell down time in the asymmetric frequency sweep mode, valid when Reg 0Eh[11]=1. |

### Table 15. Reg 07h Fractional Set-Point, Down Dwell Register (LSB)

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [17:0] | R/W | Fractional Division Ratio (LSB) | 18 | 0 | Least significant 18 bits to specify fractional set point for Sigma-Delta Modulator. Total Fractional bit are 48. |
| | | Down Dwell for Asymmetric Frequency. Ramp (LSB) | | | Defines the LSB portion of the dwell down time in the asymmetric frequency sweep mode, valid when Reg0E[11]=1. |

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### Table 16. Reg 08h GPIO Configuration Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [3:0] | R/W | GPO Output Select | 4 | 0h | Selects exported output signals to GPIO pins. See Table 5 for details. Master enable for GPIO Reg 01h[4] = 1 is required.· |
| [8:4] | R/W | GPO Static Test Value | 5 | 00000b | Static GPIO test signals for output (D4,D3,D2,D1,D0). Writing these value and reading them back test the GPIO functionality. Master enable for GPIO Reg 01h[4] = 1 is required.· |
| [13:9] | R/W | GPO Pin Enable | 5 | 11111b | Independent GPIO pin enables.<br>Reg08[13] = 0 - D4 input<br>Reg08[13] = 1 - D4 output<br>Reg08[12] = 0, D3 input<br>Reg08[12] =1, D3 output<br>Reg08[11] = 0, D2 input<br>Reg08[11] = 1, D2 output<br>Reg08[10] = 0, D1 input<br>Reg08[10] = 1, D1 output<br>Reg08[9] = 0, D0 input<br>Reg08[9] = 1, D0 output<br>Master enable for GPIO Reg 01h[4] = 1 is required. |

### Table 17. Reg 09h Companion Chip Address Local Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [2:0] | R/W | Counterpart HMC984LP4E Chip Address | 3 | 2h | Chip address of the companion chip HMC984LP4E. |

### Table 18. Reg 0Ah Sigma Delta Modulator Seed MSB Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [29:0] | R/W | Seed MSB | 30 | 4241h | Most significant bits of the Seed for the 1st accumulator in Sigma-Delta Modulator. |

### Table 19. Reg 0Bh Sigma Delta Modulator Seed LSB Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [17:0] | R/W | Seed LSB | 18 | 10081h | Least significant bits of the Seed for the 1st accumulator in Sigma-Delta Modulator. |

### Table 20. Reg 0Ch Ramp NSTEP Down MSB Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [29:0] | R/W | Down Ramp Number of Steps (MSB) | 30 | 0h | Most significant bits of the number of steps for the frequency ramp in down direction in sweep mode. |

### Table 21. Reg 0Dh Ramp NSTEP Down LSB Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [17:0] | R/W | Down Ramp Number of Steps (LSB) | 18 | 0h | Least significant bits of the number of steps for the frequency ramp in down direction in sweep mode. |



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### Table 22. Reg 0Eh Sigma Delta Modulator Configuration Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [1:0] | R/W | SD Modulator Type | 2 | 11b | DSM Type.<br>00 = MASH1 - Reserved<br>01 = MASH11 - Reserved<br>10 = MASH111 - Delta Sigma Modulator Mode B<br>11 - Delta Sigma Modulator Mode A |
| [2] | R/W | Ramp Auto Repeat Control from SPI | 1 | 0 | Recommended to write 1 to this bit in ramp mode. When this bit is 1, the ramp will repeat itself if ramp_auto_repeat_on/off_from_spi is 1 at the end of the each sweep. |
| [3] | R/W | Ramp Auto Repeat Control from SPI On/Off | 1 | 0 | Ramp will automatically repeat itself if this bit is 1 and bit 2 is also set to 1. |
| [6:4] | R/W | Integer Path Delay | 3 | 111 | Delay through the integer signal path to compensate for the fractional path.<br>000 = no delay.<br>110 = 6 clock cycles delay.<br>111 = Automatic. |
| [7] | R/W | Ramp Start Delay Enable | 1 | 0 | Delay the start of sweep as defined in Reg 05h |
| [8] | R/W | Autoseed Mode Enable | 1 | 1 | Reseed when changing the frac setpoint. |
| [9] | R/W | Phase Step | 1 | 0 | 1 = Enable Phase Step feature. Autoseed Mode must be disabled for Phase Step (Reg 0Eh [8] = 0. Seed Reg Ah & Reg Bh set the phase advance/retard in 2's complement formate. Phase Step takes effect when Reg 0Ah is written. Each time registers are written phase will advance/retard by the amount specified. |
| [10] | R/W | Maintain DSM State Enable | 1 | 0 | Maintain DSM state within the same integer boundary. |
| [11] | R/W | Ramp Mode Enable | 1 | 0 | Puts DSM in frequency sweeper (ramp) mode. |
| [12] | R/W | Ramp Start from SPI | 1 | 0 | Start ramp signal from SPI. |
| [13] | R/W | Start Ramp from Ext. Trigger | 1 | 0 | Allow external trigger to manipulate ramp. |
| [14] | R/W | Bypass All | 1 | 0 | Bypass Delta Sigma Modulator. Place synthesizer in Integer Mode without disabling the DSM. |
| [18:15] | R/W | CSP Step Size | 4 | 1111b | Cycle Slip Prevention (CSP) step size. In a PLL configuration with the HMC984LP4E one step is equivalent to one divided VCO cycle, and step size is the number of VCO cycles. |
| [19] | R/W | External DSM Sequence Enable | 1 | 0 | Use external DSM sequence imported through GPIO Port. |
| [20] | R/W | Use Falling Edge of DSM Clock for External Sequence | 1 | 0 | Use falling edge of SD clock to get the external sequence. |
| [21] | R/W | Lock using External Trigger Pin | 1 | 0 | Allow external trigger to start locking process. Writing to the Integer or Fractional Division ratio registers does not have any effect when this bit is set to 1. PLL will lock only when external trigger goes high. |
| [22] | R/W | Symmetrical Ramp Mode | 1 | 1 | Use symmetric frequency sweeping for up and down directions otherwise DN parameters are taken from Registers Reg 0Ch, Reg 0Dh, Reg 19h and Reg 1Ah for asymmetric mode. |
| [23] | R/W | Integer Mode Lock Strobe | 1 | 0 | Re-lock when integer set-point Reg 06h is updated. |
| [24] | R/W | Singlestep Ramp Mode Enable | 1 | 0 | Single-step the ramp. Each step of the ramp must be popped by strobe (either SPI or Hardware pin). |
| [25] | R/W | Single Direction Ramp Mode Enable | 1 | 0 | Single direction mode for ramp (ramp one way, pop to base the other way). |
| [26] | R/W | Ramp Start Direction | 1 | 1 | Starting direction of ramp. It is only loaded while rampmode = 0.<br>1 = Positive<br>0 = Negative |

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| | | | | | |
|---|---|---|---|---|---|
| [27] | R/W | Use External Clock for DSM | 1 | 0 | 1 = Use external clock from GPIO pin to clock DSM. |
| [28] | R/W | Reserved | 1 | 0 | |
| [29] | R/W | Use x16 CSP Step | 1 | 0 | 1 = Increase the CSP step size given in bits [18:15] by a factor of 16. |

### Table 23. Reg 0Fh VCO Divider Configuration Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [0] | R/W | Increase Divider Pulse width to DSM | 1 | 0 | Increase the width of the clock pulse going to DSM (available only when division ratio > 64). |
| [1] | R/W | Increase Divider Pulsewidth to PFD | 1 | 1 | Increase pulse width (low duration) of the clock going to PFD. |
| [4:2] | R/W | Output Buffer Current Select | 2 | 011b | Sets current for divider output buffer. Helps to control voltage swing for various impedance options.<br>000 = 5mA<br>001 = 7.5mA<br>010 = 10mA<br>011 = 12.5mA<br>100 = 10mA<br>101 = 12.5mA<br>110 = 15mA<br>111 = 17.5mA |
| [5] | R/W | Reset RF Divider | 1 | 0 | Resets the RF Divider. |
| [8:6] | R/W | Divider Resynch Bias Select | 3 | 011b | Bias current setting for divider resync. Default value recommended. |
| [11:9] | R/W | RF Buffer Bias Select | 3 | 001b | Bias current setting for input RF buffer. Default value recommended. |
| [14:12] | R/W | Divider Pulsewidth Select | 3 | 011b | Divider output pulse width control.<br>000 = 5 VCO cycles.<br>001 = 13 VCO cycles.<br>010 = 21 VCO cycles.<br>011 = 29 VCO cycles.<br>100 = 37 VCO cycles.<br>101 = 45 VCO cycles.<br>110 = 53 VCO cycles.<br>111 = 61 VCO cycles. |

### Table 24. Reg 10h Ramp DWELL Symmetrical or Up MSB Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [29:0] | R/W | Symmetric Ramp Dwell (MSB) | 30 | 0 | Represents MSB's for ramp dwell time in up and down directions for symmetric frequency sweep mode. In asymmetric mode it represents the up dwell time only. |

### Table 25. Reg 11h Ramp DWELL Symmetrical or Up LSB Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [17:0] | R/W | Symmetric Ramp Dwell (LSB) | 18 | 0 | Represents LSB's for ramp dwell time in up and down directions for symmetric frequency sweep mode. In asymmetric mode it represents the up dwell time only. |

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### Table 26. Reg 12h Ramp Step Size Symmetrical or Up MSB Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [29:0] | R/W | Symmetric Ramp Step Size (MSB) | 30 | 0 | Represents the MSB for ramp step size in up and down directions for symmetric frequency sweep mode. In asymmetric mode it represents the up step size only. |

### Table 27. Reg 13h Ramp Step Size Symmetrical or Up LSB Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [17:0] | R/W | Symmetric Ramp Step Size (LSB) | 18 | 0 | Represents the LSB for ramp step size in up and down directions for symmetric frequency sweep mode. In asymmetric mode it represents the up step size only. |

### Table 28. Reg 14h Ramp NSTEP Symmetrical or Up MSB Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [29:0] | R/W | Symmetric Ramp Number of Steps (MSB) | 30 | 0 | Represents the MSB of the number of steps for the frequency ramp in up and down directions in symmetric frequency sweep mode. In asymmetric mode it represents the number of steps in up direction only. |

### Table 29. Reg 15h Ramp NSTEP Symmetrical or Up LSB Register

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [17:0] | R/W | Symmetric Ramp Number of Steps (LSB) | 18 | 0 | Represents the LSB of the number of steps for the frequency ramp in up and down directions in symmetric frequency sweep mode. In asymmetric mode it represents the number of steps in up direction only. |

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**Table 30. Reg 16h DSM Configuration Register**

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [1:0] | R/W | DSM 1st Accumulator Size | 2 | 00b | DSM 1st accumulator width.<br>00 = 48 bits<br>01 = 32 bits<br>10 = 24 bits<br>11 = 16 bits |
| [3:2] | R/W | DSM 2nd Accumulator Size | 2 | 00b | DSM 2nd accumulator width.<br>00 = 48 bits<br>01 = 32 bits<br>10 = 24 bits<br>11 = 16 bits |
| [5:4] | R/W | DSM 3rd Accumulator Size | 2 | 00b | DSM 3rd accumulator width.<br>00 = 48 bits<br>01 = 32 bits<br>10 = 24 bits<br>11 = 16 bits |
| [8:6] | R/W | Disable Frac. Register Clock | 3 | 000b | Clock gates for the 3 accumulators (fractional part), 1 disables the clock. |
| [11:9] | R/W | Disable Integer Register Clock | 3 | 000b | Clock gates for the 3 accumulators (integer part), 1 disables the clock. |
| [12] | R/W | Disable DSM Mode A Clock | 1 | 0 | 1 = Disable Delta Sigma Modulator Mode A Clock |
| [13] | R/W | Disable DSM Mode B Clock | 1 | 0 | 1 = Disable Delta Sigma Modulator Mode B Clock |
| [14] | R/W | Reserved | 1 | 0 | |
| [15] | R/W | Disable Integer Path Clock | 1 | 0 | 1 = Disables Integer Path Clock |
| [16] | R/W | Disable Input Buffer Clock | 1 | 0 | 1 = Disables Input Buffer Clock |
| [17] | R/W | Disable Output Buffer Clock | 1 | 0 | 1 = Disables Output Buffer Clock |
| [18] | R/W | Reserved | 1 | 0 | |
| [19] | R/W | Reserved | 1 | 0 | |

**Table 31. Reg 17h This Register does not exist**

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| This Register does not exist | | | | | |

**Table 32. Reg 19h Ramp Down Step Size MSB Register**

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [29:0] | R/W | Ramp Step Down MSB. | 30 | 0 | Represents MSB's to define the step size for the ramp in down direction in ramp mode. |

**Table 33. Reg 1Ah Ramp Down Step Size LSB Register**

| BIT | TYPE | NAME | W | DEFLT | DESCRIPTION |
|---|---|---|---|---|---|
| [17:0] | R/W | Ramp Step Down LSB. | 18 | 0 | Represents LSB's to define the step size for the ramp in down direction in ramp mode. |

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