HMC981LP3E

v01.0411

ACTIVE BIAS CONTROLLER

Typical Applications

- Microwave Radio & VSAT
- Military & Space
- Test Instrumentation
- Fiber Optic Modulator Driver Biasing
- CATV Laser Driver Biasing
- Cellular Base Station
- Wireless Infrastructure Equipment

Features

Automatic Gate voltage adjustment (No Calibration required)
Supply Voltage: 4V to 12V

Digital Voltage: 3.3V to 5V

Controls both Enhancement and Depletion type devices

Adjustable Drain Current up to 200mA

Sink/Source Gate Current Capability

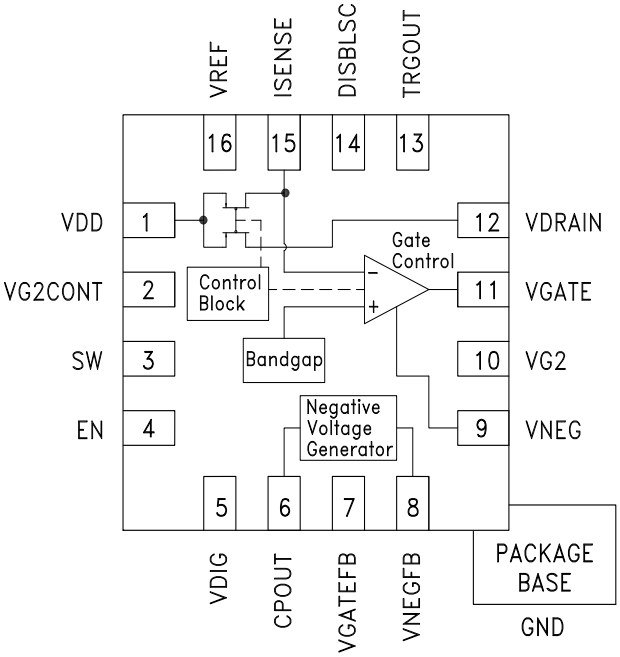
Optional Internal negative voltage generation that can be disabled to use external negative rail

Fast Enable/Disable

Trigger-out Output for Daisy Chain Power-Up and Power-Down Sequencing

16 Lead 3x3 mm SMT Package: 9 mm²

Functional Diagram



General Description

HMC981LP3E is an active bias controller that automatically adjusts the gate voltage of an external amplifier to achieve constant bias current. It can be used to bias any enhancement and depletion type amplifiers operating in Class-A regime with Drain voltages from 4V to 12V and drain currents up to 200mA, offering a complete biasing solution.

HMC981LP3E achieves excellent bias stability over supply, temperature and process variations, and eliminates the required calibration procedures usually employed to prevent RF performance degradation due to such variations.

The HMC981LP3E is housed in an RoHS compliant 3x3 mm QFN leadless package with an exposed backside pad to improve thermal characteristics.

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Electrical Specifications, T_A = +25°C, VDD=8V, VDIG= 3.3V, Depletion Master

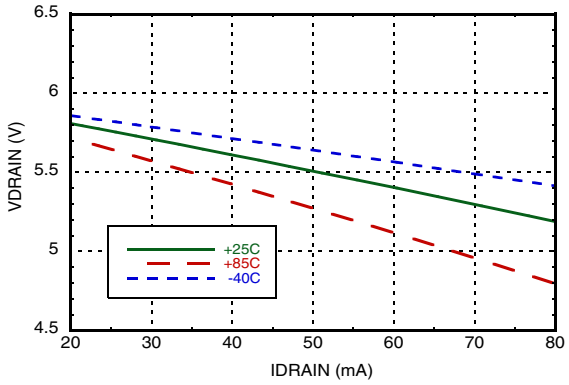
Unless Otherwise Noted

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Supply Voltage	Vdd			4		12	V
VDD Quiescent Current	IDD	VDD = 4V	EN = VDIG		7		mA
			EN = GND		3		mA
		VDD = 8V	EN = VDIG		7.5		mA
			EN = GND		4		mA
VDIG Quiescent Current	IDIG	VDIG= 3.3 V			3		mA
		VDIG= 5 V			5		mA
Negative Voltage Output	VNEG				-2.5		V
Oscillator Frequency	FOSC				300		kHz
Voltage Reference	VREF				1.42		V
Enable Input Threshold	ENTHRS	Vinlow				1	V
		Vinhigh		1.4			V
Switch Input Threshold	SWTHRS	Vinlow				1	V
		Vinhigh		1.4			V
Short Circuit Disable Input Threshold	DSCTHRS	Vinlow				1	V
		Vinhigh		1.4			V
VDRAIN Characteristics							
DRAIN Current Adjustment Range	IDRAIN	SW=GND		20		80	mA
		SW=VDIG		80		200	mA
DRAIN Current Change Over Digital Voltage	ΔIDRAINV	VDRAIN set to 8V, IDRAIN set to 160 mA			0.4		%/V
DRAIN Current Change Over Temperature					0.02		%/C
DRAIN Range	VDRAIN			4		12	V
VDRAIN Change Over Temperature	ΔVDRAIN	VDRAIN set to 8V, IDRAIN set to 160 mA			1.5		%/C
VNEG Characteristics							
Negative Voltage Output	VNEG				-2.5		V
VNEG Current Sink	INEG	VDD= 4V		0		8	mA
		VDD= 8V		0		15	mA
VGATE Characteristics							
GATE Current Supply	IG			-0.8		0.8	mA
VGATE Low Level	VG_MIN				VNEG		V
VGATE High Level	VG_MAX				VNEG+4.5		V
VG2 Characteristics							
VG2 Current Supply	IG2	VG2<1.5V		-0.1		0.1	mA
		VG2>1.5V		-1		1	mA
VG2 Adjustment Range	VG2			1		VDD-1.3	V
VDIG Characteristics							
Adjustment Range	VDIG			3.3		5	V
VDIG Quiescent Current	IDIG	VDD= 8 V, VDIG=EN =3.3 V			3		mA
SW Characteristics							
Internal Switch Resistance	RDS_ON	SW= GND			10		Ohm
		SW=VDIG			5		Ohm

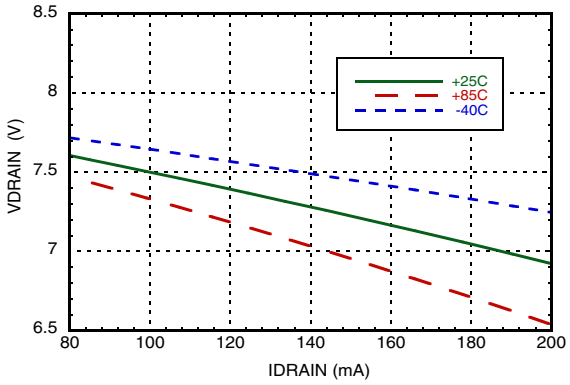
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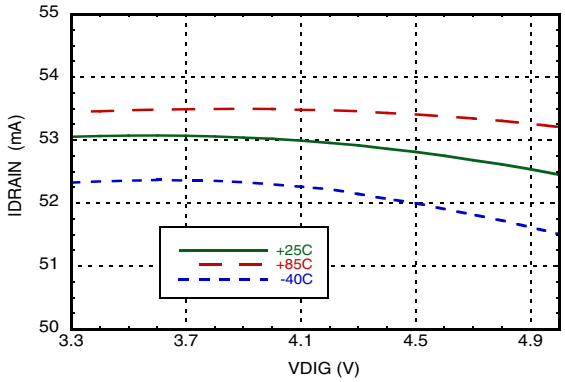
Load Regulation @ VDD=6V, VDIG=3.3V, SW=GND



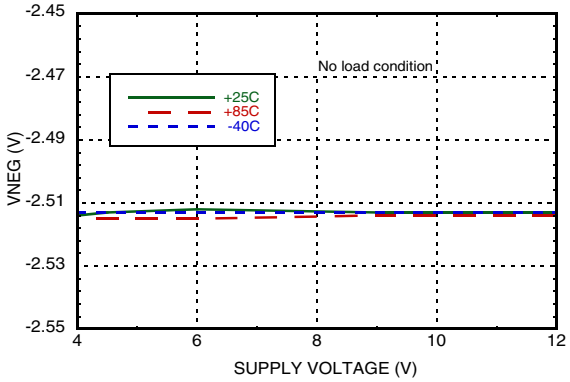
Load Regulation @ VDD=8V, SW=VDIG=3.3V



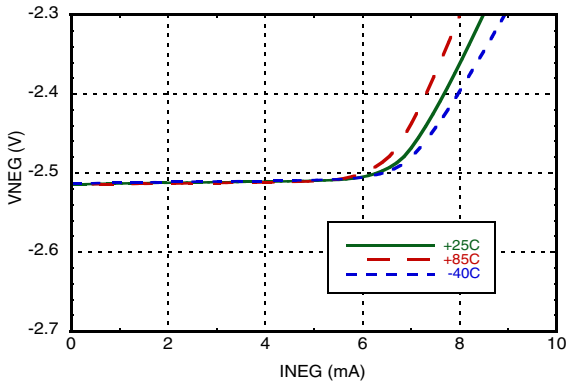
IDRAIN vs. VDIG[1][2]



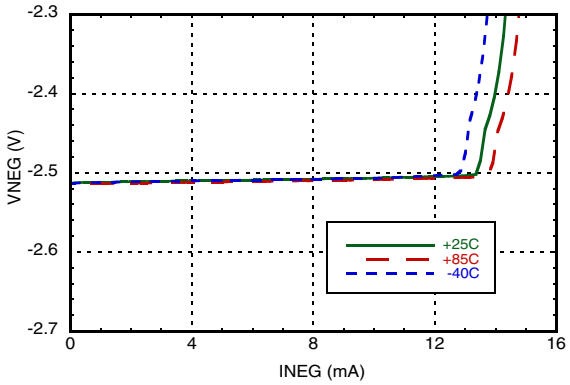
VNEG Line Regulation vs. Supply Voltage



VNEG Load Regulation @ VDD=4V



VNEG Load Regulation @ VDD=12V



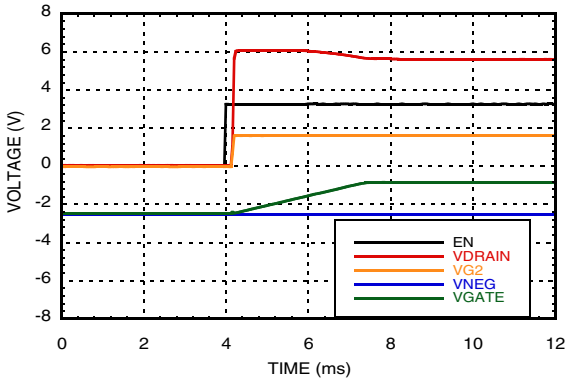
[1] IDRAIN is set to 53 mA

[2] HMC465LP5 is used as external amplifier

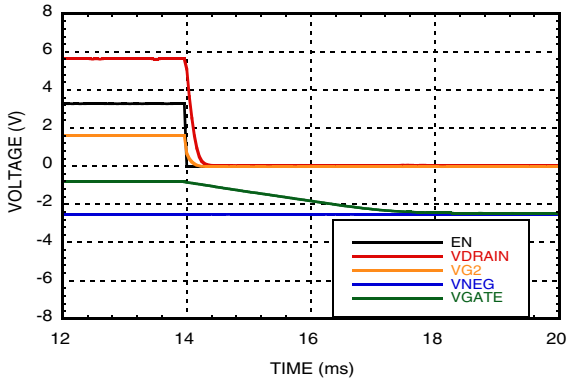
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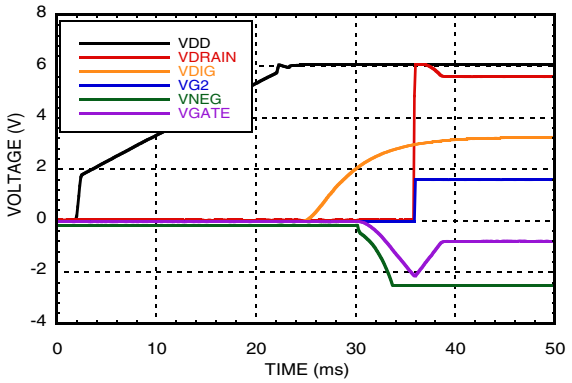
Enable Waveform



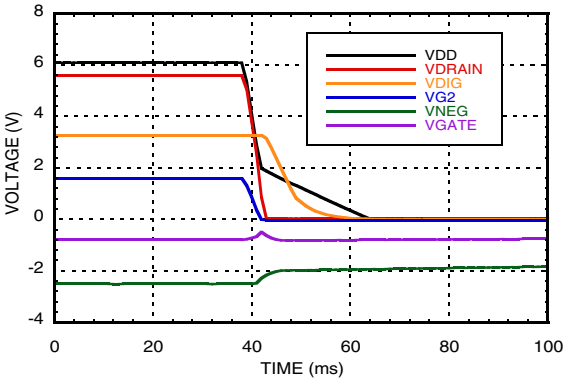
Disable Waveform



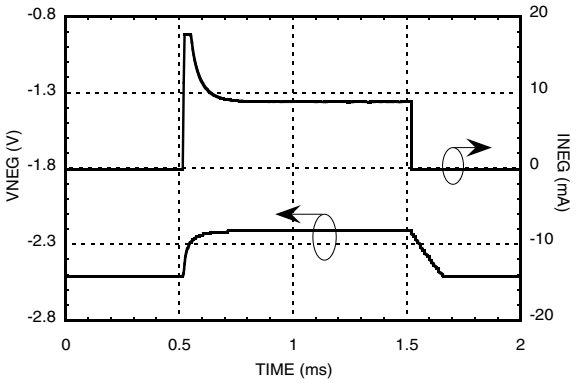
Power Up Waveform



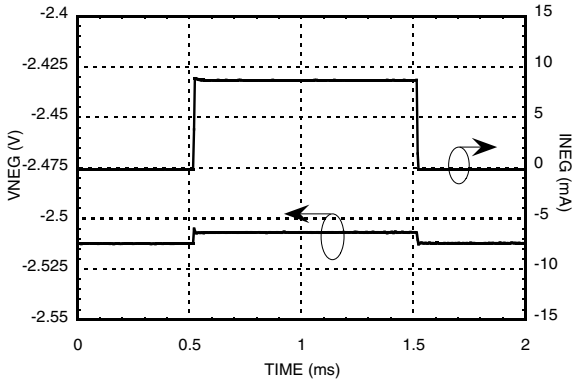
Shutdown Waveform



VNEG Load Transient VDD=4V



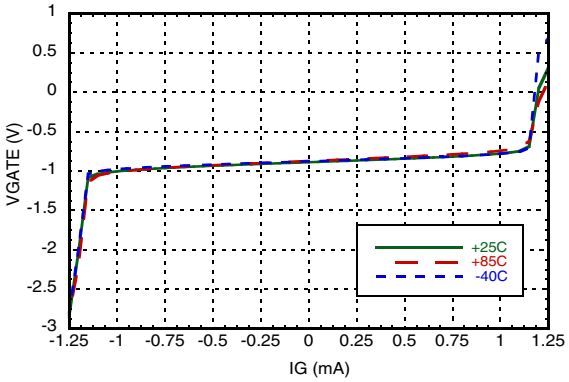
VNEG Load Transient VDD=6V



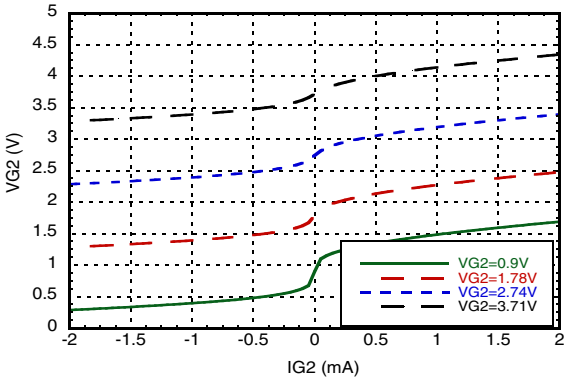
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VGATE Load Regulation @ VDD=6V



VG2 Load Regulation @ VDD=6V



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Absolute Maximum Ratings [1]

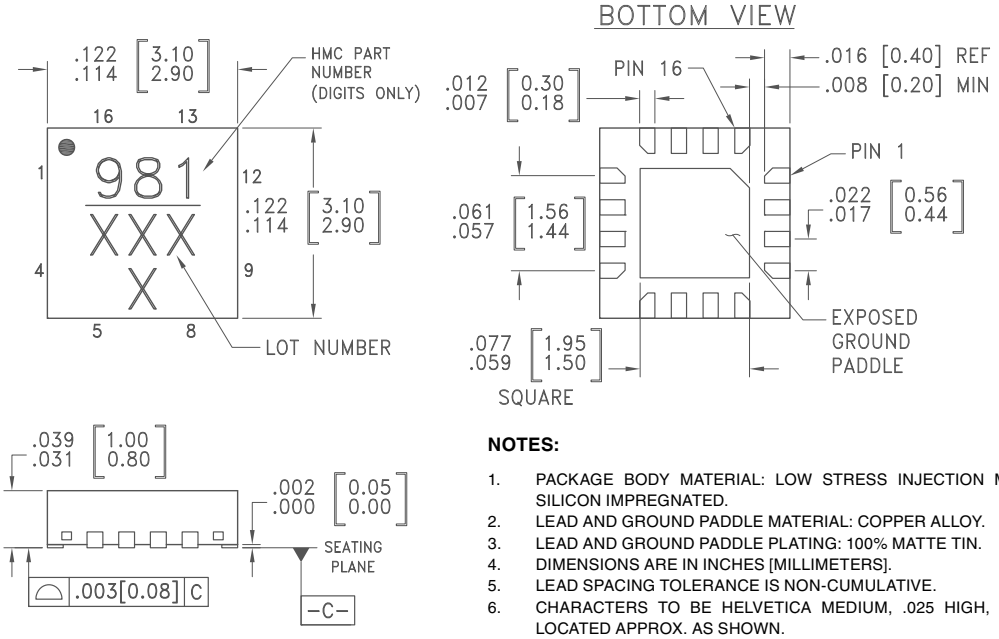
VDD	12V
VG2_CONT, VDRAIN	-0.5V to VDD + 0.5V
SW, EN, CP_OUT, VGATEFB, VNEGFB, TRIG_OUT, DISBL_SC, ISENSE	-0.5V to VDIG + 0.5V
VDIG	5.5V
VNEG	-4V to GND
VG2	-0.5V to VDD + 0.5V
Junction Temperature	125 °C
Continuous Pdiss (T = 85 °C) (Derate 19.19 mW/°C above 85 °C)	0.77 Watts

Thermal Resistance (R_{TH}) (Junction to package bottom)	52.1 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1B

Note that there are two different voltage domains on HMC981LP3E; a high voltage domain Vdd, and a low voltage domain VDIG. Take necessary precautions not to violate ABS MAX ratings of each subdomains.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.05mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

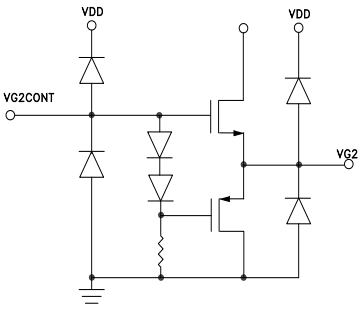
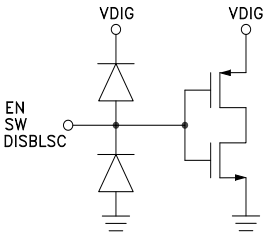
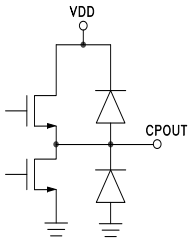
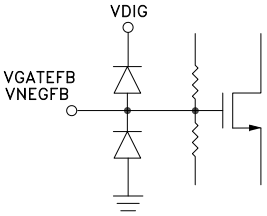
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC981LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H981 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

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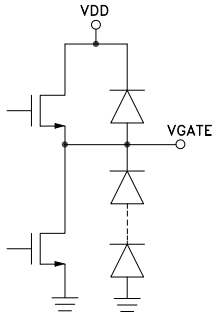
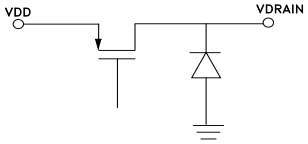
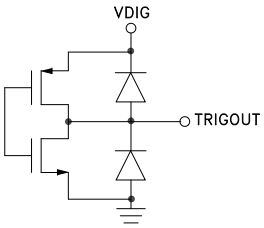
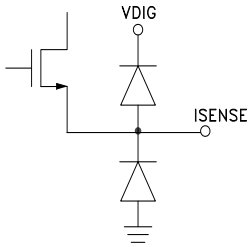
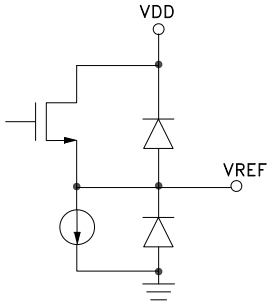
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 5	VDD, VDIG	Bias supply Pin. Connect supply voltage to this pin with appropriate filtering.	
2	VG2CONT	Control voltage of the VG2. Use a resistor divider between VDD and GND to set the voltage. VG2 is typically 1.3V lower than the VG2CONT	
10	VG2	Second gate control.	
3	SW	Internal switch resistance control pin. If left floating, VSW defaults to HIGH.	
4	EN	Enable pin. System is enabled when Ven is HIGH (VDIG). If left floating, Ven defaults to HIGH (enabled).	
14	DISBLSC	Disables short circuit lock down when pulled to ground. Leave it floating to enable short circuit lock down.	
6	CPOUT	Negative voltage generator charge pump output. Negative voltage generator needs a flying capacitor, a reservoir capacitor and two diodes to operate. Please refer to the application schematic for more info.	
7	VGATEFB	Control pin for VGATEFB. Float VGATEFB when a depletion mode transistor is biased. Selects the mode of operation along with VNEGFB pin. For detailed usage please refer to the Table 2.	
8	VNEGFB	Feedback (Control) pin for Negative Voltage Generator Charge Pump. Float to activate the negative voltage generator / Sort to GND to disable the negative voltage generator.	
9	VNEG	Negative input to the chip. Should be supplied with CPOUT when negative voltage generator is enabled, or connect to external VSS when negative voltage generator is enabled. For detailed usage please refer to the “Negative Voltage Generator” section.	

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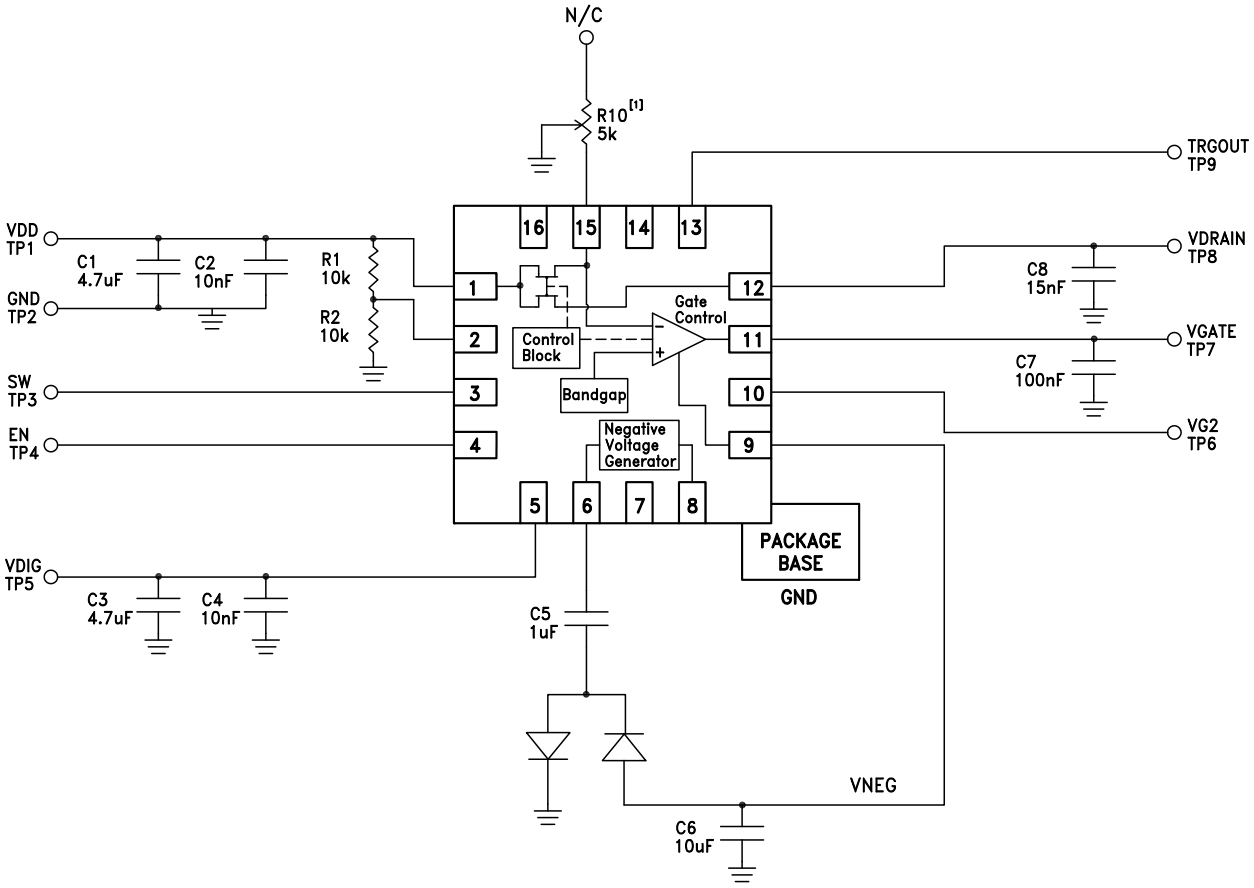
Pin Descriptions *(Continued)*

Pin Number	Function	Description	Interface Schematic
11	VGATE	Gate Control pin for external amplifier. Connect to the gate (base) of the external amplifier. In order to guarantee stability,a 10µF capacitor should be connected between the gate (base) terminal of the external amplifier and GND as close to the amplifier as possible.	
12	VDRAIN	Drain voltage. Should be connected to the supply terminal of the external amplifier. A minimum 100 nF capacitor has to be placed close to the external amplifier to improve load regulation.	
13	TRIGOUT	Trigger out signal. Generates a HIGH (3.5V) signal when the active bias system stabilizes. This signal can be used to trigger next device (ENABLE) if more than one HMC981LP3E is used in a daisy chain.	
15	ISENSE	To adjust the bias current of the external amplifier connect a resistor (Rsense) from ISENSE pin to GND. Use Eqn.2 to determine the required Rsense value.	
16	VREF	1.5V reference voltage. 0.1uF or greater capacitor to GND is needed for noise filtering.	

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Evaluation Board Circuit



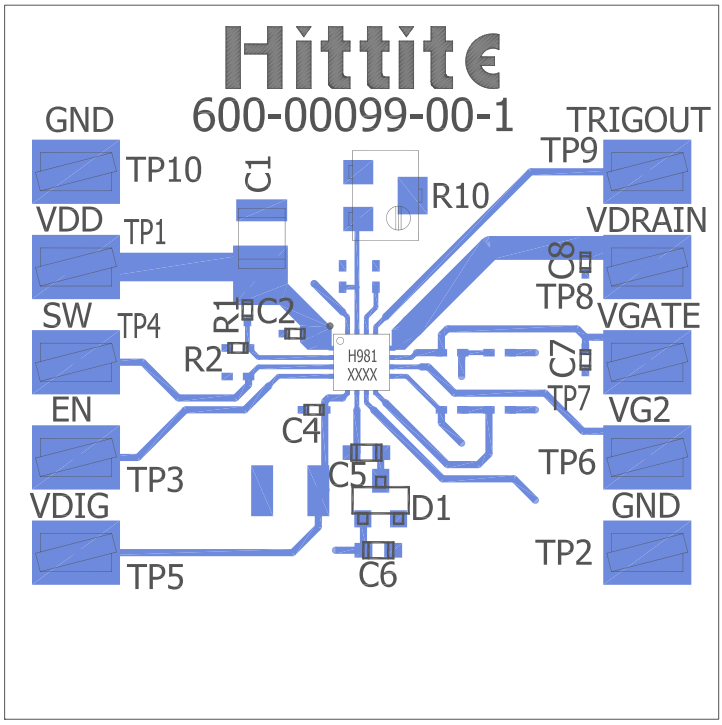
Notes:

[1] A variable resistor is assembled on R10 slot to adjust bias current for evaluating various different amplifiers without soldering.

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Evaluation PCB



List of Materials for Evaluation PCB EVAL01-HMC981LP3E [1]

Item	Description
TP1-10	Test Point
C1	4.7 µF Capacitor, 1210 Pkg.
C2, C4, C8	10 nF Capacitor, 0402 Pkg.
C5	1 µF Capacitor, 0603 Pkg.
C6	10 µF Capacitor, 0603 Pkg.
C7	0.1 µF Capacitor, 0402 Pkg.
D1	Dual Series Shottky Diode, BAT54SLT1
R1	10k Ohm Resistor, 0402 Pkg.
R2	4.02k Ohm Resistor, 0402 Pkg.
R10	Trim Potentiometer
U1	HMC981LP3E Active Bias Controller
PCB [2]	600-00099-00-1 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: FR4

Careful PCB layout is critical to achieve stable and low noise operation. The negative voltage generator charge pump stage requires particular attention.

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Application Notes

Detailed Description

The HMC981LP3E is a fully-integrated Active Bias Controller (ABC) that automatically adjusts the gate voltage of amplifiers operating in the Class-A regime. With an internal feedback the automatic gate voltage control achieves constant quiescent bias through the amplifier under bias, independent of temperature and amplifier threshold variations. The quiescent current is adjusted with a resistor connected externally. The HMC981LP3E employs an integrated control circuitry to achieve safe power-up and power-down sequencing of the targeted amplifier. The HMC981LP3E can provide auto-bias solution virtually any amplifier in the market (both enhancement and depletion type) with a quiescent current of up to 200 mA and a supply voltage of up to 12V.

The HMC981LP3E has an integrated negative voltage generator to synthesize negative voltages required to drive depletion mode amplifiers. If an external negative supply is already available or an enhancement mode device is targeted, the negative voltage generator can be disabled.

The HMC981LP3E achieves excellent bias stability over supply and temperature variations with low supply voltage down to 4V. The gate control can both sink and source current (±0.8 mA) to achieve constant bias current over input power variations applied to the amplifier. The HMC981LP3E also generates a second gate voltage (VG2). VG2 can be adjusted through a resistor divider connected to VDD for amplifiers which require second gate voltage.

The HMC981LP3E ensures the protection of the external amplifier during turn on/off by adjusting the sequence of VDRAIN, VGATE and VG2 outputs. HMC981LP3E controls the bias current of the amplifier under bias with the gate control driver. The current passing through the amplifier is continuously sampled and is used to control the VGATE voltage connected to the gate of the amplifier.

The HMC981LP3E employs a SW pin to control RDS_ON resistance of the internal switch between VDD and VDRAIN. Refer to the section under the “Supply and Drain Voltage” section for details.

The HMC981LP3E has a built-in short circuit protection feature to protect both itself and the amplifier under bias against short circuit conditions at the VDRAIN output. Refer to the section under the “Short Circuit Protection” section for details.

Digital Power Supply (VDIG)

The HMC981LP3E requires an external low voltage bias rail (3.3V to 5.0V). VDIG powers the internal logic circuitry. VDIG draws an average of 3 mA from a 3.3V. VDIG can accept voltages up to 5.0V.

Supply and Drain Voltage (VDD and VDRAIN)

The VDD supply to the HMC981LP3E is directly connected to the VDRAIN output through an internal MOSFET switch. This internal MOSFET is controlled through power-up sequencing which ensures that no voltage is applied to drain of the external amplifier until the gate voltage is pulled down to VNEG(ensuring external amplifier is pinched-off). The VDRAIN output of the HMC981LP3E should be connected to the drain (collector) of the amplifier under bias for the active bias control feedback and power-up/down sequencing to work.

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There will be a voltage drop from VDD to VDRAIN due to finite RDS_ON resistance of the internal switch. To compensate for this voltage drop choose the VDD value as shown in equation (1).

$$VDD = VDRAIN + IDRAIN \times RDS_ON \qquad (1)$$

where VDRAIN is the supply voltage of the external amplifier and IDRAIN is the desired constant bias current through the external amplifier.

Note that RDS_ON resistance of the internal FET switch can be adjusted through SW pin. RDS_ON is typically equal to 5 Ohms when SW is pulled up to VDIG, and is typically equal to 10 Ohms when SW is pulled down to GND. If SW is left floating, it is pulled up to VDIG through an internal weak pull-up. Recommended settings for the SW position are given in Table-1. Not using the HMC981LP3E in the recommended settings will increase the power dissipation of the part and may increase the part-to-part variation.

Table 1. Recommended Current Range Configuration

Current Range (mA)	Condition	RDS_ON (Ohm)
20 to 80	SW=GND	10
80 to 200	SW=VDIG	5

Negative Voltage Generator (VNEGOUT)

The HMC981LP3E has an internally regulated charge pump block to generate negative voltage (VNEGOUT) required for depletion mode devices. The HMC981LP3E generates -2.5V at the VNEGOUT output in default configuration. It requires two diodes and two capacitors connected externally as shown in the sample application schematics. The HMC981LP3E is designed to reject the ripple on the VNEGOUT by isolating VNEGOUT from the VGATE. The negative voltage is only required for depletion mode devices, and it can be disabled through the VGATEFB and VNEGFB pins. Where an enhancement device is targeted or a negative supply is already available in the system, simply connect the available negative supply to the VNEG pin. See Table-2 for detail on how to set this operation mode.

Enable/Disable (EN)

The active bias control loop is enabled when EN is pulled up to VDIG, and it is disabled when it is pulled down to GND. If EN is left floating HMC981LP3E is enabled through an internal weak pull-up. Note that VNEG operation is independent of EN condition. EN signal controls the operation of only VGATE, VG2 and VDRAIN outputs. When EN pulled down to GND, the HMC981LP3E discharges VDRAIN and VG2 down to GND and it pulls the VGATE down to VNEG. Please see the “Active Bias Control Loop” section for detailed explanation.

Active Bias Control Loop

The HMC981LP3E regulates the bias current (IDRAIN) of the amplifier under bias through VGATE output connected to the gate of the external amplifier. In this closed loop operation the current passing through the amplifier under bias is sampled and is used to adjust VGATE to achieve constant quiescent bias through the external amplifier.

The HMC981LP3E continuously compensates for any supply, temperature, process variations and threshold drifts due to aging. The part-to-part, temperature, and supply variation of the HMC981LP3E is excellent. Thus, by using an accurate sense resistor connected to the ISENSE pin, expensive calibration procedures in high volume production could be avoided.

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The gate control of the HMC981LP3E is designed to both sink and source current in to the gate of the targeted amplifier (at least ±0.8 mA). This unique feature is important to achieve nearly constant quiescent bias through the amplifier under varying gate current at different input power values.

The bias current passing through the external amplifier can be adjusted with RSENSE, where RSENSE is the R10 connected from ISENSE to GND. Use the relation given in equation (2) to set the desired bias current through the external amplifier.

$$IDRAIN=32/Rsense\ (A) \qquad (2)$$

Self Protection Feature

Due to the small resistance of the internal switch FET a large amount of current may flow through the HMC981LP3E. HMC981LP3E limits the maximum current to protect itself under such fault conditions, by turnung of VDRAIN and VGATE.

The HMC981LP3E will remain in this protection mode until a full power-cycle or enable/disable cycle is applied.

VNEG Fault Detection Feature

In depletion mode operation VNEG is continuously monitored against short circuit fault to GND. If VNEG rises above a preset value (typically -1V) the system and the external amplifier are disabled by pulling VDRAIN and VG2 to GND and VGATE to VNEG. The system will stay in this stand-by mode until short fault at VNEG is fixed.

Power-up and Enable Sequencing

To ensure the protection of the external amplifier, the HMC981LP3E provides a power-up sequence for enabling active bias control loop. During start-up VDRAIN and VG2 are kept at GND while VGATE is taken to the most negative supply available (VGATE=VNEG). This ensures that external amplifier is completely pinched-off before VDRAIN is applied. When EN signal is received, VDRAIN is applied and the active bias loop is enabled. After the VDRAIN is applied, VG2 is generated. The final phase of the power-up sequence is completed by increasing the VGATE linearly until the set IDRAIN value is achieved.
For power-down and disabling the same sequencing is applied in the reverse order.

Daisy-Chain Operation

HMC981LP3E produces a trigger out signal (TRIGOUT pin#13) when VDRAIN output is enabled. This trigger signal can be used to enable additional HMC981LP3E chips in a chain of amplifiers. The triggering sequence can be routed in any way, from input to output, or from output to input depending on the use. Figure-1 presents a sample use of three HMC981LP3Es in an amplification chain. Please note that, only one of the HMC981LP3E is used to generate the negative voltage and the remaining HMC981LP3E is set to receive external negative voltage (which is provided from the master HMC981LP3E). Generating negative voltage from a single HMC981LP3E reduces the number of the components in the system, and decreases the over all current consumption..

Please note that, to ensure proper start-up, the system enable signal should be applied to the chip that has the negative voltage generator.

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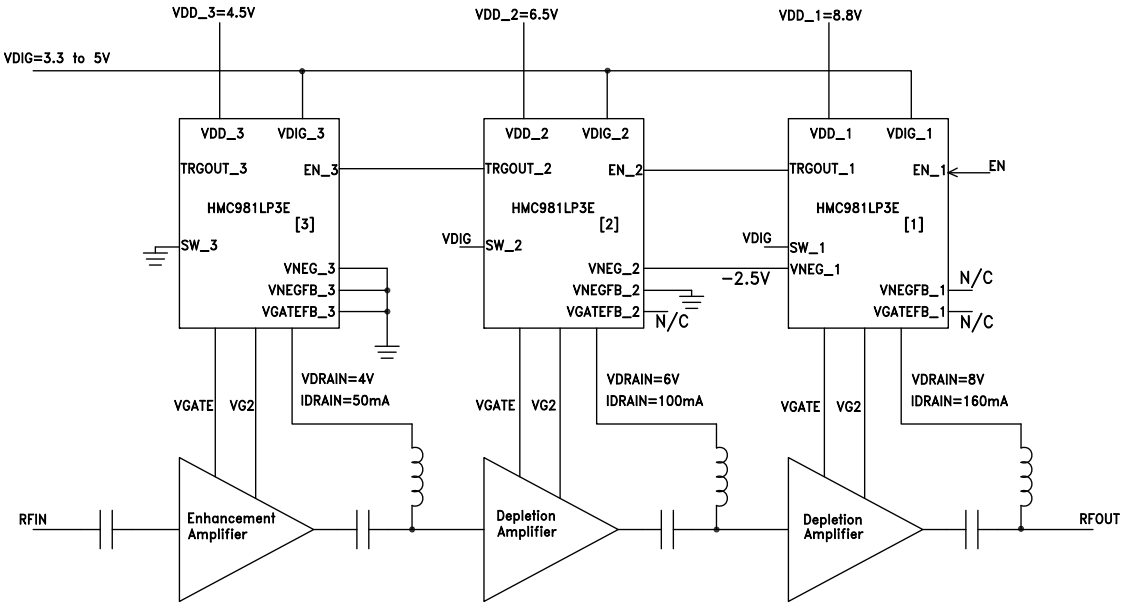


Figure 1. *Daisy Chain Operation*

Operation Modes

HMC981LP3E can be configured to bias both enhancement and depletion mode external amplifiers. The mode of operation can be selected by setting two pins (VNEGFB, VGATEFB) as tabulated in Table-2. The connection to the VNEGIN should be adjusted accordingly.

In order not to bias external amplifier in a wrong region, please make sure that the correct mode of operation is selected before powering up the HMC981LP3E.

The HMC981LP3E does not allow the internal negative voltage generator to work if an enhancement mode is selected. Therefore, if VNEGFB is left floating while VGATEFB is grounded, HMC981LP3E will stay in standby mode.

Please note that the external negative voltage should be between -2.5V to -3.5V for HMC981LP3E to operate. If your application requires negative voltages outside this range please contact Hittite application support.

Table 2. Mode Selection

	VNEGFB	VGATEFB	VNEGIN	Description
MODE1 (Depletion/Master Mode)	FLOAT	FLOAT	Connected to VNEGOUT	Depletion mode transistor. Internal negative voltage generator is active and generates -2.5V. Sample application schematic given shown in Fig.2a.
MODE2 (Depletion/Slave Mode)	GND	FLOAT	Connected to External VSS	Depletion mode transistor. Internal negative voltage generator is disabled. An external negative voltage less than -2.3V should be connected to VNEGIN. Sample application schematic given shown in Fig.2b.
---	FLOAT	GND	N/A	Not allowed. HMC981LP3E stays in standby.
MODE3 (Enhancement Mode)	GND	GND	Connected to GND	Enhancement mode transistor. Internal negative voltage generator is disabled. Sample application schematic given shown in Fig.2c.

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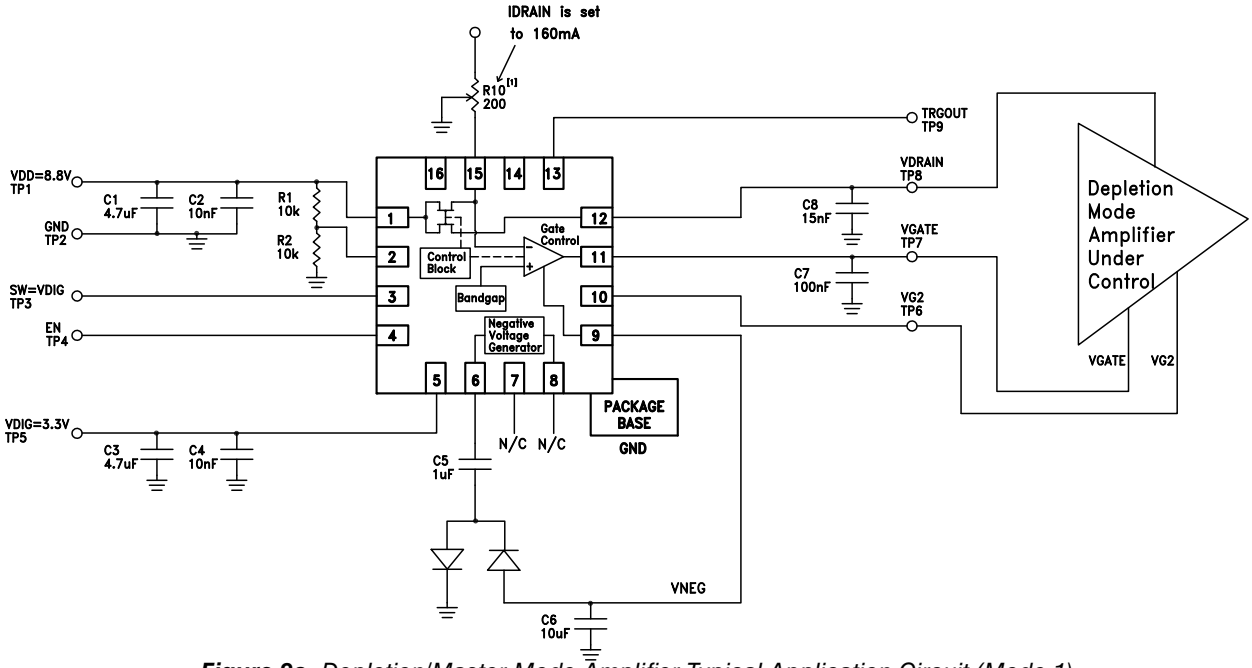


Figure 2a. *Depletion/Master Mode Amplifier Typical Application Circuit (Mode 1)*

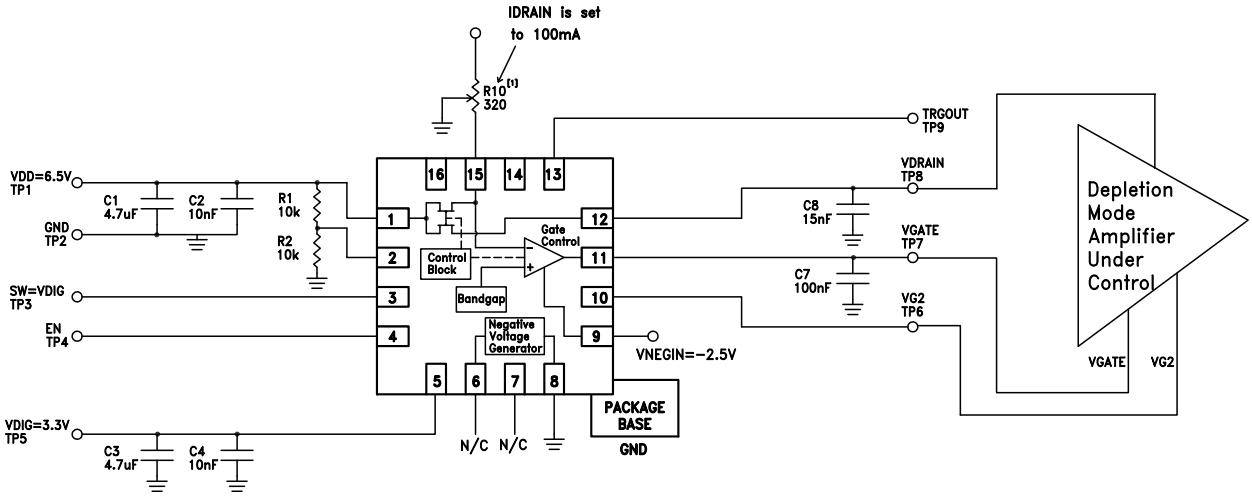


Figure 2b. *Depletion/Slave Mode Amplifier Typical Application Circuit (Mode 2)*

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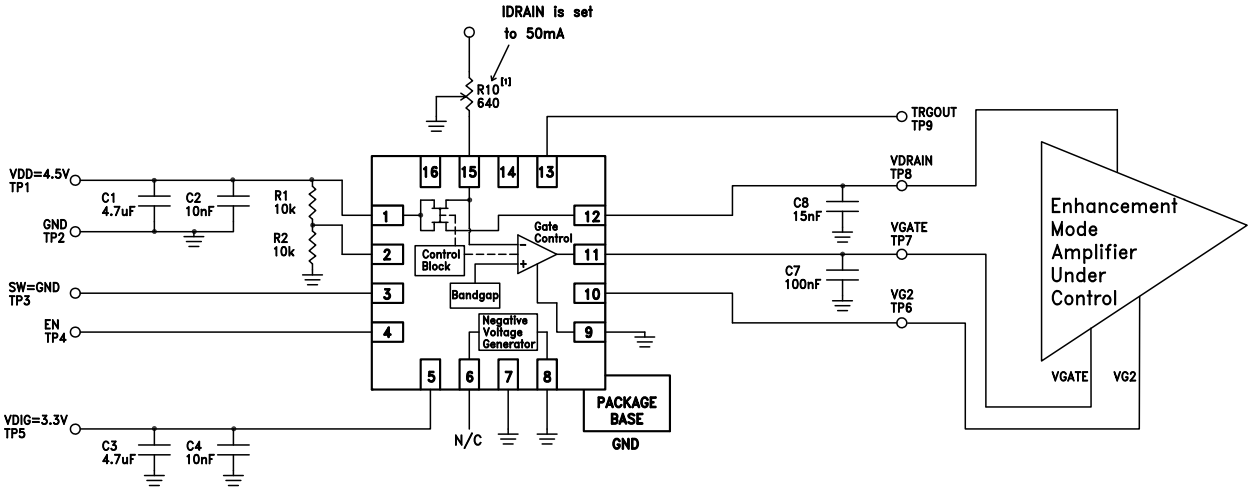


Figure 2c. *Enhancement Mode Amplifier Typical Application Circuit (Mode 3)*

Table 3 - List of Bias Settings for Various Hittite Amplifiers

Hittite Part Number	VDRAIN (V)	VDD (V)	IDRAIN (mA)	RSENSE (kOhm)	R2 (kOhm)	R1 (kOhm)	VG2 (V)
LNAs							
HMC-ALH140	4	4.60	60	0.53	open	open	-
HMC-ALH216	4	4.45	90	0.36	open	open	-
HMC-ALH244	4	4.45	45	0.71	open	open	-
HMC-ALH310[1]	2.5	3.02 [1]	52	0.62	open	open	-
HMC-ALH311[1]	2.5	3.04 [1]	54	0.59	open	open	-
HMC-ALH313[1]	2.5	3.02 [1]	52	0.62	open	open	-
HMC-ALH382[1]	2.5	3.14 [1]	64	0.50	open	open	-
HMC-ALH435	5	5.30	30	1.07	5.60	5	1.5
HMC-ALH444	5	5.55	55	0.58	5.09	5	1.5
HMC-ALH476	4	4.45	90	0.36	open	open	-
HMC490	5	6.00	200	0.16	open	open	-
HMC490LP5	5	6.00	200	0.16	open	open	-
HMC504LC4B	4	4.45	90	0.36	open	open	-
HMC594	6	6.50	100	0.32	open	open	-
HMC594LC3B	6	6.50	100	0.32	open	open	-
HMC609	6	6.85	170	0.19	open	open	-
HMC609LC4	6	6.85	170	0.19	open	open	-
HMC752LC4[1]	3	3.70 [1]	70	0.46	open	open	-
HMC753LP4E	5	5.55	55	0.58	5.09	5	1.5
HMC772LC4	4	4.45	45	0.71	open	open	-
Linear & Power							
HMC-ABH209	5	5.80	80	0.40	open	open	-
HMC-ABH264	5	5.60	120	0.27	open	open	-
HMC-AUH317	4	4.80	160	0.20	open	open	-

[1] For applications below 4V supply please contact factory.

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Table 3 - List of Bias Settings for Various Hittite Amplifiers *(Continued)*

Hittite Part Number	VDRAIN (V)	VDD (V)	IDRAIN (mA)	RSENSE (kOhm)	R2 (kOhm)	R1 (kOhm)	VG2 (V)
HMC-AUH318	4	4.80	160	0.20	open	open	-
HMC-AUH320	4	4.65	130	0.25	open	open	-
HMC442	5	5.43	85	0.38	open	open	-
HMC442LC3B	5	5.42	84	0.38	open	open	-
HMC442LM1	5	5.43	85	0.38	open	open	-
HMC499	5	6.00	200	0.16	open	open	-
HMC499LC4	5	6.00	200	0.16	open	open	-
Wideband (Distributed)							
HMC-ALH482	4	4.45	45	0.71	open	open	-
HMC-AUH232	5	5.90	180	0.18	4.52	5	1.5
HMC-AUH249	5	6.00	200	0.16	4.38	5	1.5
HMC-AUH312	8	8.60	60	0.53	2.82	5	1.8
HMC460	8	8.60	60	0.53	open	open	-
HMC460LC5	8	8.75	75	0.43	open	open	-
HMC463	5	5.60	60	0.53	open	open	-
HMC463LH250	5	5.60	60	0.53	open	open	-
HMC463LP5	5	5.60	60	0.53	open	open	-
HMC465	8	8.80	160	0.20	2.33	5	1.5
HMC465LP5	8	8.80	160	0.20	2.33	5	1.5
HMC562	8	8.80	80	0.40	open	open	-
HMC633	5	5.90	180	0.18	open	open	-
HMC633LC4	5	5.90	180	0.18	open	open	-
HMC634	5	5.90	180	0.18	open	open	-
HMC634LC4	5	5.90	180	0.18	open	open	-
HMC-930	10	10.88	175	0.18	3.95	5	3.5
Microwave & Optical Drivers							
HMC870LC5	7	7.83	165	0.19	open	open	-
HMC871LC5	8	8.38	75	0.43	open	open	-

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