DC to 28 GHz, GaAs, pHEMT, MMIC, Low Noise Amplifier

Data Sheet **HMC8401**

FEATURES

Output power for 1 dB compression (P1dB): 16.5 dBm typical
Saturated output power (P_{SAT}): 19 dBm typical
Gain: 14.5 dB typical
Noise figure: 1.5 dB
Output third order intercept (IP3): 26 dBm typical
Supply voltage: 7.5 V at 60 mA
50 Ω matched input/output
Die size: 2.55 mm x 1.62 mm x 0.05 mm

APPLICATIONS

Test instrumentation
Microwave radios and very small aperture terminals (VSATs)
Military and space
Telecommunications infrastructure
Fiber optics

GENERAL DESCRIPTION

The HMC8401 is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC). The HMC8401 is a wideband low noise amplifier which operates between dc and 28 GHz. The amplifier provides 14.5 dB of gain, 1.5 dB noise figure, 26 dBm output IP3 and 16.5 dBm of output power at 1 dB gain compression while requiring 60 mA from a 7.5 V supply. The HMC8401 also has a gain control option, $V_{GG}2$. The HMC8401 amplifier input/outputs are internally matched to 50 Ω facilitating integration into multichip modules (MCMs). All data is taken with the chip connected via two 0.025 mm (1 mil) wire bonds of minimal length 0.31 mm (12 mils).

FUNCTIONAL BLOCK DIAGRAM

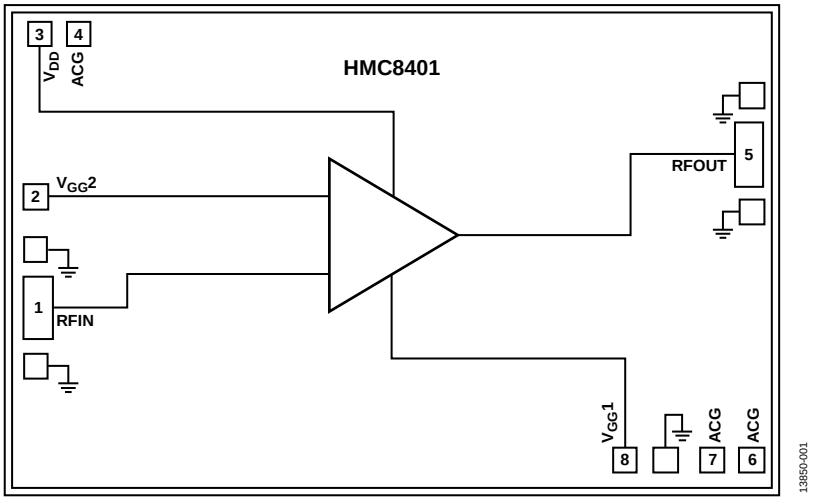


Figure 1.

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagram ... 1
Revision History ... 2
Specifications ... 3
0.01 GHz to 3 GHz Frequency Range ... 3
3 GHz to 26 GHz Frequency Range ... 3
26 GHz to 28 GHz Frequency Range ... 4
Absolute Maximum Ratings ... 5
ESD Caution ... 5
Pin Configuration and Function Descriptions ... 6
Interface Schematics ... 7
Typical Performance Characteristics ... 8
Theory of Operation ... 14
Applications Information ... 15
Biasing Procedures ... 15
Mounting and Bonding Techniques for Millimeterwave GaAs MMICs ... 15
Typical Application Circuit ... 16
Assembly Diagram ... 16
Outline Dimensions ... 17
Ordering Guide ... 17

REVISION HISTORY

4/2018—Rev. A to Rev. B

Changes to Features Section ... 1
Updated Outline Dimensions ... 17
Changes to Ordering Guide ... 17

9/2017—Rev. 0 to Rev. A

Changes to Supply Voltage Parameter, Table 1 ... 3
Changes to Supply Voltage Parameter, Table 2 ... 3
Changes to Supply Voltage Parameter, Table 3 ... 4
Changes to Thermal Resistance, θ_{JC} (Channel to Die Bottom) Parameter Heading, Table 4 ... 5
Changes to Table 5 ... 6
Changes to Figure 7 ... 7
Added Figure 41; Renumbered Sequentially ... 13

7/2016—Revision 0: Initial Version

SPECIFICATIONS

0.01 GHz TO 3 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 7.5 V, I_{DQ} = 60 mA, $V_{GG}2$ = open, unless otherwise stated.[1] When using $V_{GG}2$, it is recommended to limit $V_{GG}2$ from −2 V to +2.6 V.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			0.01		3	GHz
GAIN			13	15		dB
Gain Variation Over Temperature				0.005		dB/°C
RETURN LOSS						
Input				14		dB
Output				19		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		14.5	17		dBm
Saturated Output Power	P_{SAT}			19		dBm
Output Third Order Intercept	IP3	Measurement taken at P_{OUT}/tone = 10 dBm		27		dBm
NOISE FIGURE	NF			2.5	4.5	dB
SUPPLY CURRENT						
Total Supply Current	I_{DQ}			60		mA
SUPPLY VOLTAGE	V_{DD}		4.5	7.5	8.5	V

[1] Adjust the $V_{GG}1$ supply voltage between −2 V and 0 V to achieve I_{DQ} = 60 mA typical.

3 GHz TO 26 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 7.5 V, I_{DQ} = 60 mA, $V_{GG}2$ = open, unless otherwise stated.[1] When using $V_{GG}2$, it is recommended to limit $V_{GG}2$ from −2 V to +2.6 V.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			3		26	GHz
GAIN			12.5	14.5		dB
Gain Variation Over Temperature				0.007		dB/°C
RETURN LOSS						
Input				16		dB
Output				17		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		14	16.5		dBm
Saturated Output Power	P_{SAT}			19		dBm
Output Third Order Intercept	IP3	Measurement taken at P_{OUT}/tone = 10 dBm		26		dBm
NOISE FIGURE	NF			1.5	4.5	dB
SUPPLY CURRENT						
Total Supply Current	I_{DQ}			60		mA
SUPPLY VOLTAGE	V_{DD}		4.5	7.5	8.5	V

[1] Adjust the $V_{GG}1$ supply voltage between −2 V and 0 V to achieve I_{DQ}= 60 mA typical.

26 GHz TO 28 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 7.5 V, I_{DQ} = 60 mA, $V_{GG}2$ = open, unless otherwise stated.[1] When using $V_{GG}2$, it is recommended to limit $V_{GG}2$ from −2 V to +2.6 V.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			26		28	GHz
GAIN			12.5	14.5		dB
Gain Variation Over Temperature				0.009		dB/°C
RETURN LOSS						
Input				15		dB
Output				17		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		11.5	14		dBm
Saturated Output Power	P_{SAT}			17		dBm
Output Third Order Intercept	IP3	Measurement taken at P_{OUT}/tone = 10 dBm		24		dBm
NOISE FIGURE	NF			2	4	dB
SUPPLY CURRENT						
Total Supply Current	I_{DQ}			60		mA
SUPPLY VOLTAGE	V_{DD}		4.5	7.5	8.5	V

[1] Adjust the $V_{GG}1$ supply voltage between −2 V and 0 V to achieve I_{DQ} = 60 mA typical.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Drain Bias Voltage (V_{DD})	+10 V
Second Gate Bias Voltage ($V_{GG}2$)	−2.6 V to +3.6V
RF Input Power (RFIN)	20 dBm
Channel Temperature	175°C
Continuous Power Dissipation (P_{DISS}), T_A = 85°C (Derate 18.3 mW/°C Above 85°C)	1.67W
Thermal Resistance, θ_{JC} (Channel to Die Bottom)	54°C/W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +85°C
ESD Sensitivity, Human Body Model (HBM)	Class 1A, 250 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

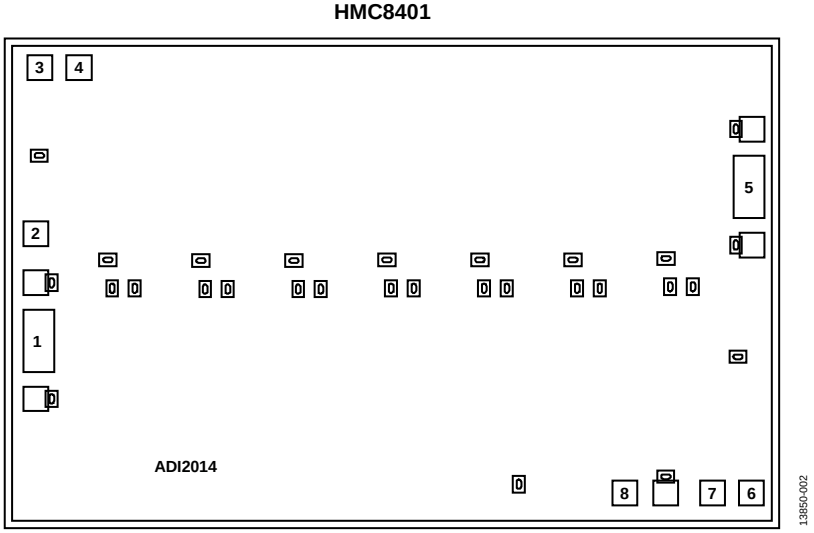


Figure 2. Pad Configuration

Table 5. Pad Function Descriptions

Pad No.	Mnemonic	Description
1	RFIN	Radio Frequency (RF) Input. This pad is dc coupled and matched to 50 Ω. See Figure 3 for the interface schematic.
2	$V_{GG}2$	Gain Control. This pad is dc-coupled and accomplishes gain control by bringing this voltage lower and becoming more negative. Attach bypass capacitors to this pad as shown in Figure 44. See Figure 4 for the interface schematic.
3	V_{DD}	Power Supply Voltage for the Amplifier. Connect a dc bias to provide drain current (I_{DD}). Attach bypass capacitors to this pad as shown in Figure 44. See Figure 5 for the interface schematic.
4, 6, 7	ACG	Low Frequency Termination. Attach bypass capacitors to this pad as shown in Figure 44. See Figure 6 for the interface schematic.
5	RFOUT	Radio Frequency (RF) Output. This pad is dc coupled and matched to 50 Ω. See Figure 3 for the interface schematic.
8	$V_{GG}1$	Gate Control for the Amplifier. Adjust $V_{GG}1$ to achieve the recommended bias current. Attach bypass capacitors to this pad as shown in Figure 44. See Figure 8 for the interface schematic.
Die Bottom	GND	Die Bottom. The die bottom must be connected to RF/dc ground. See Figure 9 for the interface schematic.

INTERFACE SCHEMATICS

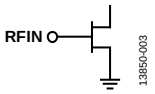


Figure 3. RFIN Interface Schematic

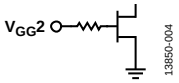


Figure 4. $V_{GG}2$ Interface Schematic

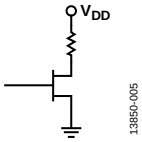


Figure 5. V_{DD} Interface Schematic

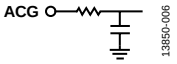


Figure 6. ACG Interface Schematic

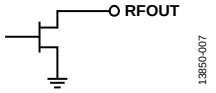


Figure 7. RFOUT Interface Schematic

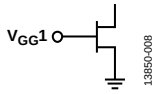


Figure 8. $V_{GG}1$ Interface Schematic



Figure 9. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

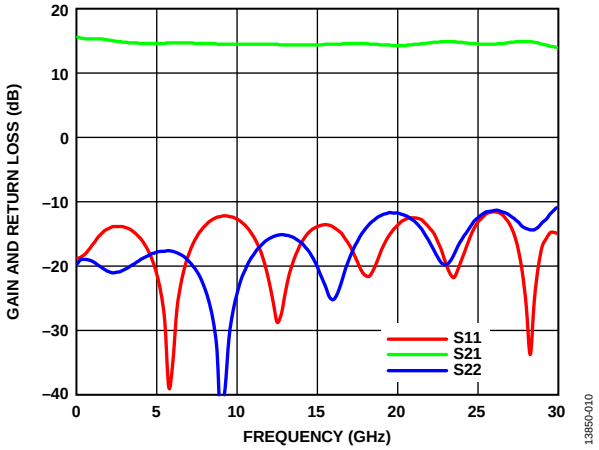


Figure 10. Response Gain and Return Loss vs. Frequency

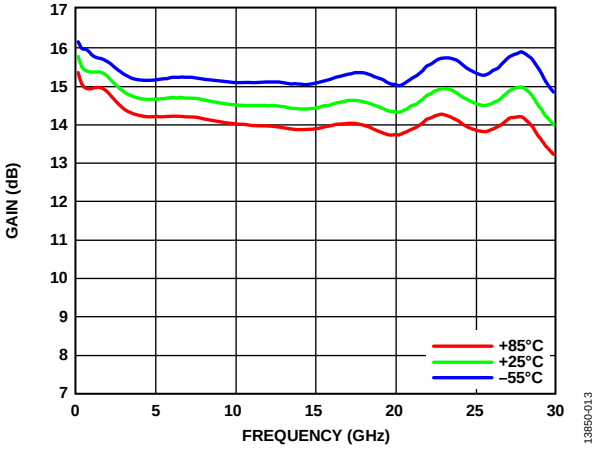


Figure 13. Gain vs. Frequency at Various Temperatures

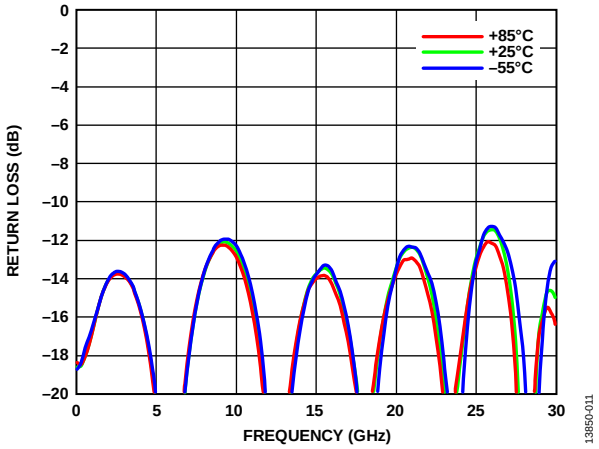


Figure 11. Input Return Loss vs. Frequency at Various Temperatures

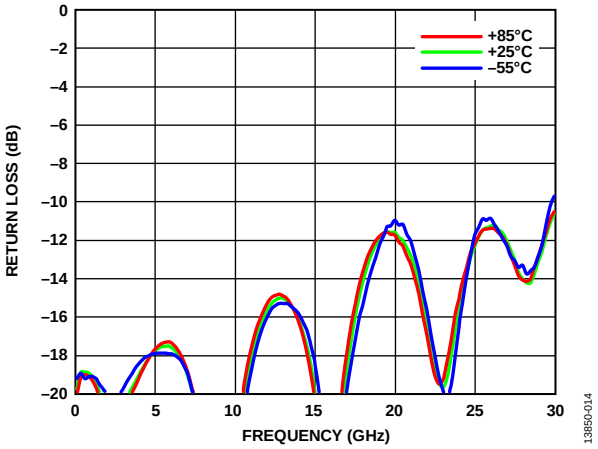


Figure 14. Output Return Loss vs. Frequency at Various Temperatures

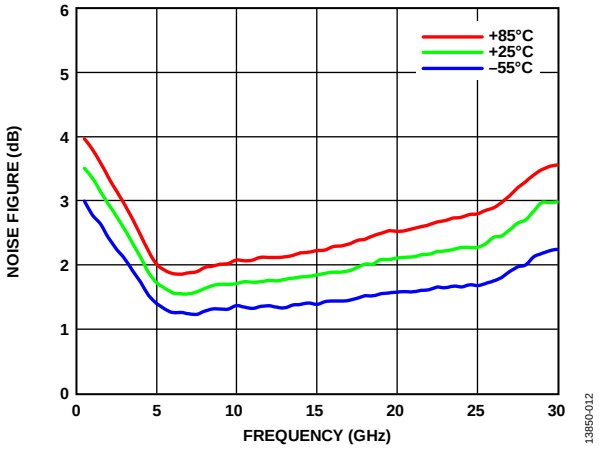


Figure 12. Noise Figure vs. Frequency at Various Temperatures

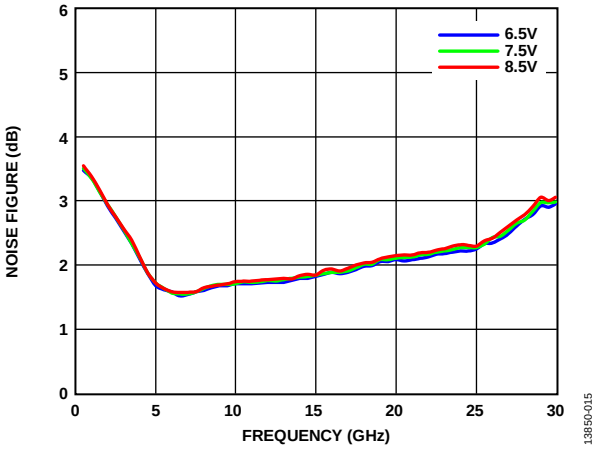


Figure 15. Noise Figure vs. Frequency at Various Supply Voltages

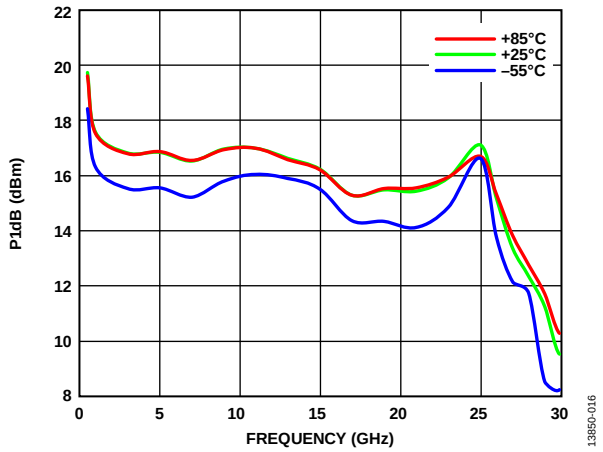


Figure 16. P1dB vs. Frequency at Various Temperatures

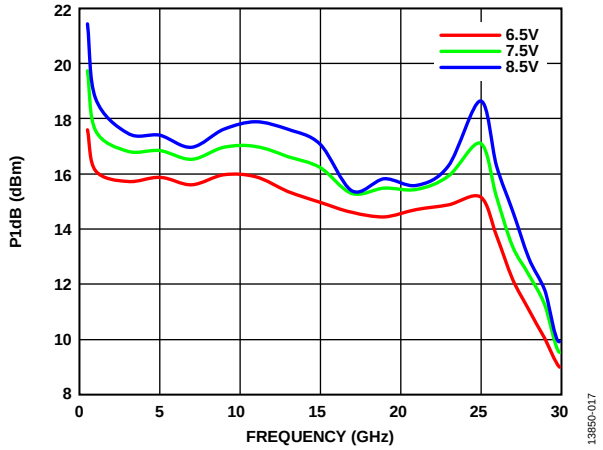


Figure 17. P1dB vs. Frequency at Various Supply Voltages

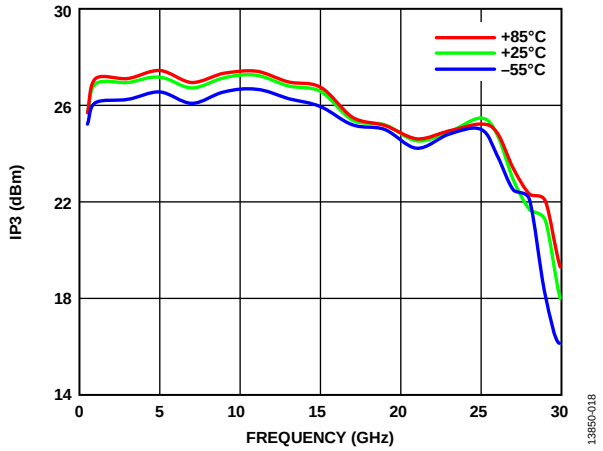


Figure 18. Output IP3 vs. Frequency for Various Temperatures at P_{OUT} = 0 dBm/Tone

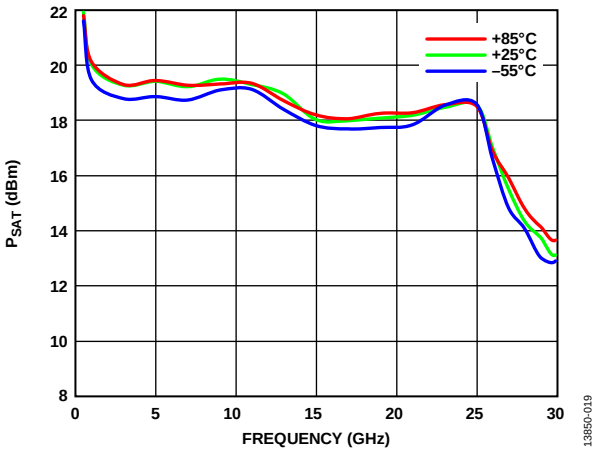


Figure 19. P_{SAT} vs. Frequency at Various Temperatures

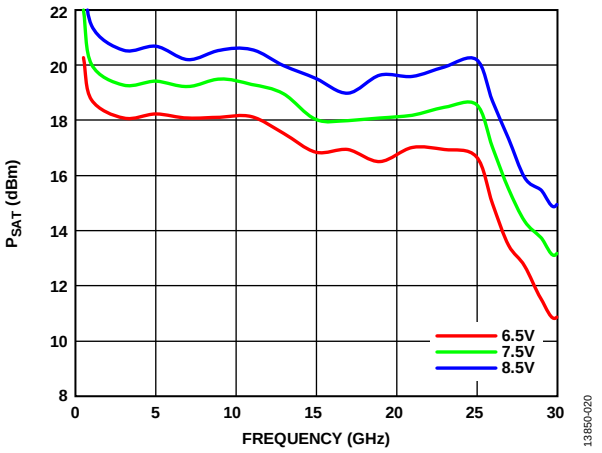


Figure 20. P_{SAT} vs. Frequency at Various Supply Voltages

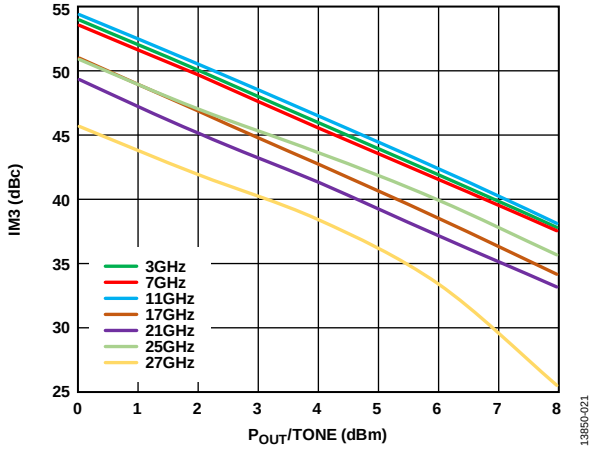


Figure 21. Output Third Order Intermodulation (IM3) vs. P_{OUT}/Tone for Various Frequencies at V_{DD} = 6.5 V

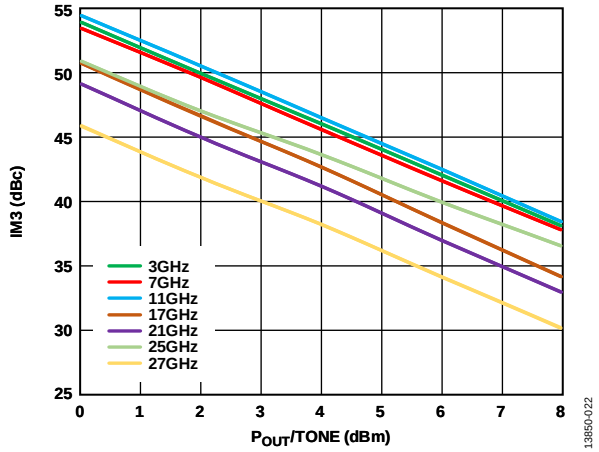


Figure 22. Output IM3 vs. P_{OUT}/Tone for Various Frequencies at V_{DD} = 7.5 V

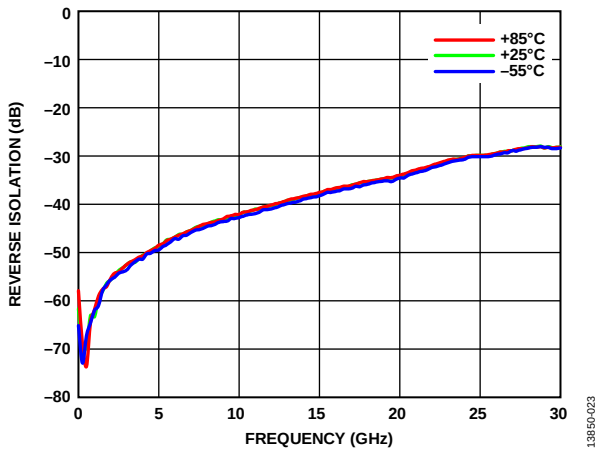


Figure 23. Reverse Isolation vs. Frequency at Various Temperatures

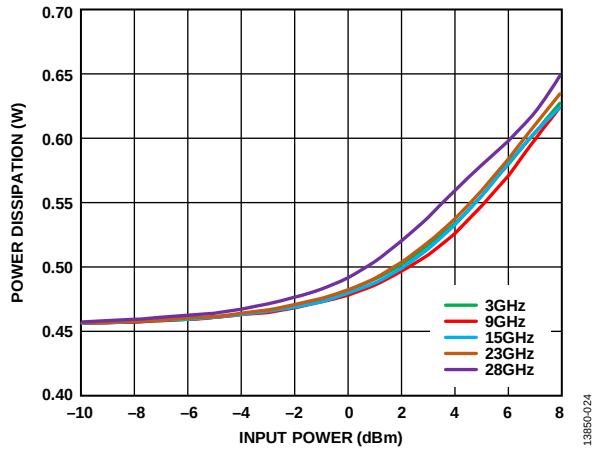


Figure 24. Power Dissipation vs. Input Power at Various Frequencies, T_A = 85°C

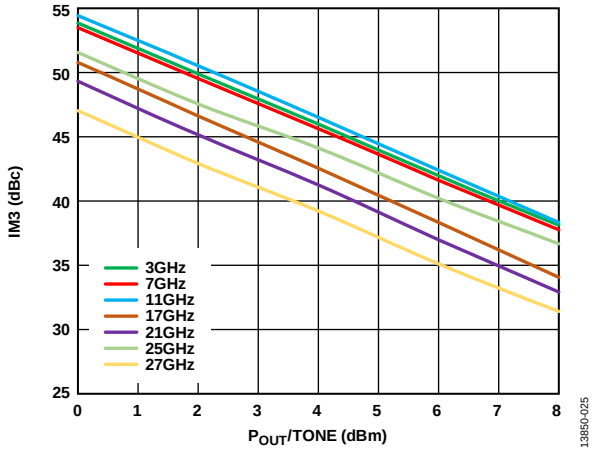


Figure 25. Output IM3 vs. P_{OUT}/Tone for Various Frequencies at V_{DD} = 8.5 V

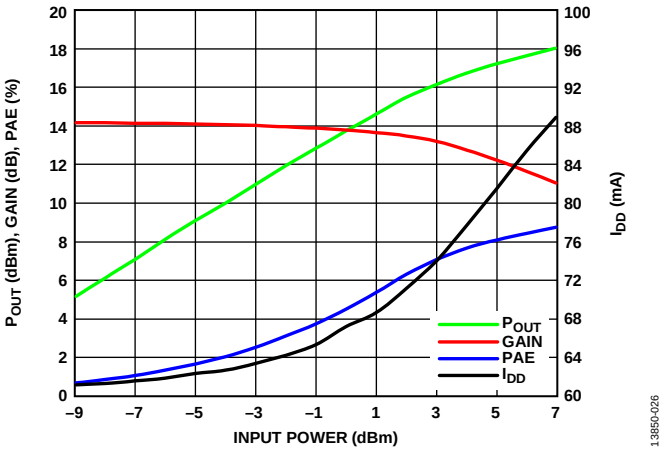


Figure 26. Power Compression at 15 GHz

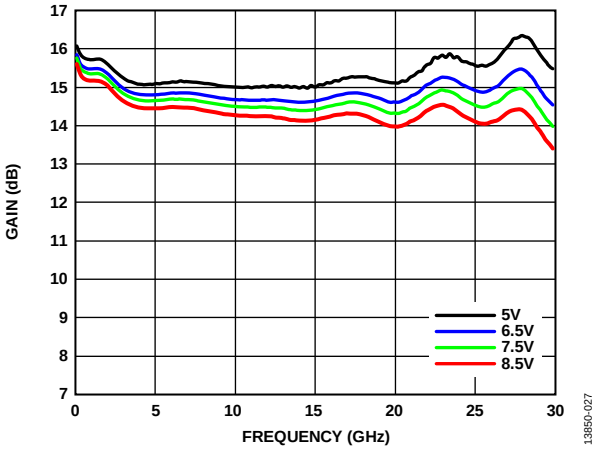


Figure 27. Gain vs. Frequency at Various Supply Voltages

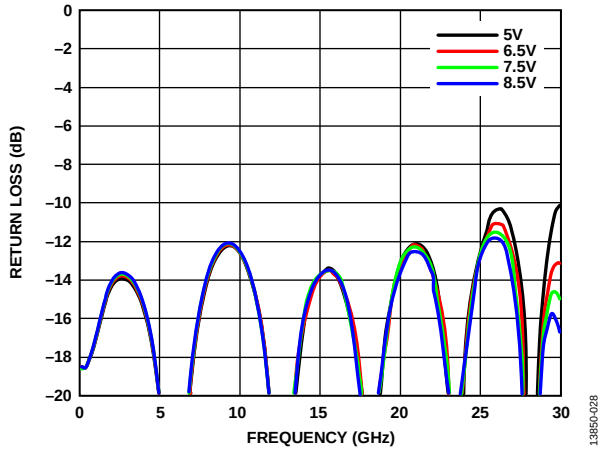


Figure 28. Input Return Loss vs. Frequency at Various Supply Voltages

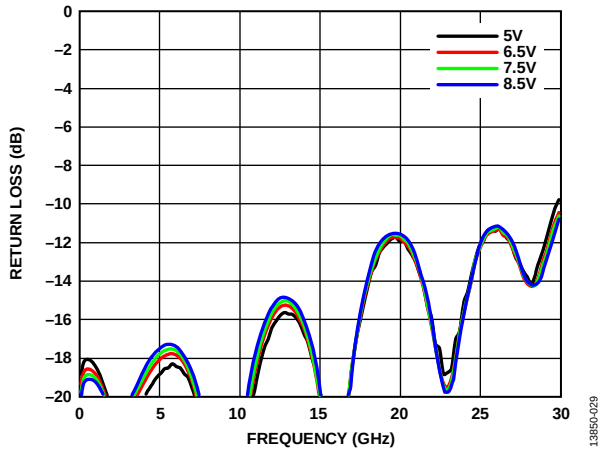


Figure 29. Output Return Loss vs. Frequency at Various Supply Voltages

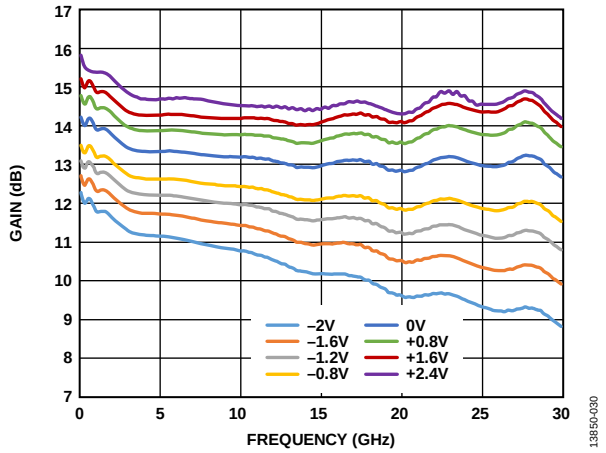


Figure 30. Gain vs. Frequency at Various $V_{GG}2$ Voltages

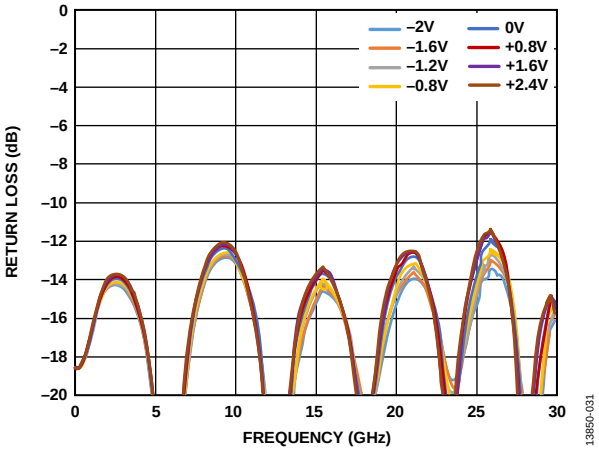


Figure 31. Input Return Loss vs. Frequency at Various $V_{GG}2$ Voltages

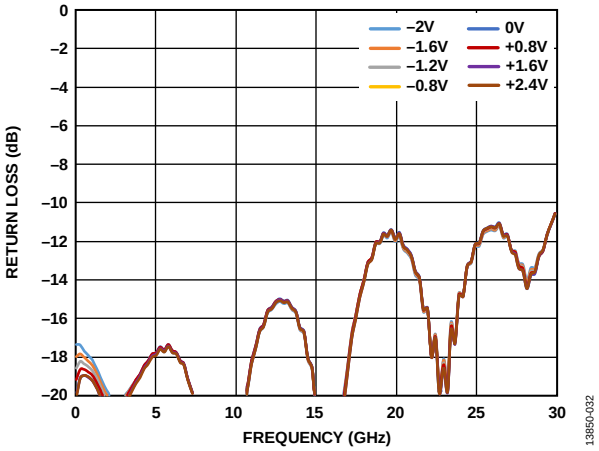


Figure 32. Output Return Loss vs. Frequency at Various $V_{GG}2$ Voltages

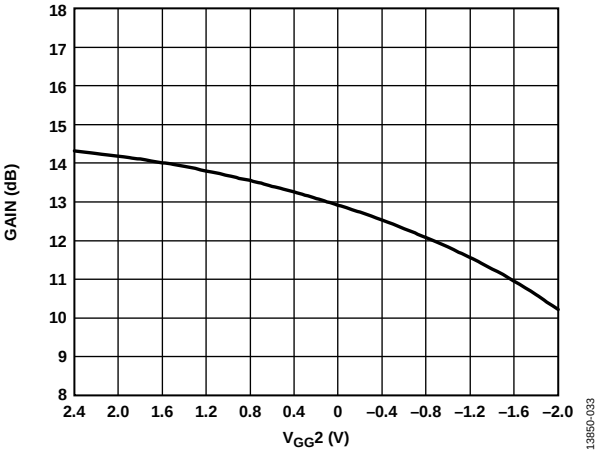


Figure 33. Gain vs. $V_{GG}2$ at 14 GHz

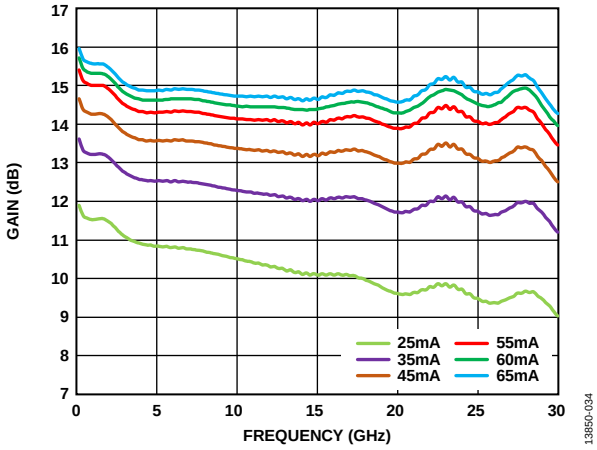


Figure 34. Gain vs. Frequency at Various I_{DQ} Currents

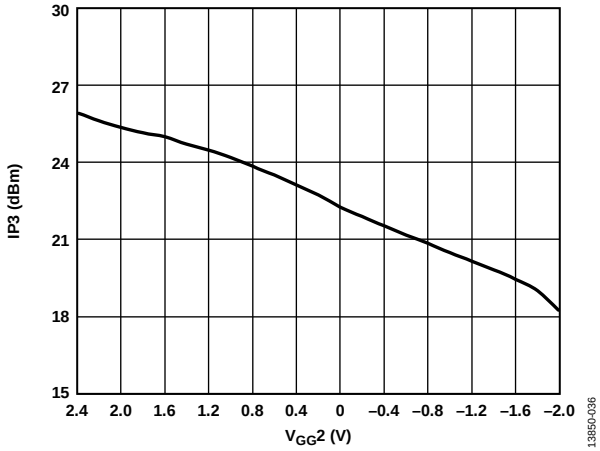


Figure 36. Output IP3 vs. $V_{GG}2$ at 16 GHz

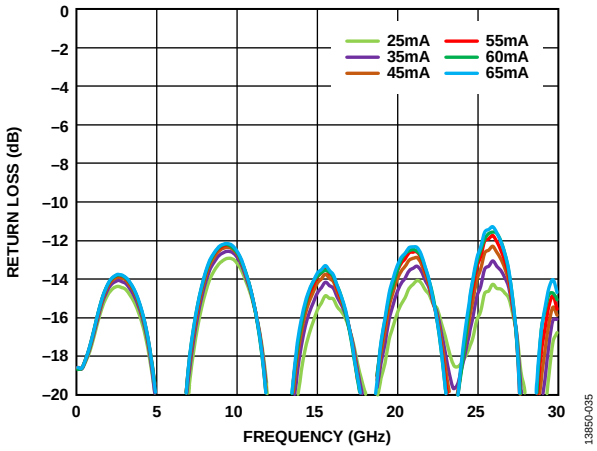


Figure 35. Input Return Loss vs. Frequency at Various I_{DQ} Currents

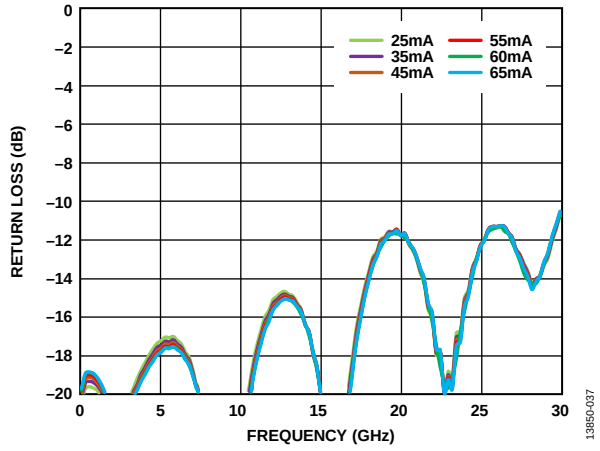


Figure 37. Output Return Loss vs. Frequency at Various I_{DQ} Currents

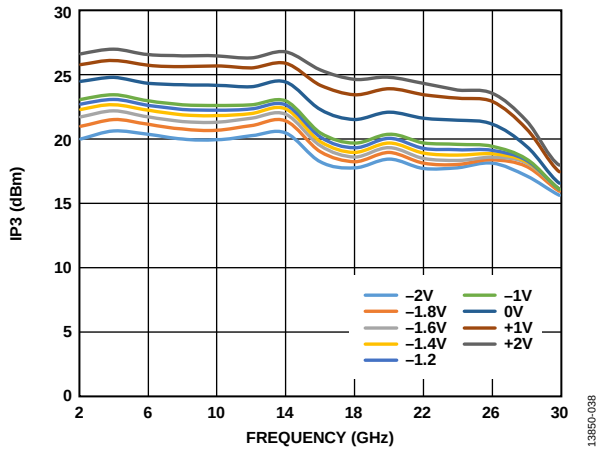


Figure 38. Output IP3 vs Frequency at Various $V_{GG}2$ Voltages

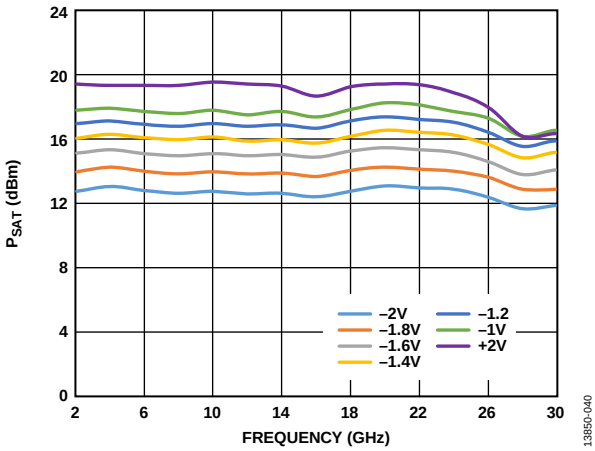


Figure 39. P1dB vs. Frequency at Various $V_{GG}2$ Voltages

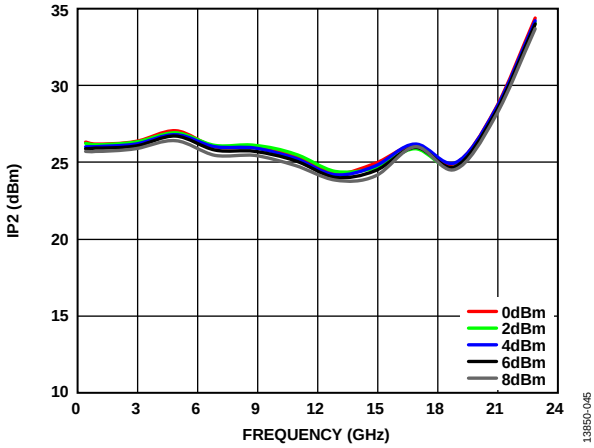


Figure 40. P_{SAT} vs. Frequency at Various $V_{GG}2$ Voltages

Figure 41. OIP2 vs. Frequency at Various RF Pout

THEORY OF OPERATION

The HMC8401 is a GaAs, pHEMT, MMIC low noise amplifier. Its basic architecture is that of a cascode distributed amplifier with an integrated resistor for the drain. The cascode distributed architecture uses a fundamental cell consisting of a stack of two field effect transistors (FETs) with the source of the upper FET connected to drain of the lower FET. The fundamental cell is then duplicated several times with an RFIN transmission line interconnecting the gates of the lower FETs and an RFOUT transmission line interconnecting the drains of the upper FETs.

Additional circuit design techniques are used around each cell to optimize the overall bandwidth and noise figure. The major benefit of this architecture is that a low noise figure is maintained across a bandwidth far greater than what a single instance of the fundamental cell provides. A simplified schematic of this architecture is shown in Figure 42.

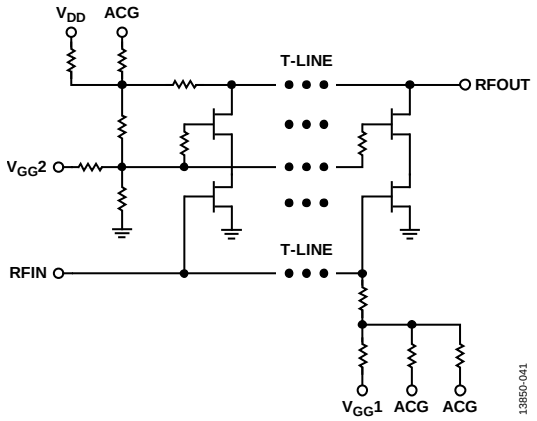


Figure 42. Architecture and Simplified Schematic

Though the gate bias voltages of the upper FETs are set internally by a resistive voltage divider tapped off of V_{DD}, the $V_{GG}2$ pad is provided to allow the user an optional means of changing the gate bias of the upper FETs. Adjustment of the $V_{GG}2$ voltage across the range from −2 V through +2.4 V changes the gate bias of the upper FETs, thus affecting gain changes of approximately 4 dB, depending on frequency. Increasing the voltage applied to $V_{GG}2$ increases the gain, while decreasing the voltage decreases the gain. For the nominal V_{DD} = 7.5 V, the resulting $V_{GG}2$ open circuit voltage is approximately 2.06 V.

A voltage applied to the $V_{GG}1$ pad sets the gate bias of the lower FETs, providing control of the drain current. Unlike the upper FETs, a gate bias voltage for the lower FETs is not generated internally. For this reason, the application of a bias voltage to the $V_{GG}1$ pad is required and not optional.

To operate the HMC8401 at voltages lower than the nominal 7.5 V, use a bias tee to apply 5.25 V to the drain via the RFOUT pad.

When using this alternate bias configuration, leave the V_{DD} pad open and adjust $V_{GG}1$ to obtain a nominal quiescent I_{DD} = 60 mA.

Though data taken using the alternate bias configuration is not presented on this data sheet, the resulting performance differs only slightly from that obtained using the typical bias configuration. The small signal gain is a few tenths of dB greater, the compression characteristics are slightly harder, and the noise figure characteristics remain mostly unchanged.

For additional information regarding this alternate bias configuration, contact Analog Devices Applications.

APPLICATIONS INFORMATION

BIASING PROCEDURES

Capacitive bypassing is required for V_{DD} and $V_{GG}1$, as shown in the typical application circuit in Figure 44. Gain control is possible through the application of a dc voltage to $V_{GG}2$. If gain control is used, then $V_{GG}2$ must be bypassed by 100 pF, 0.1 µF, and 4.7 µF capacitors. If gain control is not used, then $V_{GG}2$ can be either left open or capacitively bypassed as described.

The recommended bias sequence during power-up is as follows:

1. Set $V_{GG}1$ to −2.0 V to pinch off the channels of the lower FETs.
2. Set V_{DD} to 7.5 V. Because the lower FETs are pinched off, I_{DQ} remains very low upon application of V_{DD}.
3. Adjust $V_{GG}1$ to be more positive until the desired quiescent drain current is obtained.
4. Apply the RF input signal.
5. If the gain control function is to be used, apply to $V_{GG}2$ a voltage within the range of −2.0 V to +2.4 V until the desired gain is achieved.

Use of the $V_{GG}2$ (the gain control function) affects the drain current.

The recommended bias sequence during power-down is as follows:

1. Turn off the RF input signal.
2. Remove the $V_{GG}2$ voltage or set it to 0 V.
3. Set $V_{GG}1$ to −2.0 V to pinch off the channels of the lower FETs.
4. Set V_{DD} to 0 V.
5. Set $V_{GG}1$ to 0 V.

Power-up and power-down sequences may differ from the ones described, though care must always be taken to ensure adherence to the values shown in the Absolute Maximum Ratings.

Unless otherwise noted, all measurements and data shown were taken using the typical application circuit (see Figure 44), configured as shown on the assembly diagram (see Figure 45) and biased per the conditions in this section. The bias conditions shown in this section are the operating points recommended to optimize the overall performance. Operation using other bias conditions may provide performance that differs from what is shown in this data sheet. To obtain the best performance while not damaging the device, follow the recommended biasing sequence outlined in this section.

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICs

Attach the die directly to the ground plane eutectically or with conductive epoxy. To bring RF to and from the chip, use 50 Ω microstrip transmission lines on 0.127 mm (5 mil) thick alumina thin film substrates (see Figure 43).

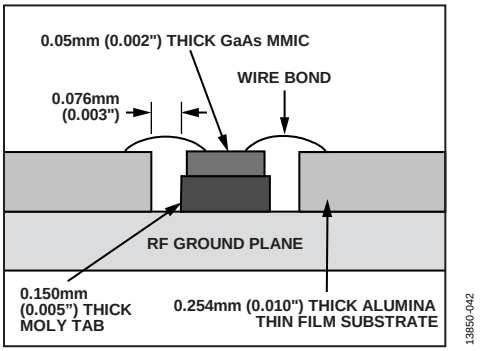


Figure 43. Routing RF Signals with Molytab

To minimize bond wire length, place microstrip substrates as close to the die as possible. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

Handling Precautions

To avoid permanent damage, adhere to the following precautions:

- All bare die ship in either waffle or gel-based ESD protective containers, sealed in an ESD protective bag. After the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chips in a clean environment. Never use liquid cleaning systems to clean the chip.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. To minimize inductive pickup, use shielded signal and bias cables.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip may have fragile air bridges and must not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back metallized and can be die mounted with gold/tin (AuSn) eutectic preforms or with electrically conductive epoxy. The mounting surface must be clean and flat.

Eutectic Die Attach

It is best to use an 80% gold/20% tin preform with a work surface temperature of 255°C and a tool temperature of 265°C. When hot 90% nitrogen/10% hydrogen gas is applied, maintain tool tip temperature at 290°C. Do not expose the chip to a temperature greater than 320°C for more than 20 sec. No more than 3 sec of scrubbing is required for attachment.

Epoxy Die Attach

ABLETHERM 2600BT is recommended for die attachment. Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after placing it into position. Cure the epoxy per the schedule provided by the manufacturer.

Wire Bonding

RF bonds made with 0.003 in. × 0.0005 in. gold ribbon are recommended for the RF ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. DC bonds of 1 mil (0.025 mm) diameter, thermosonically bonded, are recommended.

Create ball bonds with a force of 40 g to 50 g and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Keep all bonds as short as possible, less than 12 mil (0.31 mm).

TYPICAL APPLICATION CIRCUIT

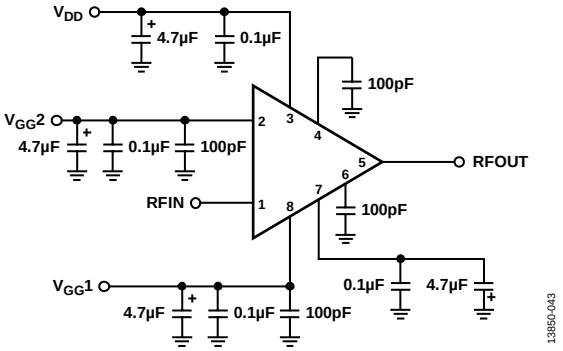


Figure 44. Typical Application Circuit

ASSEMBLY DIAGRAM

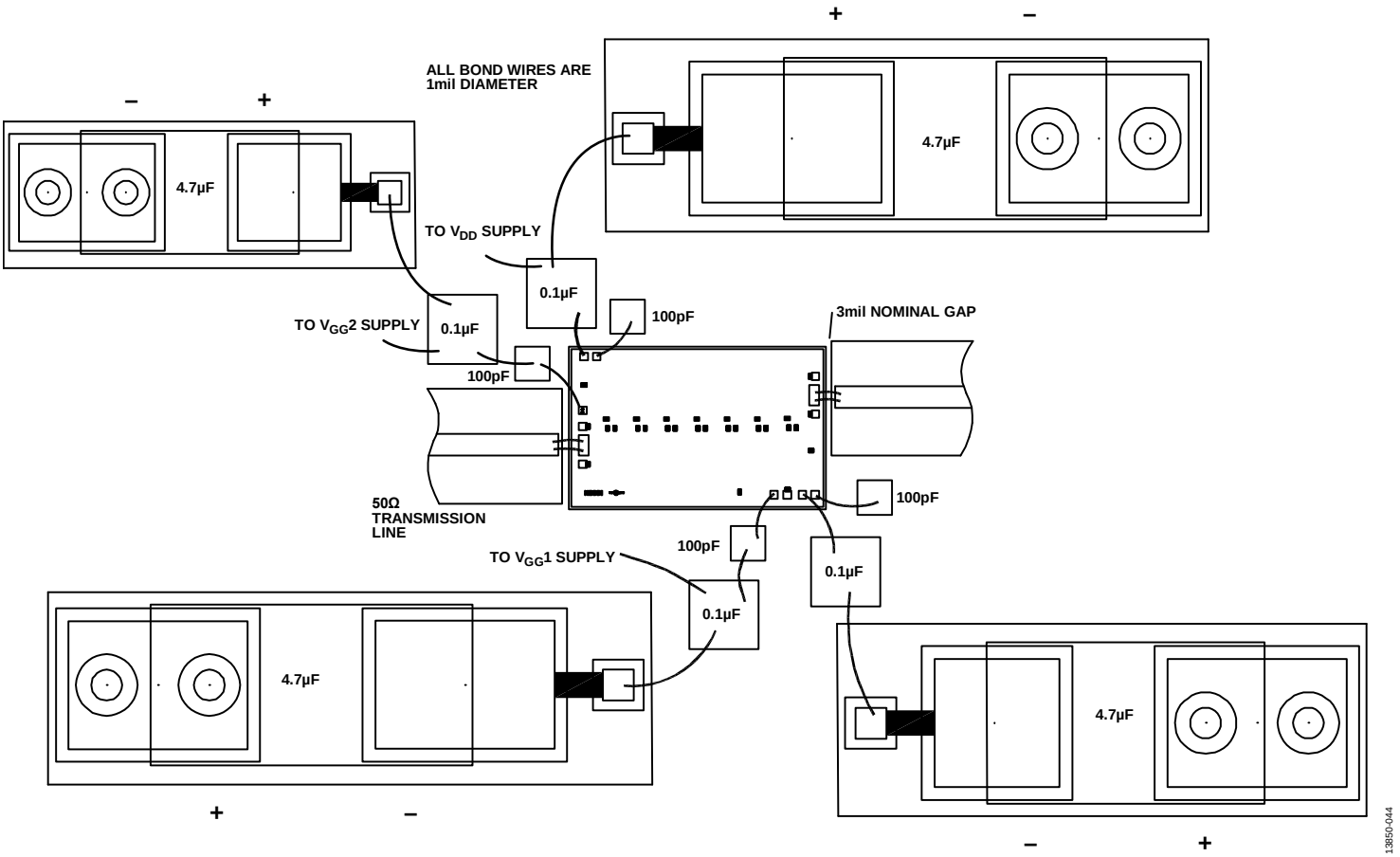


Figure 45. Assembly Diagram

OUTLINE DIMENSIONS

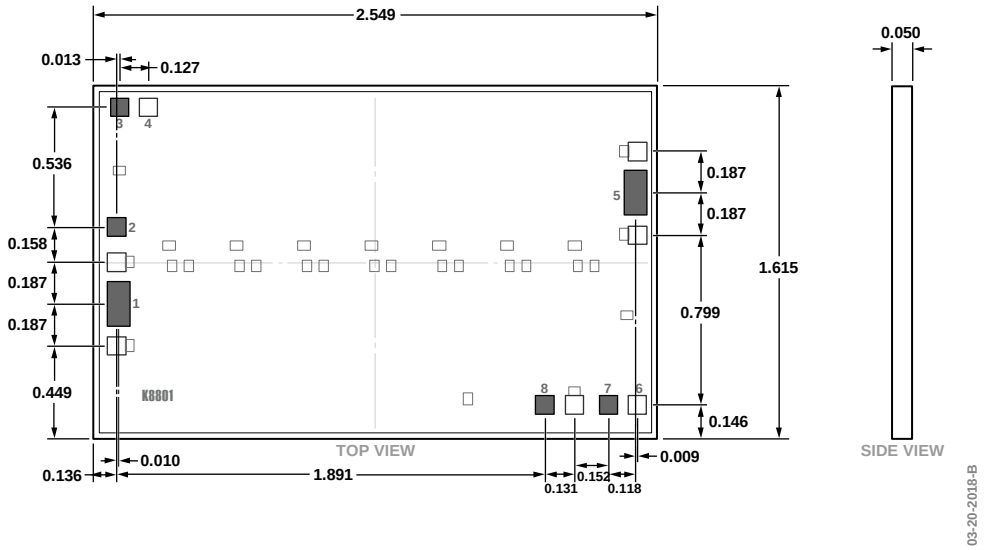


Figure 46. 8-Pad Bare Die [CHIP]
(C-8-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
HMC8401	−55°C to +85°C	8-Pad Bare Die [CHIP]	C-8-8
HMC8401-SX	−55°C to +85°C	8-Pad Bare Die [CHIP]	C-8-8

[1] The HMC8401-SX is a sample order of two devices.
[2] All models are RoHS compliant parts.

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D13850-0-4/18(B)