81 GHz to 86 GHz, E-Band Power Amplifier With Power Detector

Data Sheet **HMC8142**

FEATURES

Gain: 21 dB typical
Output power for 1 dB compression (P1dB): 25 dBm typical
Saturated output power (P_{SAT}): 26 dBm typical
Output third-order intercept (OIP3): 29 dBm typical
Input return loss: 12 dB typical
Output return loss: 8 dB typical
DC supply: 4 V at 450 mA
No external matching required
Die size: 3.039 mm × 1.999 mm × 0.05 mm

APPLICATIONS

E-band communication systems
High capacity wireless backhaul radio systems
Test and measurement

GENERAL DESCRIPTION

The HMC8142 is an integrated E-band gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), medium power amplifier with a temperature compensated on-chip power detector that operates from 81 GHz to 86 GHz. The HMC8142 provides 21 dB of gain, 25 dBm of output power at 1 dB compression, 29 dBm of output third-order intercept, and 26 dBm of saturated output power at 20% power added efficiency (PAE) from a 4 V power supply. The HMC8142 exhibits excellent linearity and is optimized for E-band communications and high capacity wireless backhaul radio systems. The amplifier configuration and high gain make it an excellent candidate for last stage signal amplification before the antenna. All data is taken with the chip in a 50 Ω test fixture connected via a 3 mil wide × 0. 5 mil thick × 7 mil long ribbon on each port.

FUNCTIONAL BLOCK DIAGRAM

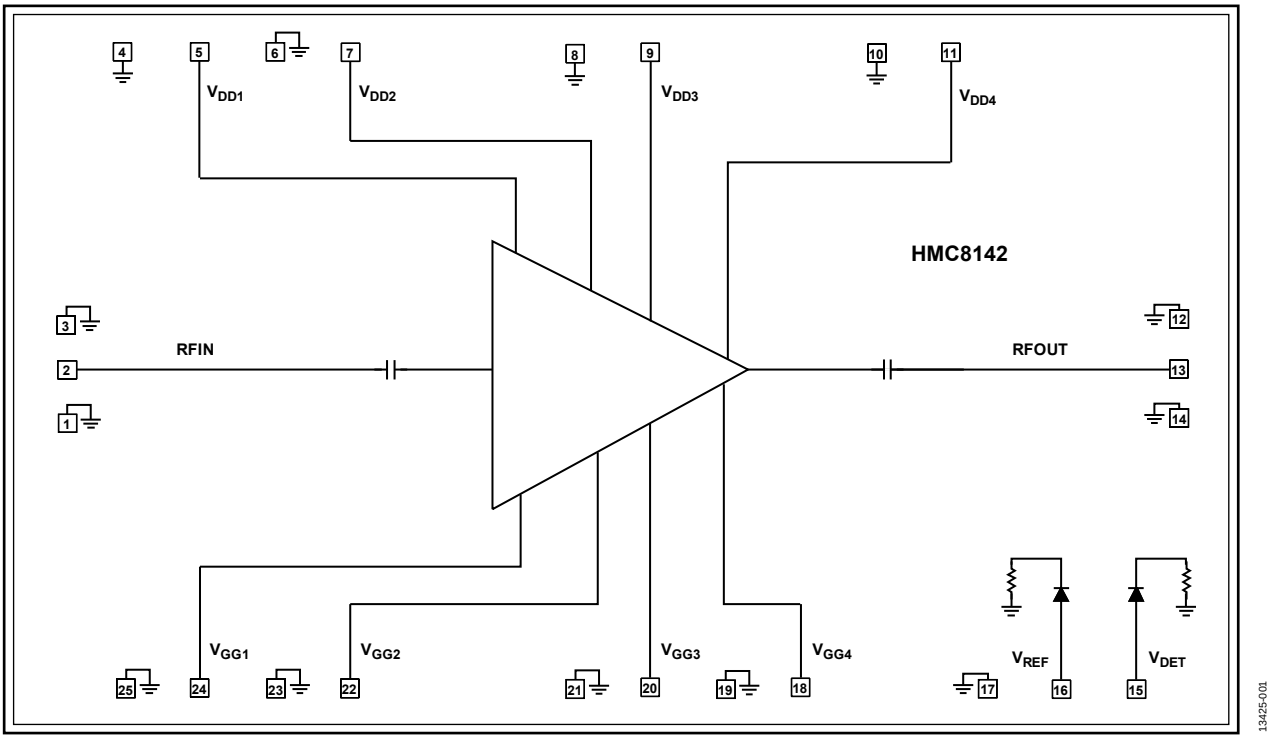


Figure 1.

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REVISION HISTORY

2/16—Revision A: Initial Version

SPECIFICATIONS

T_A = 25°C, V_{DDx} = 4 V, I_{DD} = 450 mA, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
OPERATING CONDITIONS				
Radio Frequency (RF) Range	81		86	GHz
PERFORMANCE				
Gain	19	21		dB
Gain Variation over Temperature		0.02		dB/°C
Output Power for 1 dB Compression (P1dB)	22.5	25		dBm
Saturated Output Power (P_{SAT})		26		dBm
Output Third-Order Intercept (OIP3) at Maximum Gain[1]		29		dBm
Input Return Loss		12		dB
Output Return Loss		8		dB
POWER SUPPLY				
Total Supply Current (I_{DD})[2]		450		mA

[1] Data taken at output power (P_{OUT}) = 12 dBm/tone, 1 MHz spacing.
[2] Adjust V_{GGx} from −2 V to 0 V to achieve the total drain current, I_{DD} = 450 mA.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Drain Bias Voltage (V_{DD1} to V_{DD4})	4.5 V
Gate Bias Voltage (V_{GG1} to V_{GG4})	−3 V to 0 V
Maximum Junction Temperature (to Maintain 1 Million Hours Mean Time to Failure (MTTF))	175°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
25-Pad Bare Die [CHIP]	48.33	°C/W

[1] Based on ABLETHERM® 2600BT as die attach epoxy with thermal conductivity of 20 W/mK.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

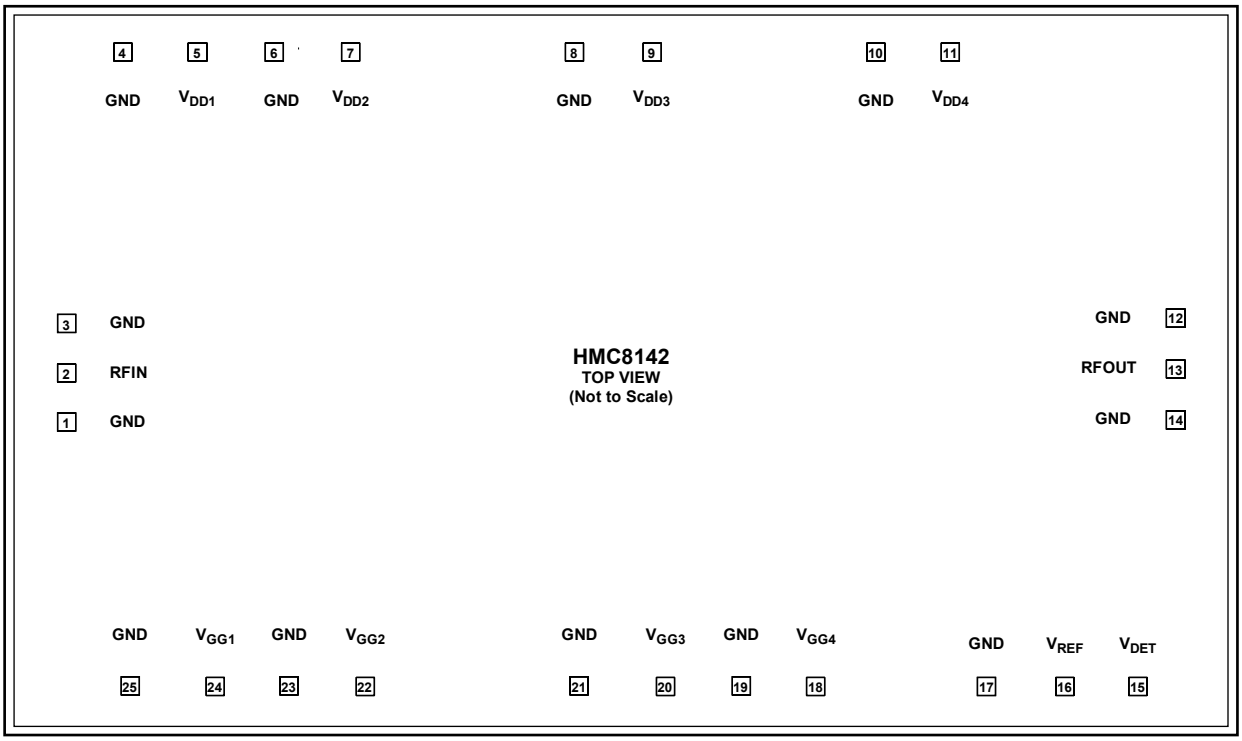


Figure 2. Pad Configuration

Table 4. Pad Function Descriptions

Pad No.	Mnemonic	Description
1, 3, 4, 6, 8, 10, 12, 14, 17, 19, 21, 23, 25	GND	Ground Connection (See Figure 3).
2	RFIN	RF Input. AC couple RFIN and match it to 50 Ω (See Figure 4).
5, 7, 9, 11	V_{DD1} to V_{DD4}	Drain Bias Voltage for the Power Amplifier (See Figure 5).
13	RFOUT	RF Output. AC couple RFOUT and match it to 50 Ω (see Figure 6).
15	V_{DET}	Detector Voltage for the Power Detector (See Figure 7). V_{DET} is the dc voltage representing the RF output power rectified by the diode, which is biased through an external resistor. Refer to the typical application circuit for the required external components (see Figure 40).
16	V_{REF}	Reference Voltage for the Power Detector (See Figure 7). V_{REF} is the dc bias of diode biased through an external resistor used for the temperature compensation of V_{DET}. Refer to the typical application circuit for the required external components (see Figure 40).
18, 20, 22, 24	V_{GG4} to V_{GG1}	Gate Bias Voltage for the Power Amplifier (See Figure 8). Refer to the typical application circuit for the required external components (see Figure 40).
Die Bottom	GND	Ground. The die bottom must be connected to the RF/dc ground (see Figure 3).

INTERFACE SCHEMATICS



Figure 3. GND Interface

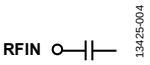


Figure 4. RFIN Interface

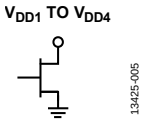


Figure 5. V_{DD1} to V_{DD4} Interface

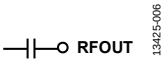


Figure 6. RFOUT Interface



Figure 7. V_{DET}, V_{REF} Interface

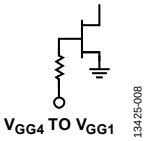


Figure 8. V_{GG4} to V_{GG1} Interface

TYPICAL PERFORMANCE CHARACTERISTICS

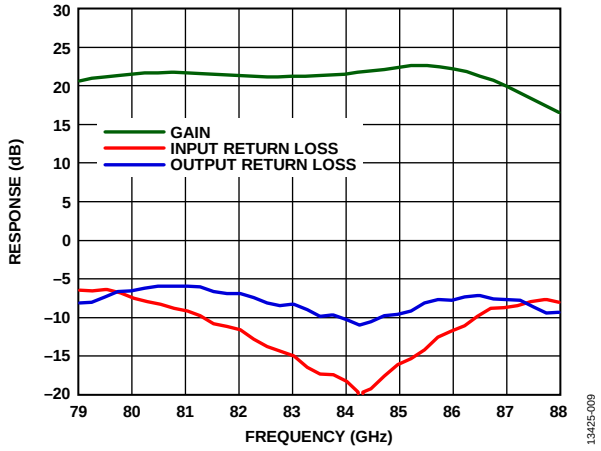


Figure 9. Broadband Gain and Return Loss Response vs. Frequency, Drain Current (I_{DD}) = 450 mA

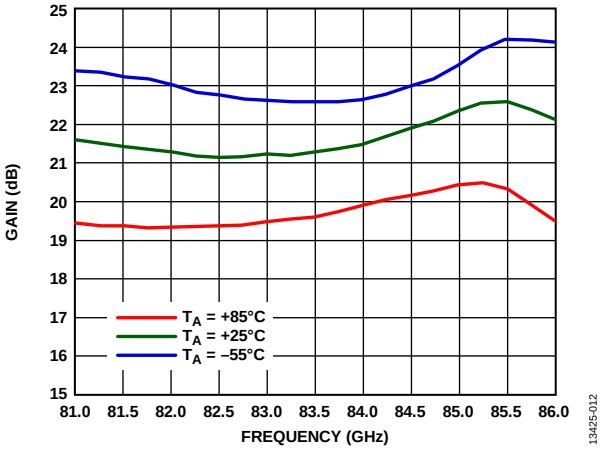


Figure 12. Gain vs. Frequency at Various Temperatures, Drain Current (I_{DD}) = 450 mA

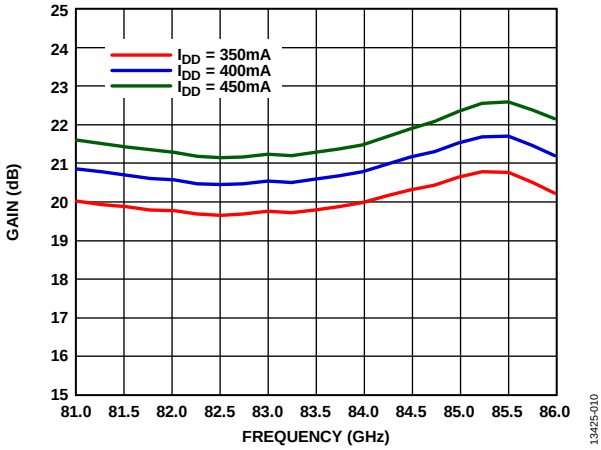


Figure 10. Gain vs. Frequency at Various Drain Currents (I_{DD})

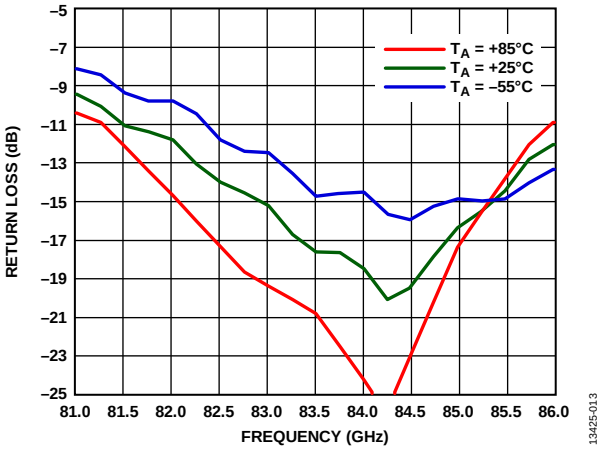


Figure 13. Input Return Loss vs. Frequency at Various Temperatures, Drain Current (I_{DD}) = 450 mA

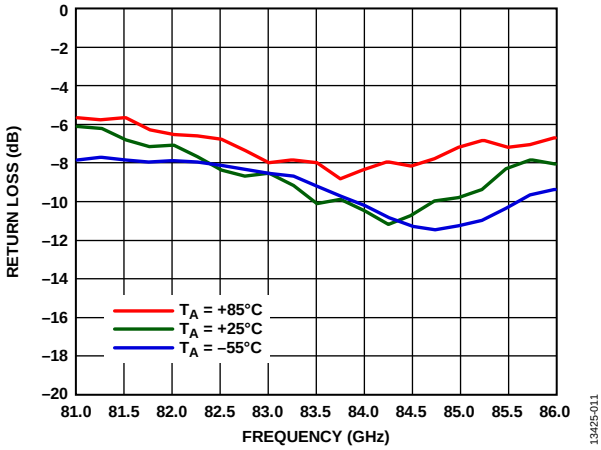


Figure 11. Output Return Loss vs. Frequency at Various Temperatures, Drain Current (I_{DD}) = 450 mA

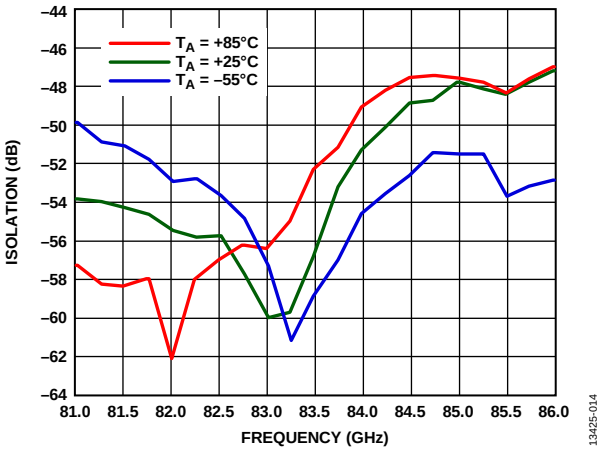


Figure 14. Reverse Isolation vs. Frequency at Various Temperatures, Drain Current (I_{DD}) = 450 mA

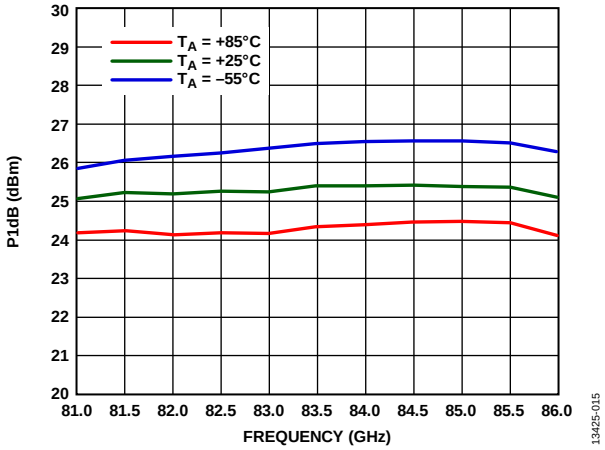


Figure 15. Output P1dB vs. Frequency at Various Temperatures, Drain Current (I_{DD}) = 450 mA

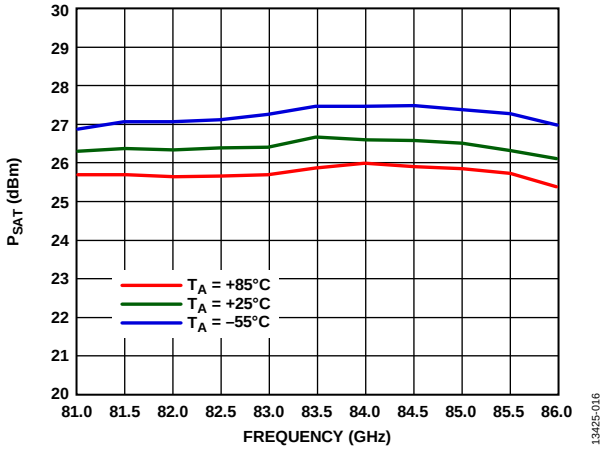


Figure 16. P_{SAT} vs. Frequency at Various Temperatures, Drain Current (I_{DD}) = 450 mA

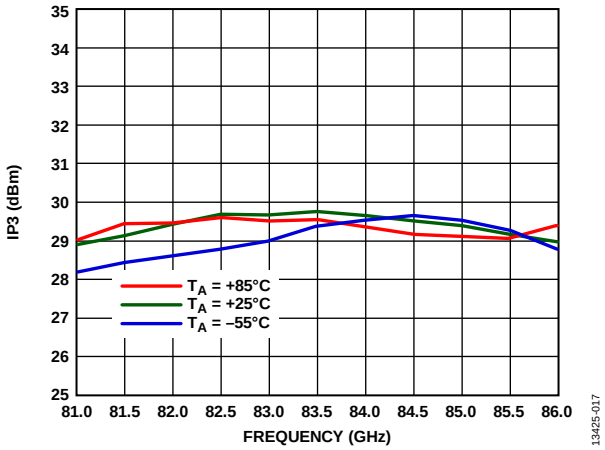


Figure 17. Output IP3 vs. Frequency at Various Temperatures, Drain Current (I_{DD}) = 450 mA, P_{OUT}/Tone = 12 dBm

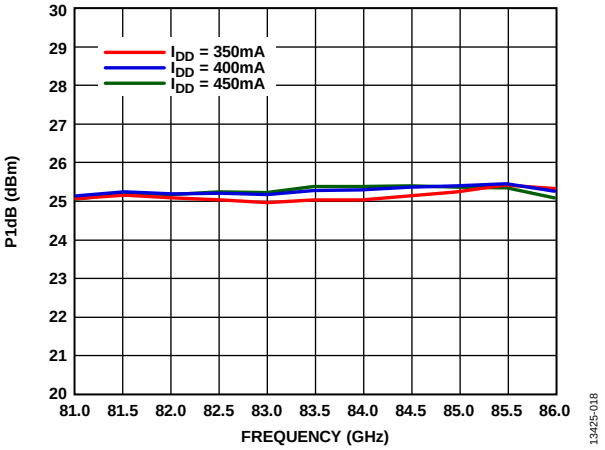


Figure 18. Output P1dB vs. Frequency at Various Drain Currents (I_{DD})

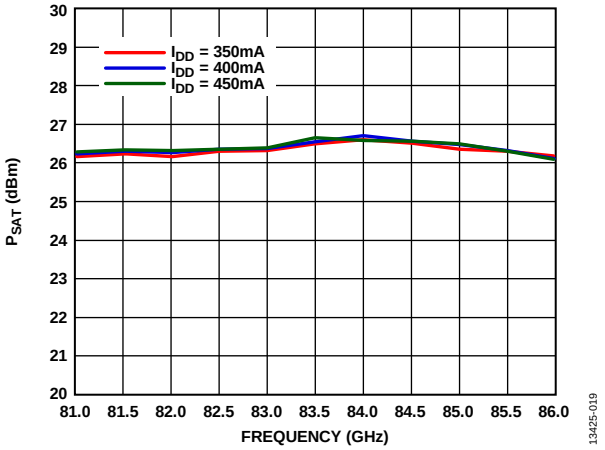


Figure 19. P_{SAT} vs. Frequency at Various Drain Currents (I_{DD})

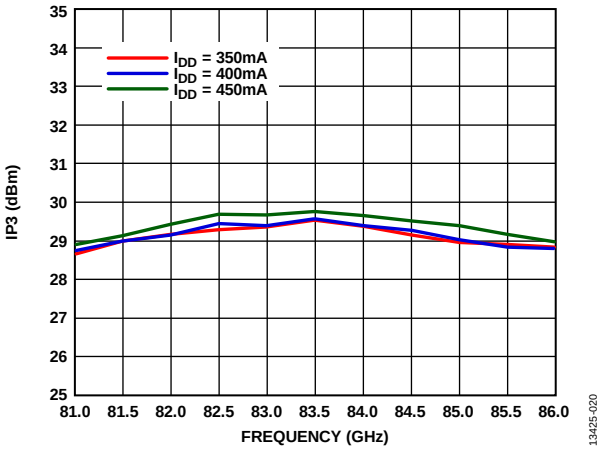


Figure 20. Output IP3 vs. Frequency at Various Drain Currents (I_{DD}), P_{OUT}/Tone = 12 dBm

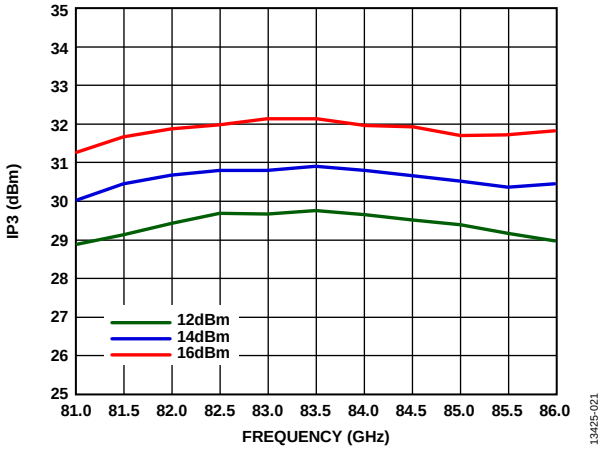


Figure 21. Output IP3 vs. Frequency at Various P_{OUT}/Tones, Drain Current (I_{DD}) = 450 mA

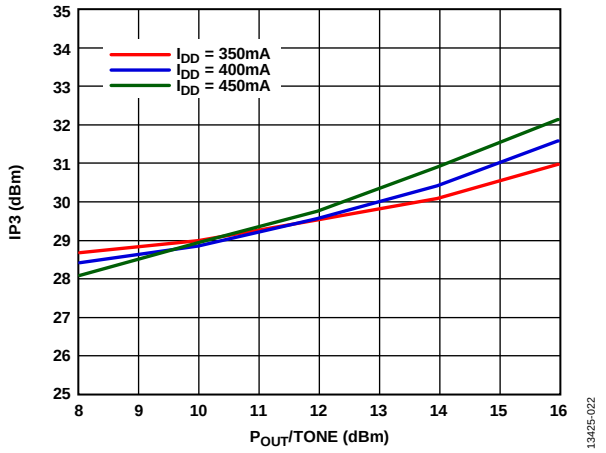


Figure 22. Output IP3 vs. P_{OUT}/Tone at Various Drain Currents (I_{DD}) at RF = 83.5 GHz

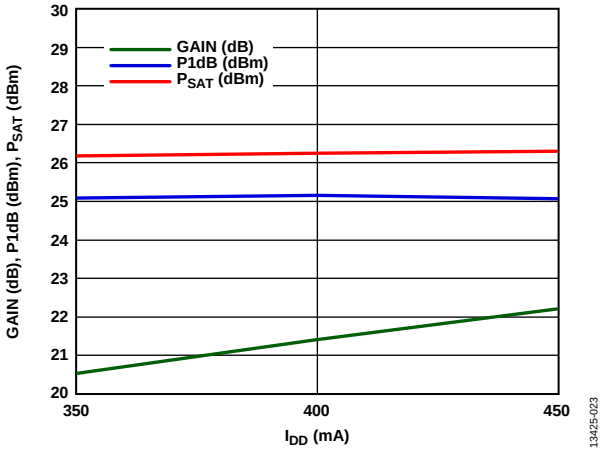


Figure 23. Gain, Output P1dB, and P_{SAT} vs. Drain Current (I_{DD}) at RF = 81 GHz

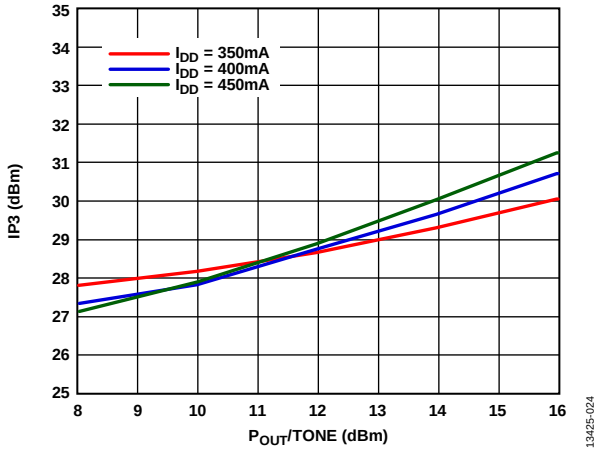


Figure 24. Output IP3 vs. P_{OUT}/Tone at Various Drain Currents (I_{DD}) at RF = 81 GHz

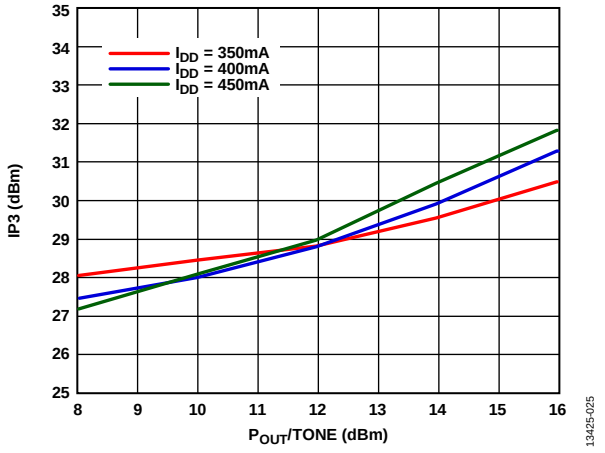


Figure 25. Output IP3 vs. P_{OUT}/Tone at Various Drain Currents (I_{DD}) at RF = 86 GHz

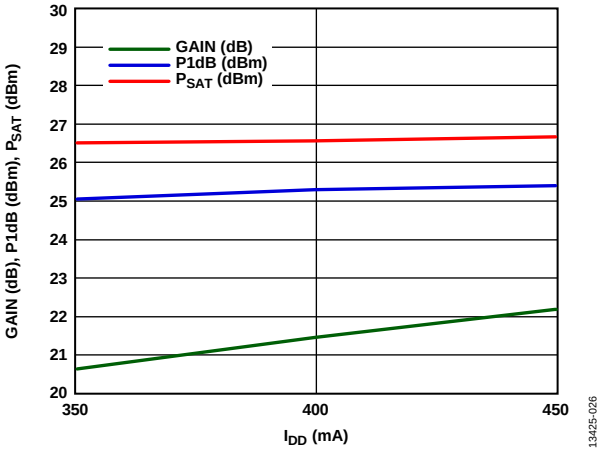


Figure 26. Gain, Output P1dB, and P_{SAT} vs. Drain Current (I_{DD}) at RF = 83.5 GHz

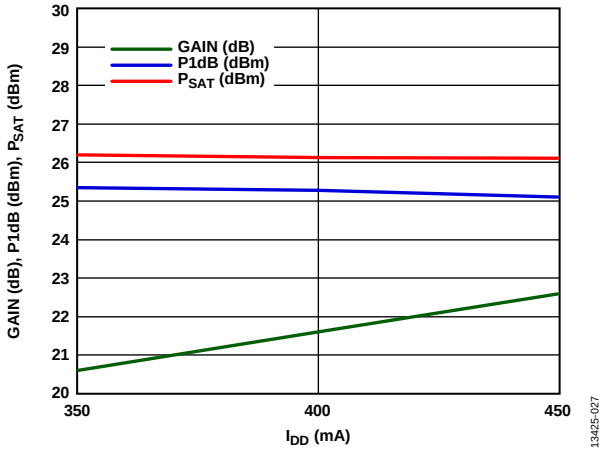


Figure 27. Gain, Output P1dB, and P_{SAT} vs. Drain Current (I_{DD}) at RF = 86 GHz

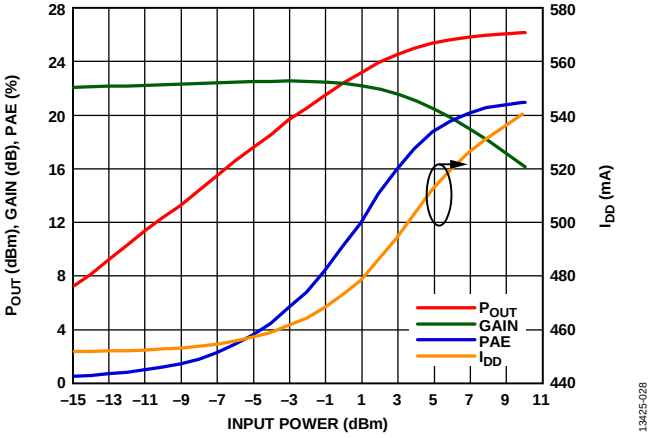


Figure 28. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at RF = 83.5 GHz, Drain Current (I_{DD}) = 450 mA

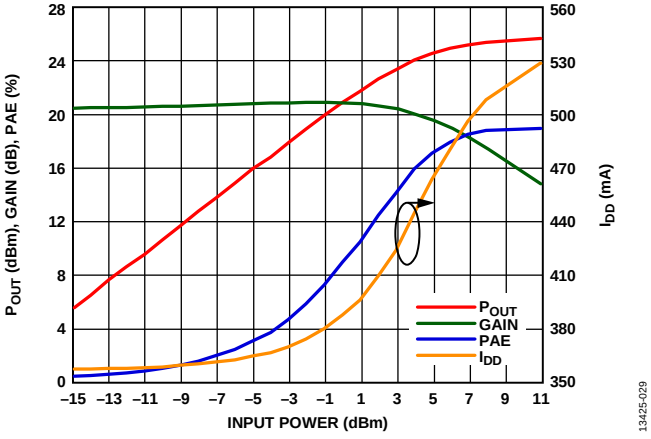


Figure 29. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at RF = 81 GHz, Drain Current (I_{DD}) = 350 mA

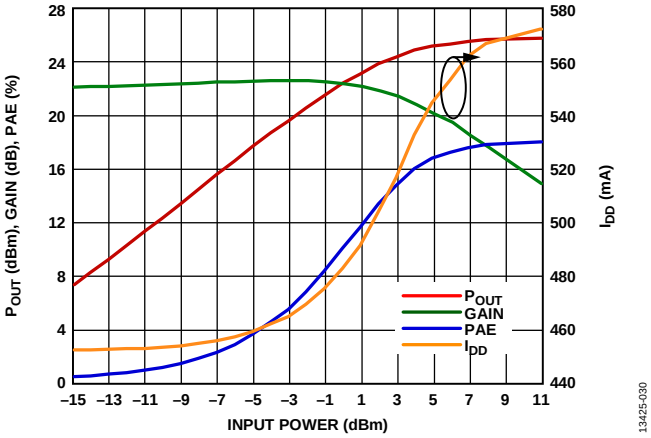


Figure 30. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at RF = 81 GHz, Drain Current (I_{DD}) = 450 mA

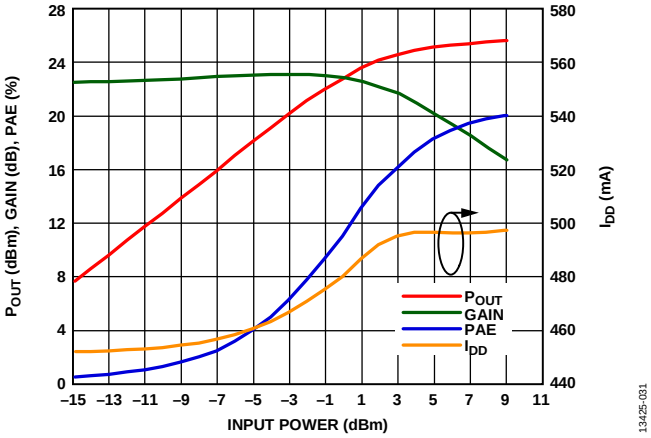


Figure 31. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at RF = 86 GHz, Drain Current (I_{DD}) = 450 mA

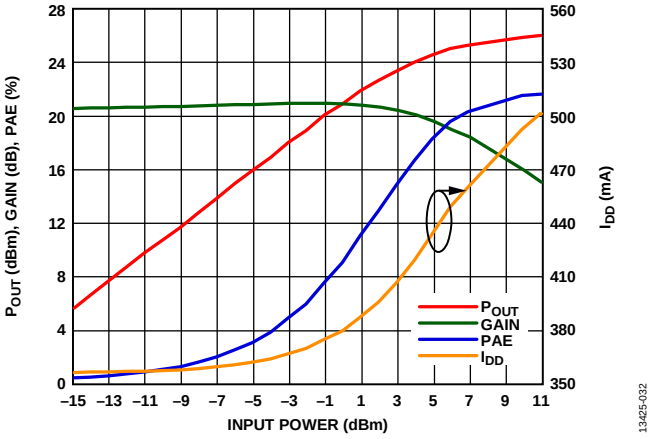


Figure 32. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at RF = 83.5 GHz, Drain Current (I_{DD}) = 350 mA

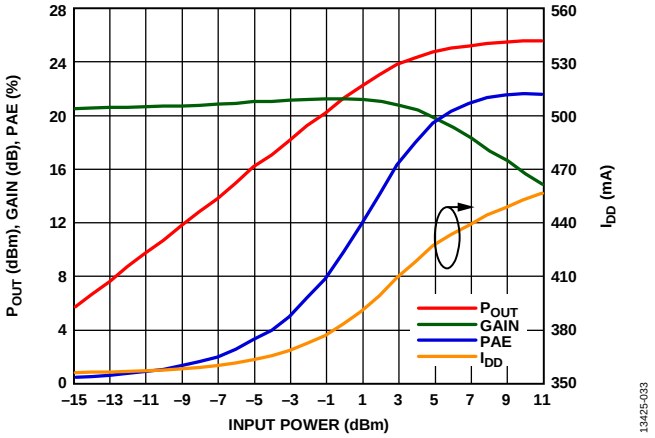


Figure 33. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at RF = 86 GHz, Drain Current (I_{DD}) = 350 mA

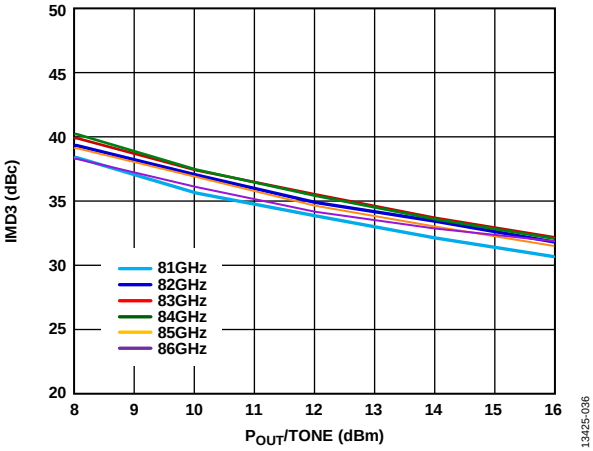


Figure 36. Output IMD3 vs. P_{OUT}/Tone at Various Frequencies, Drain Current (I_{DD}) = 450 mA

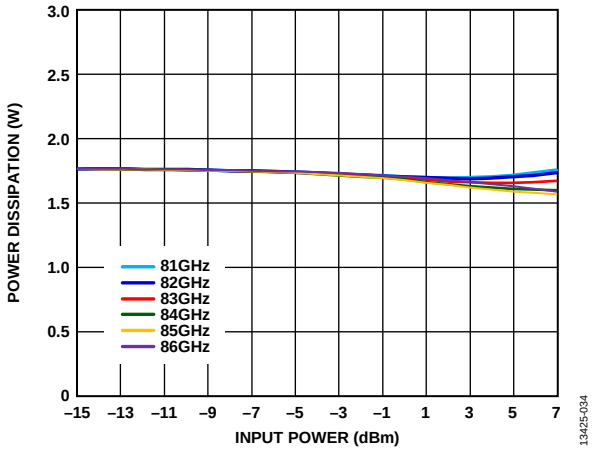


Figure 34. Power Dissipation vs. Input Power at Various Frequencies, Drain Current (I_{DD}) = 450 mA, T_A = 85°C

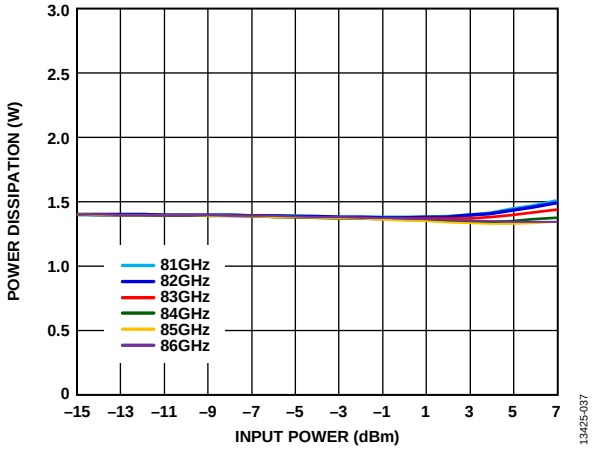


Figure 37. Power Dissipation vs. Input Power at Various Frequencies, Drain Current (I_{DD}) = 350 mA, T_A = 85°C

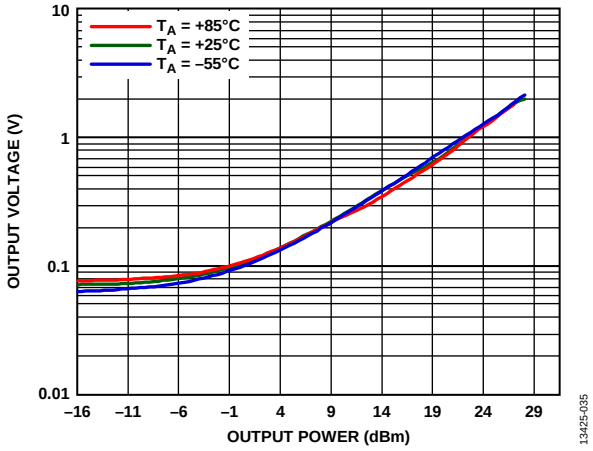


Figure 35. Detector Output Voltage (V_{OUT}) vs. Output Power at Various Temperatures, Drain Current (I_{DD}) = 450 mA, RF = 81 GHz

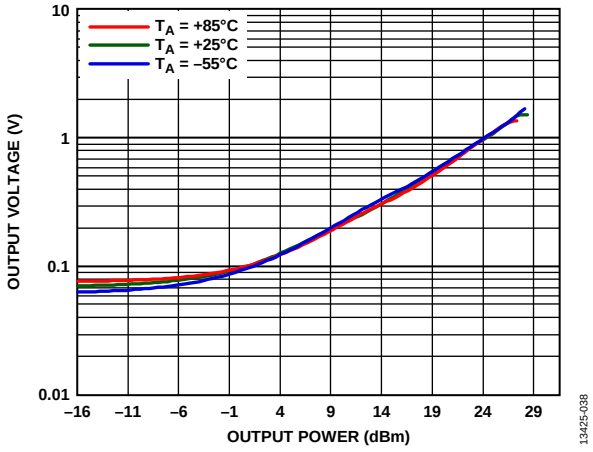


Figure 38. Detector Output Voltage (V_{OUT}) vs. Output Power at Various Temperatures, Drain Current (I_{DD}) = 450 mA, RF = 86 GHz

THEORY OF OPERATION

The architecture of the HMC8142 power amplifier is shown in Figure 39. The HMC8142 uses four cascaded gain stages to form an amplifier with a combined gain of 21 dB and saturated output power (P_{SAT}) of 26 dBm. At the output of the last stage, a coupler taps off a small portion of the output signal. The coupled signal is presented to an on-chip diode detector for external monitoring of the output power. A matched reference diode is included to help correct for detector temperature dependencies. See the application circuit shown in Figure 40 for further details on biasing the different blocks and using the detector features.

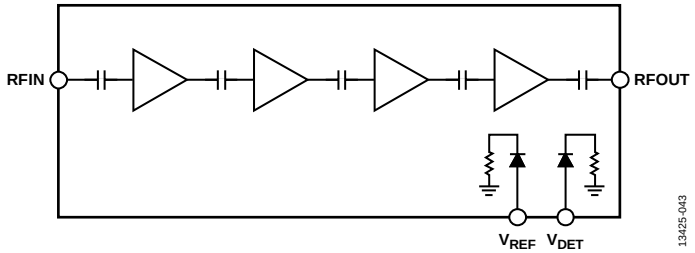


Figure 39. Power Amplifier Circuit Architecture

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

A typical application circuit for the HMC8142 is shown in Figure 40. Combine supply lines as shown in the application circuit schematic to minimize external component count and simplify power supply routing.

The HMC8142 uses several amplifier, detector, and attenuator stages. All stages use depletion mode pHEMT transistors. It is important to follow the following power-up bias sequence to ensure transistor damage does not occur.

1. Apply a −2 V bias to the V_{GG1} to V_{GG4} pads.
2. Apply 4 V to the V_{DD1} to V_{DD4} pads.
3. Adjust V_{GG1} to V_{GG4} between −2 V and 0 V to achieve a total amplifier drain current of 450 mA.

To power down the HMC8142, follow the procedure in reverse.

For additional guidance on general bias sequencing, see the *MMIC Amplifier Biasing Procedure* application note.

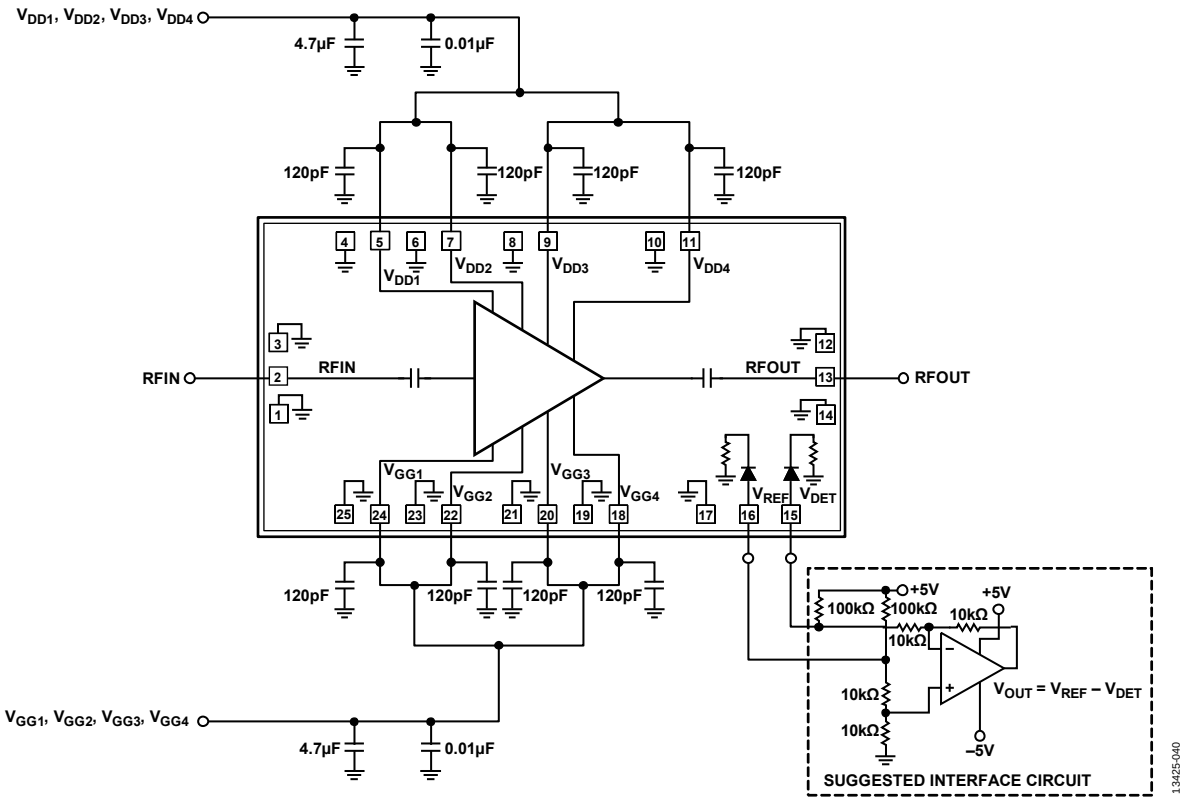


Figure 40. Typical Application Circuit

ASSEMBLY DIAGRAM

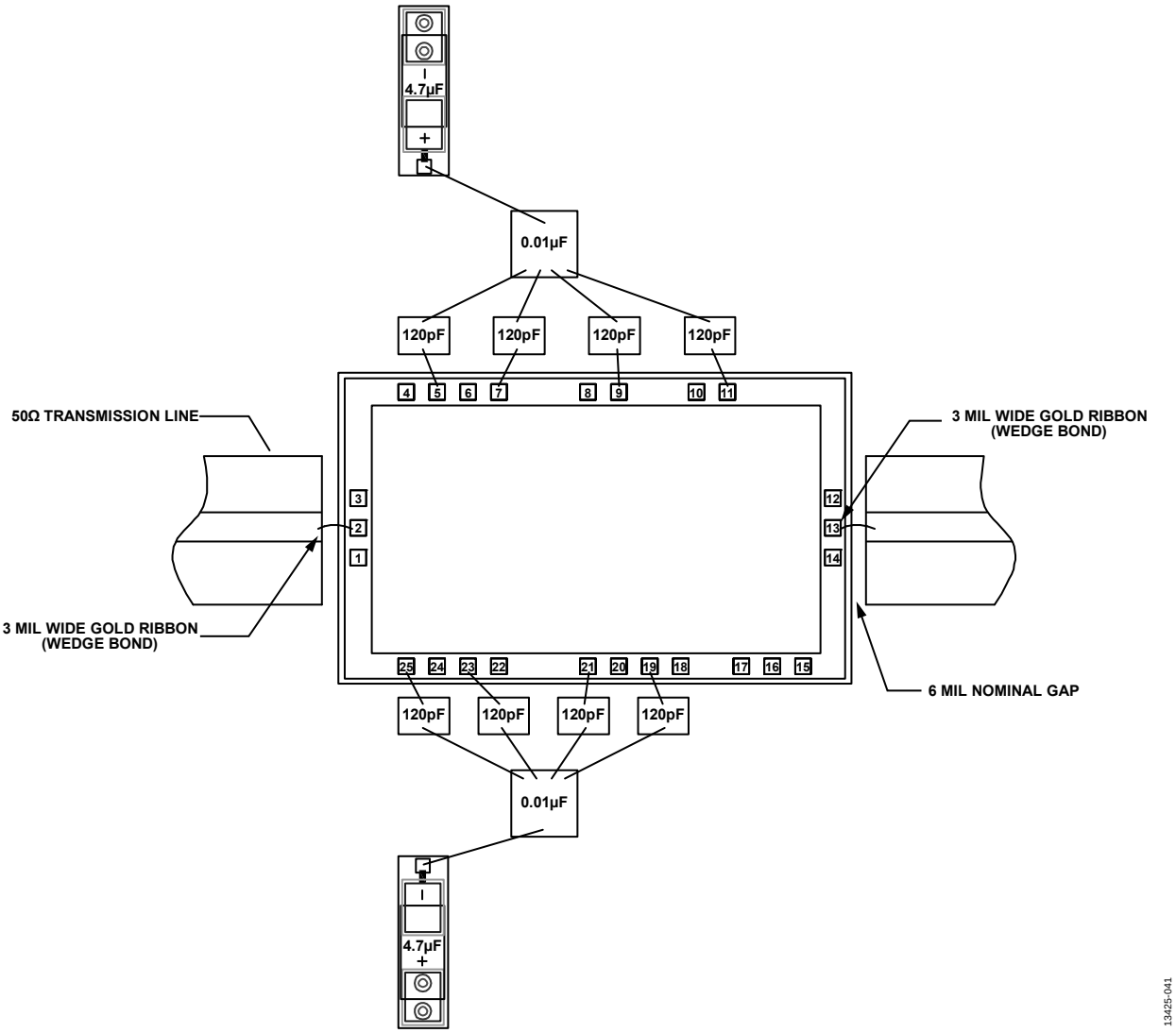


Figure 41. Assembly Diagram

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GAAS MMICS

Attach the die directly to the ground plane eutectically or with conductive epoxy.

To bring RF to and from the chip, use 50 Ω microstrip transmission lines on 0.127 mm (5 mil) thick alumina thin film substrates (see Figure 42).

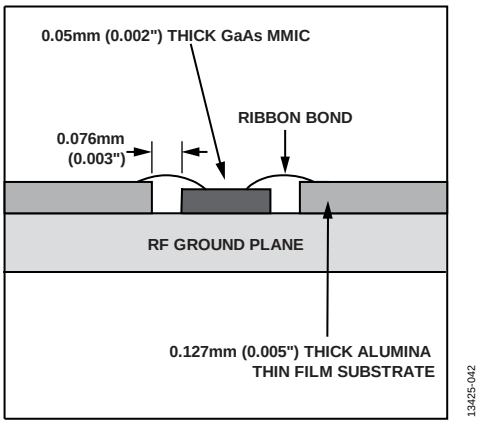


Figure 42. Routing RF Signals

To minimize bond wire length, place microstrip substrates as close to the die as possible. The typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

HANDLING PRECAUTIONS

To avoid permanent damage, adhere to the precautions in the following sections.

Storage

All bare die ship in either waffle or gel-based ESD protective containers, sealed in an ESD protective bag. After opening the sealed ESD protective bag, all die must be stored in a dry nitrogen environment.

Cleanliness

Handle the chips in a clean environment. Never use liquid cleaning systems to clean the chip.

Static Sensitivity

Follow ESD precautions to protect against ESD strikes.

Transients

Suppress instrument and bias supply transients while bias is applied. To minimize inductive pickup, use shielded signal and bias cables.

General Handling

Handle the chip on the edges only using a vacuum collet or with a sharp pair of bent tweezers. Because the surface of the chip has fragile air bridges, never touch the surface of the chip with a vacuum collet, tweezers, or fingers.

MOUNTING

The chip is back metallized and can be die mounted with gold/tin (AuSn) eutectic preforms or with electrically conductive epoxy. The mounting surface must be clean and flat.

Eutectic Die Attach

It is best to use an 80% gold/20% tin preform with a work surface temperature of 255°C and a tool temperature of 265°C. When hot 90% nitrogen/10% hydrogen gas is applied, maintain tool tip temperature at 290°C. Do not expose the chip to a temperature greater than 320°C for more than 20 sec. No more than 3 sec of scrubbing is required for attachment.

Epoxy Die Attach

ABLETHERM 2600BT is recommended for die attachment. Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after placing it into position. Cure the epoxy per the schedule provided by the manufacturer.

WIRE BONDING

RF bonds made with 3 mil × 0.5 mil gold ribbon are recommended for the RF ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. DC bonds of 1 mil (0.025 mm) diameter, thermosonically bonded, are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Keep all bonds as short as possible, less than 12 mil (0.31 mm).

OUTLINE DIMENSIONS

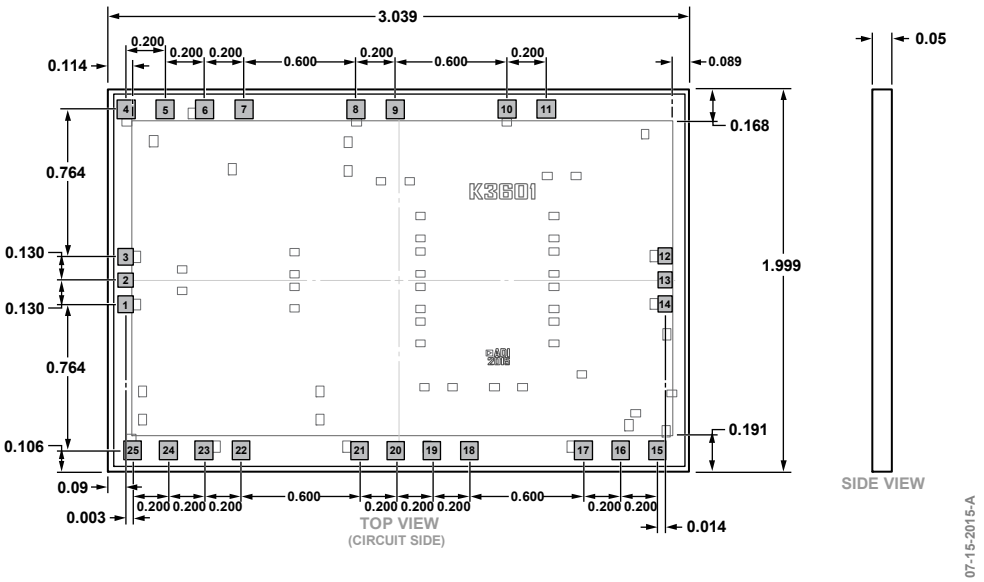


Figure 43. 25-Pad Bare Die [CHIP]
(C-25-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
HMC8142	−55°C to +85°C	25-Pad Bare Die [CHIP]	C-25-2
HMC8142-SX	−55°C to +85°C	25-Pad Bare Die [CHIP]	C-25-2

[1] The HMC8142-SX consists of two pairs of the die in a gel pack for sample orders.
[2] This is a waffle pack option; contact Analog Devices, Inc., sales representatives for additional packaging options.

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