HMC714LP5 / 714LP5E

DUAL RMS POWER DETECTOR 0.1 - 3.9 GHz

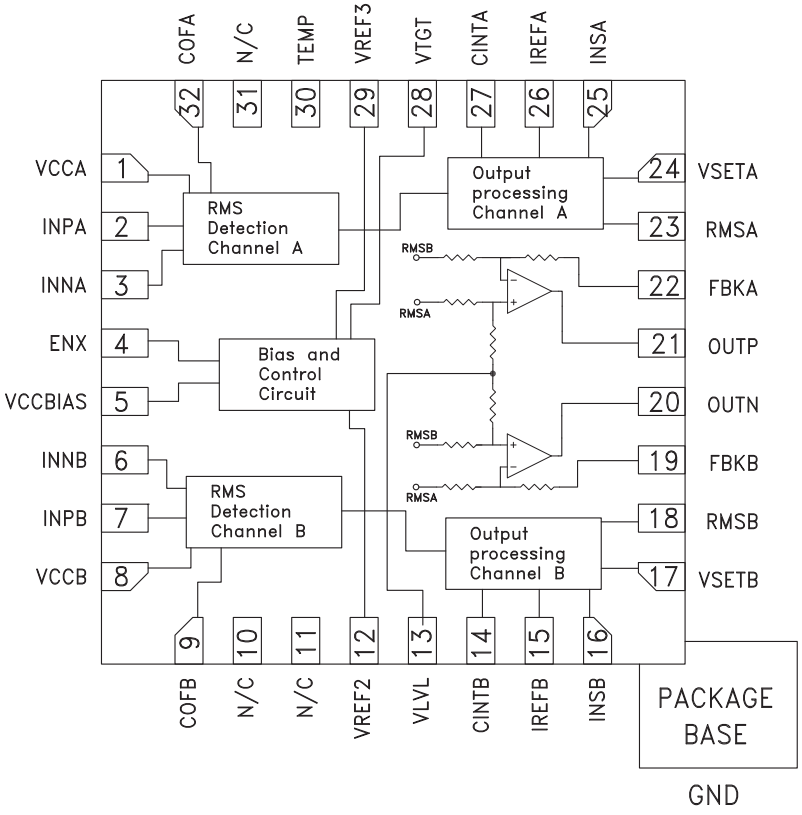
Features

- Crest Factor (Peak-to-Average Power Ratio) Measurement
- Envelope-to-Average Power Ratio Measurement
- Dual channel and channel difference output ports
- Excellent Channel Matching and Channel Isolation
- RF Signal Wave Shape & Crest Factor Independent
- Supports Controller Mode[1]
- ± 1 dB Detection Accuracy to 3.9 GHz
- Input Dynamic Range -55 dBm to +15 dBm
- +5V Operation from -40° C to +85° C
- Excellent Temperature Stability
- Integrated Temperature Sensor
- Power-Down Mode
- 32 Lead 5x5mm SMT Package: 25mm²

Typical Applications

- Log -> Root - Mean - Square (RMS) Conversion
- Transmitter Power Control
- Receiver Automatic Gain Control
- Antenna VSWR Monitor
- Received Signal Strength Indication (RSSI)
- Transmitter Signal Strength Indication (TSSI)
- Dual Channel wireless infrastructure radio

Functional Diagram



[1] For more information regarding controller mode operation, please contact your Hittite sales representative or email sales@hittite.com

General Description

The HMC714LP5E is a dual-channel RMS power detector designed for high accuracy RF power signal measurement and control applications over the 0.1 to 3.9 GHz frequency range. The device can be used with input signals having RMS values from -55 dBm to +15 dBm referenced to 50 Ω and large crest factors with no accuracy degradation.

Each RMS detection channel is fully specified for operation up to 3.9 GHz, over a wide dynamic range of 70 dB. The HMC714LP5E operates from a single +5V supply and provides two linear-in-dB detection outputs at the RMS_A and RMSB pins with scaled slopes of 37 mV/dB. The RMSA and RMSB channel outputs provide RMS detection performance in terms of dynamic range, logarithmic linearity and temperature stability similar to Hittite's HMC614LPE RMS Detector. The RMSA and RMSB outputs provide a read of average input signal power, or true-RMS power. Frequency detection up to 5.8 GHz is possible, with excellent channel matching of less than 0.5 dB (for the single-ended configuration), over a wide range of input frequencies and with low temperature drift.

The HMC714LP5E also provides "channel difference" output ports via pins OUTP and OUTN, permitting measurements of the input signal power ratio between the two power detection channels. These outputs may be used in single-ended or differential configurations. An input voltage applied to the VLVL input pin is used to set the common mode voltage reference level for OUTP and OUTN. On the Hittite evaluation board, the VLVL pin is shorted to VREF2 output to provide a nominal bias voltage of 2.5V; but any external bias voltage may be used to set VLVL.

The HMC714LP5E also features INSA and INSB pins which provide a measurement of instantaneous signal power normalized to average power level in each channel. Reading both the INSA/INSB and RMSA/RMSB output voltage signals provides a very informative picture of the RF input signal; providing peak power, average power, peak-to-average power, and RF wave shape.

The device also includes a buffered PTAT temperature sensor output with a temperature scaling factor of 2.2 mV/°C yielding a typical output voltage of 600 mV at 0°C.

The HMC714LP5E operates over the -40 to +85C temperature range, and is available in a compact, 32-lead 4x4 mm leadless QFN package

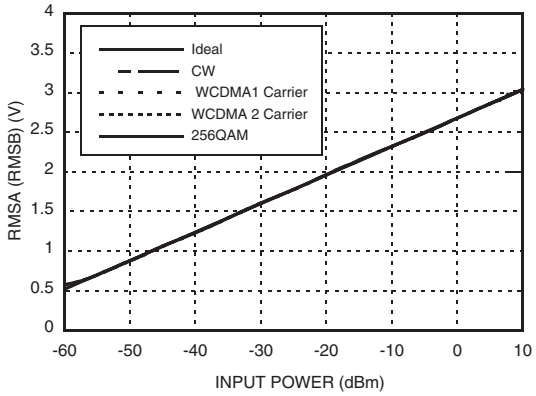
Electrical Specifications I, T_A = +25°C, VCCA = VCCB = VCCBIAS = 5V, CINT = 0.1 µF

Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Dynamic Range (± 1 dB measurement error)									
Input Signal Frequency	100	500	900	1900	2200	3000	3500	3900	MHz
Differential Input Configuration, Channel A	68	68	69	72	71	66	47	42	dB
Differential Input Configuration, Channel B	68	69	69	71	71	64	45	41	dB
Input Signal Frequency	100	900	1800 ± 300		2200 ± 300		3600 ± 300		MHz
Single-Ended Input Configuration, Channel A	70	62	71		69		61		dB
Single-Ended Input Configuration, Channel B	70	62	71		69		61		dB
Channel Isolations									
Input Signal Frequency	100	500	900	1900	2200	3000	3500	3900	MHz
Input A to Input B Isolation (Baluns Macom ETC1-1-13 at both channels)	72	70	69	53	51	56	48	47	dB
Input A to RMS_B Isolation (PIN_B = -45 dBm, RMS_B = $RMSB_{INB}$ ±1 dB)		60+	56	46	44	47			dB
Input B to RMS_A Isolation (PIN_A = -45 dBm, RMS_A = $RMSA_{INA}$ ±1 dB)		60+	58	46	44	48			dB
Input A to RMS_B Isolation (PIN_B = -40 dBm, RMS_B = $RMSB_{INB}$ ±1 dB)							47	39	dB
Input B to RMS_A Isolation (PIN_A=-40 dBm, RMS_A=$RMSA_{INA}$ ±1 dB)							43	28	dB

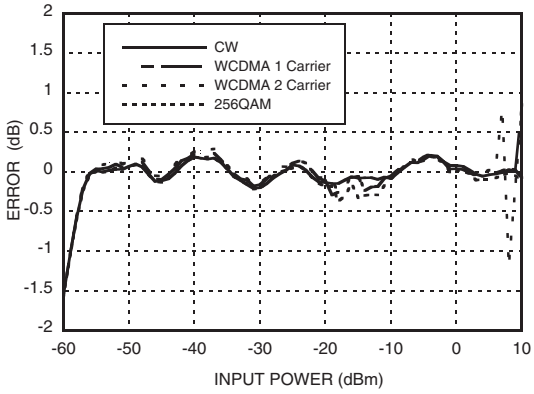
Electrical Specifications II, T_A = +25°C, VCCA = VCCB = VCCBIAS = 5V, CINT = 0.1 µF

Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Deviation vs Temperature: (Over full temperature range -40°C to 85°C. Deviation is measured from reference, which is CW input at 25°C									
Differential Input Interface with 1:1 Balun Transformer (over full input frequency range)							± 0.6		dB
Wideband Single-Ended Input Interface suitable for input signal frequencies below 1000 MHz							± 0.5		dB
Tuned Single-Ended Input Interface Suitable for input signal frequencies above 1000 MHz							± 0.6		dB
Modulation Deviation (Deviation measured from reference, which is measured with CW input at equivalent input signal power, VTGT=2V)									
Input Signal Frequency	100	500	900	1900	2200	3000	3500	3900	MHz
256QAM (2 Mbps, 8dB Crest Factor)	-0.13	-0.1	-0.1	-0.1	-0.1	-0.1	-0.3	-0.3	mV/dB
WCDMA Single Carrier (Test Model 1 with 64DPCH)	-0.3	-0.2	-0.2	-0.2	-0.2	-0.2	-0.2	-0.2	dBm
WCDMA 2 Carrier (Test Model 1 with 64DPCH)	-0.5	-0.5	-0.4	-0.4	-0.3	-0.4	-0.4	-0.4	dBm
Modulation Deviation (Deviation measured from reference, which is measured with CW input at equivalent input signal power, VTGT=1V)									
Input Signal Frequency	100	500	900	1900	2200	3000	3500	3900	MHz
256QAM (2 Mbps, 8dB Crest Factor)	0.1	0.1	0.1	0.1	0.1	0.1	-0.2	-0.1	dB
WCDMA Single Carrier (Test Model 1 with 64DPCH)	-0.1	-0.1	-0.1	-0.1	-0.1	-0.1	-0.1	-0.1	dB
WCDMA 2 Carrier (Test Model 1 with 64DPCH)	-0.1	-0.1	-0.1	-0.1	-0.1	-0.1	-0.1	-0.1	dB
Differential Input Configuration Logarithmic Slope and Intercept									
Input Signal Frequency	100	500	900	1900	2200	3000	3500	3900	MHz
Logarithmic Slope	37.3	37.1	37	36	36	36.1	36.2	38.2	mV/dB
Logarithmic Intercept	-70	-70	-69.5	-72	-71.5	-68.5	-68.5	-64	dBm
Max. Input Power at +-1dB Error	12	14	13	15	15	13	-5	-8	dBm
Min. Input Power at +-1dB Error	-56	-55	-56	-56	-56	-52	-52	-49	dBm
Single Ended Input Configuration Logarithmic Slope and Intercept									
Input Signal Frequency	100	900	1800 ± 300		2200 ± 300		3600 ± 300		MHz
Logarithmic Slope	38.2	37.9	36.6		35.4		36.8		mV/dB
Logarithmic Intercept	-67	-67.5	-67		-67		-64.5		dBm
Max. Input Power at +-1dB Error	14	6	15		15		12		dBm
Min. Input Power at +-1dB Error	-56	-56	-56		-54		-49		dBm
iPAR Feature: INS[A,B] outputs follow Amplitude Modulated Envelope Power, scaled to Average (RMS) Signal Power									
INS[A,B] and IREF[A,B] are measured with Rext = 3.9 kΩ and 50 kΩ active scope probe									
IREF[A,B] Output Voltage								1.6	V
INS[A,B] Output Voltage, with CW Input Signal (EAR = 1: Reference Condition)[1]								1.6	V
INS[A,B] Scaling Factor (SF) with V_{TGT} = 2V								190	mV
INS[A,B] Scaling Factor (SF) with V_{TGT} = 1V								95	mV
INS[A,B] Output: Variation over Temperature (-40C to 85C)								± 2	%
INS[A,B] Output: 3 dB Video BW								35	MHz
[1] EAR: Amplitude Modulated Envelope Signal Power-to-Average (RMS) Signal Power Ratio; EAR = 1 for CW signals									

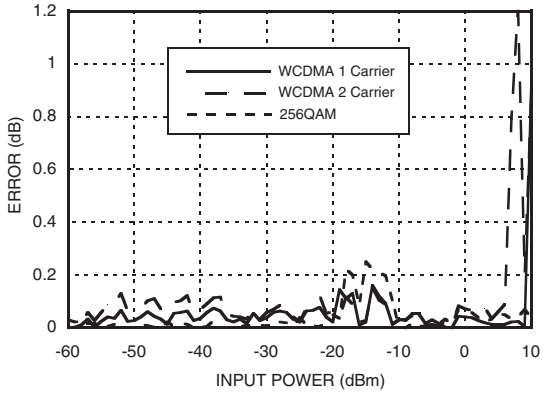
RMS [A,B] vs. Pin with Different Modulations @ 1900 MHz, VTGT= 1V



RMS [A,B] Error vs. Pin with Different Modulations @ 1900 MHz, VTGT= 1V



Logarithmic Error wrt to CW Response @ 1900 MHz for Different Modulation Schemes, VTGT= 1V



Logarithmic Error wrt to CW Response @ 1900 MHz for Different Modulation Schemes, VTGT= 2V

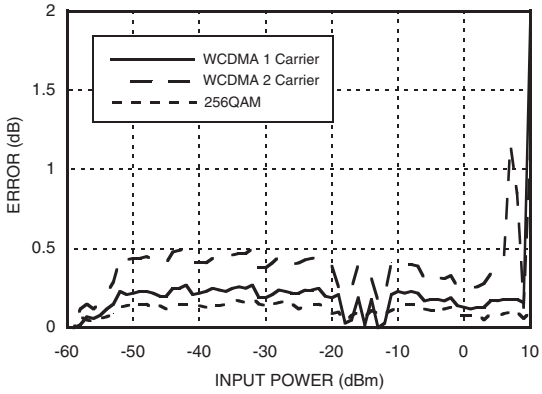


Table 3: Electrical Specifications [III],

HMC714LP5E Differential Configuration, TA=25°C, VCCA = VCCB = VCCBIAS = 5V, Cint = 0.1 uF, unless otherwise noted

Parameter	Conditions	Min.	Typ.	Max.	Units
Differential Input Configuration					
Input Network Return Loss	up to 2.5 GHz[1]		> 10		dB
Input Resistance between INP_A and INN_A	Between pins 2 and 3		220		Ohms
Input Resistance between INP_B and INN_B	Between pins 6 and 7		220		Ohms
Input Voltage Range	$V_{DIFFINA} = V_{INPA} - V_{INNA}$ and $V_{DIFFINB} = V_{INPB} - V_{INNB}$			2.25	V
RMSOUT [A,B] Output					
Output Voltage Range	RL = 1kOhm, CL = 4.7pF [2]		0.4 to 3.2		V
Openloop Output Voltage Range	RMS-VSET disconnected for control applications		0.4 to Vcc-1		V
Source/Sink Current Compliance	Measured with 900 MHz input RF signal at -30 dBm power		10/1.1		mA
Output Slew Rate (rise/fall)	With C_{INT}=0, Cofs=0		110/6		10^6 V/sec

Table 3: Electrical Specifications [III],

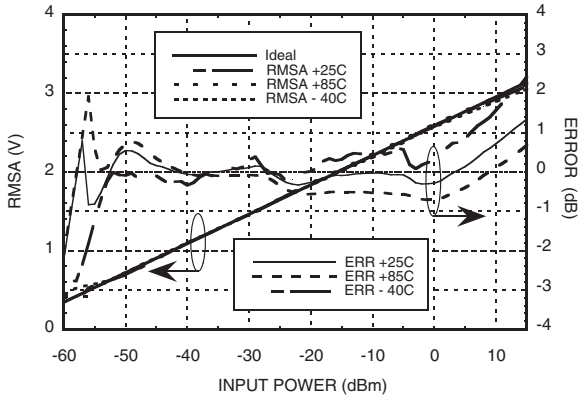
HMC714LP5E Differential Configuration, TA=25°C, VCCA = VCCB = VCCBIAS = 5V, Cint = 0.1 uF, unless otherwise noted

Parameter	Conditions	Min.	Typ.	Max.	Units
V_{SET} [A,B] Outputs					
Input Voltage Range [2]	For control applications with nominal slope/intercept settings		0.4 to 3.2		V
Input Resistance			15		kOhm
OUTP and OUTN Outputs					
Output Voltage Range	RL=1kOhm, CL=4.7pF [2]		1 to 3.9		V
Openloop Output Voltage Range	OUTP-FBKA and OUTN-FBKB disconnected for control applications		0.1 to Vcc-0.9		V
Source/Sink Current Compliance	Measured with 900 MHz input RF signal at -30 dBm power		20/4.2		mA
V_{LVL}, Common Mode Reference Level for OUT[P,N]					
Voltage Range	OUT[P,N]=FBK[A,B]	0		5	V
Input Resistance			6		kOhm
V_{REF2}, Voltage Reference Output					
Output Voltage			2.43		V
Temperature Sensitivity			0.15		mV/°C
Source/Sink Current Compliance			5.5 / 2.6		mA
V_{REF3}, Voltage Reference Output					
Output Voltage			2.94		V
Temperature Sensitivity			0.15		mV/°C
Source/Sink Current Compliance			0.15 / 0.7		mA
TEMP, Temperature Sensor Output					
Output Voltage	measured at 0°C		0.6		V
Temperature Sensitivity			2.2		mV/°C
Source/Sink Current Compliance			1.7 / 0.5		mA
ENX Logic Input, Power Down Control					
Input High Voltage		0.7*VCC			V
Input Low Voltage				0.3*VCC	V
Input Capacitance			0.5		pF
Power Supply					
Supply Voltage		4.5	5	5.5	V
Supply Current with no input power	115 mA nominal at -40°C; 153mA nominal at 85°C		138		mA
Supply Current with 0dBm at one channel	128 mA nominal at -40°C; 166mA nominal at 85°C		150		mA
Supply Current with 0dBm at both channels			164		mA
Standby Mode Supply Current			6.5		mA

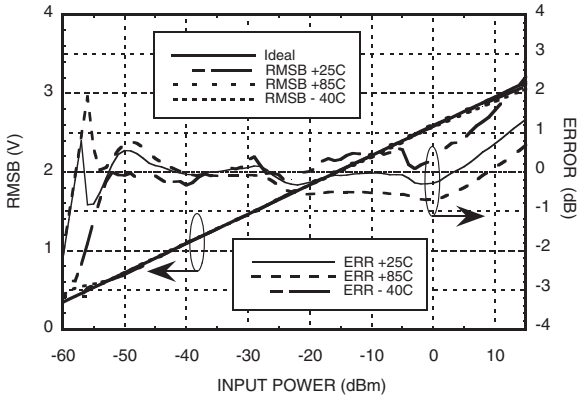
[1] Performance of differential input configuration is limited by the balun. Baluns used are M/A-COM ETC1-1-13 specified 4.5 MHz to 3000 MHz

[2] For nominal slope/intercept setting, please see application section to change this range

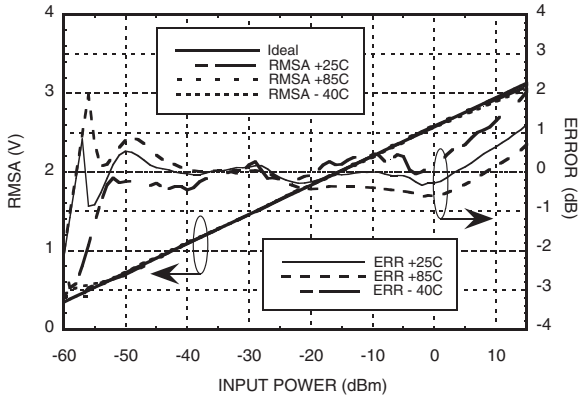
RMSA & Error vs. Pin @ 100 MHz [1]



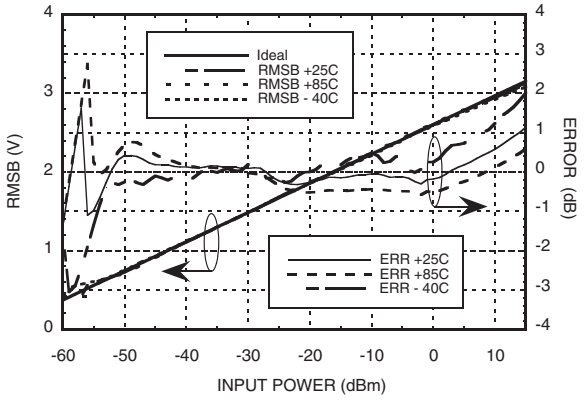
RMSB & Error vs. Pin @ 100 MHz [1]



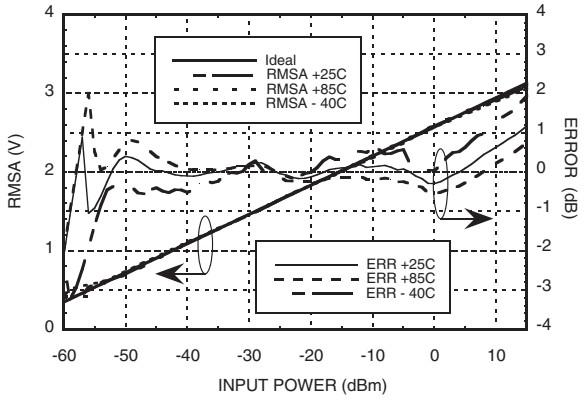
RMSA & Error vs. Pin @ 500 MHz [1]



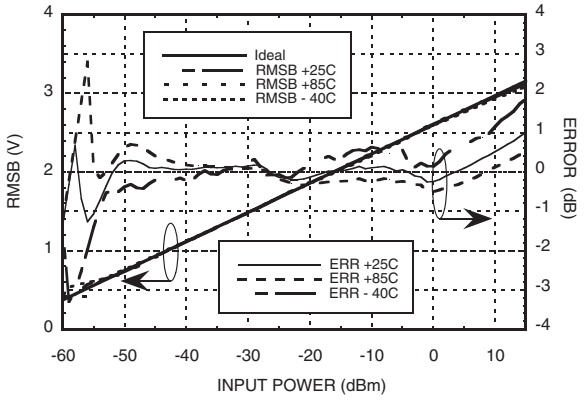
RMSB & Error vs. Pin @ 500 MHz [1]



RMSA & Error vs. Pin @ 900 MHz [1]

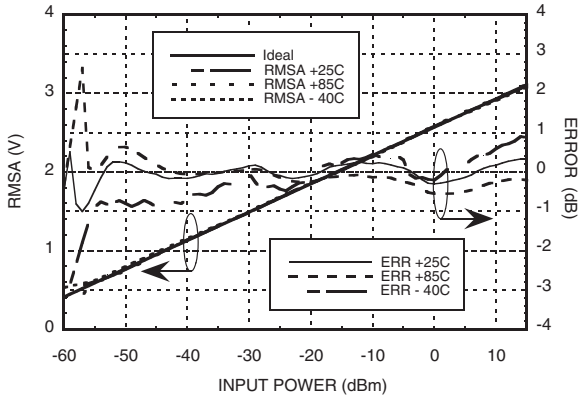


RMSB & Error vs. Pin @ 900 MHz [1]

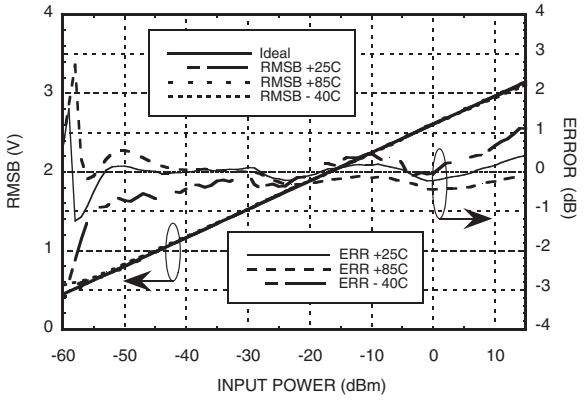


[1] CW Input Waveform

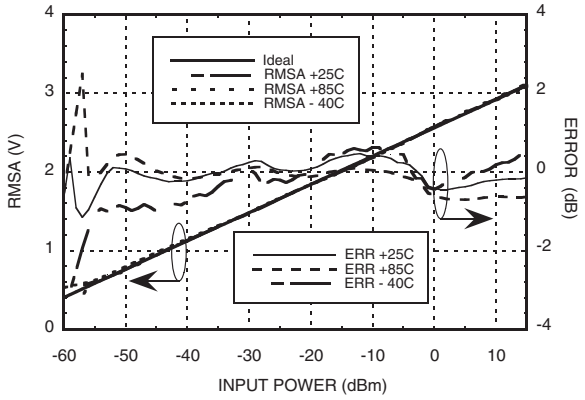
RMSA & Error vs. Pin @ 1900 MHz [1]



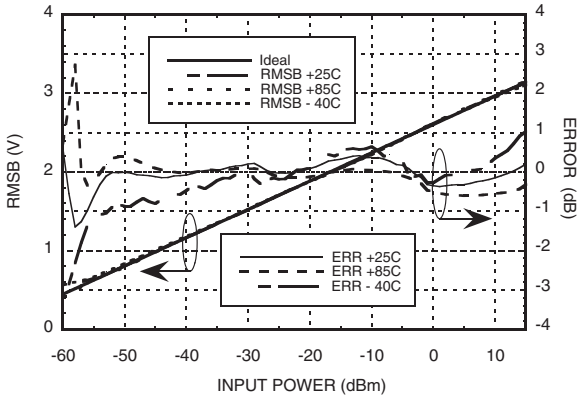
RMSB & Error vs. Pin @ 1900 MHz [1]



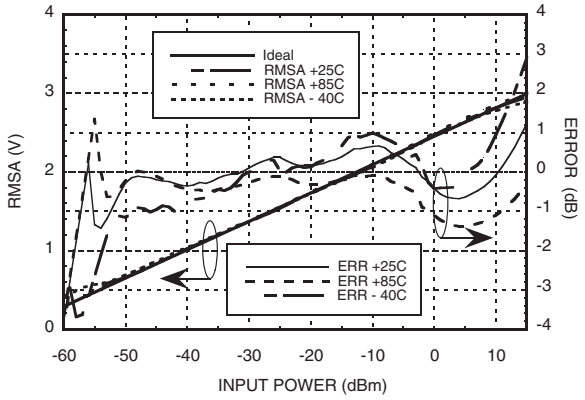
RMSA & Error vs. Pin @ 2200 MHz [1]



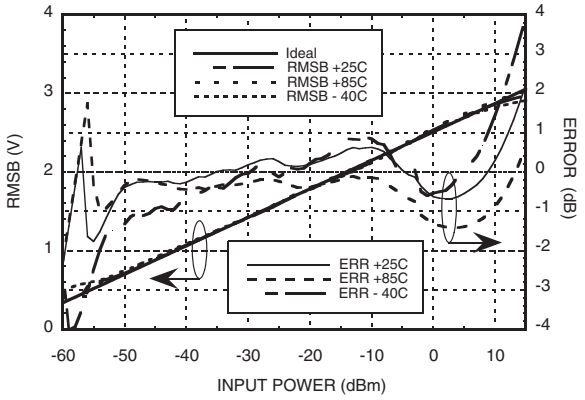
RMSB & Error vs. Pin @ 2200 MHz [1]



RMSA & Error vs. Pin @ 3000 MHz [1]



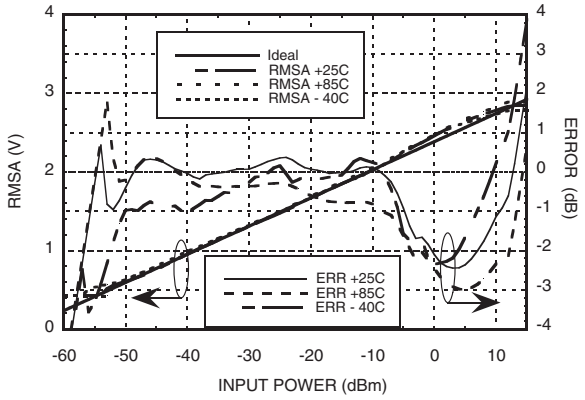
RMSB & Error vs. Pin @ 3000 MHz [1]



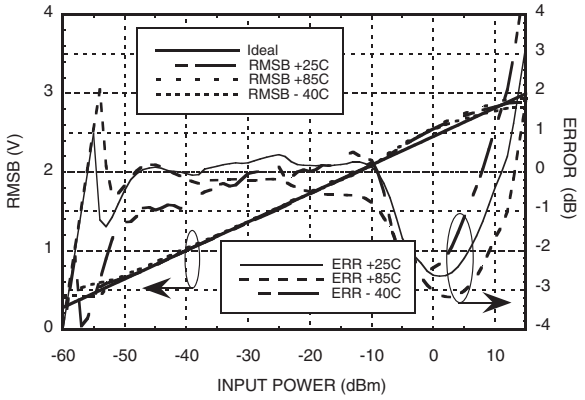
[1] CW Input Waveform

For price, delivery, and to place orders, please contact Hittite Microwave Corporation:
20 Alpha Road, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
Order On-line at www.hittite.com

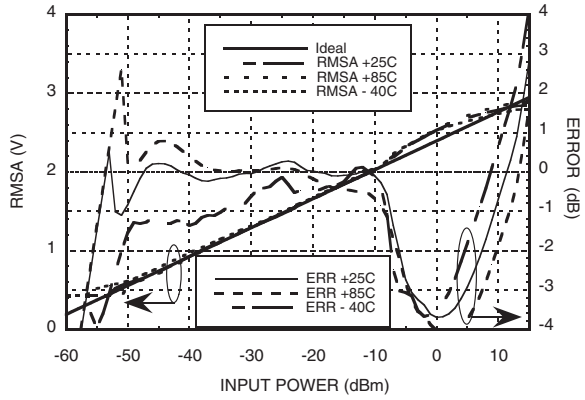
RMSA & Error vs. Pin @ 3500 MHz [1]



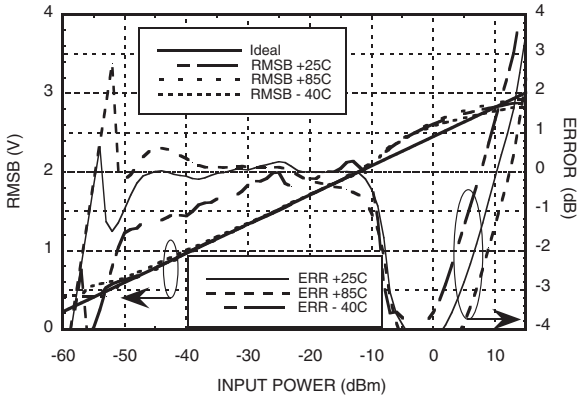
RMSB & Error vs. Pin @ 3500 MHz [1]



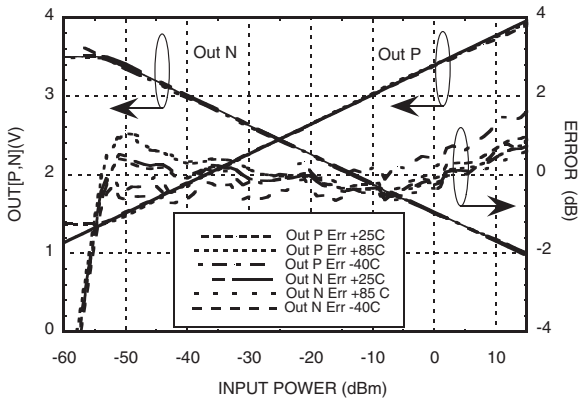
RMSA & Error vs. Pin @ 3900 MHz [1]



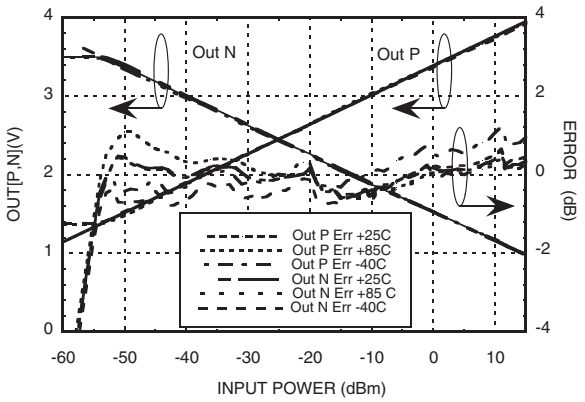
RMSB & Error vs. Pin @ 3900 MHz [1]



OUT [P,N] & Error vs. Pin @ 100 MHz, INPA Power Swept, INPB Fixed Power @ -25 dBm [1]

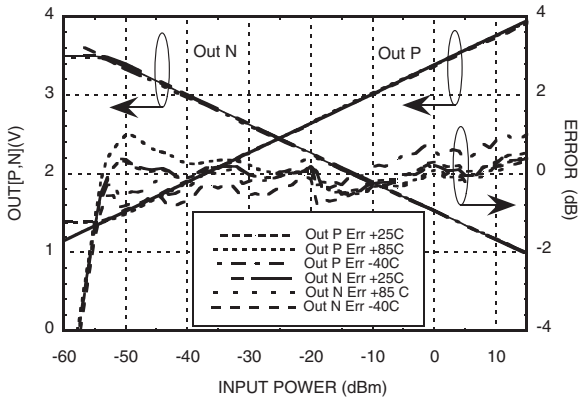


OUT [P,N] & Error vs. Pin @ 500 MHz, INPA Power Swept, INPB Fixed Power @ -25 dBm [1]

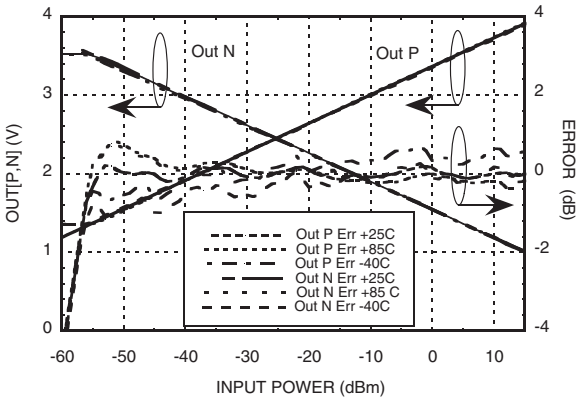


[1] CW Input Waveform

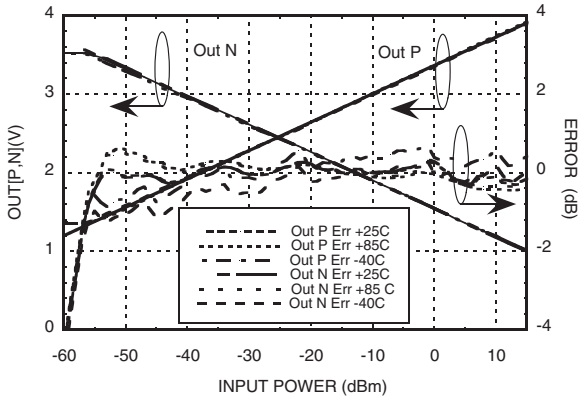
OUT [P,N] & Error vs. Pin @ 900 MHz, INPA Power Swept, INPB Fixed Power @ -25 dBm [1]



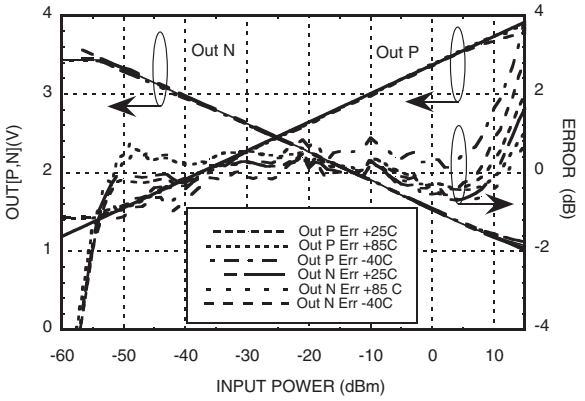
OUT [P,N] & Error vs. Pin @ 1900 MHz, INPA Power Swept, INPB Fixed Power @ -25 dBm [1]



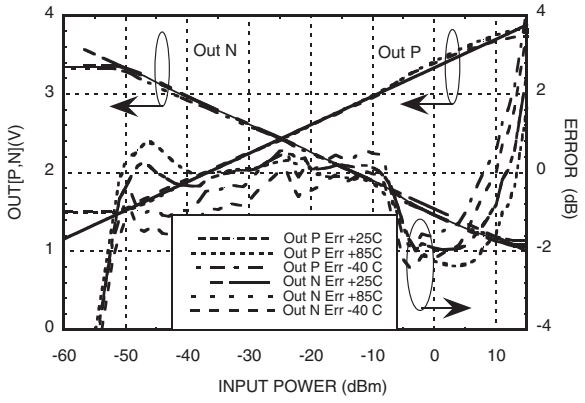
OUT [P,N] & Error vs. Pin @ 2200 MHz, INPA Power Swept, INPB Fixed Power @ -25 dBm [1]



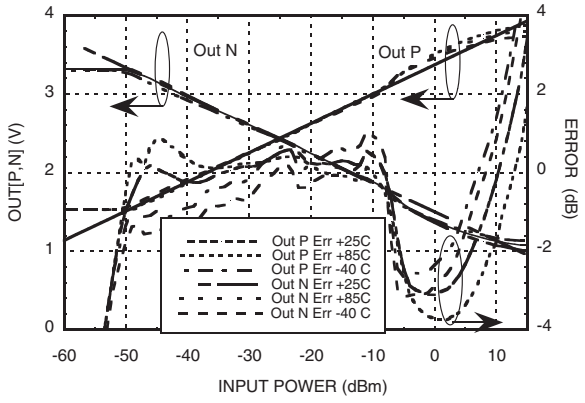
OUT [P,N] & Error vs. Pin @ 3000 MHz, INPA Power Swept, INPB Fixed Power @ -25 dBm [1]



OUT [P,N] & Error vs. Pin @ 3500 MHz, INPA Power Swept, INPB Fixed Power @ -25 dBm [1]

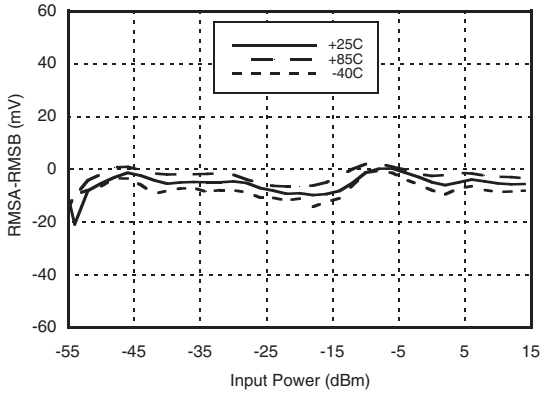


OUT [P,N] & Error vs. Pin @ 3900 MHz, INPA Power Swept, INPB Fixed Power @ -25 dBm [1]

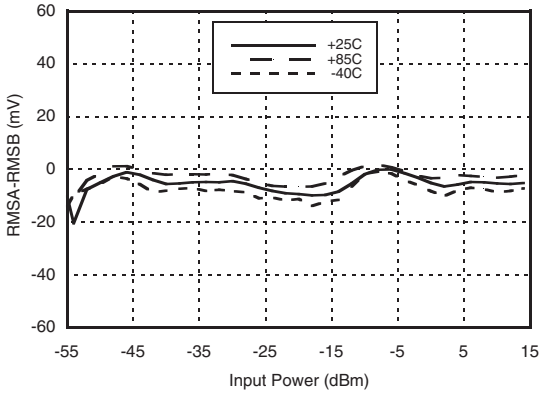


[1] CW Input Waveform

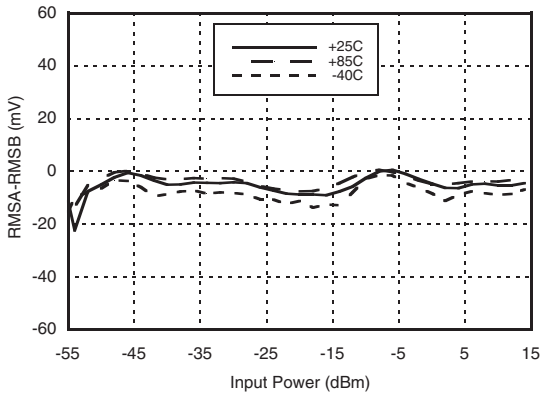
RMSA-RMSB, Channel Matching vs. Pin over Temperature @ 100 MHz [1][2]



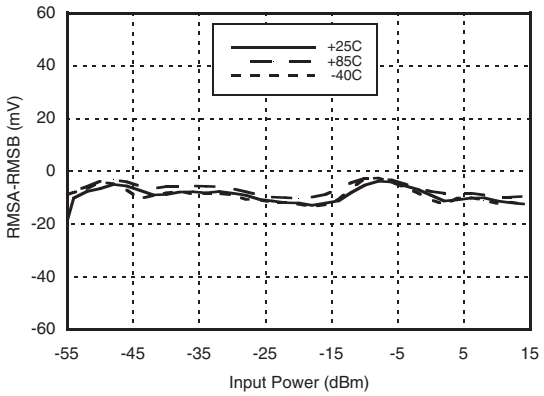
RMSA-RMSB, Channel Matching vs. Pin over Temperature @ 500 MHz [1][2]



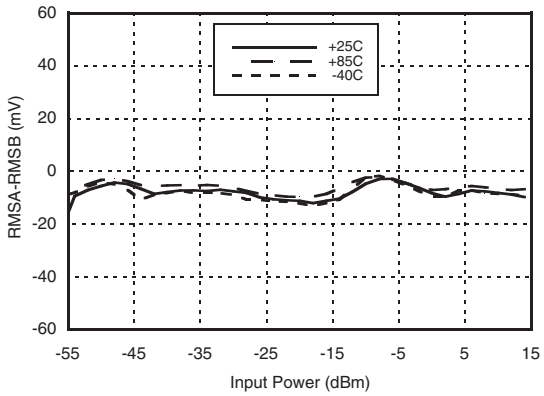
RMSA-RMSB, Channel Matching vs. Pin over Temperature @ 900 MHz [1][2]



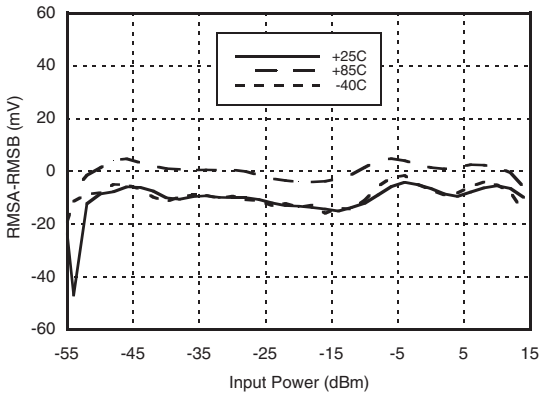
RMSA-RMSB, Channel Matching vs. Pin over Temperature @ 1900 MHz [1][2]



RMSA-RMSB, Channel Matching vs. Pin over Temperature @ 2200 MHz [1][2]



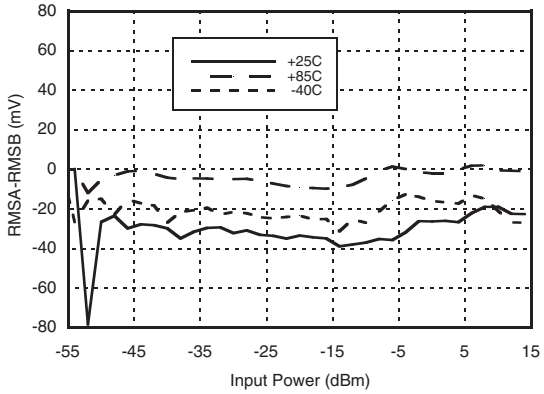
RMSA-RMSB, Channel Matching vs. Pin over Temperature @ 3000 MHz [1][2]



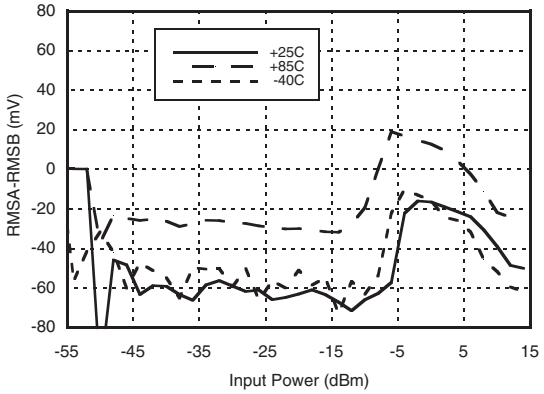
[1] CW Input Waveform

[2] Differential Input Configuration. Baluns selected for matching performance, mismatch between channels is limited by the input baluns.

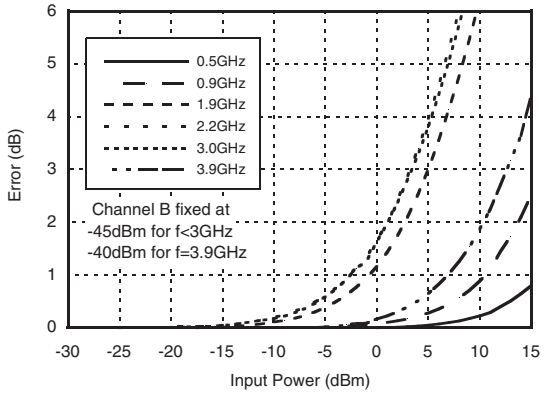
RMSA-RMSB, Channel Matching vs. Pin over Temperature @ 3500 MHz [1][2]



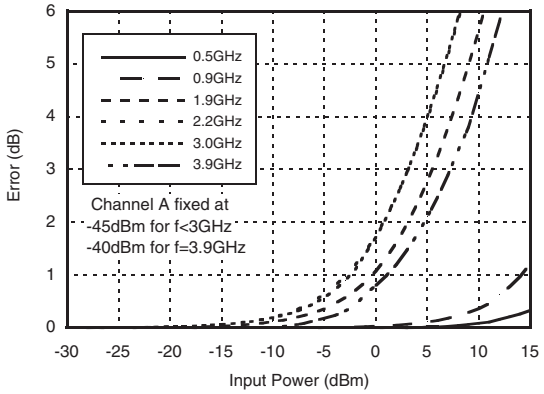
RMSA-RMSB, Channel Matching vs. Pin over Temperature @ 3900 MHz [1][2]



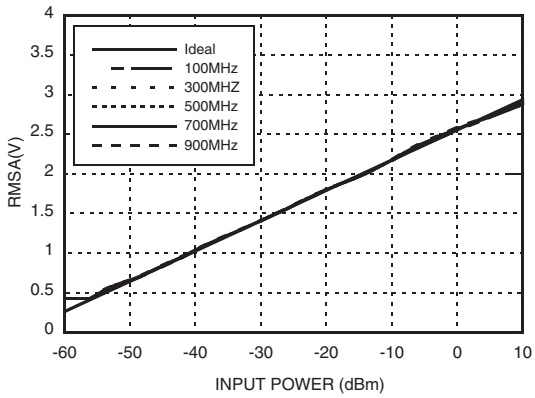
Interference to an Input Signal (INB Power Fixed) with Interfering Signal on the other Channel (INA Power Swept) [1]



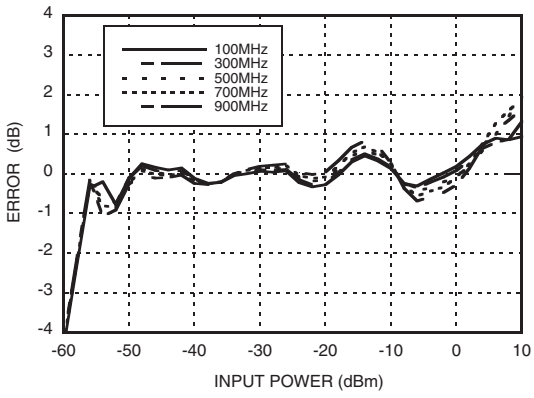
Interference to an Input Signal (INA Power Fixed) with Interfering Signal on the other Channel (INB Power Swept) [1]



RMSA Out vs. Pin over Frequency, with SE Wideband Tune [1]



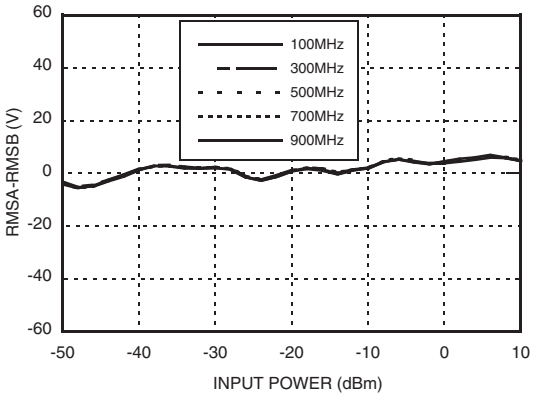
RMSA Out Error vs. Pin over Frequency, with SE Wideband Tune [1]



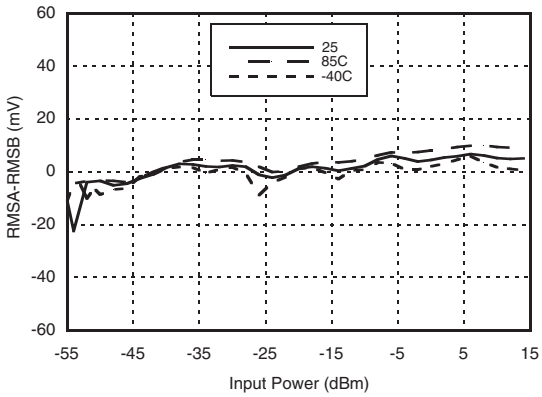
[1] CW Input Waveform

[2] Differential Input Configuration. Baluns selected for matching performance, mismatch between channels is limited by the input baluns.

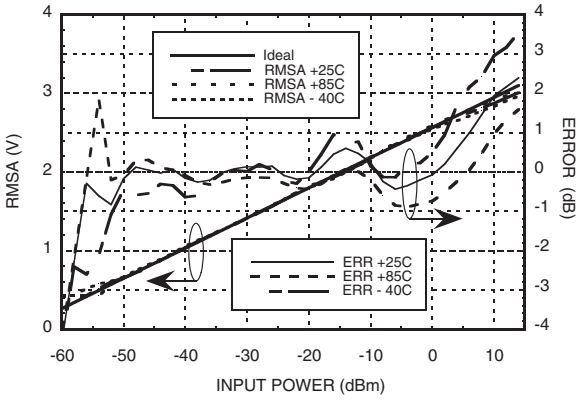
RMSA-RMSB, Channel Matching vs. Pin over Frequency, with SE Wideband Tune [1]



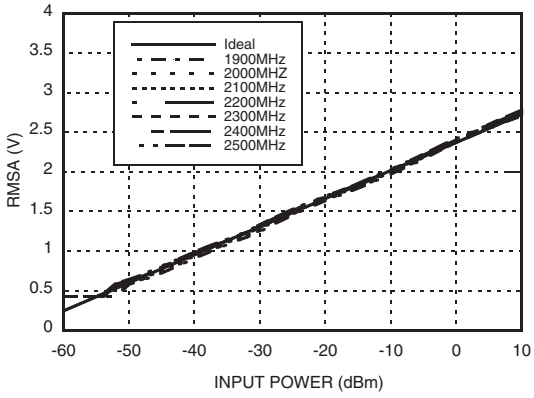
RMSA-RMSB, Channel Matching vs. Pin over Temperature @ 500 MHz, with SE Wideband Tune [1]



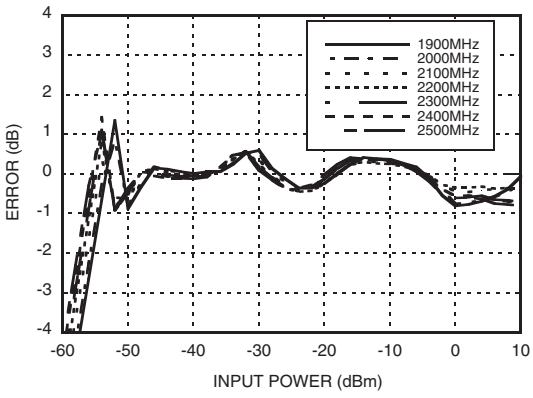
RMSA Out & Error vs. Pin over Temperature @ 500 MHz with SE Wide-band Tune [1]



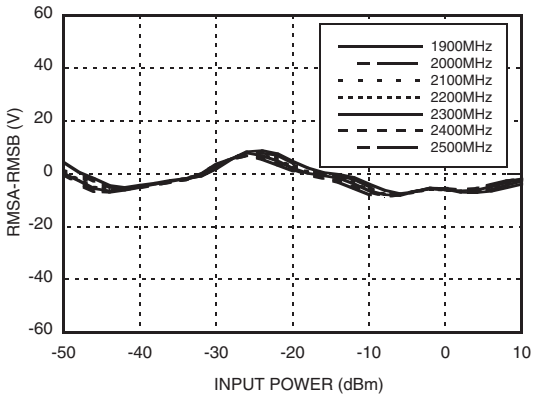
RMSA Out vs. Pin over Frequency , with 2200 MHz SE Tune [1]



RMSA Out Error vs. Pin over Frequency with 2200 MHz SE Tune [1]

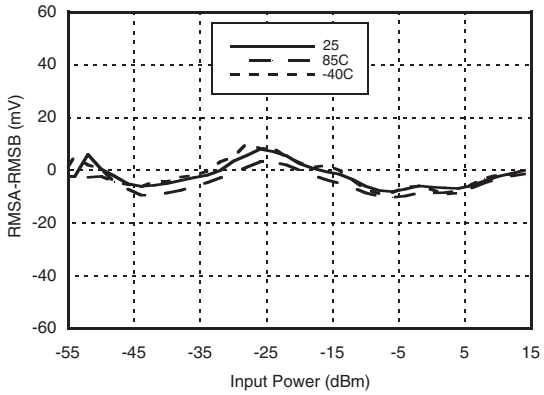


RMSA-RMSB, Channel Matching vs. Pin over Frequency, with 2200 MHz SE Wide-band Tune [1]

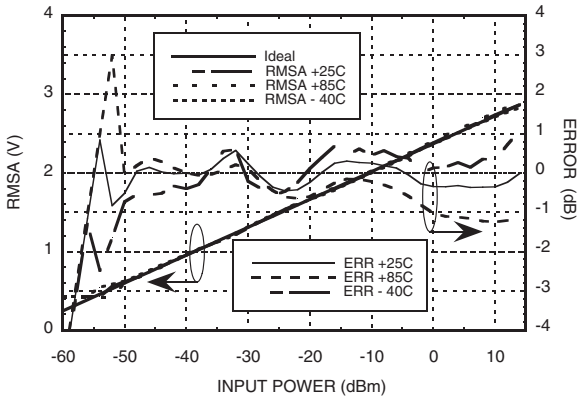


[1] CW Input Waveform

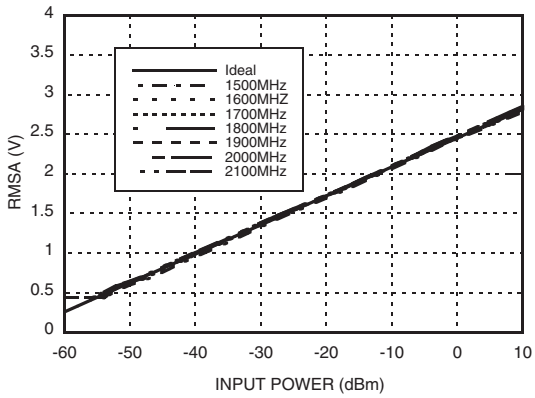
RMSA-RMSB, Channel Matching vs. Pin over Temperature, with 2200 MHz SE Tune [1]



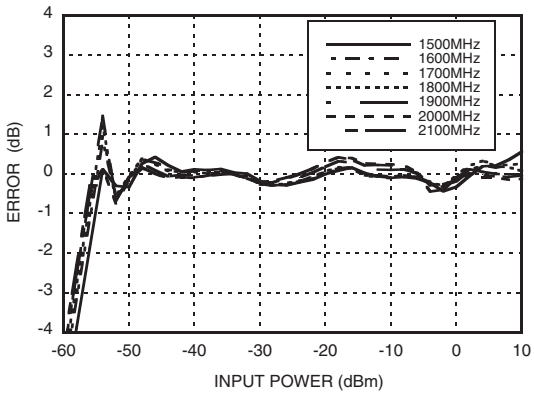
RMSA Out & Error vs. Pin over Temperature @ 2200 MHz, with 2200 MHz SE Tune [1]



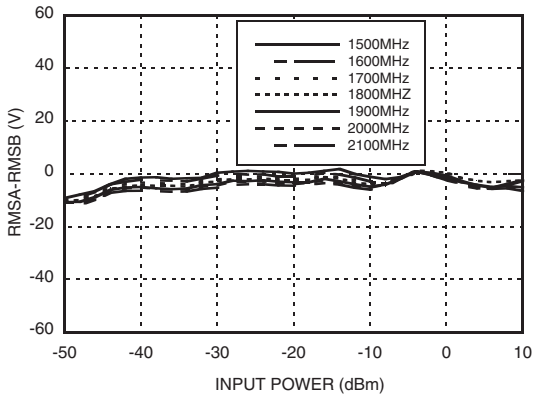
RMSA Out vs. Pin over Frequency, with 1800 MHz SE Tune [1]



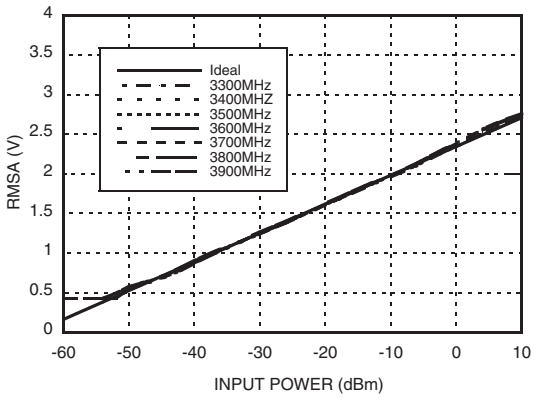
RMSA Out Error vs. Pin over Frequency, with 1800 MHz SE Tune [1]



RMSA-RMSB, Channel Matching vs. Pin over Frequency, with 1800 MHz SE Tune [1]

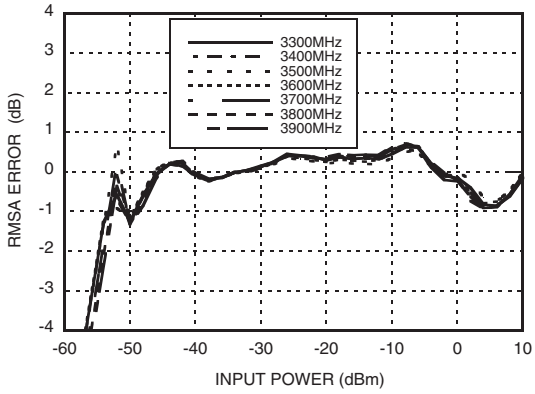


RMSA Out vs. Pin over Frequency, with 3600 MHz SE Tune [1]

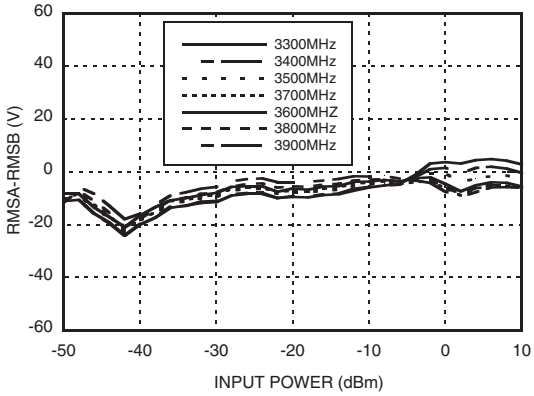


[1] CW Input Waveform

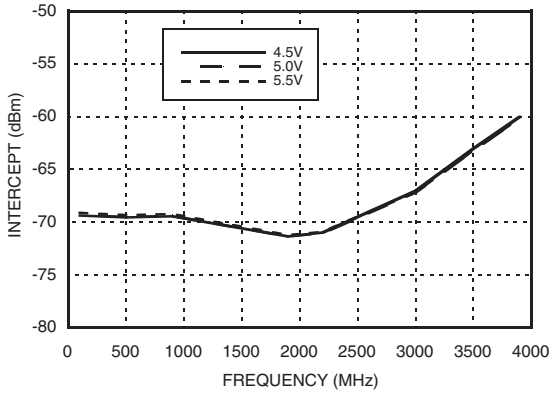
RMSA Out Error vs. Pin over Frequency, with 3600 MHz SE Tune[1]



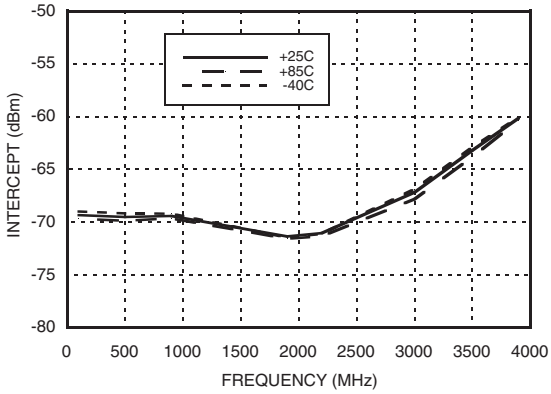
RMSA - RMSB, Channel Matching vs. Pin over Temperature, with 3600 MHz SE Tune[1]



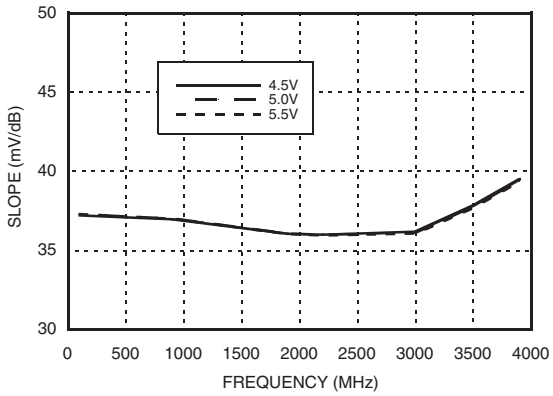
Intercept vs. Frequency Over Supply Voltage[1]



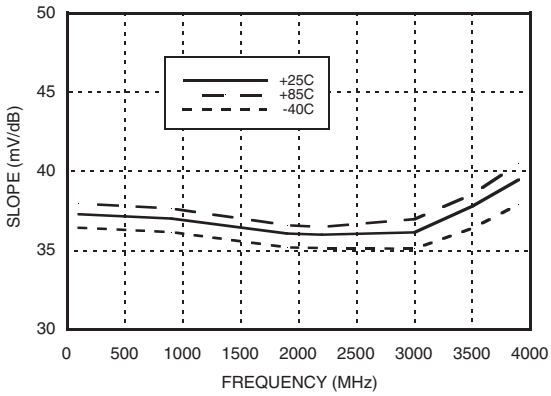
Intercept vs. Frequency Over Temperature[1]



Slope vs. Frequency Over Supply Voltage[1]

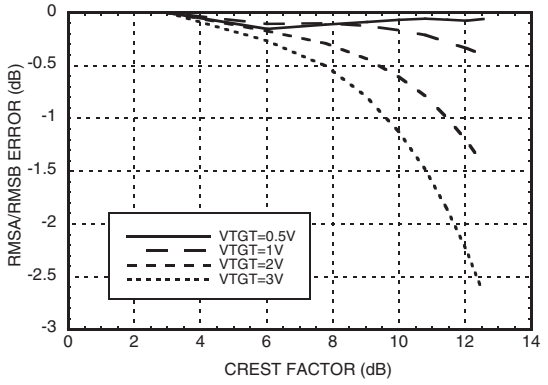


Slope vs. Frequency Over Temperature[1]

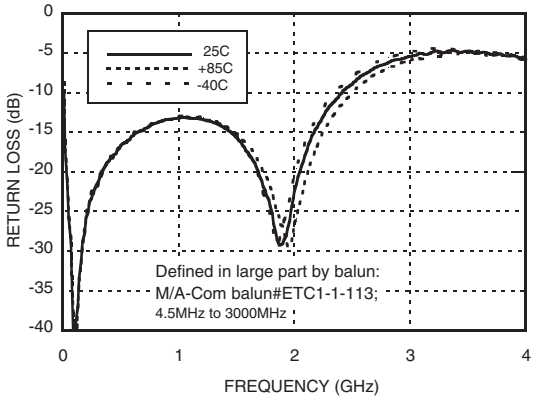


[1] CW Input Waveform

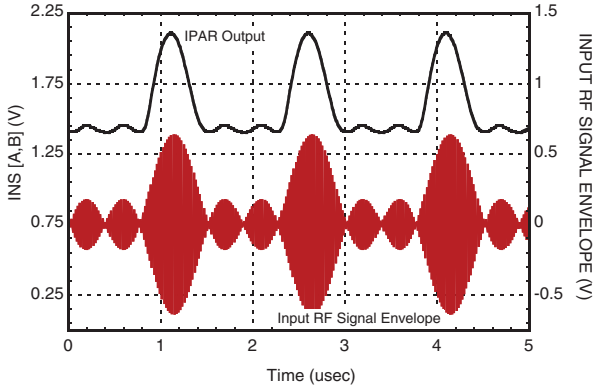
RMS Error vs. Crest Factor Over VTGT



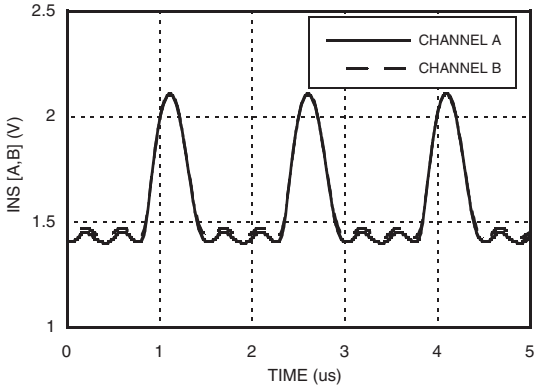
Input Return Loss [1]



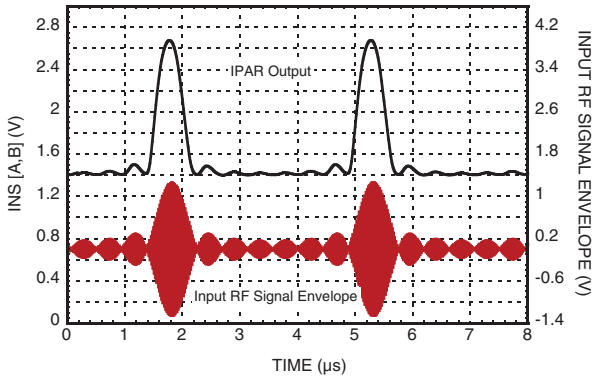
iPAR Output & Input RF Signal Envelope vs. Time for an Input Crest Factor of 9.03 dB @ 1900 MHz [2]



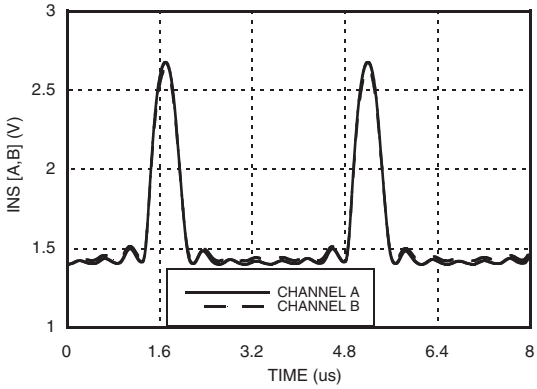
iPAR Output with an Input Crest Factor of 9.03 dB, Channel [A,B] @ 1900 MHz [2]



iPAR Output & Input RF Signal Envelope vs. Time for an Input Crest Factor of 12.04 dB @ 1900 MHz [2]



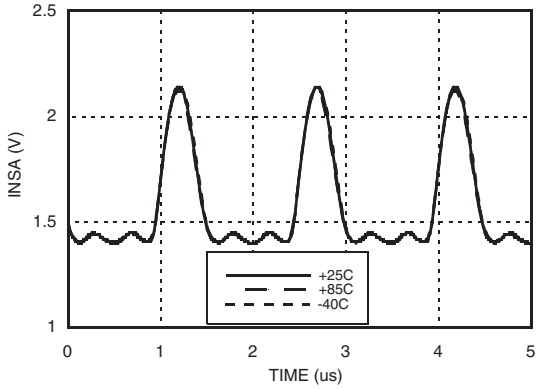
iPAR Output with an Input Crest Factor of 12.04 dB, Channel [A,B] @ 1900 MHz [2]



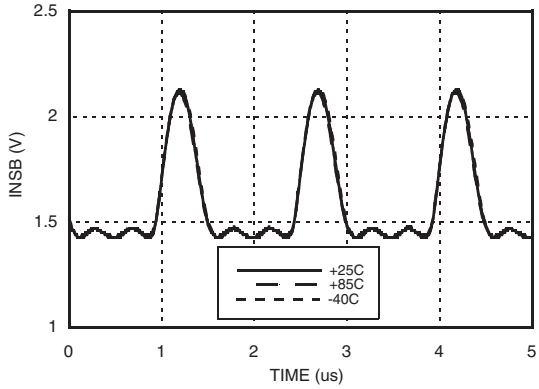
[1] CW Input Waveform
[2] RF Input Power @ -20 dBm

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20 Alpha Road, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
Order On-line at www.hittite.com

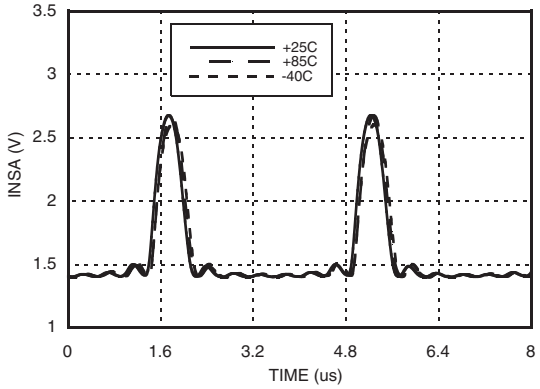
iPAR Output with an Input Crest Factor of 9.03 dB, Channel A over Temp @ 1900 MHz [1]



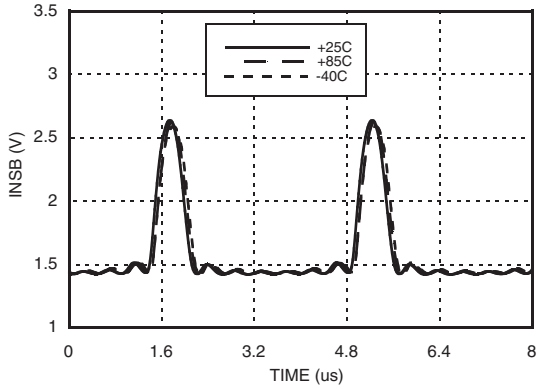
iPAR Output with an Input Crest Factor of 9.03 dB, Channel B over Temp @ 1900 MHz [1]



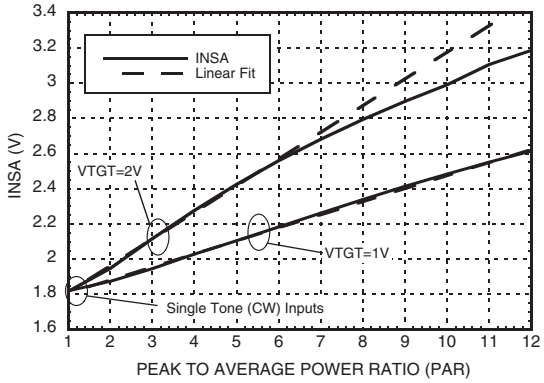
iPAR Output with an Input Crest Factor of 12.04 dB, Channel A over Temp @ 1900 MHz [1]



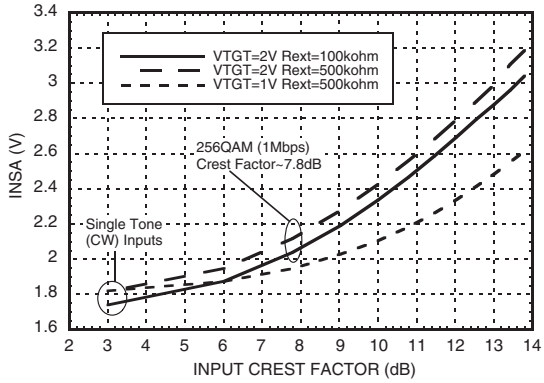
iPAR Output with an Input Crest Factor of 12.04 dB, Channel B over Temp @ 1900 MHz [1]



iPAR Feature Peak-to-Average Power Detection Configuration (R_{EXT} = 500kΩ, C_{EXT} = 100 nF)

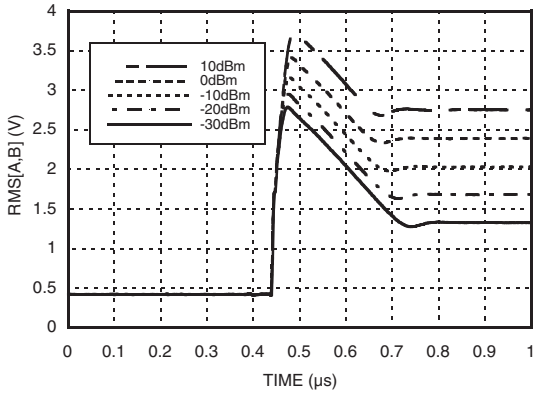


iPAR Feature Peak-to-Average Power Detection Configuration (C_{EXT} = 100 nF)

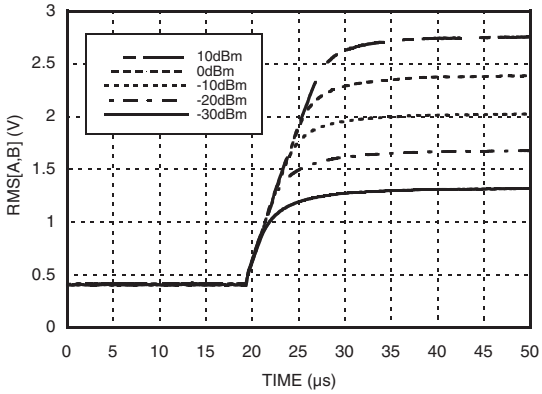


[1] RF Input Power @ -20 dBm

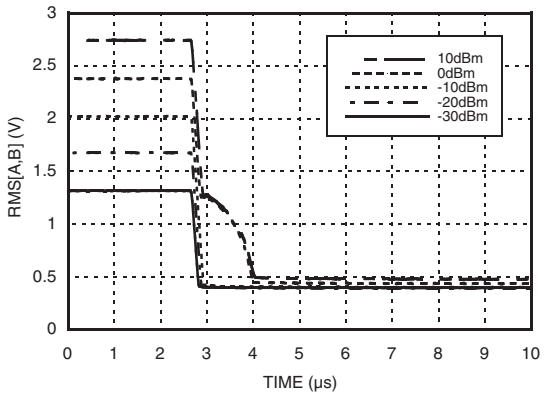
Output Response
Rise Time @ 1900 MHz, C_{INT} [A,B] = Open



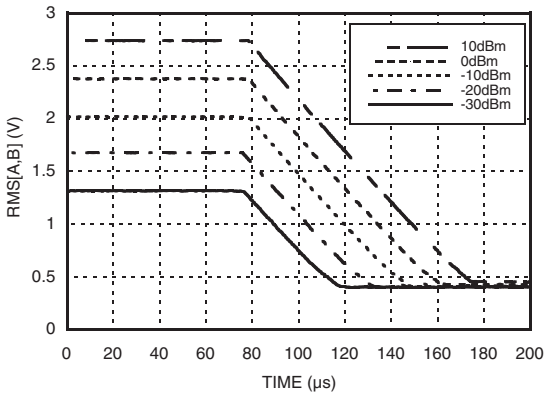
Output Response
Rise Time @ 1900 MHz, C_{INT} [A,B] = 10 nF



Output Response
Fall Time @ 1900 MHz, C_{INT} [A,B] = Open



Output Response
Fall Time @ 1900 MHz, C_{INT} [A,B] = 10 nF

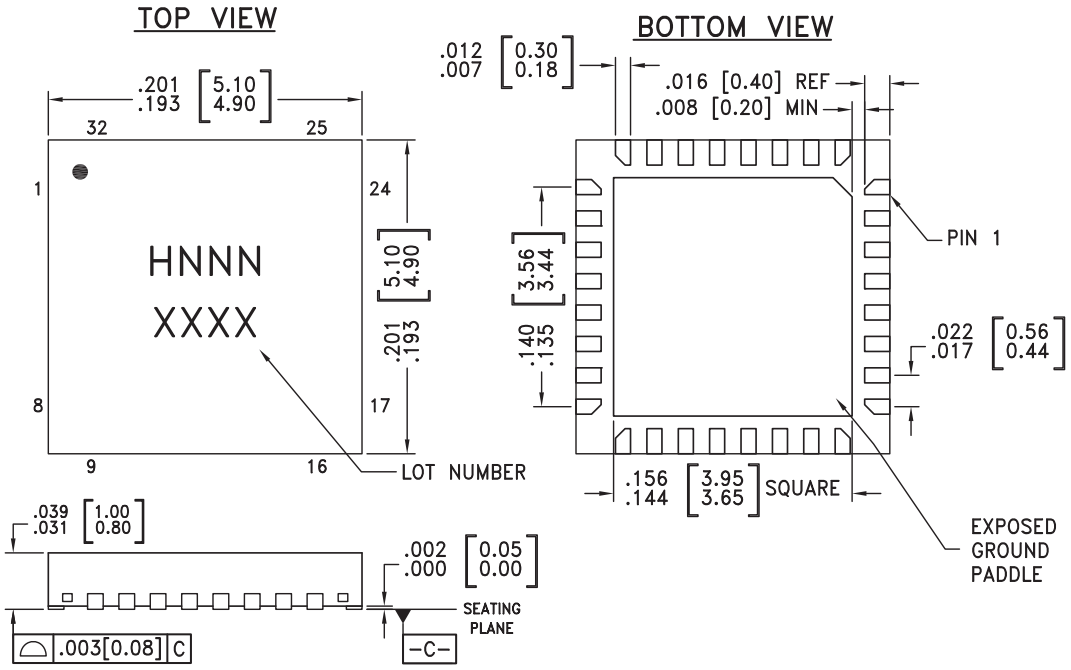


Absolute Maximum Ratings

Supply Voltage	5.6V
RF Input Power	20 dBm
Channel / Junction Temperature	125 °C
Continuous Pdiss (T = 85°C) (Derate 50 mW/°C above 85°C)	2 Watts
Thermal Resistance (R_{th}) (junction to ground paddle)	20 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

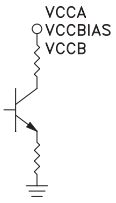
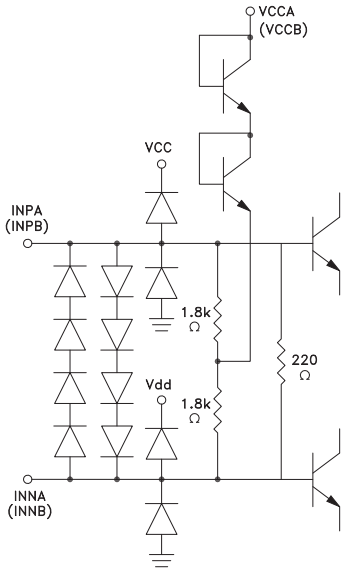
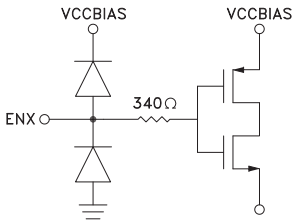
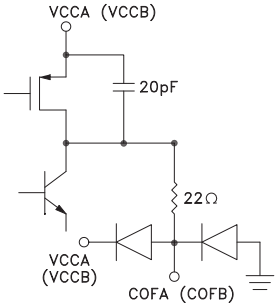
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HMC APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

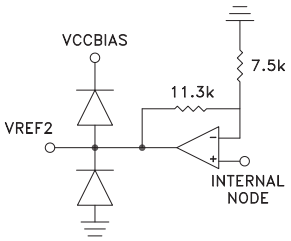
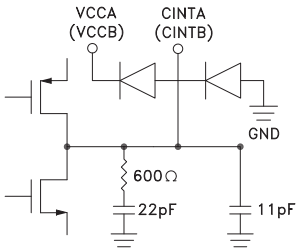
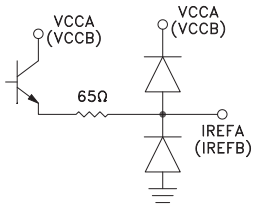
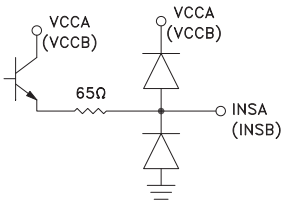
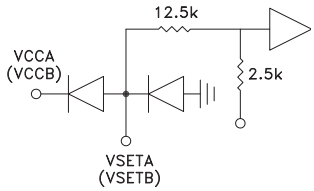
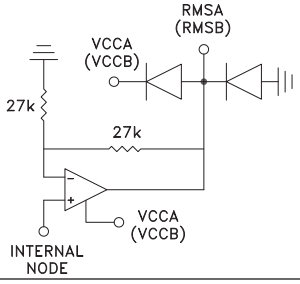
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC714LP5	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H714 XXXX
HMC714LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H714 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

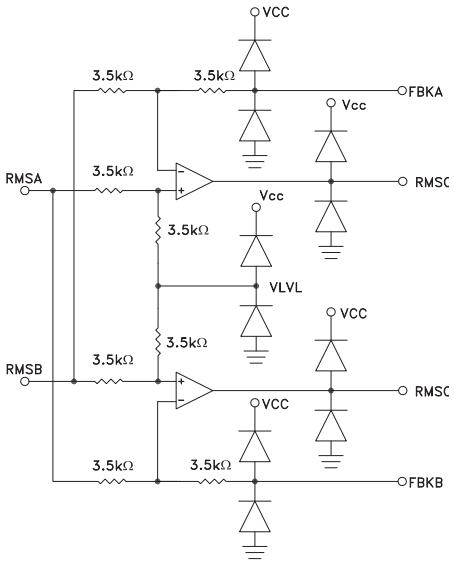
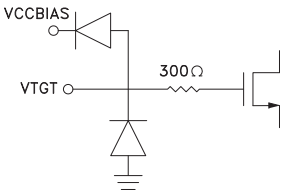
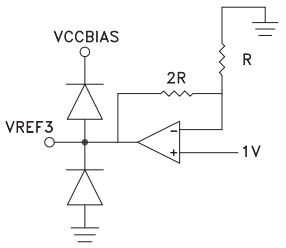
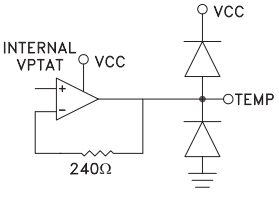
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 5, 8	VCCA, VCCBIAS, VCCB	Bias Supply. Connect supply voltage to these pins with appropriate filtering.	
	GND	Package bottom has an exposed metal paddle that must be connected to RF/DC ground.	
2, 3	INPA, INNA	Channel A RF Inputs, Connect RF to INNA through a 1:1 balun for differential configuration.	
6, 7	INNB, INPB	Channel B RF Inputs, Connect RF to INNB through a 1:1 balun for differential configuration.	
4	ENX	Disable pin. Connect to GND for normal operation. Applying voltage V > 0.8 Vcc will initiate power saving mode.	
9, 32	COFB, COFA	Input high pass filter capacitor. Connect to common via a capacitor to determine 3 dB point of input signal high-pass filter. See Application Note section.	
10, 11	N/C	These pins are not connected internally.	

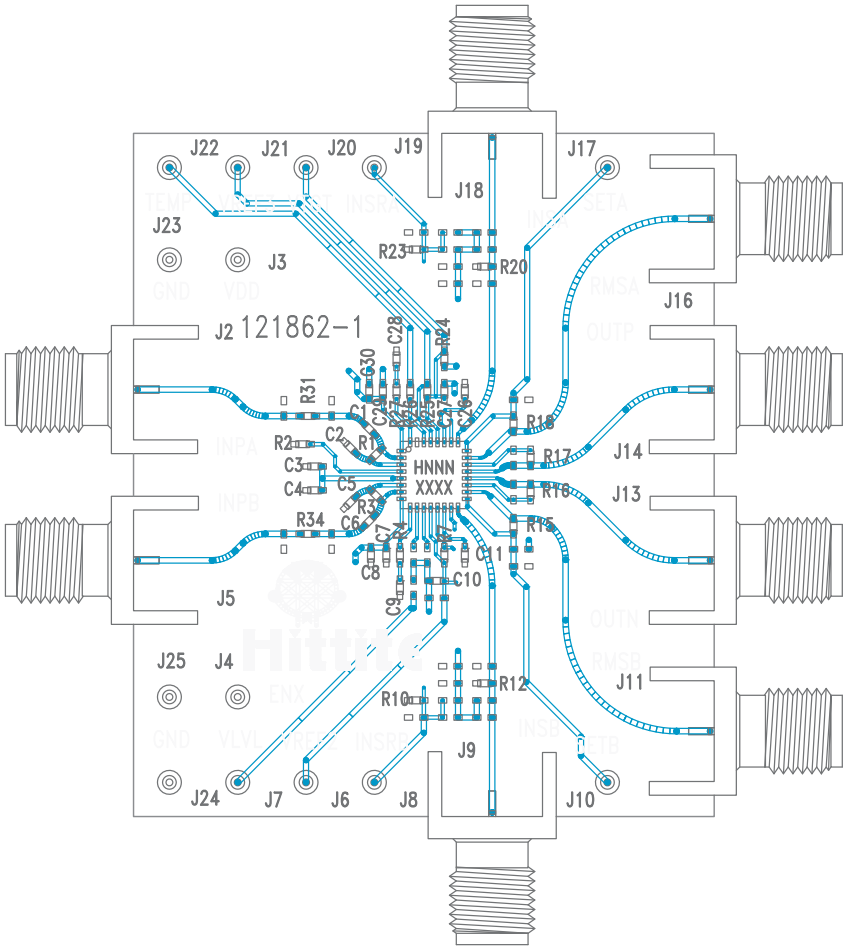
Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
12	VREF2	2.5V Reference voltage output.	
13	VLVL	Reference level input for OUTP and OUTN. Connect to VREF for normal operation.	
14, 27	CINTB, CINTA	Connection for ground referenced loop filter integration capacitor for channels A and B. See application schematic.	
15, 26	IREFB, IREFA	Reference DC Voltage for INSB - INSA to replicate voltage at no input modulation case.	
16, 25	INSB, INSA	Instantaneous Power Output for channels A and B continuous tracking of Input Power Envelope.	
17, 26	VSETB, VSETA	VSET inputs. Set point inputs for controller mode.	
18, 23	RMSB, RMSA	Logarithmic outputs that convert the input power to a DC level for channel A and channel B.	

Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
19	FBKB	Feedback through 3.5K Ohms to the negative terminal of the integrated Op Amp driving OUTN	
20	OUTN	Output providing the difference of RMS outputs using an Op Amp. For normal operation, connected to FBKB to provide the function: OUTN = RMSB - RMSA + VLVL	
21	OUTP	Output providing the difference of RMS outputs using an Op Amp. For normal operation, connected to FBKA to provide the function: OUTP = RMSA - RMSB + VLVL	
22	FBKA	Feedback through 3.5K Ohms to the negative terminal of the integrated Op Amp driving OUTP	
28	VTGT	This voltage input changes the logarithmic intercept point. Use of lower target voltage reduces error for complex signals with large crest factors. Normally connected to VREF3 via resistor voltage divider. See Application Note section.	
29	VREF3	3V Reference voltage output for use with VTGT. See Application Note section.	
30	TEMP	Temperature sensor output. See Application Note section.	

Evaluation PCB - Wideband Single-Ended



List of Materials for Evaluation PCB 121864 [1]

Item	Description
J2, J5, J9, J11, J13, J14, J16, J18	SMA Connector
J3, J4, J6 - J8, J10, J17, J19 - J25	DC Pin
C1, C2, C5, C6, C9, C28	1 nF Capacitor, 0402 Pkg.
C3, C8, C10, C29	100 pF Capacitor, 0402 Pkg.
C4, C7, C11, C26, C27, C30	100 nF Capacitor, 0402 Pkg.
R1, R3	68 Ohm Resistor, 0402 Pkg.
R2	10K Ohm Resistor, 0402 Pkg.
R4, R7, R15 - R18, R27, R31, R34	0 Ohm Resistor, 0402 Pkg.
R10, R12, R20, R23	3.92K Ohm Resistor, 0402 Pkg.
R24	61.9K Ohm Resistor, 0402 Pkg.
R25	33K Ohm Resistor, 0402 Pkg.
R26	1K Ohm Resistor, 0402 Pkg.

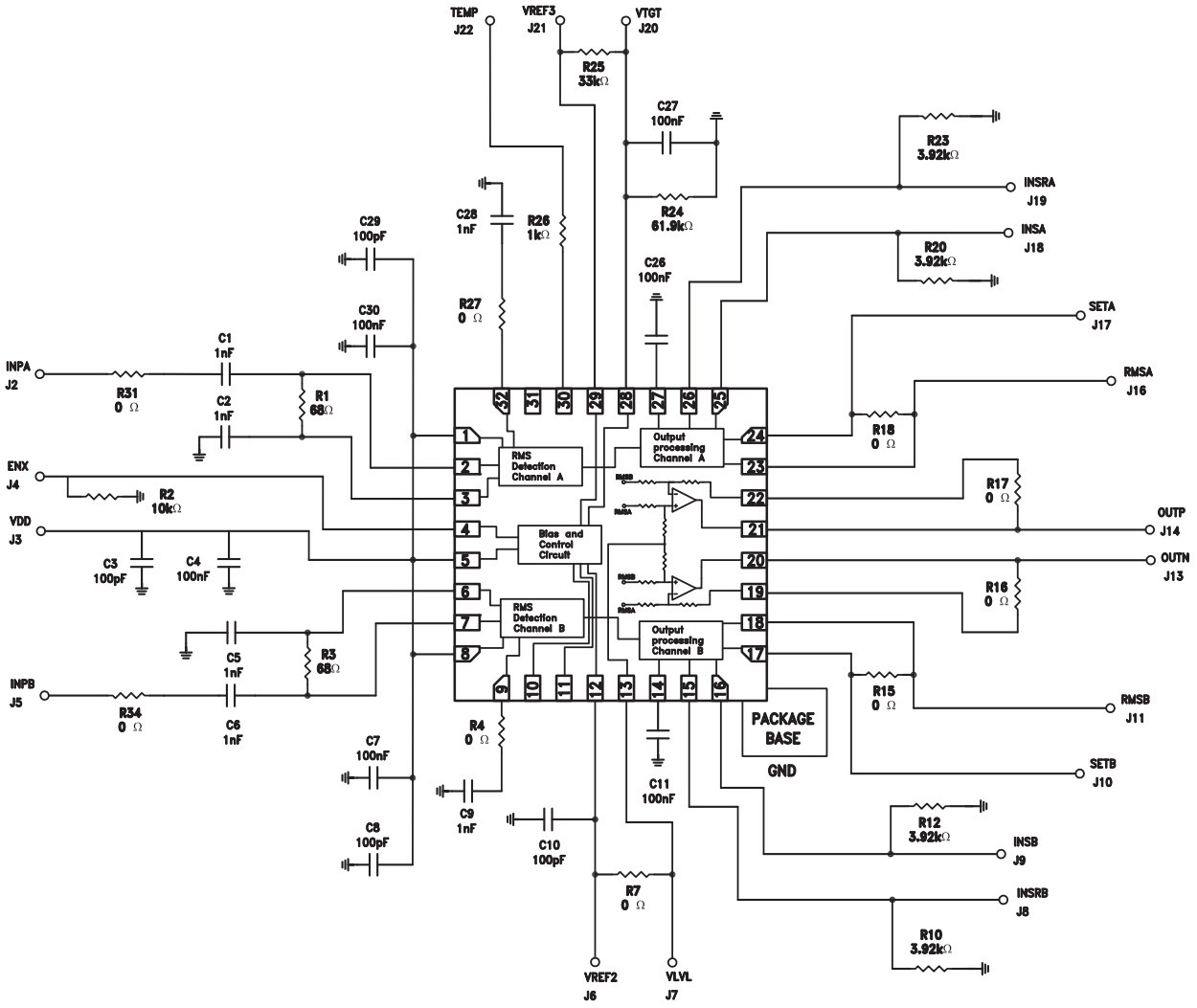
Item	Description
U1	HMC714LP5(E) Single-Ended Dual RMS Power Detector
PCB [2]	121862 Evaluation PCB

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

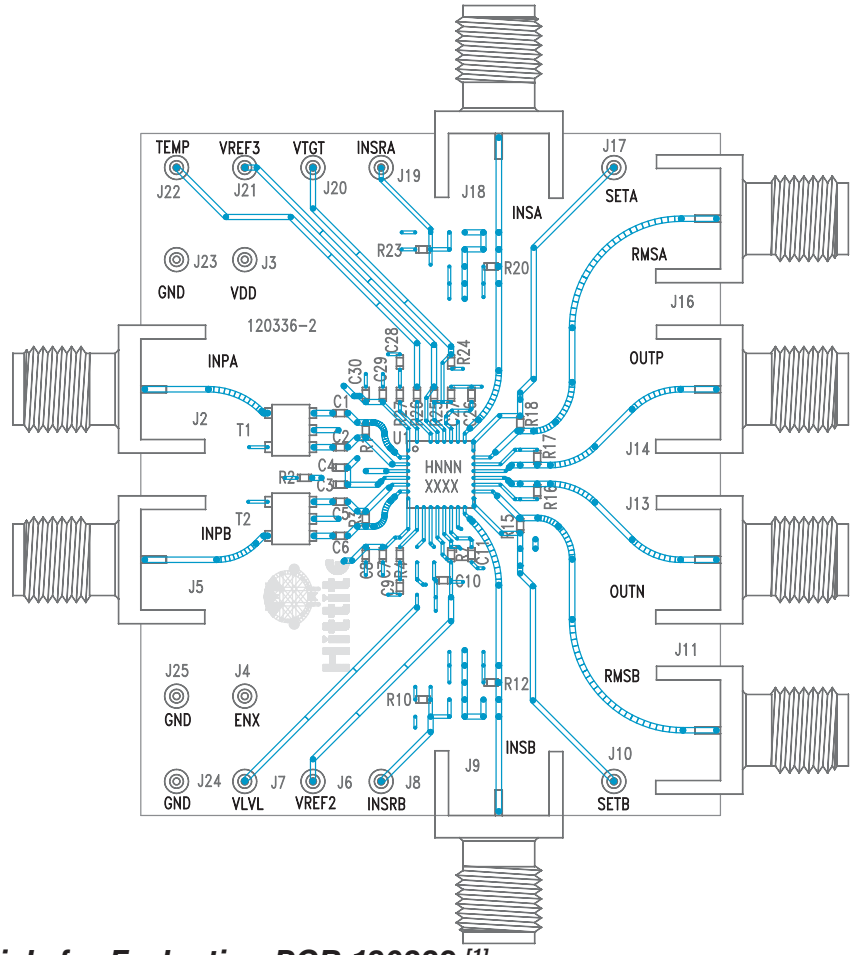
[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

Application Circuit - Wideband Single-Ended



Evaluation PCB - Differential



List of Materials for Evaluation PCB 120339 [1]

Item	Description
J2, J5, J9, J11, J13, J14, J16, J18	SMA Connector
J3, J4, J6 - J8, J10, J17, J19 - J25	DC Pin
C1, C2, C5, C6, C9, C28	1 nF Capacitor, 0402 Pkg.
C3, C8, C10, C29	100 pF Capacitor, 0402 Pkg.
C4, C7, C11, C26, C27, C30	100 nF Capacitor, 0402 Pkg.
R1, R3	68.1 Ohm Resistor, 0402 Pkg.
R2	10K Ohm Resistor, 0402 Pkg.
R4, R7, R15 - R18, R27	0 Ohm Resistor, 0402 Pkg.
R10, R12, R20, R23	3.92K Ohm Resistor, 0402 Pkg.
R24	61.9K Ohm Resistor, 0402 Pkg.
R25	33K Ohm Resistor, 0402 Pkg.
R26	1K Ohm Resistor, 0402 Pkg.

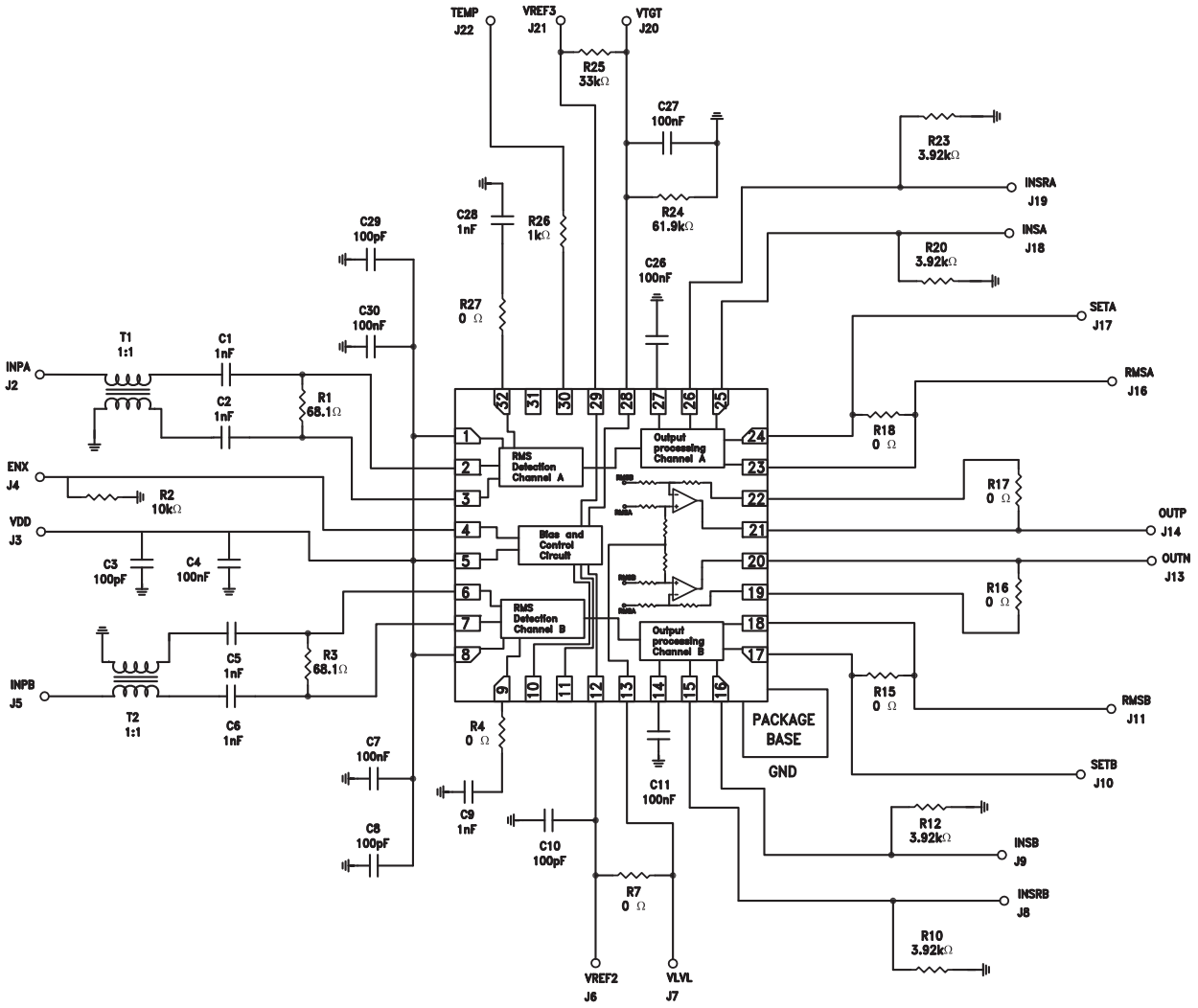
Item	Description
T1, T2	Transformer, E-Series RF 1:1,
U1	HMC714LP5(E) Differential Dual RMS Power Detector
PCB [2]	120336 Evaluation PCB

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

[1] Reference this number when ordering complete evaluation PCB

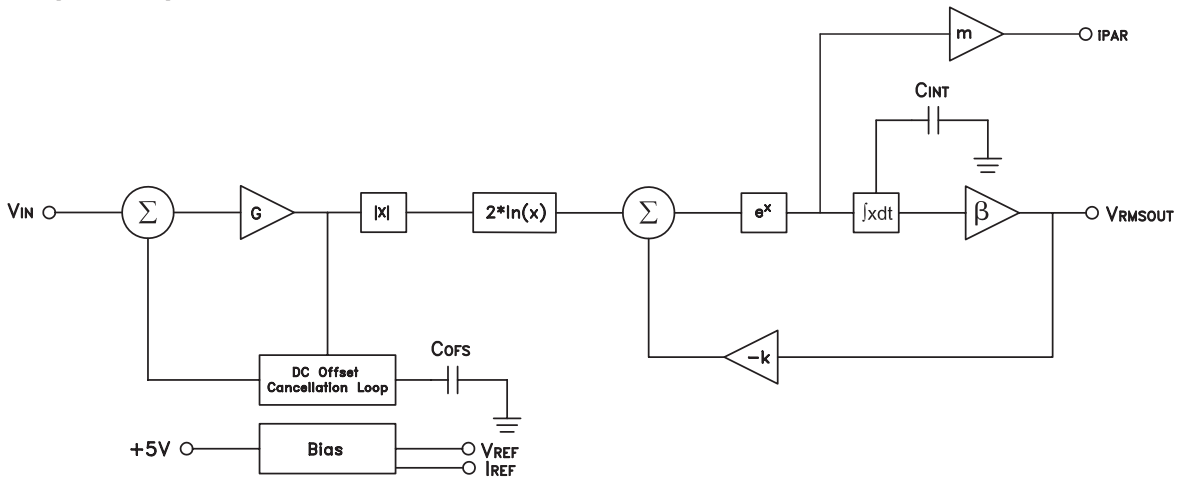
[2] Circuit Board Material: Rogers 4350

Application Circuit - Differential



Application Information

Principle of Operation



$$V_{RMSOUT} = \frac{1}{k} \ln(\beta k G^2 \int V_{IN}^2 dt)$$

$$V_{iPAR} = \frac{m}{\beta k}\left(\frac{V_{IN}^2}{\int V_{IN}^2 dt} - 1\right) + iREF$$

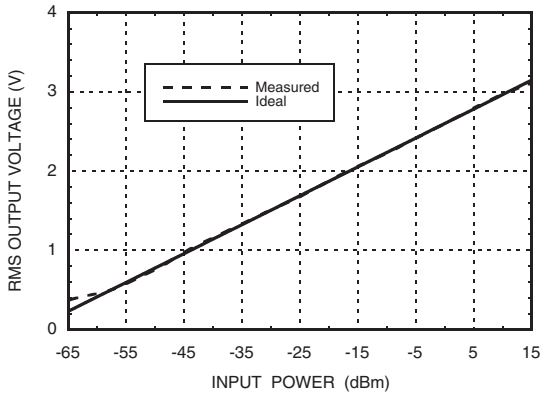
Where ß is op-amp gain set via resistors on the V_{set} pin.

$P_{in} = V_{RMS}$/[log-slope]+[log-intercept], dBm

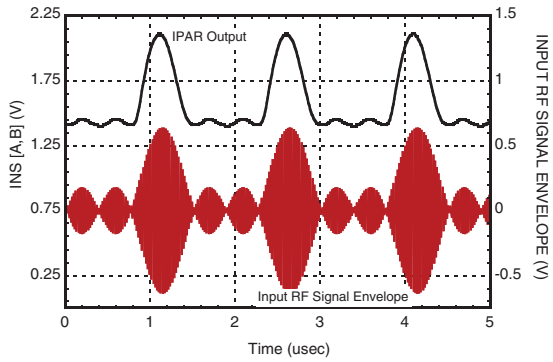
Monolithic true-RMS detectors are in-effect analog calculators, calculating the RMS value of the input signal, unlike other types of power detectors which are designed to respond to the RF signal envelope. At the core of an RMS detector is a full-wave rectifier, log/antilog circuit, and an integrator. The RMS output signal is directly proportional to the logarithm of the time-averaged $V_{IN}2$. The bias block also contains temperature compensation circuits which stabilize output accuracy over the entire operating temperature range. The DC offset cancellation circuit actively cancels internal offsets so that even very small input signals can be measure accurately.

The iPAR feature tracks the RF envelope and provides a signal which is directly proportional to signal power, normalized to average real power calculated by the RMS circuitry. Reading both the iPAR and RMS output voltage signals provides a very informative picture of the RF input signal: peak power, average power, peak-to-average power, and RF wave-shape. Simultaneous measurement of signal power and average power is essential for taking full advantage of a receive signal chain's available dynamic range, while avoiding saturation, or to maximize transmitter efficiency.

V_{RMS} vs. P_{IN}



iPAR Output & Input RF Signal Envelope vs. Time for an Input Crest Factor of 9.03 dB @ 1900 MHz [2]

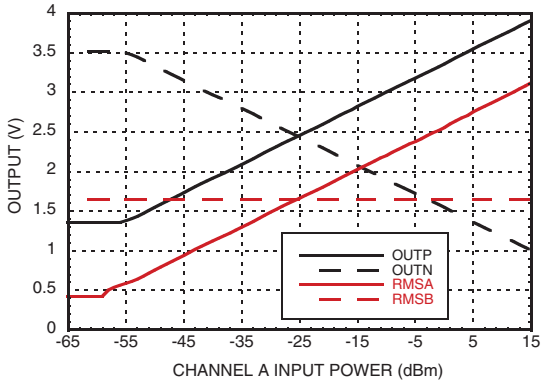


Dual RMS Detection Channels

The HMC714LP5E integrates two HMC614LP4E RMS detection channels with shared bias and control circuitry. The linear-in-dB channel outputs at the RMS_A and RMS_B pins provide RMS detection performance in terms of dynamic range, temperature stability, and logarithmic linearity similar to Hittite's HMC614LP4E with improved frequency detection range extending up to 5.8 GHz. Proprietary design techniques enable extremely good matching between channels (within less than 0.5 dB with single-ended cnfiguration) over a wide range of input frequencies with low temperature drift.

HMC714LP5E also provides "channel difference" outputs via pins OUTP and OUTN that can be either used differentially or single-ended. The V_{LVL} input is used to set the common mode reference level for those outputs. On the Hittite evaluation board, the V_{LVL} pin is shorted to V_{REF2} output to provide a nominal bias voltage of 2.5V; but any external bias voltage can be used to set V_{LVL}.

**Channel Difference Outputs @ 1900 MHz,
Channel A Power Swept,
Channel B @ -25 dBm**



A ratio of two signal powers is a simple difference in the log domain. The OUTP and OUTN outputs can provide a direct read of input signal power ratio between the signals presented to the two power detection channels.

When OUTP is connected directly to FBK_A

$OUTP = RMS_A - RMS_B + V_{LVL}$

And when OUTN is connected directly to FBK_B

$OUTN = RMS_B - RMS_A + V_{LVL}$

With the channels of HMC714LP5E having very low mismatch, channel outputs RMS_A and RMS_B track very closely over temperature. The difference operation also allows the OUTP and OUTN to reject common-mode changes in channels A and B.

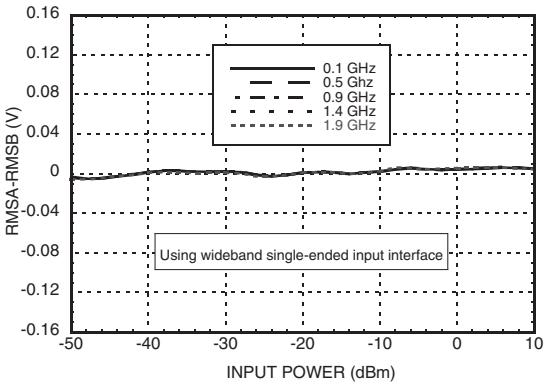
HMC714LP5E also features iPAR output on each power detector. The RMS_A and RMS_B outputs provide a read of average input signal (i.e True RMS power). The INS_A and INS_B pins are iPAR outputs providing a simultaneous read of input signal Peak Power, Peak-to-Average Ratio, and RF waveshape. Refer to the section under "iPAR – Envelope Power Normalized To Average Power" for more details on iPAR measurements.

Channel Matching

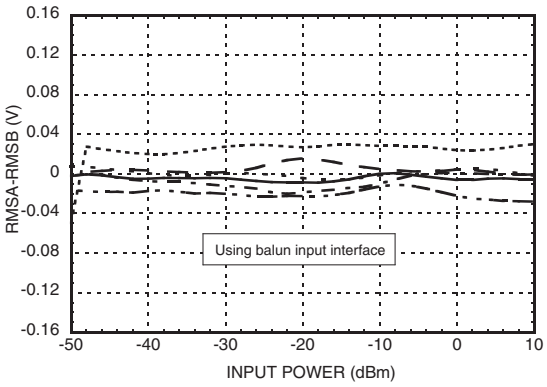
Single channel RMS detectors exhibit part-to-part variations that tend to complicate simultaneous power readings. Simultaneous signal power measurements are particularly useful for automatic gain/level control and VSWR measurements. When separate power detectors are used, the lack of an accurate match between the power detectors will produce measurement errors. Calibration and compensation methods are required to counteract the differences between the separate power detectors. The Dual RMS detector package greatly simplifies that activity, and will reliably produce more accurate measurements.

The HMC714LP5E provides industry leading channel matching performance with the use of proprietary techniques. The channel mismatch is typically less than 20 mV over the specified temperature and frequency range when the single-ended input interface is used. Hittite "differential" evaluation kits use M/A Com's ETC1-1-13 balun, which are designed to work up to 3 GHz. At frequencies lower than 3 GHz, the mismatch between the two input baluns cause a larger variation between the channels when compared to the single-ended interface (typically ±25 mV up to 900 MHz and ±50 mV up to 2700 MHz). The input impedance mismatch presented by the balun at signal frequencies beyond 3 GHz will further increase the channel-to-channel variation. The "single-ended" input interface does not have this limitation. The "single-ended" interface can utilize the full input signal bandwidth of the power detector; however the "single-ended" input interface is tuned. The differential or balun input interface is best suited to very wideband power measurements (100 MHz to 3 GHz), whereas the single-ended input interface is best suited to signal power measurement over bandwidths up to ±300 MHz (for ±1 dB error tolerance) in the hole RF frequency range.

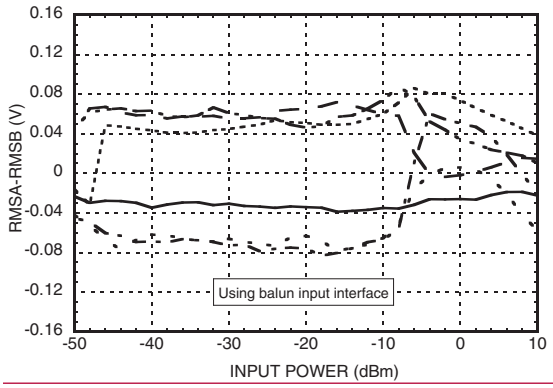
Channel Matching [RMSA-RMSB] in Wideband Single Ended Configuration



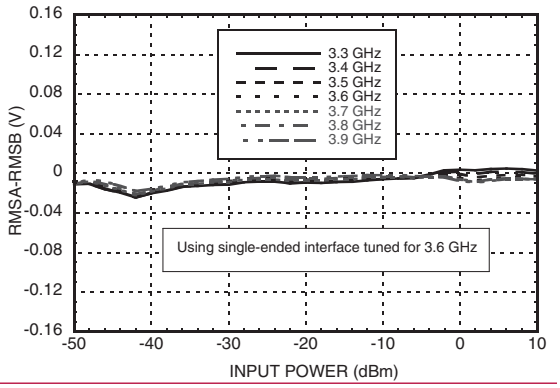
Channel Matching [RMSA-RMSB] @ 900 MHz



Channel Matching [RMSA-RMSB] @ 3.5 GHz



Channel Matching [RMSA-RMSB] in Single Ended Configuration tuned @ 3.6 GHz



Channel Isolation/Interface

Channel isolation/interference is grouped into two categories:

On-chip inter-channel interference, and

Off-chip inter-channel interference.

Off-chip interference between channels should be considered, especially at small signal levels, since HMC714LP5E is capable of detecting a signal over a very wide dynamic range (70 dB+). There are two main mechanisms through which the interference between the channels may affect measurement accuracy. The first one is the direct coupling of the RF signal from one RF channel input to the other RF channel input. Baluns on the detector inputs usually contribute to inter-channel coupling, as does PC board design and the quality of the soldered connections.

On-chip inter-channel interference, herein referred to as "input-output channel isolation", usually manifests itself as drift on one detector output due to a relatively strong signal present at the other detector input. Quantitatively, the input-output channel isolation is defined as the difference between the input power levels at both channels when the interfering (higher power level) channel causes a 1 dB measurement drift in the interfered (lower power level) channel. Worst case channel interference occurs when one channel has an input signal level just over its detection threshold.

Input-Output Channel isolation for HMC714LP5E is:

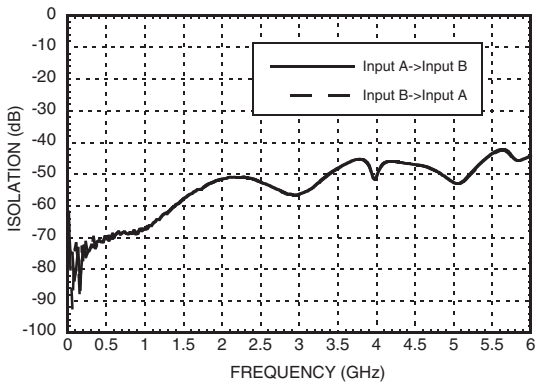
55+ dB input-output isolation at 900 MHz

45 dB input-output isolation up to 2.7 GHz

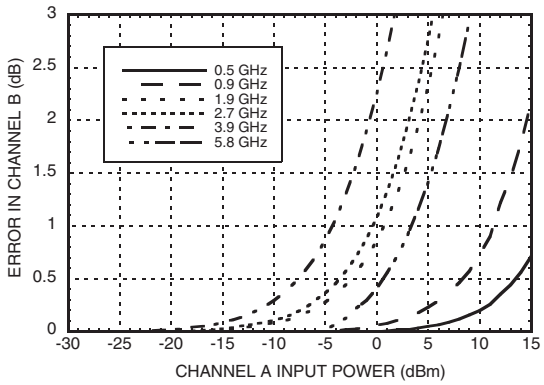
35 dB input-output isolation up to 5.8 GHz.

If the same signal frequency is injected into both channels for this Input-Output Channel Isolation measurement, the interference will manifest as a phase delay. A slight offset in signal frequency between the two channels can be seen as a ripple at the output of the channel with the lower power level applied at its input. Peaks in the output ripple correspond to the worst-case phase shift for input-output interference. The frequency of the output ripple will be equal to the "beat" frequency between the two channels. The magnitude of the output ripple will depend on the integration and offset capacitors connected to C_{INT} and C_{OFS} pins, respectively. The output ripple is reduced by increasing the value of the integration capacitance (C_{INT}), thereby decreasing the integrator bandwidth. The data was collected using a 100kHz offset between the channels.

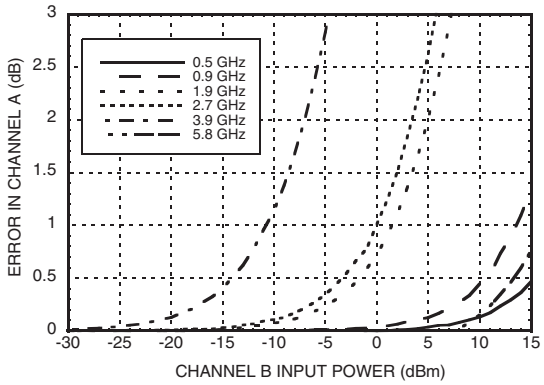
Input to Input Isolations with ETC1-1-13 Baluns



Interference to an Input Signal (INB Power Fixed) with Interfering Signal on the other Channel (INA Power Swept) [1]



Interference to an Input Signal (INA Power Fixed) with Interfering Signal on the other Channel (INB Power Swept) [1]



For price, delivery, and to place orders, please contact Hittite Microwave Corporation:
20 Alpha Road, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
Order On-line at www.hittite.com

Configuration for the Typical Application

The RF inputs can be connected in either a differential or single-ended configuration: see “RF Input Interface” section for details on each input configuration. With the appropriate input tuning components, the part can provide the full performance with a single-ended input.

The RMS_A & RMS_B output signals are typically connected directly to V_{SETA} & V_{SETB} inputs, providing a Pin->V_{RMS} transfer characteristic slope of 36.5 mV/dBm at both channels; however the RMS output can be re-scaled to “magnify” a specific portion of the input sensing range, and to fully utilize the dynamic range of the RMS output. Refer to the section under the “log-slope and intercept” for details.

The INS_A & INS_B pins are the instantaneous peak-to-average ratio (iPAR) outputs; on each detector. This iPAR measurement pulls it’s signal from the internals of the RMS detector, just before the RMS calculation is processed. Each iPAR output (INS_A & INS_B) produces a voltage signal which provides a direct read of the RF signal AM envelope. So between the simultaneous measurement of RMS power and iPAR on each power detector, a system can monitor average power, peak power, peak-to-average power, and the RF waveshape. See the section under “iPAR Envelope Power Normalized to Average Power” for application details.

V_{TGT} with a nominal value of 2V is typically generated from the V_{REF} reference output of 3V; however the V_{TGT} voltage can be adjusted to optimize measurement accuracy, especially when measurement at higher crest factors is important: see “Adjusting V_{TGT} for greater precision” section for technical details.

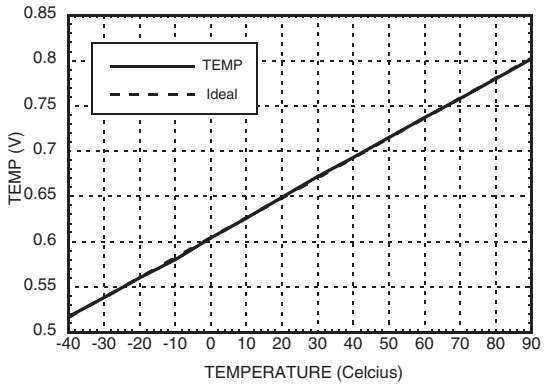
Due to part-to-part variations in log-slope and log-intercept, a system-level calibration is recommended to satisfy absolute accuracy requirements: refer to the “System Calibration” section for more details.

The HMC714LP5E requires a single 5V supply connected to three pins: V_{CCA}, V_{CCB}, and V_{CCBIAS}. Adequate power supply decoupling is required on these pins. The supply pins should be decoupled to ground using two parallel capacitors with the values shown in the application schematic. The capacitors should be placed close to the part (with the smaller value as close as possible to the supply pin) and must provide a low impedance path to RF GND over the entire input frequency range.

Temperature Sensor Interface

The HMC714LP5E provides a buffered PTAT temperature sensor output that provides a temperature scaling factor of 2.2 mV/°C with a typical output voltage of 600 mV at 0°C. The output is capable of sourcing 1.5 mA.

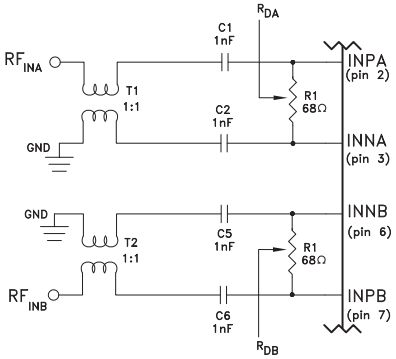
TEMP Output



RF Input Interface

The INP_A and INN_A pins are differential inputs on one of two power detectors, which we will refer to as channel A. INP_B and INN_B pins are differential inputs on the other power detector, channel B. The inputs for both channels can be externally configured with differential or single-ended input. Power match components are placed on these input terminals, along with DC blocking capacitors. The coupling capacitor values also set the lower spectral boundary of the input signal bandwidth. The inputs can be reactively matched (refer to input return loss graphs), but a resistor network should be sufficient for good wideband performance.

Differential Input Interface:

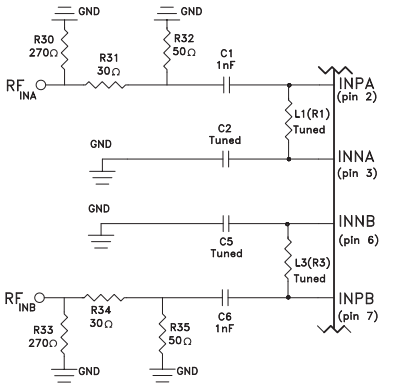


The value of RD (=RDA=RDB) depends on the balun used; if the balun is 50Ω on both sides of the SE-Diff conversion,

then $R_D = \frac{220 * R_M}{220 - R_M}$ where

R_M = the desired power match impedance in ohms.

For R_M = 50Ω, RD = 67Ω ≈ 68Ω



Single-Ended Input Interface:

Tuned SE-interface: for signal frequencies > 900MHz

Choose L and C elements from the following graph for narrowband tuning of the SE-interface:

R31/34 = 30Ω, R32/35 = 50Ω, C1/6 =1 nF
R30/33 = 270Ω,

Wideband SE-interface: for signal frequencies < 900 MHz

R31/34 = 0Ω, R32/35 = OPEN, R1/R3 = 68Ω,
R30/33 = Open

C2, C5 is 1 nF decoupling caps.

For wideband (un-tuned) input interfaces, choose the input decoupling capacitor values by first determining the lowest spectral component the power detector is required to sense, f_L.

Input decoupling capacitor value

$$\approx \frac{1}{p \times f_L \times 3.2}$$

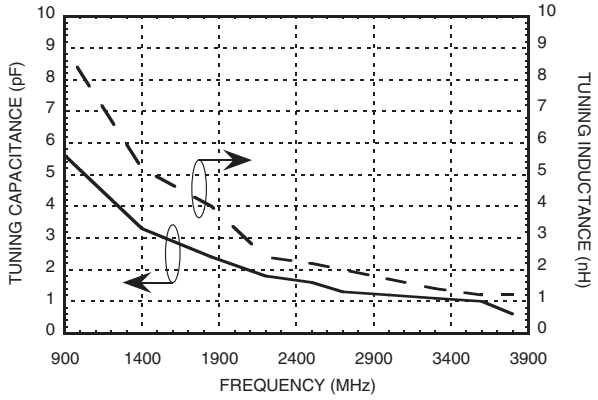
farads, where f_L is in Hertz.

Ex. If the power detector needs to sense down to 10 MHz, the decoupling capacitor value should be 1/(π*10E6*3.2) = 10 nF

A DC bias (Vcc-1.5V) is present on the INP[A,B] and IN[A,B] pins, and should not be overridden.

RF Input Interface *(Continued)*

Tuning, Single Ended Interface: fc ± 300 MHz



RMS Output Interface and Transient Response

Output transient response is determined by the integration capacitances C_{INTA} & C_{INTB} and output load conditions. Using larger values of C_{INT} will narrow the operating bandwidth of the integrator, resulting in a longer averaging time-interval and a more filtered output signal; however it will also slow the power detector's transient response. A larger C_{INT} value favors output accuracy over speed. For the fastest possible transient settling times, leave the C_{INT} pins free of any external capacitance. This configuration will operate the integrator at its widest possible bandwidth, resulting in short averaging time-interval and an output signal with little filtering. Most applications will choose to have some external integration capacitance, maintaining a balance between speed and accuracy. Furthermore, error performance over crest factor is degraded when C_{INT} is very small (for C_{INT} < 100 pF).

Modulation and deviation results in Electrical Specification Table 2 are provided with CINT = 0.1 uF.

Start by selecting C_{INT} using the following expression, and then adjust the value as needed, based on the application's preference for faster transient settling or output accuracy.

$C_{INT} = 1500\ uF/(2*\pi*f_{lam})$, in Farads, where f_{lam} = lowest amplitude-modulation component frequency in Hertz

Example: when f_{lam} = 10 kHz, C_{INT} = 1500 µF/(2*π*1000) = 24E-9 Farads ~ 22 nF

Table: Transient response vs. C_{INT} capacitance: with C_{OFS} = 0

C_{INT}	RMS Rise - Time over Dynamic Range Pin = 0 dBm	RMS Fall - Time		
		Pin = -30 dBm	Pin = -10 dBm	Pin = 0 dBm
0	35 nsec	120 nsec	200 nsec	1.18 usec
100 pF	80 nsec	410 nsec	720 nsec	1.26 usec
1 nF	780 nsec	3.3 usec	5.6 usec	7 usec
10 nF	7.8 usec	32.4 usec	54 usec	66.4 usec

Input signal is 1900 MHz CW-tone switched on and off

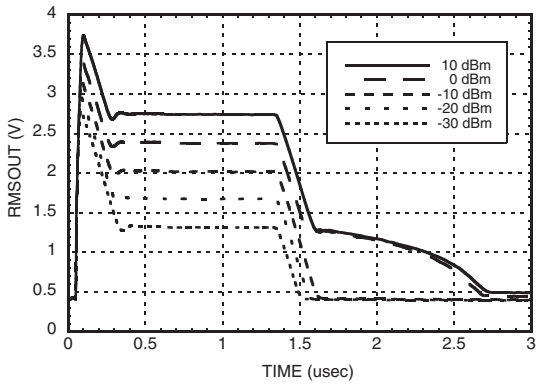
RMS is loaded with 1kΩ, 4 pF, and V_{TGT} = 2V,

RMS Output Interface and Transient Response *(Continued)*

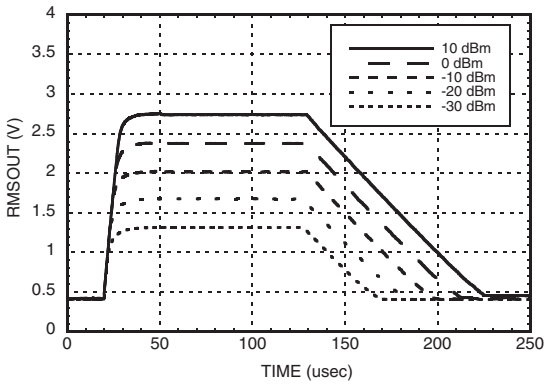
Transient response can also be slewed by the RMS output if it is excessively loaded: keep load resistance above 375Ω. An optimal load resistance of approximately 500Ω to 1kΩ will allow the output to move as quickly as it is able. For increased load drive capability, consider a buffer amplifier on the RMS output.

Using an integrating amplifier on the RMS output allows for an alternative treatment for faster settling times. An external amplifier optimized for transient settling can also provide additional RMS filtering, when operating HMC714LP5E with a lower C_{INT} capacitance value.

Rise/Fall Characteristics, CINT = 0 pF



Rise/Fall Characteristics, CINT = 10 nF

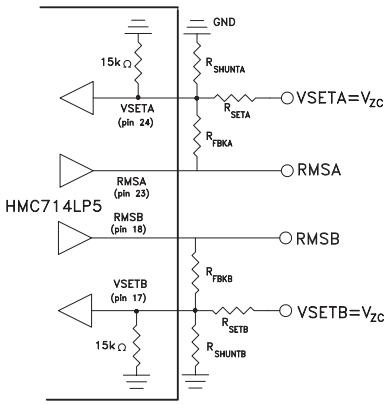


LOG-Slope and Intercept

The HMC714LP5E provides for an adjustment of output scale by controlling the fraction of RMS_A/RMS_B that is fed-back to the setpoint interface at the V_{SETA}/V_{SETB} pins. Log-slope and intercept can be adjusted to "magnify" a specific portion of the input sensing range, and to fully utilize the dynamic range of the RMS output.

A log-slope of 36.5 mV/dBm is set by connecting the RMS_A/RMS_B outputs directly to V_{SETA}/V_{SETB} pins using 0Ω resistors $RFBK_A$ and $RFBK_B$. The log-slope is adjusted by using the appropriate resistors $RFBK_A$, $RFBK_B$, $RSHUNT_A$, $RSHUNT_B$ on the RMS_A/RMS_B and V_{SETA}/V_{SETB} pins. Log-intercept is adjusted by applying a DC voltage to the V_{SETA}/V_{SETB} pins through resistors R_{SETA} and R_{SETB} .

Due to the 15 kΩ input resistance at the V_{SETA}/V_{SETB} pins, moderately low resistance values should be used to minimize the scaling errors. Very low resistor values will reduce the load driving capabilities of RMS_A/RMS_B outputs while larger values will result in scaling errors and increase of the temperature errors because of the mismatch of the on-chip and external resistor temperature coefficients.



Optimized slope = ß * log slope

Optimized intercept = log intercept - (R_{FBK} / R_{SET}) * Vzc

$$ß = \frac{R_{FBK}}{R_{FBK} // R_{SHUNT} // R_{SET}}$$

When R_{FBK} = 0 Ohm to set RMS = V_{SET}, then ß = 1

Note: Avoid excessive loading of the RMS output; keep C_{LOAD} < 35 pF, and R_{LOAD} > 375Ω

For price, delivery, and to place orders, please contact Hittite Microwave Corporation:
20 Alpha Road, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
Order On-line at www.hittite.com

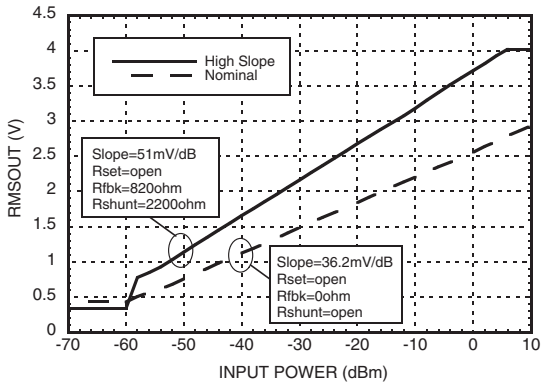
LOG-Slope and Intercept *(Continued)*

Example: The logarithmic slope can be simply increased by choosing appropriate RFBK and RSHUNT values while not populating the R_{SET} resistor on the evaluation board to keep the intercept at nominal value. Setting RFBK = 820Ω and RSHUNT = 2200Ω results in an optimized slope of:

Optimized Slope = ß * log_slope = 1.42 * 36.5 mV / dB

Optimized Slope = 52 mV / dB

Slope Adjustment



Example: The logarithmic intercept can also be adjusted by choosing appropriate R_{FBK}, R_{SHUNT}, and R_{SET} values while keeping the logarithmic slope at about 50mV/dB. Setting R_{FBK} = 820 Ohm and R_{SHUNT} = R_{SET} = 4700Ω results in an optimized slope of:

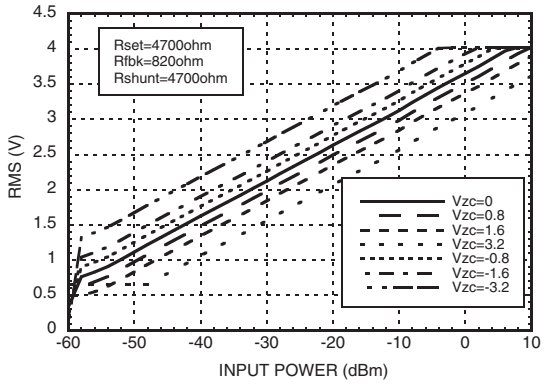
Optimized Slope = ß * log_slope = 1.4 * 36.5 mV / dB

Optimized Slope = 51 mV / dB

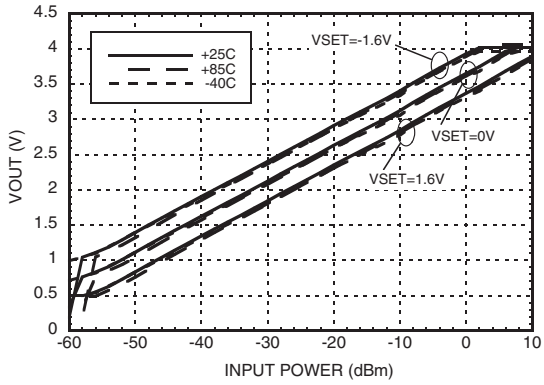
Optimized Intercept = log_intercept - $\frac{R_{FBK} * V_{ZC}}{R_{SET}}$

Optimized Intercept = log_intercept - 0.174 * V_{ZC}

Intercept Adjustment



Intercept Adjustment (with Temp)



iPAR – Envelope Power Normalized To Average Power

The INSA and INSB are envelope detector outputs for A & B channels that provide a measurement of instantaneous signal power *normalized* average power. This feature is called Instantaneous Peak to Average Ratio **(iPAR)**. The iPAR makes peak-to-average power comparisons immediately obvious. This simultaneous measurement of envelope power and average power in HMC714LP5E has two fundamental advantages over traditional methods of which employ two different power detectors working in parallel.

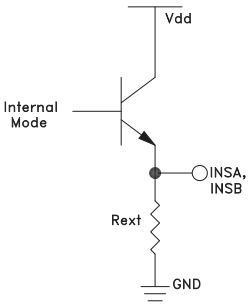
- Both the iPAR and RMS detectors share the same measurement structures, and
- Both the iPAR and RMS detectors share the same temperature compensation mechanisms.

With traditional implementation of peak-to-average power detection, the dominant source of errors is due to the uncorrelated measurement deviations between the two separate detectors. Both detectors in the HMC714LP5E share the same circuits (INS_A-RMS_A pair and INS_B-RMS_B pair), so any deviations, however small, are *fully* correlated.

The iPAR feature can be configured to provide two major functions:

1. A measurement of instantaneous signal power normalized to average power

In this most basic measurement mode, INS_A (INS_B) output is terminated to ground using an external resistor which forms an output buffer with the internal transistor Q1 connected in emitter-follower configuration. With Rext = 3.9 kOhm (R20 and R12 on the evaluation board for A & B channels), INS_A (INS_B) output can track the input envelope up to a modulation bandwidth of 35 MHz at which point the output swing drops by 50%. For an unmodulated input signal with f>>35 MHz, the INS_A (INS_B) output will provide a constant value of approximately 1.6V indicating that the instantaneous power is equal to the average power.



The INS_A (INS_B) output voltages linearly follow the instantaneous power levels at the detector input with the transfer gain scaled by an external voltage applied to V_{TGT} (pin 28). For a nominal voltage of 2V on V_{TGT} the scaling factor of the INS_A (INS_B) output is 200 mV.

$$\mathbf{INS_{[A,B]} = IREF_{[A,B]} + SF*(EAR_{[A,B]} - 1)}$$

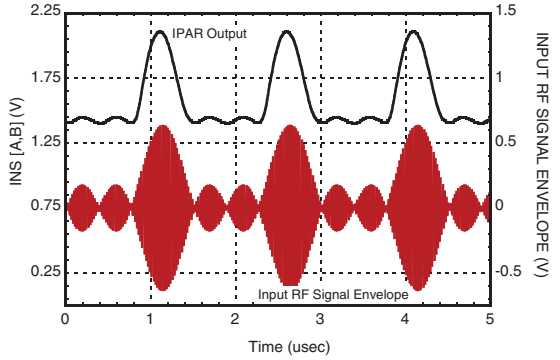
where $IREF_{[A,B]} = (VCC_{[A,B]}*R_{EXT}) /(3*(R_{EXT}+65\ Ohm)) \approx 1.6$ V (for VCC = 5V, R_{EXT} = 2 kΩ)

where $EAR_{[A,B]}$ = input signal RF AM envelope-to-average power ratio on channel [A,B]

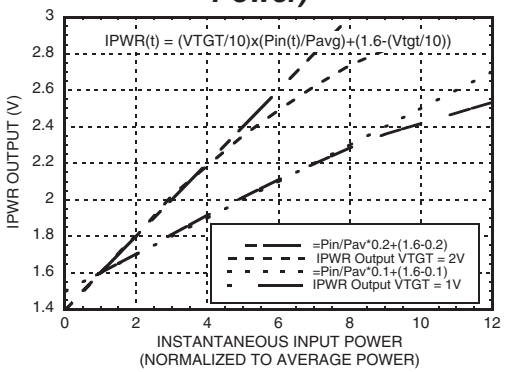
and SF = the scaling factor set by an external voltage applied to V_{TGT} (200 mV when V_{TGT} = 2.0V)

For example, the INS_A (INS_B) voltage will drop to 1.4 V (1.6-0.2V) when the input power instantaneously drops to zero, and will increase to 2.2V (1.6+0.2*3) when the input power instantaneously increases to 4 times the average power. With lower V_{TGT} values the scaling factor also decreases, allowing INS_A (INS_B) to linearly track larger swings of input power.

iPAR Output & Input RF Signal Envelope vs. Time for an Input Crest Factor of 9.03 dB @ 1900 MHz [2]



INS [A,B] Output vs. Instantaneous Input Power (Normalized to Average Power)

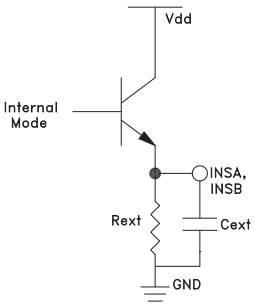


PAR – Envelope Power Normalized To Average Power (Continued)

The INS_A (INS_B) output is highly independent from input signal frequency, input average power, and temperature. Proprietary design techniques assure very little part-to-part variation and maintain a very high degree of match between channels.

2. A measurement of peak-power normalized to average power

To measure peak power, a peak-hold mechanism is required at the INS_A (INS_B) output. The peak-hold circuit can be as simple as an RC combination on the INS_A (INS_B) pin. In this configuration, peak excursions of the input signal is stored as a peak voltage on the external Cext capacitor. Rext is used to set the quiescent bias point of Q1, and together with Cext will for a time-constant for the peak-hold function. The larger Cext is the longer the peak-detector will "remember" the largest signal excursion; conversely a smaller value of Cext will result in a shorter memory, and less filtering. The value of Rext for this "peak-power" mode of the iPAR function should be much larger than the value used for the iPAR mode described previously (instantaneous power tracking mode) to extend the RextCext time-constant.



$$\mathbf{INS_{[A,B]} = IREF_{[A,B]} + SF*(PAR_{[A,B]} - 1)}$$

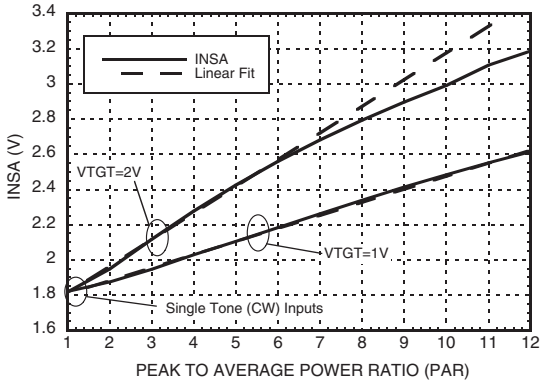
where $IREF_{[A,B]} = VCC_{[A,B]} / 3 + 0.15V \approx 1.82V$ (for VCC = 5V, R_{EXT} = 500 kΩ)

where $PAR_{[A,B]}$ = input signal peak-to-average ratio on channel [A,B]

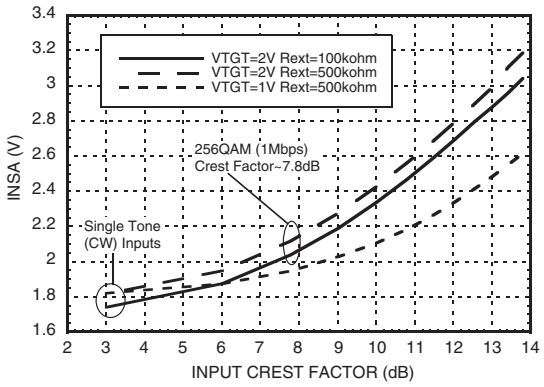
and SF = the scaling factor set by an external voltage applied to V_{TGT} (150 mV when V_{TGT} = 2.0V)

The graphs below describes the INS_A (INS_B) peak-hold levels as a function of input peak-to-average ratio (PAR) and also crest factor. Note how the voltage applied at V_{TGT} affects the INS_A (INS_B) reading. The voltage applied to the V_{TGT} pin also has a secondary effect on crest-factor performance. The V_{TGT} signal optimizes internal bias points for measurement accuracy at higher crest factors: refer to the section under "Adjusting V_{TGT} for greater precision" for a

iPAR Feature Peak-to-Average Power Detection Configuration (R_{EXT} = 500Ω, C_{EXT} = 100 nF)



iPAR Feature Peak-to-Average Power Detection Configuration vc Crest Factor (CEXT = 100 nF)



PAR – Envelope Power Normalized To Average Power *(Continued)*

full description on crest factor optimization.

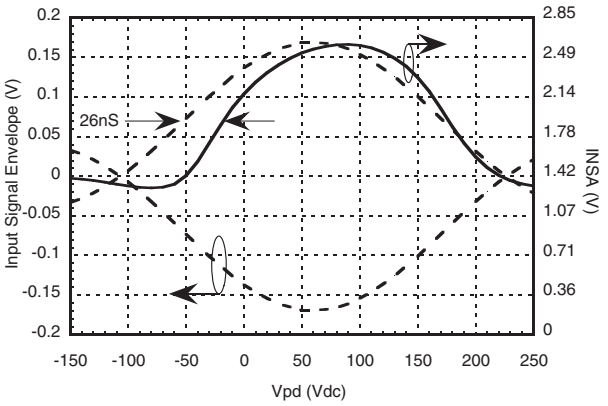
iPAR Reference Outputs: IREFA & IREFB

HMC714LP5E also provides two reference voltage outputs, $IREF_A$ (pin 26) and $IREF_B$ (pin 15) for A & B channels, which when used with the INS_A/INS_B outputs allows cancellation of temperature and supply related variations of the INS_A/INS_B DC offsets. INS_A/INS_B DC offsets are equal to the $IREF_A/IREF_B$ reference voltages, and these levels corresponds to the envelope-to-average ratio (EAR) or peak-to-average ratio (PAR) of an unmodulated carrier (CW-tone crest factor = 3 dB). For the best cancellation of the effects of temperature and supply voltage on INS_A/INS_B DC offsets, load both the INS_A/INS_B and $IREF_A/IREF_B$ outputs with an equivalent RC network.

Propagation Delay of INS_A & INS_B

The proper operation of the iPAR feature depends on the proper settling of the RMS outputs because both the iPAR feature and the RMS detection feature share the same internal structures. After internal mechanisms of the detector have settled, the RMS outputs (RMS_A & RMS_B) provide a reading of input average power while iPAR outputs (INS_A & INS_B) provides the instantaneous (or peak) power value of the input signal. There is of course some finite propagation delay from the instant of input power change to the change of INS_A (INS_B). That propagation delay is defined by the external capacitor, Cext. The figure illustrates the propagation delay from a 900 MHz, 6-tone (multi-carrier) input signal at -10 dBm average power to the INS_A output of HMC714LP5E. As illustrated, the propagation delay is 26 nsec with the detector configured with the wideband, single-ended input interface. The use of the differential input interface with the balun increases the propagation delay to 37 nsec under similar test conditions.

Propagation Delay with Wideband Single Ended Input Itnerface



Standby Mode

The ENX can be used to force the power detector into a low-power standby mode. In this mode, the entire power detector is powered-down. As ENX is deactivated, power is restored to all of the circuits. There is no memory of previous conditions. Coming-out of stand-by, C_{INT} and C_{OFS} capacitors will require recharging, so if large capacitor values have been chosen, the wake-up time will be lengthened.

DC Offset Compensation Loop

Internal DC offsets, which are input signal dependant, require continuous cancellation. Offset cancellation is a critical function needed for maintenance of measurement accuracy and sensitivity. The DC offset cancellation loop performs this function, and its response is largely defined by the capacitance off. Setting DC offset cancellation, loop bandwidth strives to strike a balance between offset cancellation accuracy, and loop response time. A larger value of C_{OFS} results in a more precise offset cancellation, but at the expense of a slower offset cancellation response. A smaller value of C_{OFS} tilts the performance trade-off towards a faster offset cancellation response. The optimal loop bandwidth setting will allow internal offsets to be cancelled at a minimally acceptable speed.

DC Offset Compensation Loop *(Continued)*

DC Offset Cancellation Loop Bandwith $\approx \frac{1}{\pi(500)(C_{OFS} + 20 \times 10^{12})}$ Hz

For example: loop bandwidth for DC cancellation with COFS = 1nF, bandwidth is ~62 kHz

Note: The measurement error produced by internal DC offsets cannot be measured repeatably at any single operating point, in terms of input signal frequency and level. Measurement error must be calculated to a best fit line, over the entire range of input signal (again, in terms of signal level and frequency).

Adjusting V_{TGT} for Greater Precision

There are two competing aspects of performance, for which V_{TGT} can be used to set a preference. Depending on which aspect of precision is more important to the application, the V_{TGT} pin can be used to find a compromise between two sources of RMS output error: internal DC offset cancellation error and deviation at high crest factors (>12dB).

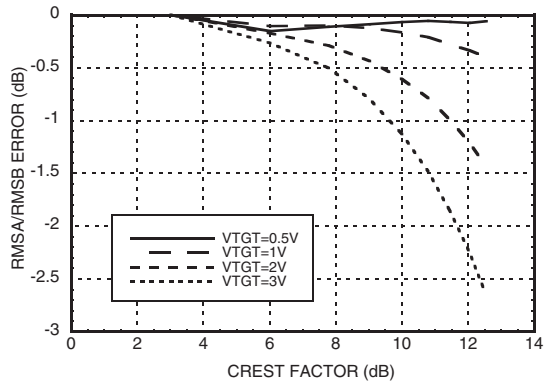
- Increasing V_{TGT} input voltage will reduce the effect of internal DC offsets, but deviation at high crest factors will increase slightly. A 50% increase in V_{TGT} should produce an 18% improvement in RMS precision due to a reduction in internal DC offsets effects.
- Decreasing V_{TGT} input voltage will reduce errors at high crest factors, but internal DC offsets will have more of an effect on measurement accuracy.

If input signal crest factor is not expected to exceed 10dB, you can improve RMS precision by increasing V_{TGT} voltage. Keep in mind that changing V_{TGT} also adjusts the log-intercept point, which shifts the “input dynamic range”. The best set-point for V_{TGT} will be the lowest voltage that still maintains the “input dynamic range” over the required range of input power. This new V_{TGT} set-point should optimize the amount of DC offset related errors.

If error performance at high crest factors requires optimization, set V_{TGT} for the *maximum tolerable error at the highest expected crest factor*. Increasing V_{TGT} beyond that point will unnecessarily compromise internal DC offset cancellation performance. After changing V_{TGT}, re-verify that the “input dynamic range” still covers the required range of input power.

V_{TGT} should be referenced to V_{REF} for best performance. It is recommended to use a temperature stable DC amplifier between V_{TGT} and V_{REF} to create $V_{TGT} > V_{REF}$. The V_{REF} pin is a temperature compensated voltage reference output, only intended for use with V_{TGT}.

RMS Output Error vs. Crest Factor



V_{TGT} influence on DC offset compensation

V_{GTG}	Error due to internal DC offsets
1.0 V	nominal + 0.2 dB
1.5 V	nominal + 0.1 dB
2.0 V	nominal
3.0 V	7.nominal + 0.06 dB
3.5 V	nominal + 0.1 dB

System Calibration

Due to part-to-part variations in log-slope and log-intercept, a system-level calibration is recommended to satisfy absolute accuracy requirements. When performing this calibration, choose at least two test points: near the top-end and bottom-end of the measurement range. It is best to measure the calibration points in the regions (of frequency and amplitude) where accuracy is most important. Derive the log-slope and log-intercept, and store them in non-volatile memory. Calibrate iPAR scaling by measuring the peak-to-average ratio of a known signal.

For example if the following two calibration points were measured at 2.35 GHz:

With Vrms = 2.34V at Pin= -7dBm,
and Vrms=1.84V at Pin= -16dBm
Slope Calibration Constant = SCC
SCC = (-16+7)/(1.84-2.34) = 18 dB/V
Intercept Calibration Constant = ICC
ICC = Pin – SCC*Vrms = -7 – 18.0 * 2.34 = -49.12dBm

Now performing a power measurement:
Vrms measures 2.13V
[Measured Pin] = [Measured Vrms]*SCC + ICC
[Measured Pin] = 2.13*18.0 – 49.12 = -10.78dBm
An error of only 0.22dB

Factory system calibration measurements should be made using an input signal representative of the application. If the power detector will operate over a wide range of frequencies, choose a central frequency for calibration.

Layout Considerations

- Mount RF input coupling capacitors close to the IN+ and IN- pins.
- Solder the heat slug on the package underside to a grounded island which can draw heat away from the die with low thermal impedance. The grounded island should be at RF ground potential.
- Connect power detector ground to the RF ground plane, and mount the supply decoupling capacitors close to the supply pins.

Definitions:

- Log-slope: slope of P_{IN} –> V_{RMS} transfer characteristic. In units of mV/dB
- Log-intercept: x-axis intercept of P_{IN} –> V_{RMS} transfer characteristic. In units of dBm.
- RMS Output Error: The difference between the measured P_{IN} and actual P_{IN} using a line of best fit.

  [measured_P_{IN}] = [measured_V_{RMS}] / [best-fit-slope] + [best-fit-intercept], dBm
- Input Dynamic Range: the range of average input power for which there is a corresponding RMS output voltage with “RMS Output Error” falling within a specific error tolerance.
- Crest Factor: Peak power to average power ratio for time-varying signals.

Notes: