HMC619LP5 / 619LP5E

v07.0908

GaAs PHEMT MMIC POWER AMPLIFIER, DC - 10 GHz

Typical Applications

The HMC619LP5(E) wideband PA is ideal for:

- Telecom Infrastructure
- Microwave Radio & VSAT
- Military & Space
- Test Instrumentation
- Fiber Optics

Features

P1dB Output Power: +27 dBm

Gain: 11 dB

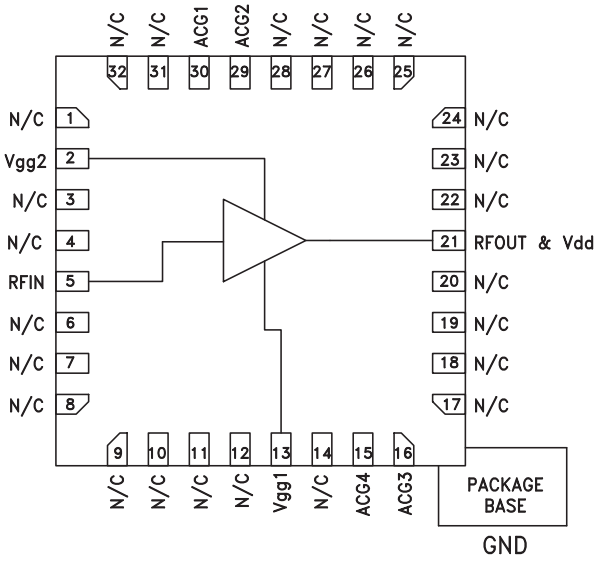
Output IP3: +37 dBm

Supply Voltage: +12V @ 300 mA

50 Ohm Matched Input/Output

32 Lead 5x5mm Lead SMT Package: $25mm^2$

Functional Diagram



General Description

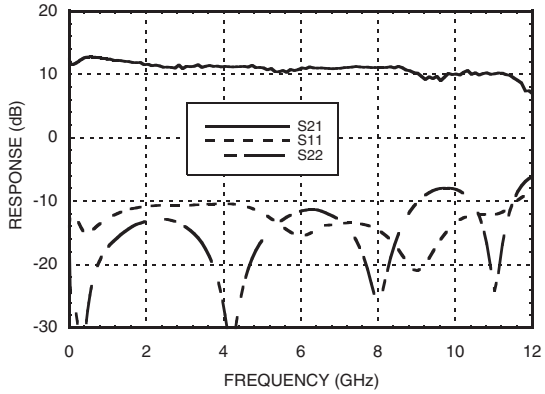
The HMC619LP5(E) is a GaAs MMIC PHEMT Distributed Power Amplifier die which operates between DC and 10 GHz. The amplifier provides 11 dB of gain, +37 dBm output IP3 and +27 dBm of output power at 1 dB gain compression while requiring 300 mA from a +12V supply. Gain flatness is excellent at ±0.5 dB from DC - 10 GHz making the HMC619LP5(E) ideal for EW, ECM, Radar and test equipment applications. The HMC619LP5(E) amplifier I/Os are internally matched to 50 ohms.

Electrical Specifications, T_A = +25° C, Vdd= +12V, Vgg2= +5V, Idd= 300 mA*

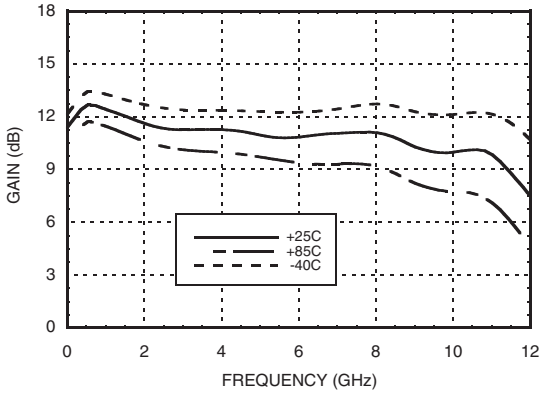
Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		DC - 2.0			2.0 - 8.0			8.0 - 10.0		GHz
Gain	10	12		9	11		8	10.5		dB
Gain Flatness		±0.5			±0.25			±0.5		dB
Gain Variation Over Temperature		0.016			0.02			0.03		dB/ °C
Input Return Loss		11			12.5			17		dB
Output Return Loss		16			16			12		dB
Output Power for 1 dB Compression (P1dB)		28		25	27		23	25		dBm
Saturated Output Power (Psat)		29			28			25.5		dBm
Output Third Order Intercept (IP3)		41			37			32		dBm
Noise Figure		5			5			7		dB
Supply Current (Idd) (Vdd= +12V, Vgg1= -0.8V Typ.)		300			300			300		mA

** Adjust Vgg1 between -2 to 0V to achieve Idd= 300 mA typical.*

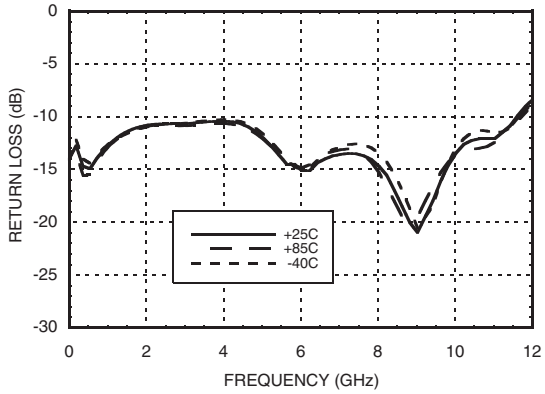
Gain & Return Loss



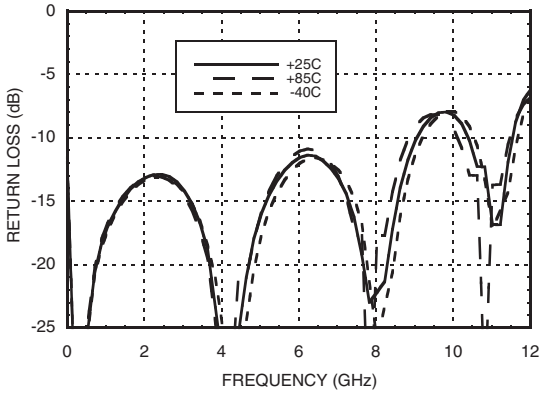
Gain vs. Temperature



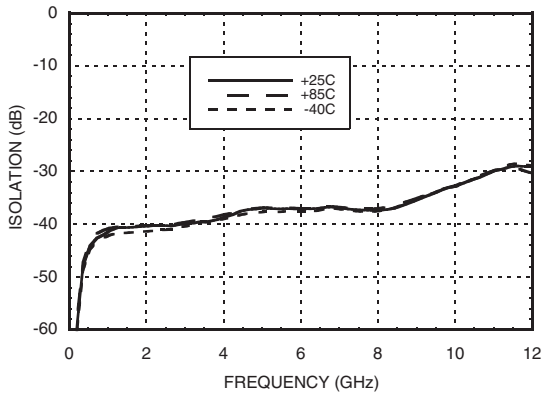
Input Return Loss vs. Temperature



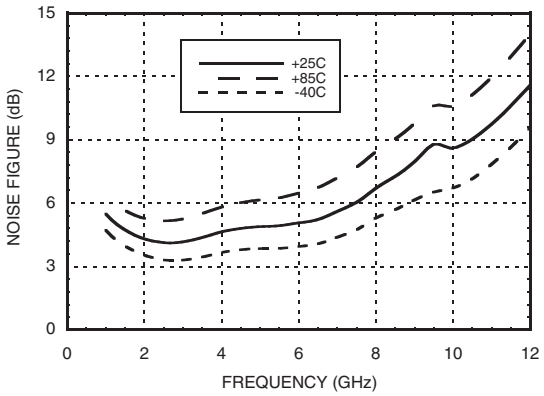
Output Return Loss vs. Temperature



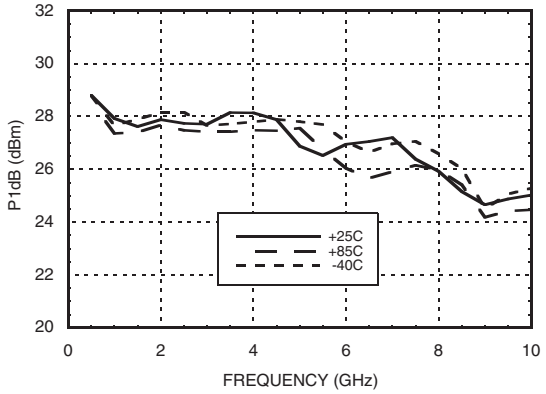
Reverse Isolation vs. Temperature



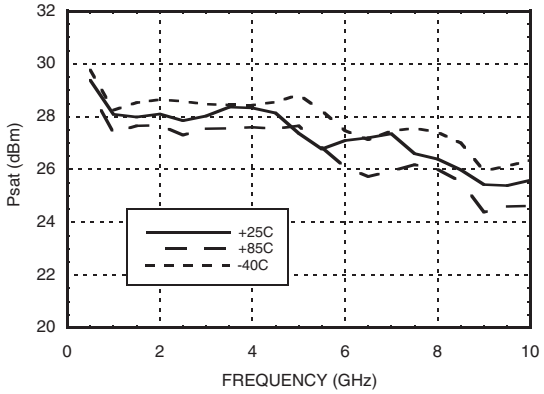
Noise Figure vs. Temperature



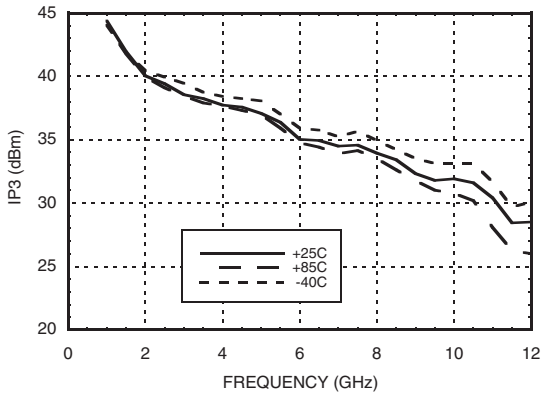
P1dB vs. Temperature



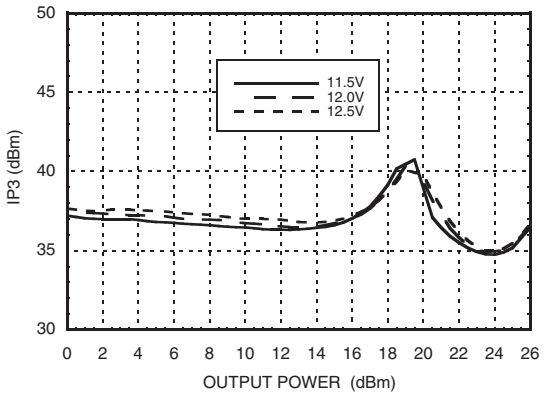
Psat vs. Temperature



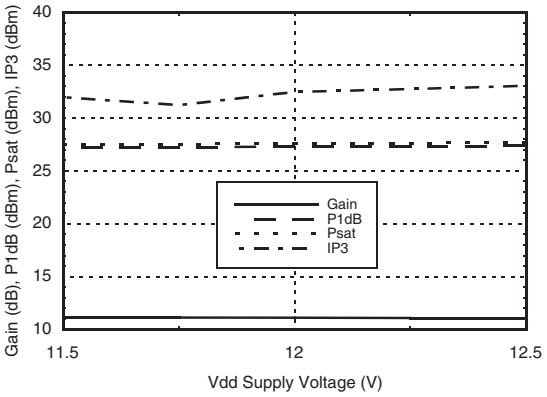
Output IP3 vs. Temperature



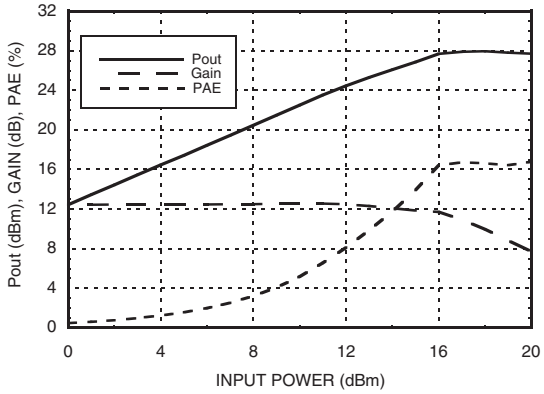
Output IP3 vs. Output Power @ 5GHz



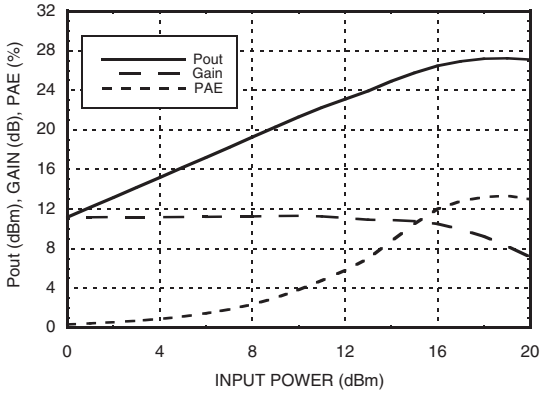
Gain, Power & Output IP3 vs. Supply Voltage @ 10 GHz, Fixed Vgg



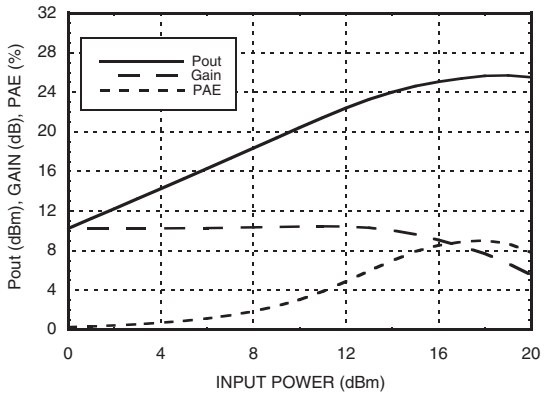
Power Compression @ 1 GHz



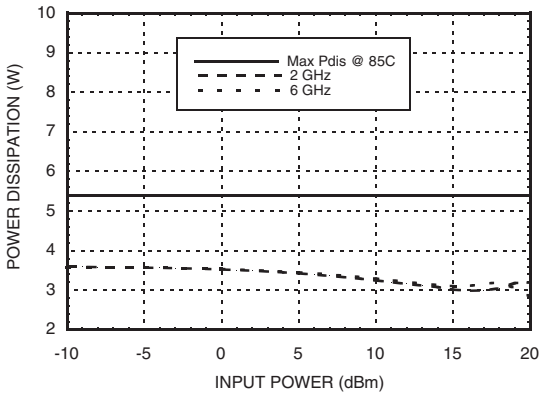
Power Compression @ 5 GHz



Power Compression @ 10 GHz



Power Dissipation



Absolute Maximum Ratings

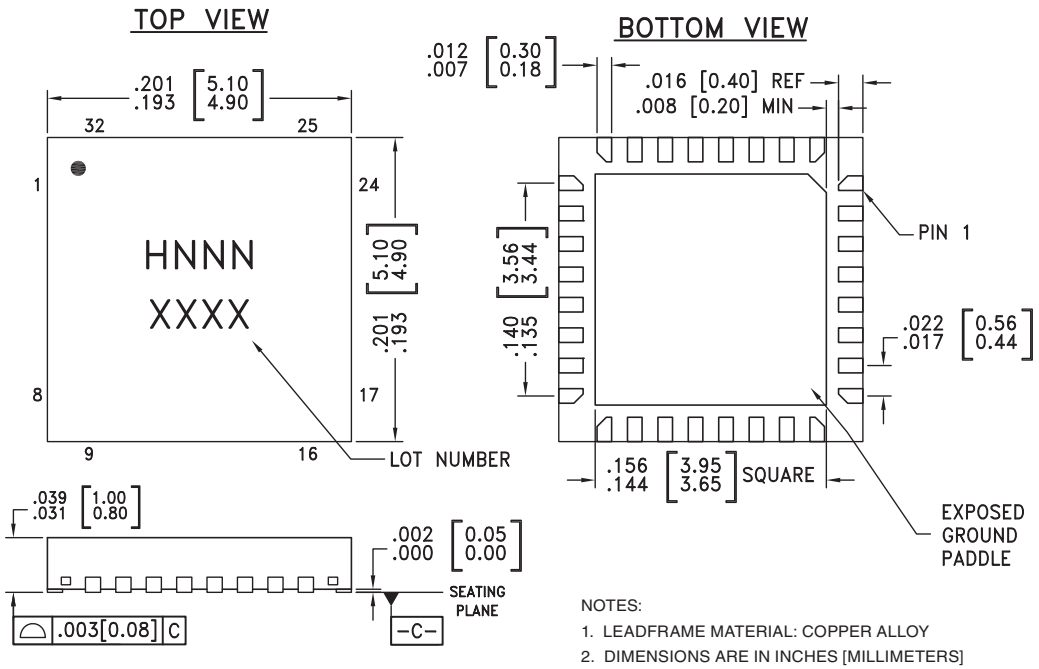
Drain Bias Voltage (Vdd)	13 Vdc
Gate Bias Voltage (Vgg1)	-2.5 to 0 Vdc
Gate Bias Voltage (Vgg2)	+4V to +6V
RF Input Power (RFIN)(Vdd = +12 Vdc)	27 dBm
Channel Temperature	150 °C
Continuous Pdiss (T= 85 °C) (derate 65 mW/°C above 85 °C)	4.2 W
Thermal Resistance (channel to package bottom)	15.3 °C/W
Storage Temperature	-65 to 150 °C
Operating Temperature	-40 to 85 °C

Typical Supply Current vs. Vdd

Vdd (V)	Idd (mA)
11.5	299
12.0	300
12.5	301

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

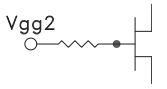
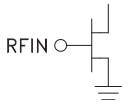
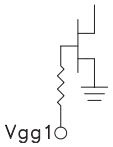
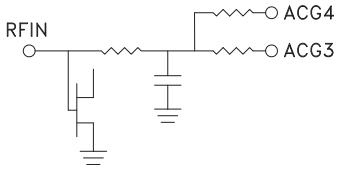
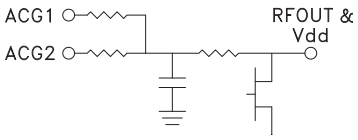
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

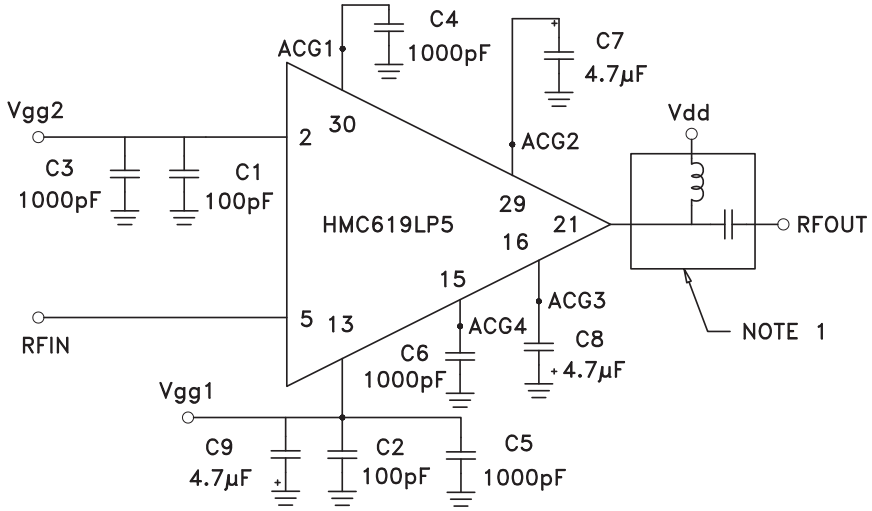
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC619LP5	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H619 XXXX
HMC619LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H619 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Descriptions

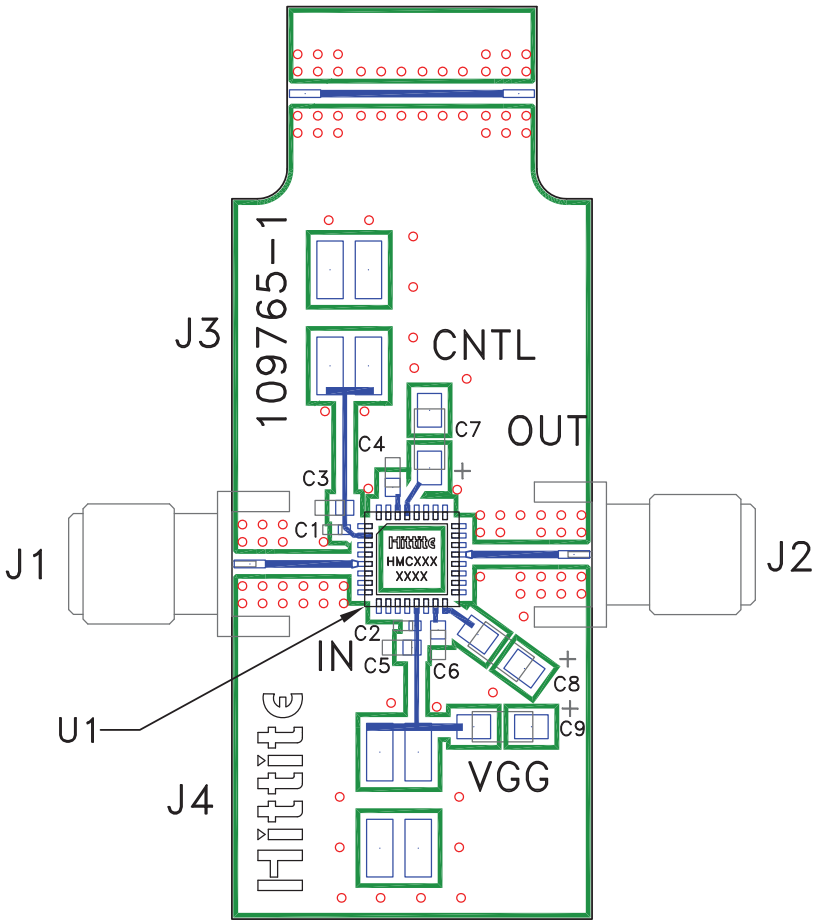
Pin Number	Function	Description	Interface Schematic
1, 3, 4, 6-12, 14, 17, 18, 19, 20, 22-28, 31, 32	N/C	No connection. These pins may be connected to RF ground. Performance will not be affected.	
2	Vgg2	Gate Control 2 for amplifier. +5V should be applied to Vgg2 for nominal operation.	
5	RFIN	This pad is DC coupled and matched to 50 Ohms.	
13	Vgg1	Gate Control 1 for amplifier.	
15	ACG4	Low frequency termination. Attach bypass capacitor per application circuit herein.	
16	ACG3		
21	RFOUT & Vdd	RF output for amplifier. Connect the DC bias (Vdd) network to provide drain current (Idd). See application circuit herein.	
29	ACG2	Low frequency termination. Attach bypass capacitor per application circuit herein.	
30	ACG1		
Ground Paddle	GND	Ground paddle must be connected to RF/DC ground.	

Application Circuit



NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee or external bias network.

Evaluation PCB



List of Materials for Evaluation PCB 108347 [1]

Item	Description
J1 - J2	SRI K Connector
J3 - J4	2mm Molex Header
C1, C2	100 pF Capacitor, 0402 Pkg.
C3 - C6	1000 pF Capacitor, 0603 Pkg.
C7 - C9	4.7 µF Capacitor, Tantalum
U1	HMC619LP5 / HMC619LP5E
PCB [2]	109765 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and package bottom should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.