# HMC467LP3 / 467LP3E

v01.0705

## 2 dB LSB GaAs MMIC 2-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, DC - 6 GHz

### Typical Applications

The HMC467LP3 / HMC467LP3E is ideal for:

- Cellular; UMTS/3G Infrastructure
- Fixed Wireless & WLL
- Microwave Radio & VSAT
- Test Equipment

### Features

2 dB LSB Steps to 6 dB

High IP3: +50 dBm

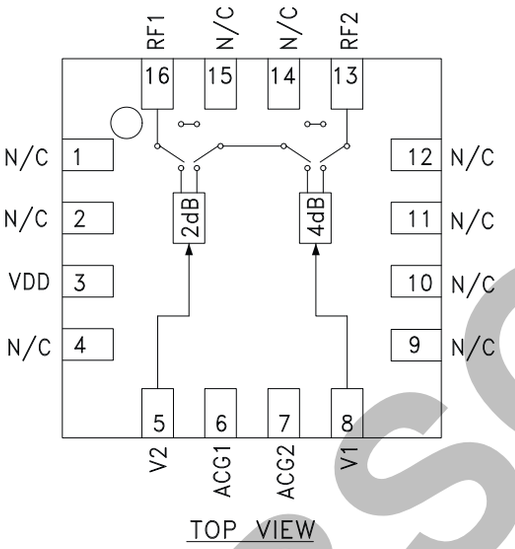
± 0.2 dB Typical Bit Error

Single Control Line Per Bit

Single +5V Supply

3x3 mm SMT Package

### Functional Diagram




### General Description

The HMC467LP3 & HMC467LP3E are broadband 2-bit GaAs IC digital attenuators in low cost leadless surface mount packages. Covering DC to 6.0 GHz, the insertion loss is less than 0.7 dB typical. The attenuator bit values are 2 (LSB) and 4 dB for a total attenuation of 6 dB. Attenuation accuracy is excellent at ± 0.2 dB typical step error with an IIP3 of +50 dBm. Two control voltage inputs, toggled between 0 and +5V, are used to select each attenuation state. A single Vdd bias of +5V is required.

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### Electrical Specifications, $T_A$ = +25° C, With Vdd = +5V & Vctl = 0/+5V*

| Parameter | Frequency (GHz) | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Insertion Loss | DC - 2.5 GHz<br>2.5 - 6.0 GHz | | 0.5<br>0.8 | 0.8<br>1.2 | dB<br>dB |
| Attenuation Range | DC - 6 GHz | | 6 | | dB |
| Return Loss (RF1 & RF2, All Atten. States) | DC - 2.5 GHz<br>2.5 - 6.0 GHz | | 20<br>15 | | dB<br>dB |
| Attenuation Accuracy: (Referenced to Insertion Loss) 2 dB State<br>4, 6 dB States | DC - 6 GHz | | ± 0.2 + 2% of Atten. Setting Max.<br>± 0.4 + 2% of Atten. Setting Max. | | dB<br>dB |
| Input Power for 0.1 dB Compression | 0.25 - 6.0 GHz | | 22 | | dBm |
| Input Third Order Intercept Point (Two-Tone Input Power= 0 dBm Each Tone) | 0.25 - 6.0 GHz | | 50 | | dBm |
| Switching Characteristics<br>tRISE, tFALL (10/90% RF)<br>tON, tOFF (50% CTL to 10/90% RF) | DC - 6 GHz | | <br>135<br>155 | | <br>ns<br>ns |

** Bypass capacitor connecting ACG1 & ACG2 to RF ground required per pin description herein.*

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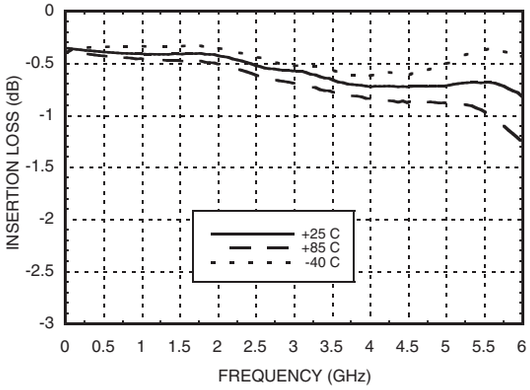
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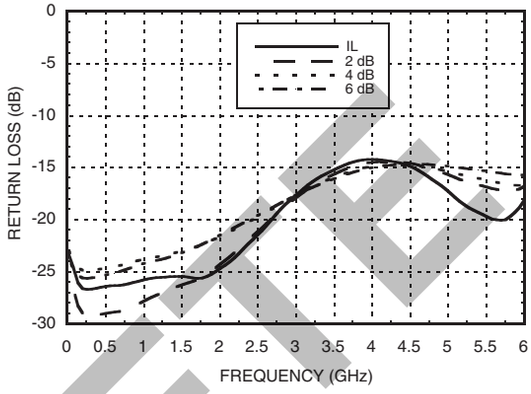


## Insertion Loss



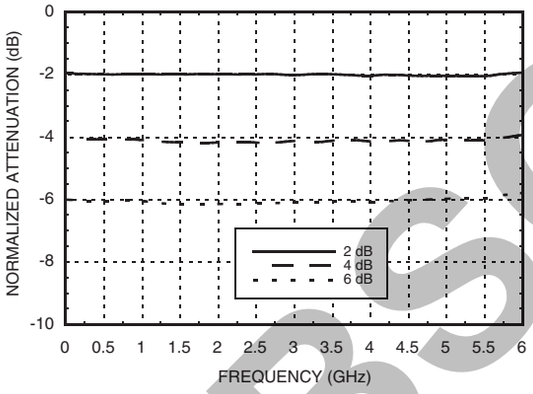

## Return Loss RF1, RF2

*(Only Major States are Shown)*

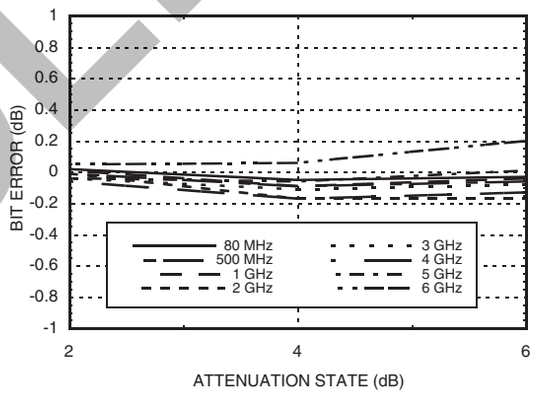



## Normalized Attenuation

*(Only Major States are Shown)*

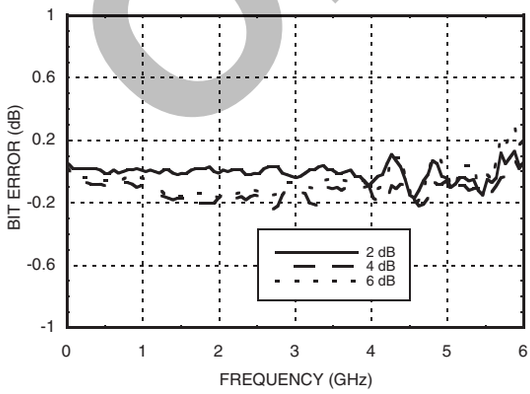



## Bit Error vs. Attenuation State



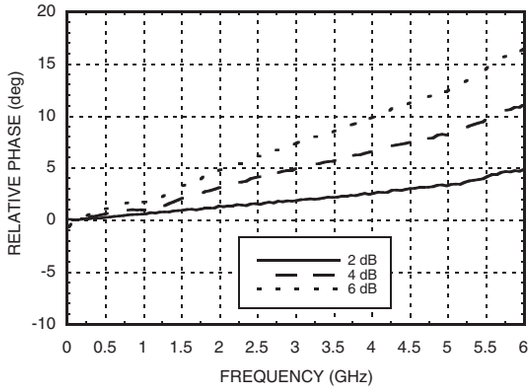

## Bit Error vs. Frequency

*(Only Major States are Shown)*




## Relative Phase vs. Frequency

*(Only Major States are Shown)*




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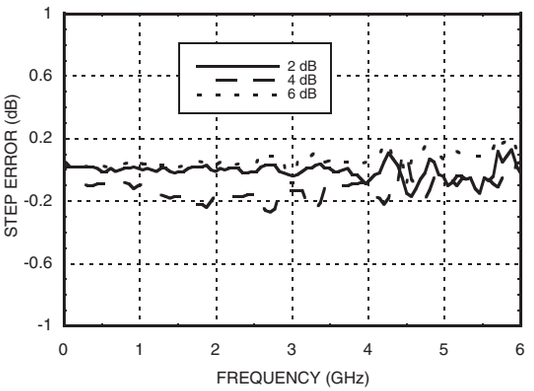
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### Worst Case Step Error Between Successive Attenuation States




### Truth Table

| Control Voltage Input | | Attenuation Setting RF1 - RF2 |
|---|---|---|
| V1 4 dB | V2 2 dB | |
| High | High | Reference I.L. |
| High | Low | 2 dB |
| Low | High | 4 dB |
| Low | Low | 6 dB Max. Atten. |
| Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected. | | |

### Bias Voltage & Current

| Vdd Range= +5.0 Vdc ± 10% | | |
|---|---|---|
| Vdd (Vdc) | Idd (Typ.) (mA) | Idd (Max.) (mA) |
| +5.0 | 0.7 | 1.2 |

### TTL/CMOS Control Voltages

| State | Bias Condition |
|---|---|
| Low | 0 to 0.8 Vdc @ -5 uA Typ. |
| High | +2.0 to +5.0 Vdc @ 40 uA Typ. |

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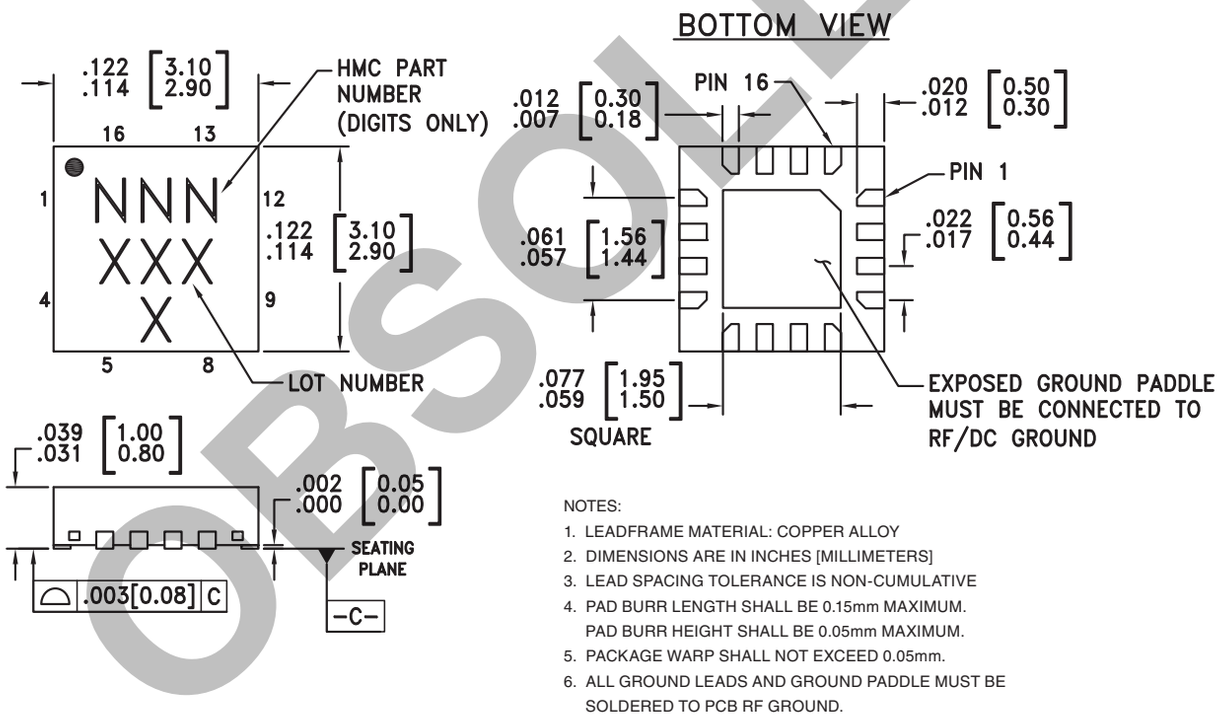


## Absolute Maximum Ratings

| | |
|---|---|
| Control Voltage (V1, V2) | -0.5 Vdc to Vdd +1 Vdc |
| Bias Voltage (Vdd) | +7.0 Vdc |
| Staorage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |
| RF Input Power | +30 dBm |
| ESD Sensitivity (HBM) | Class 1A |

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

## Outline Drawing




NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

## Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking [3] |
|---|---|---|---|---|
| HMC467LP3 | Low Stress Injection Molded Plastic | Sn/Pb Solder | MSL1 [1] | 467<br>XXXX |
| HMC467LP3E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 [2] | 467<br>XXXX |

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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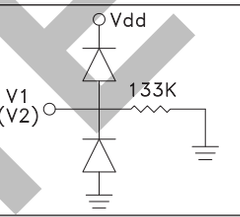
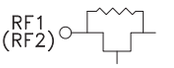
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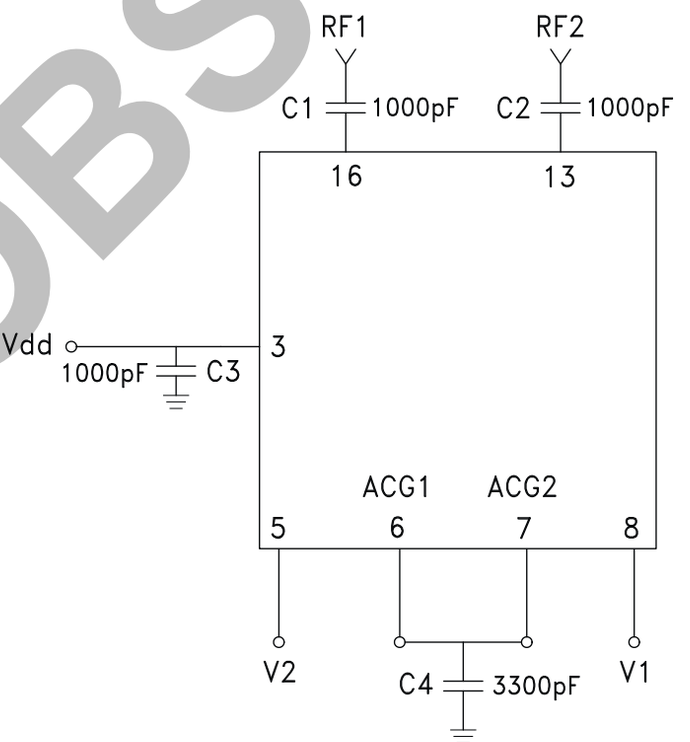
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### Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 1, 2, 4, 9 - 12, 14, 15 | N/C | These pins should be connected to PCB RF ground to maximize performance. | |
| 3 | Vdd | Supply Voltage | |
| 5, 8 | V2, V1 | See truth table and control voltage table. |   |
| 6, 7 | ACG1, ACG2 | External capacitor to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible. | |
| 13, 16 | RF2, RF1 | These pins are DC coupled and matched to 50 Ohm. Blocking capacitors are required. |   |
| | GND | Package bottom has an exposed metal paddle that must be connected to RF/DC ground. |   |

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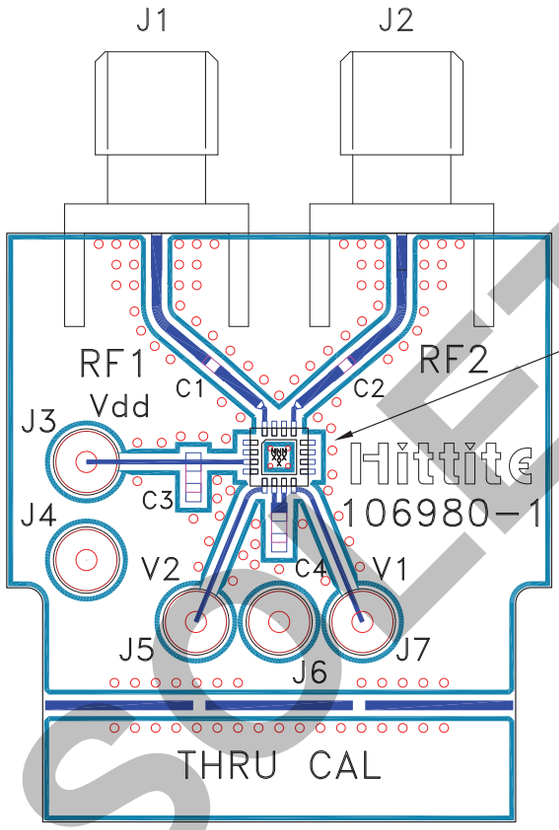
### Application Circuit




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## Evaluation PCB




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## List of Materials for Evaluation PCB 107008 [1]

| Item | Description |
|---|---|
| J1 - J2 | PCB Mount SMA Connector |
| J3 - J7 | DC Pin |
| C1, C2 | 1000 pF Capacitor, 0402 Pkg. |
| C3 | 1000 pF Capacitor, 0603 Pkg. |
| C4 | 3300 pF Capacitor, 0603 Pkg. |
| U1 | HMC467LP3 / HMC467LP3E Digital Attenuator |
| PCB [2] | 106980 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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