HM6287 Series

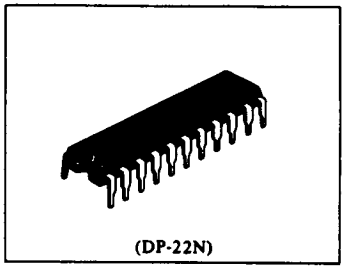
Maintenance Only

Refer to HM6287H Series

65536-word x 1-bit High Speed CMOS Static RAM

■ FEATURES

- High Speed: Fast Access Time 45/55/70ns (max.)
- Single 5V Supply and High Density 22 Pin Package
- Low Power Standby and Low Power Operation
  Standby: 100μW (typ.)/10μW (typ.) (L-version)
  Operation: 300mW (typ.)
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible: All Inputs and Output
- Capability of Battery Back Up Operation (L-version)

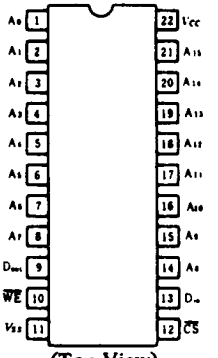


(DP-22N)

■ ORDERING INFORMATION

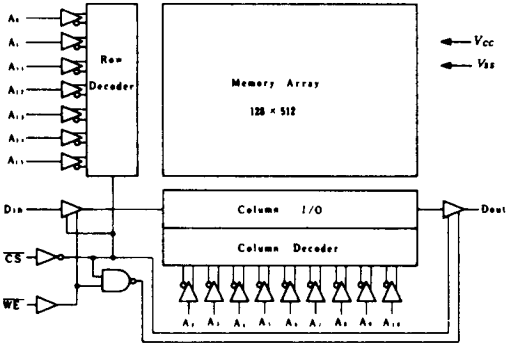
Type No.	Access Time	Package
HM6287P-45	45ns	300 mil 22 pin Plastic DIP
HM6287P-55	55ns	
HM6287P-70	70ns	
HM6287LP-45	45ns	
HM6287LP-55	55ns	
HM6287LP-70	70ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



This Material Copyrighted By Its Respective Manufacturer

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High Z	Write Cycle

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.5V for pulse width ≦ 20ns

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 20ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5V, V_{in} = V_{SS} to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$ = V_{IH}, V_{out} = V_{SS} to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{out} = 0mA, min. cycle	–	60	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, min. cycle	–	10	30	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC}$−0.2V,	–	0.02	2.0	mA
		0V ≦ V_{in} ≦ 0.2V or V_{CC} − 0.2V ≦ V_{in}	–	2*2	100*2	μA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	V
	V_{OH}	I_{OH} = −4.0mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC} = 5.0V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	5	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	7.5	pF

Note) This parameter is sampled and not 100% tested.

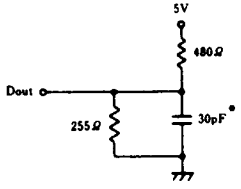
This Material Copyrighted By Its Respective Manufacturer

■ AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

• AC TEST CONDITIONS

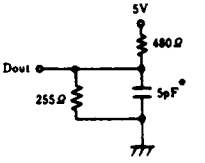
Input Pulse Levels: V_{SS} to 3.0V
Input Rise and Fall Times: 5ns
Input and Output Timing Reference Levels: 1.5V
Output Load: See Figure

Output Load A



*Including scope & jig capacitance

Output Load B

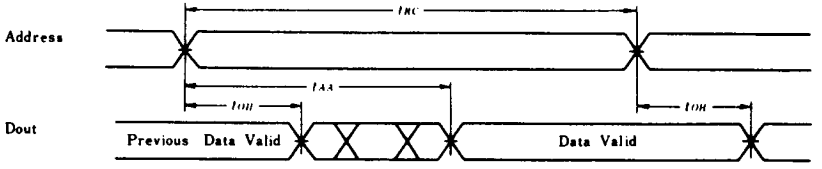


*Including scope & jig capacitance

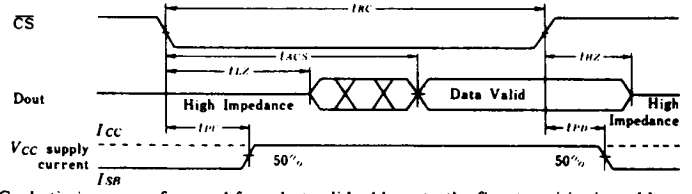
• READ CYCLE

Item	Symbol	HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	45	–	55	–	70	–	ns	1
Address Access Time	t_{AA}	–	45	–	55	–	70	ns	
Chip Select Access Time	t_{ACS}	–	45	–	55	–	70	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	5	–	ns	2, 3, 7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	2, 3, 7
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	0	–	ns	7
Chip Deselection to Power Down Time	t_{PD}	–	40	–	40	–	40	ns	7

• Timing Waveform of Read Cycle No. 1 (4)(5)



• Timing Waveform of Read Cycle No. 2 (4)(6)



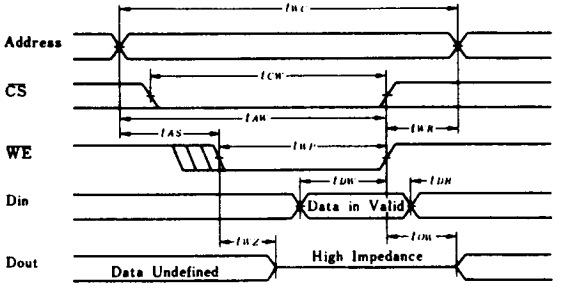
Notes:
1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is high for READ Cycle.
5. Device is continuously selected, while $\overline{CS}$ = V_{IL}.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

This Material Copyrighted By Its Respective Manufacturer

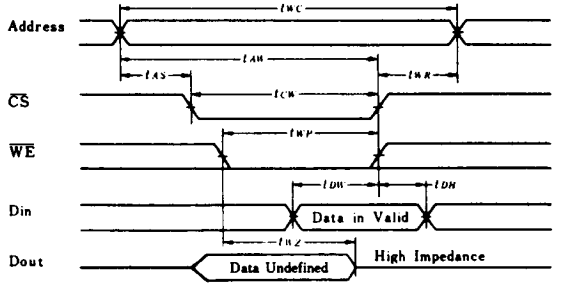
• WRITE CYCLE

Item	Symbol	HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	45	–	55	–	70	–	ns	2
Chip Selection to End of Write	t_{CW}	40	–	50	–	55	–	ns	
Address Valid to End of Write	t_{AW}	40	–	50	–	55	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns	
Write Pulse Width	t_{WP}	25	–	35	–	40	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	25	–	25	–	30	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns	
Write Enabled to Output in High Z	t_{WZ}	0	25	0	25	0	30	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	0	–	ns	3, 4

• Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



• Timing Waveform of Write Cycle No. 1 ($\overline{CS}$ Controlled)



Notes) 1. If $\overline{CS}$ goes high Simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

This Material Copyrighted By Its Respective Manufacturer

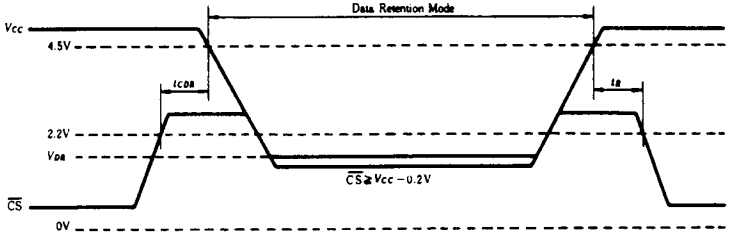
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristics is guaranteed only for L-version.

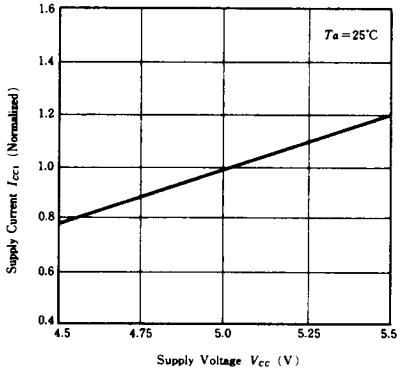
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC} - 0.2V$, $V_{in} \geqq V_{CC} - 0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	2.0	–	–	V
Data Retention Current	I_{CCDR}		–	1	50*2	µA
Chip Deselect to Data Retention Time	t_{CDR}	See retention waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*1	–	–	ns

Note) *1. t_{RC} = Read Cycle Time
*2. V_{CC} = 3.0V

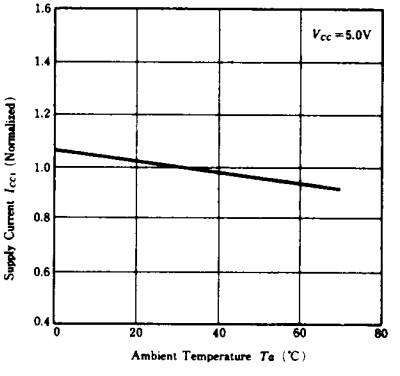
● LOW V_{CC} DATA RETENTION WAVEFORM



SUPPLY CURRENT vs. SUPPLY VOLTAGE

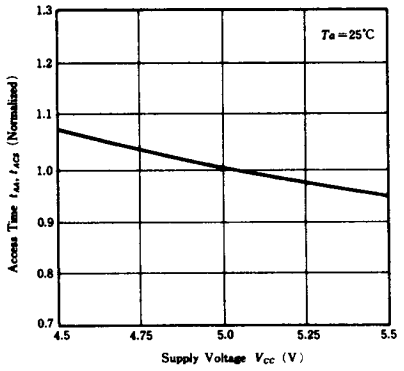


SUPPLY CURRENT vs. AMBIENT TEMPERATURE

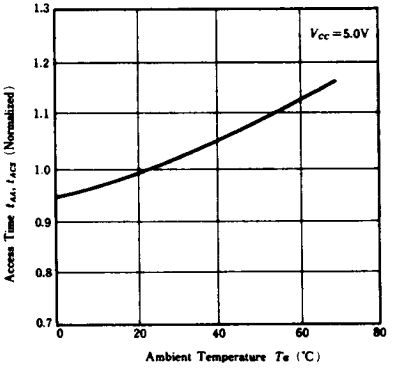


This Material Copyrighted By Its Respective Manufacturer

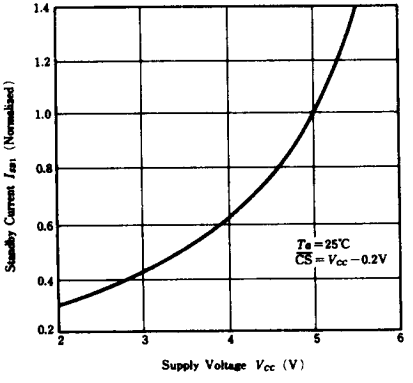
ACCESS TIME vs. SUPPLY VOLTAGE



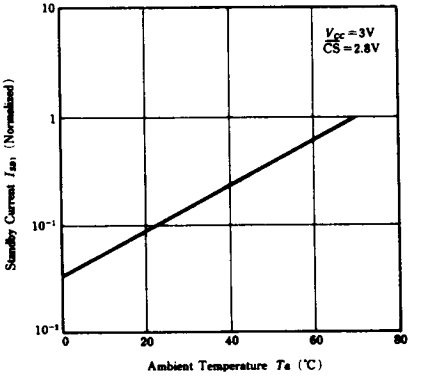
ACCESS TIME vs. AMBIENT TEMPERATURE



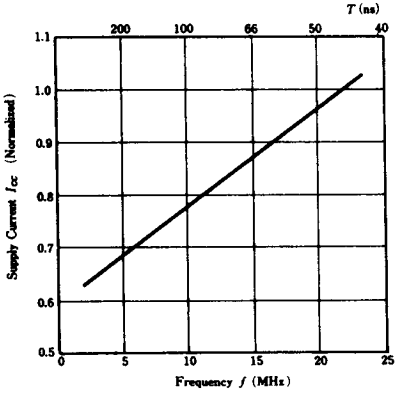
STANDBY CURRENT vs. SUPPLY VOLTAGE



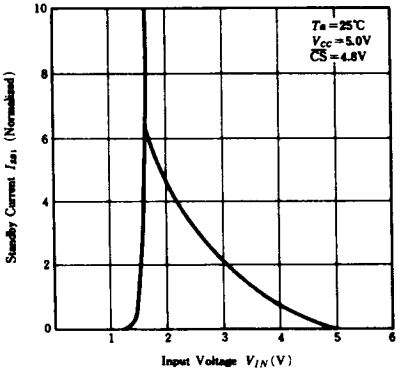
STANDBY CURRENT vs. AMBIENT TEMPERATURE



SUPPLY CURRENT vs. FREQUENCY

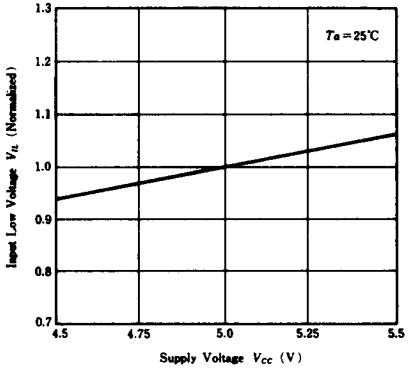


STANDBY CURRENT vs. INPUT VOLTAGE

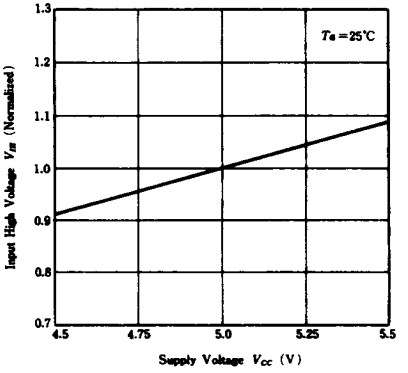


This Material Copyrighted By Its Respective Manufacturer

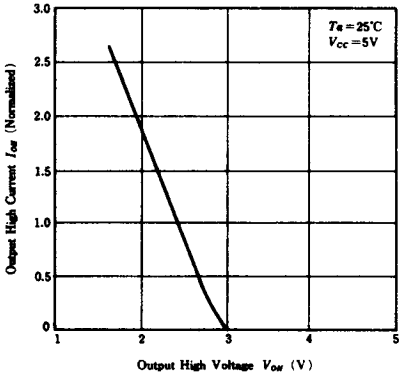
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



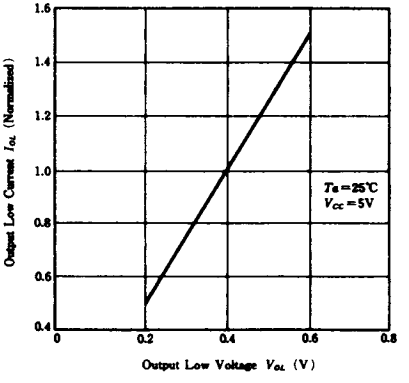
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



2

This Material Copyrighted By Its Respective Manufacturer