Two-Wire Serial EEPROM

1024K (8-bit wide)

FEATURES

- Low voltage and low power operations:
  - HM24C1024: V_{CC} = 1.8V to 5.5V
- Maximum Standby current < 1μA.
- 256 bytes page write mode.
- Partial page write operation allowed.
- Internally organized: 131,072 X 8 (1024K).
- Standard 2-wire bi-directional serial interface.
- Schmitt trigger, filtered inputs for noise protection.
- Self-timed programming cycle (5ms maximum).
- Automatic erase before write operation.
- Write protect pin for hardware data protection.
- High reliability: typically 1,000,000 cycles endurance.
- 40 years data retention.
- Industrial temperature range (-40^{o} C to 85^{o} C).
- Standard 8-pin DIP/SOP Pb-free packages.

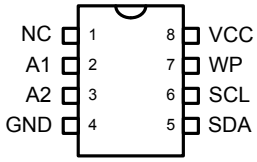
DESCRIPTION

The HM24C1024 series are 1,048,576 bits of serial Electrical Erasable and Programmable Read Only Memory, commonly known as EEPROM. They are organized as 131,072 words of 8 bits (one byte) each. The devices are fabricated with proprietary advanced CMOS process for low power and low voltage applications. These devices are available in standard 8-lead DIP, and 8-lead SOP packages. A standard 2-wire serial interface is used to address all read and write functions. Our extended V_{CC} range (1.8V to 5.5V) devices enables wide spectrum of applications.

PIN CONFIGURATION

Pin Name	Pin Function
A2, A1	Device Address Inputs
SDA	Serial Data Input / Open Drain Output
SCL	Serial Clock Input
WP	Write Protect
NC	No-Connect

All three packaging types come in Pb-free certified.

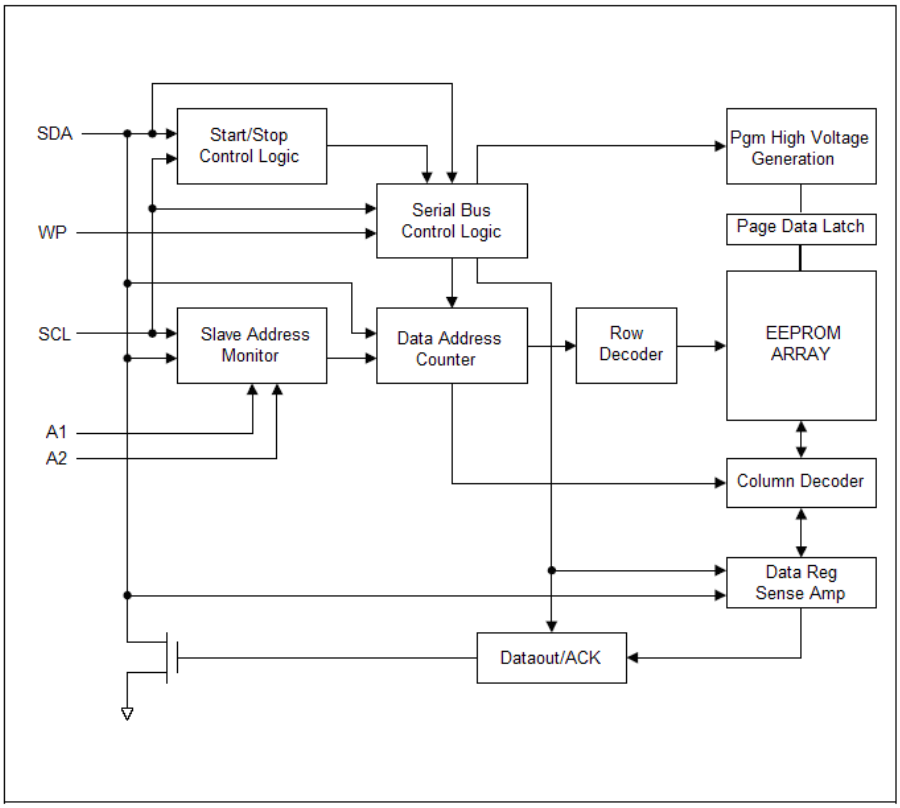


8L DIP
8L SOP

ABSOLUTE MAXIMUM RATINGS

Industrial operating temperature:	-40°C to 85°C
Storage temperature:	-50°C to 125°C
Input voltage on any pin relative to ground:	-0.3V to V_{CC} + 0.3V
Maximum voltage:	8V
ESD Protection on all pins	>2000V

** Stresses exceed those listed under "Absolute Maximum Rating" may cause permanent damage to the device. Functional operation of the device at conditions beyond those listed in the specification is not guaranteed. Prolonged exposure to extreme conditions may affect device reliability or functionality*.



Block Diagram

PIN DESCRIPTIONS

(A) SERIAL CLOCK (SCL)

The rising edge of this SCL input is to latch data into the EEPROM device while the falling edge of this clock is to clock data out of the EEPROM device.

(B) DEVICE / CHIP SELECT ADDRESSES (A2, A1)

These are the chip select input signals for the serial EEPROM devices. Typically, these signals are hardwired to either V_{IH} or V_{IL}. If left unconnected, they are internally recognized as V_{IL}.

(C) SERIAL DATA LINE (SDA)

SDA data line is a bi-directional signal for the serial devices. It is an open drain output signal and can be wired-OR with other open-drain output devices.

(D) WRITE PROTECT (WP)

The HM24C1024 device has a WP pin to protect the whole EEPROM array from programming. Programming operations are allowed if WP pin is left un-connected or input to V_{IL}. Conversely all programming functions are disabled if WP pin is connected to V_{IH} or V_{CC}. Read operations is not affected by the WP pin's input level.

MEMORY ORGANIZATION

The HM24C1024 devices have 512 pages respectively. Since each page has 256 bytes, random word addressing to HM24C1024 will require 17 bits data word addresses.

DEVICE OPERATION

(A) SERIAL CLOCK AND DATA TRANSITIONS

The SDA pin is typically pulled to high by an external resistor. Data is allowed to change only when Serial clock SCL is at V_{IL}. Any SDA signal transition may interpret as either a START or STOP condition as described below.

(B) START CONDITION

With SCL V_{IH}, a SDA transition from high to low is interpreted as a START condition. All valid commands must begin with a START condition.

(C) STOP CONDITION

With SCL V_{IH}, a SDA transition from low to high is interpreted as a STOP condition. All valid read or write commands end with a STOP condition. The device goes into the STANDBY mode if it is after a read command. A STOP condition after page or byte write command will trigger the chip into the STANDBY mode after the self-timed internal programming finish (see Figure 1).

(D) ACKNOWLEDGE

The 2-wire protocol transmits address and data to and from the EEPROM in 8 bit words. The EEPROM acknowledges the data or address by outputting a "0" after receiving each word. The ACKNOWLEDGE signal occurs on the 9^{th} serial clock after each word.

(E) STANDBY MODE

The EEPROM goes into low power STANDBY mode after a fresh power up, after receiving a STOP bit in read mode, or after completing a self-time internal programming operation.

Figure 1: Timing diagram for START and STOP conditions

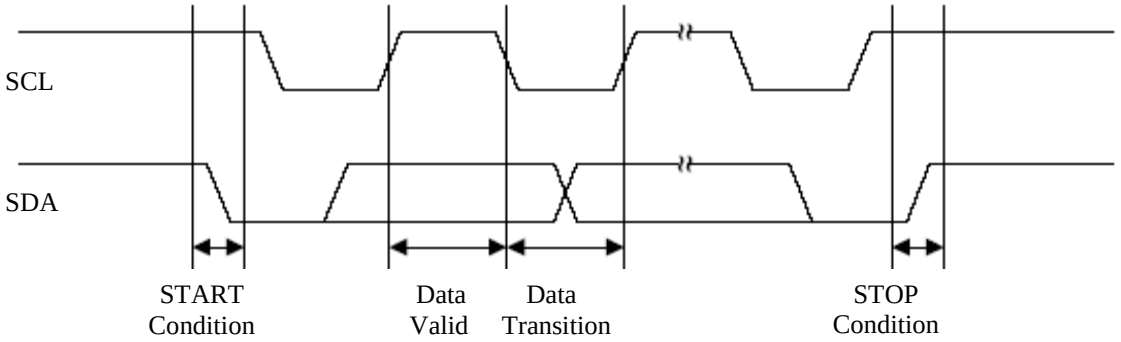
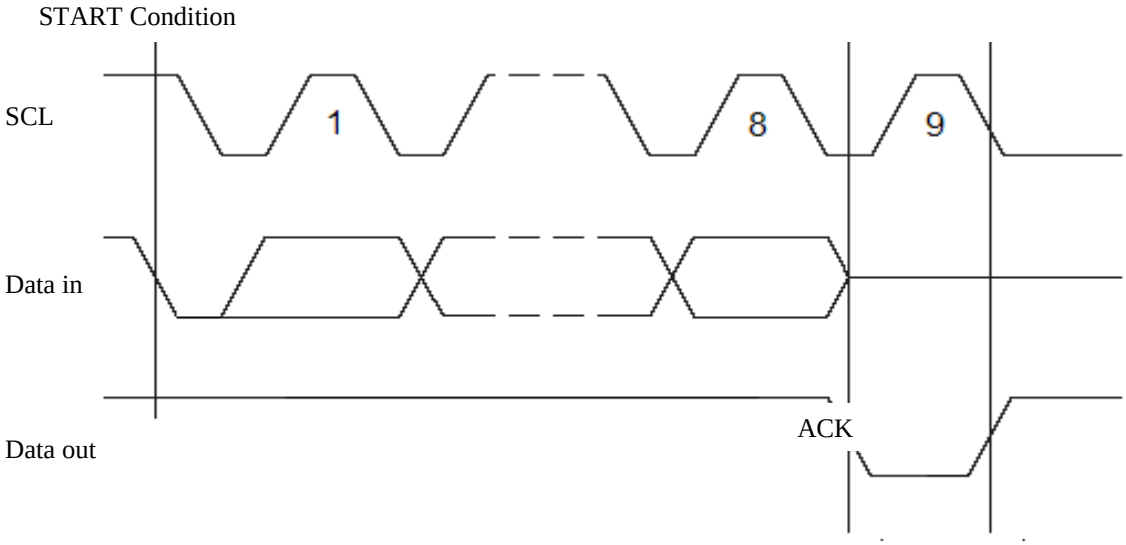


Figure 2: Timing diagram for output ACKNOWLEDGE



DEVICE ADDRESSING

The 2-wire serial bus protocol mandates an 8 bits device address word after a START bit condition to invoke a valid read or write command. The first four most significant bits of the device address must be 1010, which is common to all serial EEPROM devices. The next two bits are device address bits. These two device address bits (5^{th} and 6^{th}) are to match with the external chip select/address pin states. If a match is made, the EEPROM device outputs an ACKNOWLEDGE signal after the 8^{th} read/write bit, otherwise the chip will go into STANDBY mode. However, matching may not be needed for some or all device address bits (5^{th} and 6^{th}) as noted below. The seventh bit of the device address (P0) is a memory page address bit. The last or 8th bit is a read/write command bit. If the 8th bit is at V_{IH} then the chip goes into read mode. If a "0" is detected, the device enters programming mode.

WRITE OPERATIONS

(A) BYTE WRITE

A write operation requires the seventh bit of the device address (P0) and two 8-bit data word address following the device address word and ACKNOWLEDGE signal. Upon receipt of this address, the EEPROM will respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will again output a "0". The addressing device, such as a microcontroller, must terminate the write sequence with a STOP condition. At this time the EEPROM enters into an internally-timed write cycle state. All inputs are disabled during this write cycle and the EEPROM will not respond until the writing is completed (figure 3).

(B) PAGE WRITE

The 1024K EEPROM are capable of 256-byte page write.

A page write is initiated the same way as a byte write, but the microcontroller does not send a STOP condition after the first data word is clocked in. The microcontroller can transmit up to 255 more data words after the EEPROM acknowledges receipt of the first data word. The EEPROM will respond with a "0" after each data word is received. The microcontroller must terminate the page write sequence with a STOP condition (see Figure 4).

The lower 8 bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. If more than 256 data words are transmitted to the EEPROM, the data word address will "roll over" and the previous data will be overwritten.

(C) ACKNOWLEDGE POLLING

ACKNOWLEDGE polling may be used to poll the programming status during a self-timed internal programming. By issuing a valid read or write address command, the EEPROM will not acknowledge at the 9^{th} clock cycle if the device is still in the self-timed programming mode. However, if the programming completes and the chip has returned to the STANDBY mode, the device will return a valid ACKNOWLEDGE signal at the 9^{th} clock cycle.

READ OPERATIONS

The read command is similar to the write command except the 8^{th} read/write bit in address word is set to "1". The three read operation modes are described as follows:

(A) CURRENT ADDRESS READ

The EEPROM internal address word counter maintains the last read or write address plus one if the power supply to the device has not been cut off. To initiate a current address read operation, the micro-controller issues a START bit and a valid device address word with the read/write bit (8^{th}) set to "1". The EEPROM will response with an ACKNOWLEDGE signal on the 9^{th} serial clock cycle. An 8-bit data word will then be serially clocked out. The internal address word counter will then automatically increase by one. For current address read the micro-controller will not issue an ACKNOWLEDGE signal on the 18^{th} clock cycle. The micro-controller issues a valid STOP bit after the 18^{th} clock cycle to terminate the read operation. The device then returns to STANDBY mode (see Figure 5).

(B) SEQUENTIAL READ

The sequential read is very similar to current address read. The micro-controller issues a START bit and a valid device address word with read/write bit (8^{th}) set to "1". The EEPROM will response with an ACKNOWLEDGE signal on the 9^{th} serial clock cycle. An 8-bit data word will then be serially clocked out. Meanwhile the internally address word counter will then automatically increase by one.

Unlike current address read, the micro-controller sends an ACKNOWLEDGE signal on the 18th clock cycle signaling the EEPROM device that it wants another byte of data. Upon receiving the ACKNOWLEDGE signal, the EEPROM will serially clocked out an 8-bit data word based on the incremented internal address counter. If the micro-controller needs another data, it sends out an ACKNOWLEDGE signal on the 27th clock cycle. Another 8-bit data word will then be serially clocked out. This sequential read continues as long as the micro-controller sends an ACKNOWLEDGE signal after receiving a new data word. When the internal address counter reaches its maximum valid address, it rolls over to the beginning of the memory array address. Similar to current address read, the micro-controller can terminate the sequential read by not acknowledging the last data word received, but sending a STOP bit afterwards instead (figure 6).

(C) RANDOM READ

Random read is a two-steps process. The first step is to initialize the internal address counter with a target read address using a "dummy write" instruction. The second step is a current address read.

To initialize the internal address counter with a target read address, the micro-controller issues a START bit first, follows by a valid device address with the read/write bit (8th) set to "0". The EEPROM will then acknowledge. The micro-controller will then send two address words. Again the EEPROM will acknowledge. Instead of sending a valid written data to the EEPROM, the micro-controller performs a current address read instruction to read the data. Note that once a START bit is issued, the EEPROM will reset the internal programming process and continue to execute the new instruction - which is to read the current address (figure 7).

Figure 3: Byte Write

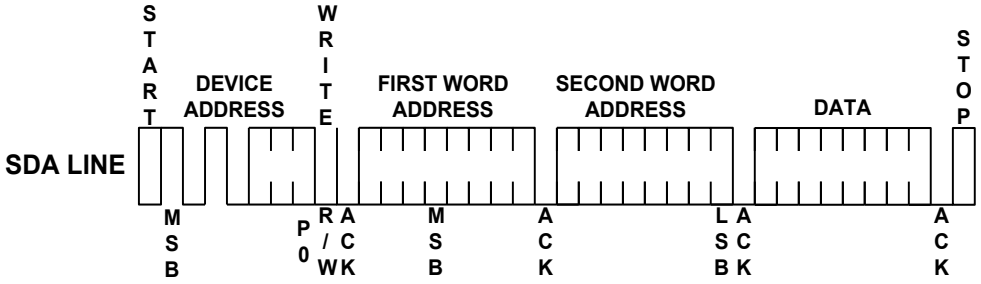


Figure 4: Page Write

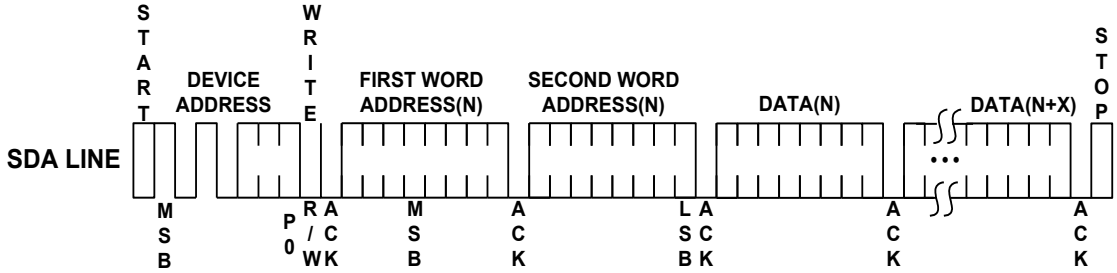


Figure 5: Current Address Read

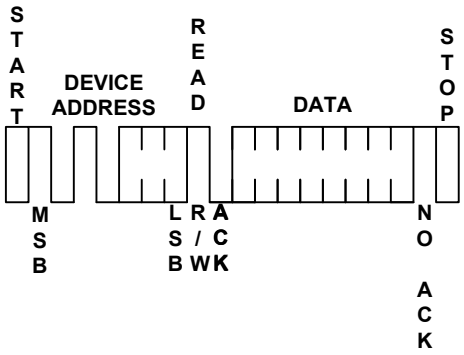


Figure 6: Sequential Read

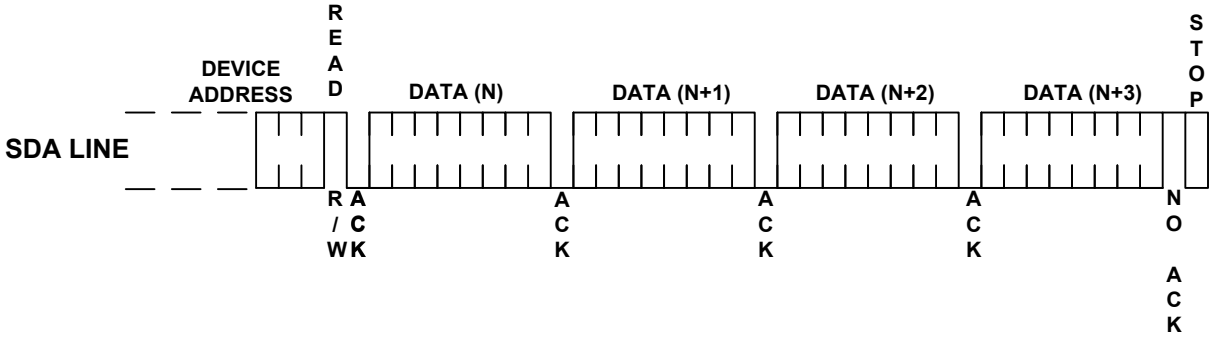


Figure 7: Random Read

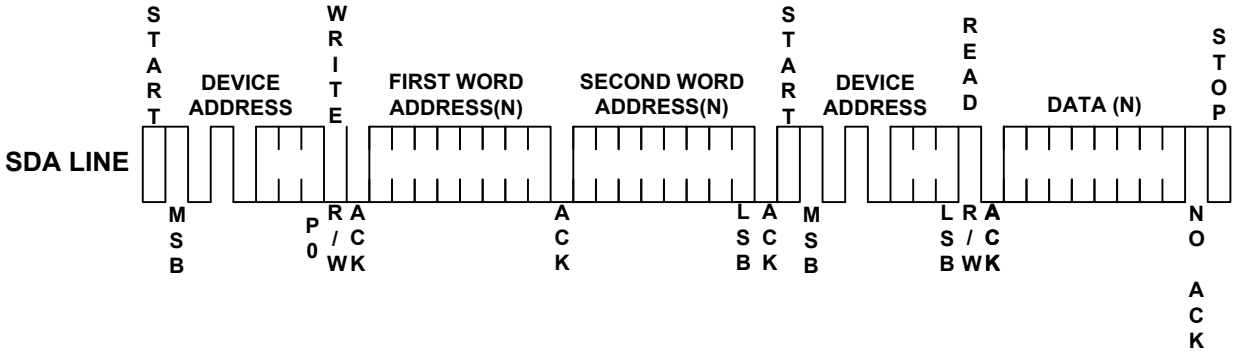
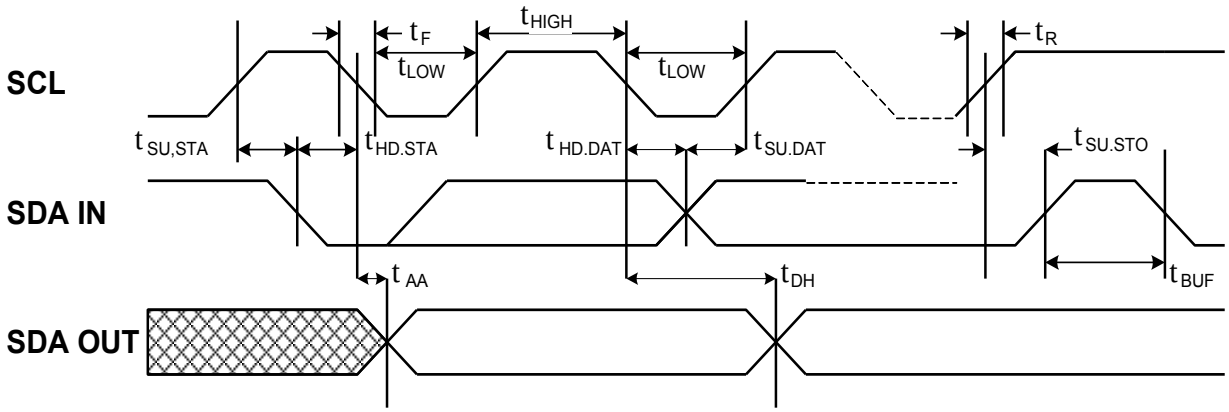


Figure 8: SCL and SDA Bus Timing



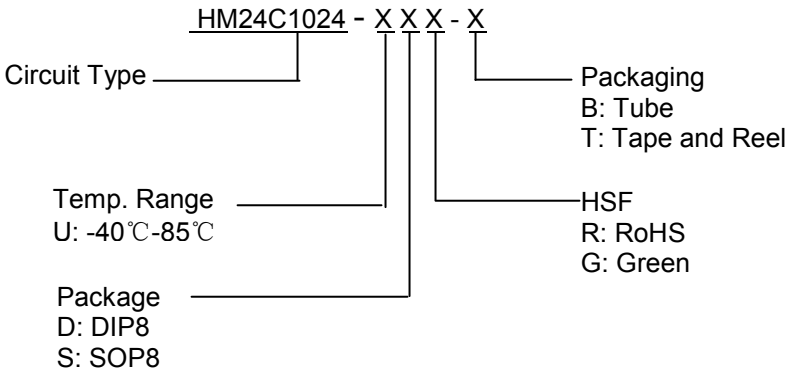
AC CHARACTERISTICS

Symbol	Parameter	1.8 V		2.5-5.0 V		Unit
		Min	Max	Min	Max	
f_{SCL}	Clock frequency, SCL		400		1000	kHz
t_{LOW}	Clock pulse width low	1.2		0.6		μs
t_{HIGH}	Clock pulse width high	0.4		0.3		μs
t_I	Noise suppression time		100		50	ns
t_{AA}	Clock low to data out valid	0.3	1.2	0.2	0.5	μs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3		1.3		μs
$t_{HD.STA}$	START hold time	0.6		0.6		μs
$t_{SU.STA}$	START set-up time	0.6		0.6		μs
$t_{HD.DAT}$	Data in hold time	0		0		μs
$t_{SU.DAT}$	Data in set-up time	100		100		ns
t_R	Input rise time		300		300	ns
t_F	Input fall time		300		300	ns
$t_{SU.STO}$	STOP set-up time	0.6		0.6		μs
t_{DH}	Date out hold time	50		50		ns
t_{WR}	Write cycle time		5		5	ms

DC CHARACTERISTICS

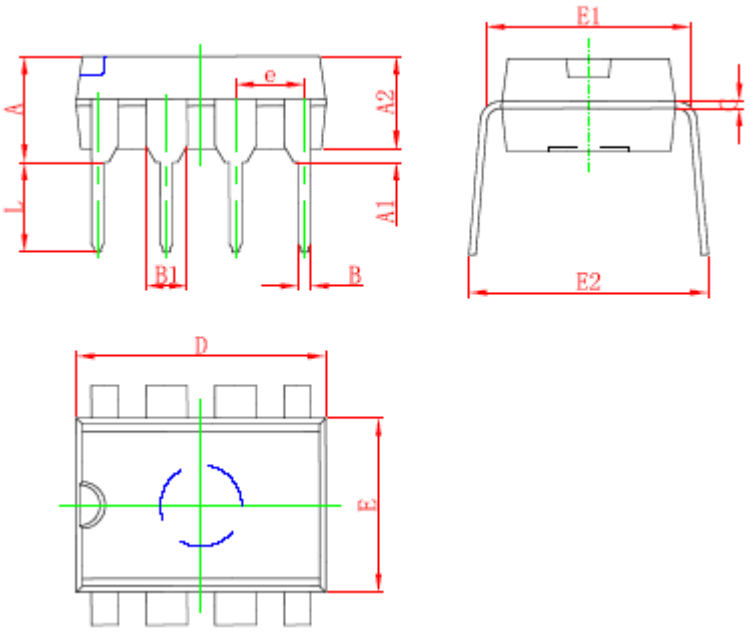
Symbol	Parameter	Test Conditions	Min	Typical	Max	Units
V_{CC1}	supply V_{CC}		1.8		5.5	V
I_{CC}	Supply read current	V_{CC} @ 5.0V SCL = 400 kHz		0.5	1.0	mA
I_{CC}	Supply write current	V_{CC} @ 5.0V SCL = 400 kHz		2.0	3.0	mA
I_{SB1}	Supply current	V_{CC} @ 1.8V, V_{IN} = V_{CC} or V_{SS}			1.0	μA
I_{SB2}	Supply current	V_{CC} @ 2.5V, V_{IN} = V_{CC} or V_{SS}			1.0	μA
I_{SB3}	Supply current	V_{CC} @ 5.0V, V_{IN} = V_{CC} or V_{SS}			1.0	μA
I_{IL}	Input leakage current	V_{IN} = V_{CC} or V_{SS}			3.0	μA
I_{LO}	Output leakage current	V_{IN} = V_{CC} or V_{SS}			3.0	μA
V_{IL}	Input low level		-0.6		V_{CC} × 0.3	V
V_{IH}	Input high level		V_{CC} × 0.7		V_{CC} + 0.5	V
V_{OL2}	Output low level	V_{CC} @ 3.0V, I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output low level	V_{CC} @ 1.8V, I_{OL} = 0.15 mA			0.2	V

ORDER INFORMATION



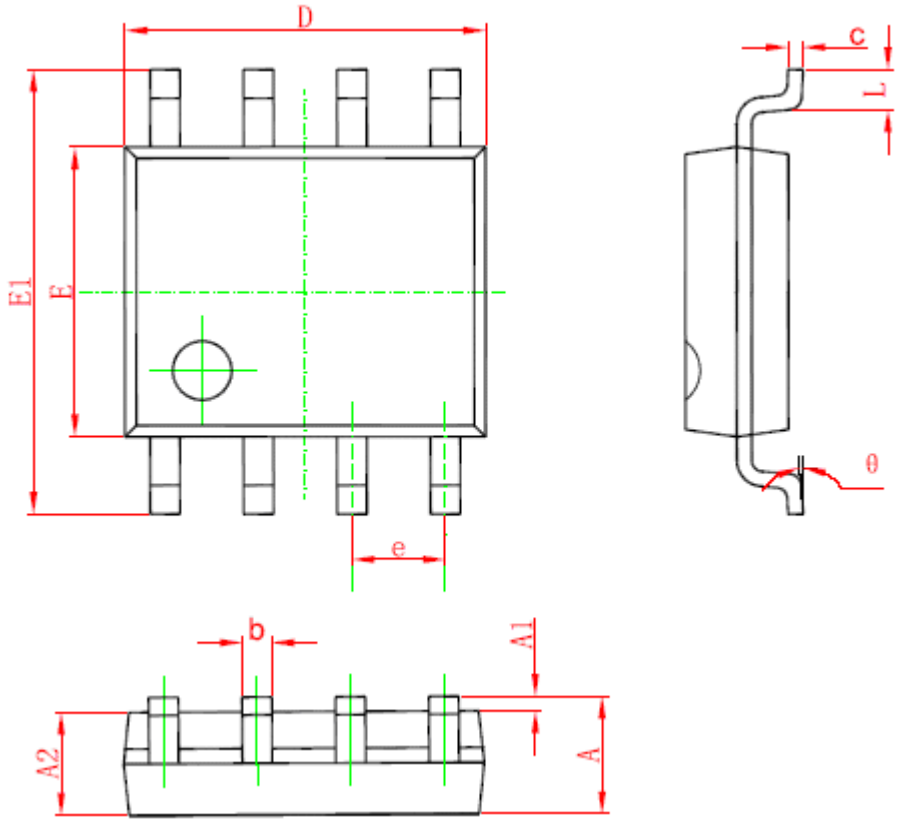
Density	Package	Temperature Range	Vcc	HSF	Packaging	Ordering Code
1024 kbits	DIP8	-40℃-85℃	1.8V-5.5V	RoHS	Tube	HM24C1024-UDR-B
				Green	Tube	HM24C1024-UDG-B
	SOP8	-40℃-85℃	1.8V-5.5V	RoHS	Tube	HM24C1024-USR-B
					Tape and Reel	HM24C1024-USR-T
				Green	Tube	HM24C1024-USG-B
					Tape and Reel	HM24C1024-USG-T

DIP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524（BSC）		0.060（BSC）	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100（BSC）	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°