HM-6518/883

March 1997

1024 x 1 CMOS RAM

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Power Standby . . . . . 50μW Max**
- **Low Power Operation . . . . . 20mW/MHz Max**
- **Fast Access Time. . . . . .180ns Max**
- **Data Retention . . . . . .at 2.0V Min**
- **TTL Compatible Input/Output**
- **High Output Drive - 2 TTL Loads**
- **High Noise Immunity**
- **On-Chip Address Register**
- **Two-Chip Selects for Easy Array Expansion**
- **Three-State Output**

Description

The HM-6518/883 is a 1024 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

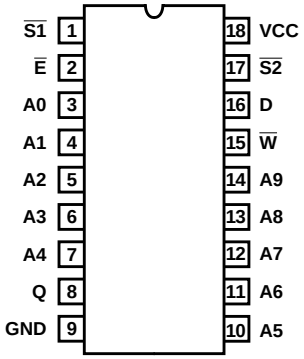
The HM-6518/883 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

PACKAGE	TEMP. RANGE	PART NUMBER	PKG. NO.
CERDIP	-55^{o}C to +125^{o}C	HM1-6518/883	F18.3

Pinout

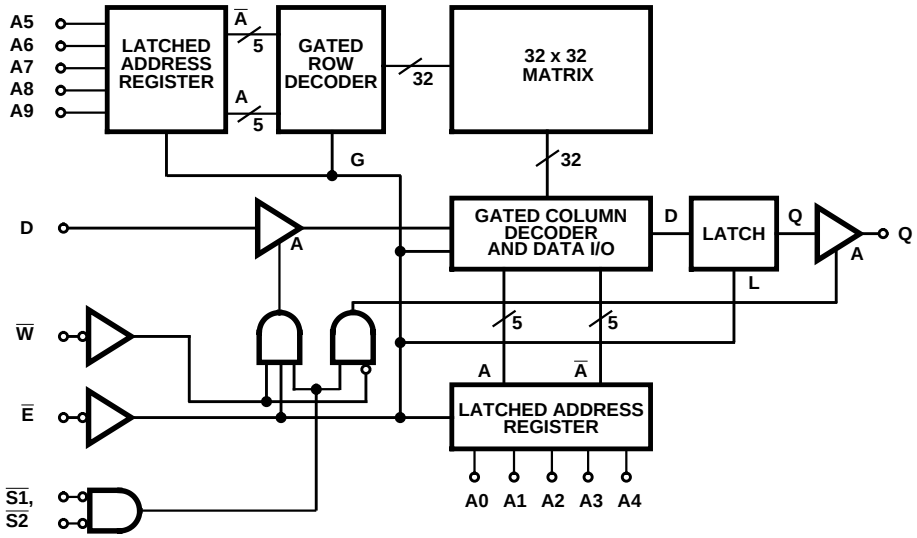
HM-6518/883
(CERDIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
S	Chip Select
D	Data Input
Q	Data Output

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Functional Diagram



NOTES:

1. All lines positive logic - active high.
2. Three-state buffers: A high $\rightarrow$ output active.
3. Data latches: L high $\rightarrow$ Q = D; Q Latches on rising edge of L.
4. Address latches and gated decoders: Latch on falling edge of $\overline{E}$ and gate on falling edge of $\overline{E}$.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55^oC to $+125^oC$
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . VCC -2.0V to VCC
Input Rise and Fall Time . . . . . 40ns Max

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}	θ_{JC}
CERDIP Package	$75^oC/W$	$15^oC/W$

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature . . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 1936 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. HM-6518/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V, IOL = 3.2mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V, IOH = -0.4mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	+1.0	µA
Output Leakage Current	IOZ	VCC = 5.5V, VO = GND or VCC	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	+1.0	µA
Data Retention Supply Current HM-6518B/883	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC, IO = 0mA, VI = VCC or GND	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	5	µA
HM-6518/883					-	10	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 2), $\overline{E}$ = 1MHz, IO = 0mA, VI = VCC or GND	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	4	mA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, VI = VCC or GND	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	10	µA

NOTES:

1. All voltages referenced to device GND.
2. Typical derating 1.5mA/MHz increase in ICCOP.

TABLE 2. HM-6518/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS				UNITS
					HM-6518B/883		HM-6518/883		
					MIN	MAX	MIN	MAX	
Chip Enable Access Time	(1) TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	180	-	250	ns
Address Access Time	(2) TAVQV	VCC = 4.5 and 5.5V, Note 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	180	-	250	ns
Chip Select Output Enable Time	(3) TSLQX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	5	-	5	-	ns
Write Enable Output Disable Time	(4) TWLQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	160	ns
Chip Select Output Disable Time	(5) TSHQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	160	ns
Chip Enable Pulse Negative Width	(6) TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	180	-	250	-	ns
Chip Enable Pulse Positive Width	(7) TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	100	-	ns
Address Setup Time	(8) TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Address Hold Time	(9) TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	50	-	ns
Data Setup Time	(10) TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	80	-	110	-	ns
Data Hold Time	(11) TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Chip Select Write Pulse Setup Time	(12) TWLSH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	130	-	ns
Chip Enable Write Pulse Setup Time	(13) TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	130	-	ns
Chip Select Write Pulse Hold Time	(14) TSLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	130	-	ns
Chip Enable Write Pulse Hold Time	(15) TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	130	-	ns
Write Enable Pulse Width	(16) TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	130	-	ns
Read or Write Cycle Time	(17) TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	280	-	350	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC -2.0V; input rise and fall times: 5ns (max); input and output timing reference level: 1.5V; output load: -1TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 3. HM-6518/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	$T_A = +25^oC$	-	6	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	$T_A = +25^oC$	-	10	pF

NOTE: 1. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Timing Waveforms

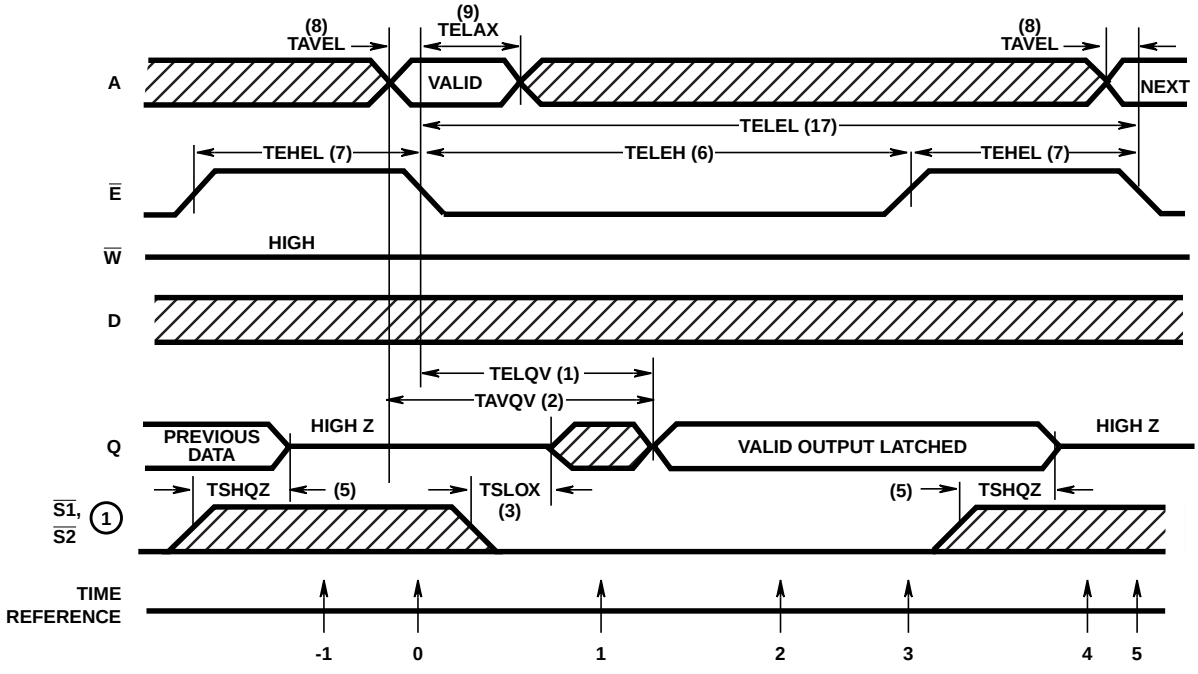


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS					OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	Z	Memory Disabled
0	↘	X	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	L	H	X	X	X	Output Enabled
2	L	L	H	X	X	V	Output Valid
3	↗	L	H	X	X	V	Output Latched
4	H	H	X	X	X	Z	Device Disabled, Prepare for Next Cycle (Same as -1)
5	↘	X	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

In the HM-6518/883 read cycle the address information is latched into the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. In order for the output to be read $\overline{S1}$, $\overline{S2}$ and $\overline{E}$ must be low, $\overline{W}$ must be high. When $\overline{E}$ goes high the output data is latched into an on chip register. Taking either or both $\overline{S1}$ or $\overline{S2}$ high, forces the output buffer to a high impedance state. The output data may be re-enabled at any time by taking $\overline{S1}$ and $\overline{S2}$ low. On the falling edge of $\overline{E}$ the data will be unlatched.

Timing Waveforms

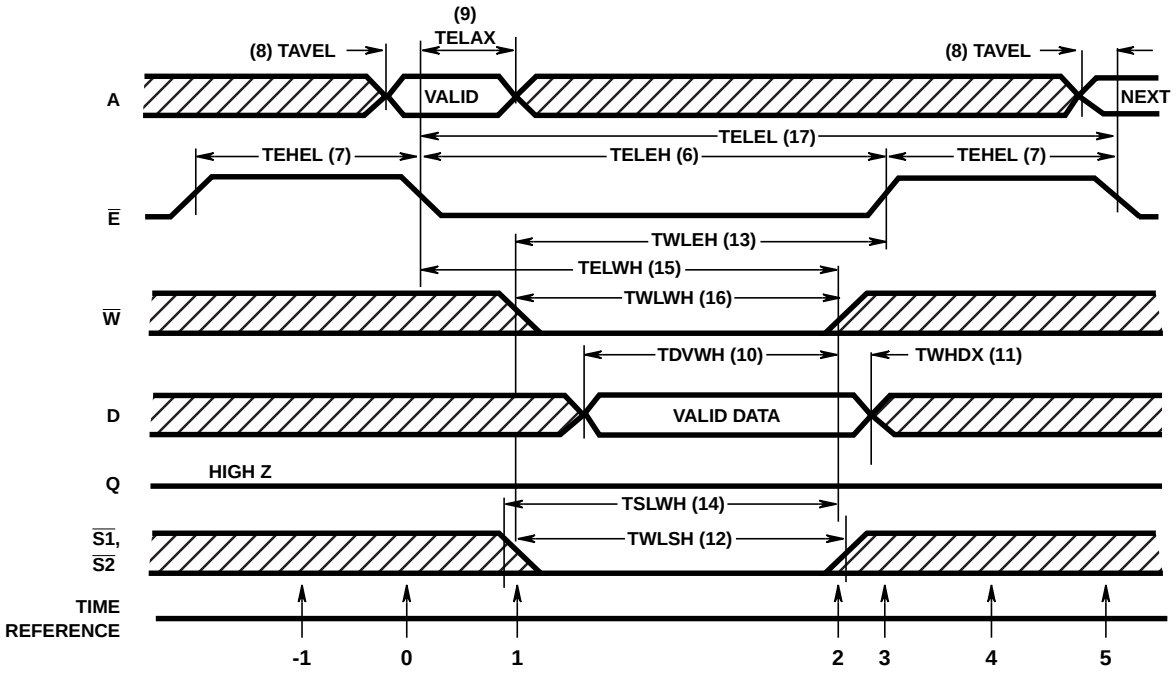


FIGURE 2. WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS					OUTPUTS	FUNCTION
	$\overline{E}$	S1	$\overline{W}$	A	D	Q	
-1	H	X	X	X	X	Z	Memory Disabled
0	↘	X	X	V	X	Z	Cycle Begins, Addresses are Latched
1	L	L	L	X	V	Z	Write Mode has Begun
2	L	↗	L	X	V	Z	Data is Written
3	↗	X	X	X	X	Z	Write Completed
4	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

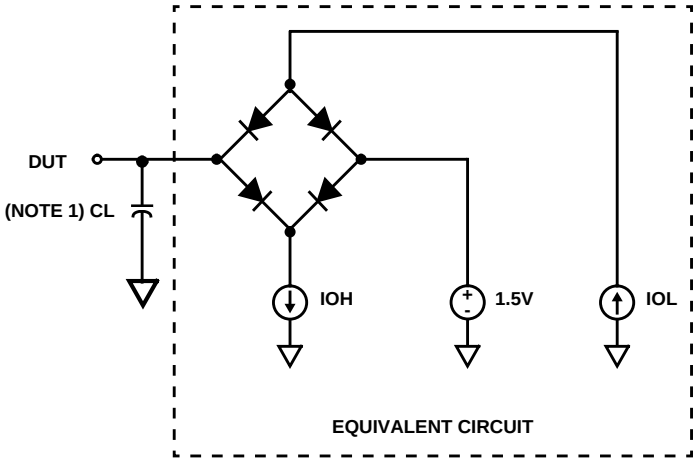
The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ and $\overline{S2}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$, $\overline{W}$, $\overline{S1}$ or $\overline{S2}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed. If the $\overline{E}$ low time (TELEH) is greater than the W pulse (TWLWH), plus an output enable time (TSLQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will ensure that the output buffers are not active.

Test Load Circuit

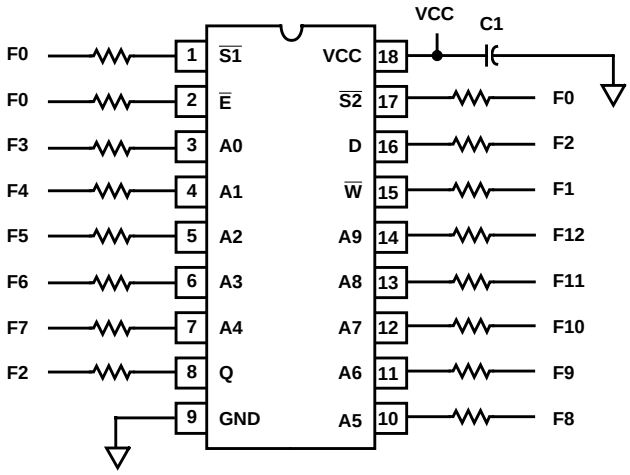


NOTE:

1. Test head capacitance includes stray and jig capacitance.

Burn-In Circuit

HM-6518/883 CERDIP



NOTES:

All resistors 47kΩ ±5%.

F0 = 100kHz ±10%.

F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2. . . . F12 = F11 ÷ 2.

VCC = 5.5V ±0.5V.

VIH = 4.5V ±10%.

VIL = -0.2V to +0.4V.

C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
130 x 150 x 19 ±1mils

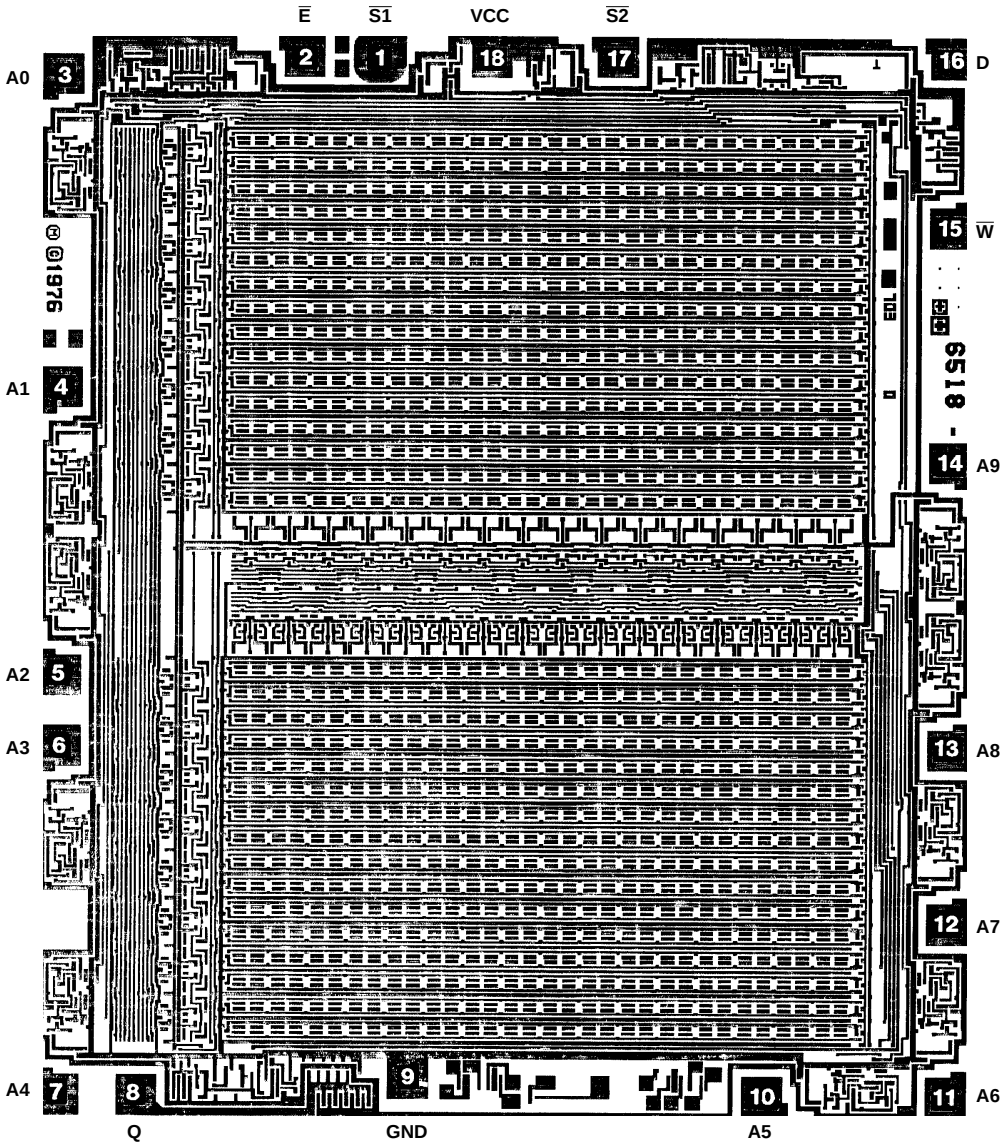
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
1.342×10^5 A/cm^2

Metallization Mask Layout

HM-6518/883



NOTE: Pin numbers correspond to DIP package only.

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