Data Sheet | January 6, 2006 | FN4367.2

Engine Knock Signal Processor

The HIP9011 is used to provide a method of detecting premature detonation often referred to as “Knock or Ping” in internal combustion engines.

The IC is shown in the Simplified Block Diagram. The chip can select between one of two sensors, if needed for accurate monitoring or for “V” type engines. Internal control via the SPI bus is fast enough to switch sensors between each firing cycle. A programmable bandpass filter processes the signal from either of the sensor inputs. The bandpass filter can be selected to optimize the extraction the engine knock or ping signals from the engine background noise. Further single processing is obtained by full wave rectification of the filtered signal and applying it to an integrator whose output voltage level is proportional to the knock signal amplitude. The chip is under microprocessor control via a SPI interface bus.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (^{O}C)	PACKAGE	PKG. DWG. #
HIP9011AB	HIP9011AB	-40 to 125	20 Ld SOIC	M20.3
HIP9011ABZ (See Note)	HIP9011ABZ	-40 to 125	20 Ld SOIC (Pb-free)	M20.3

Add “T” suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

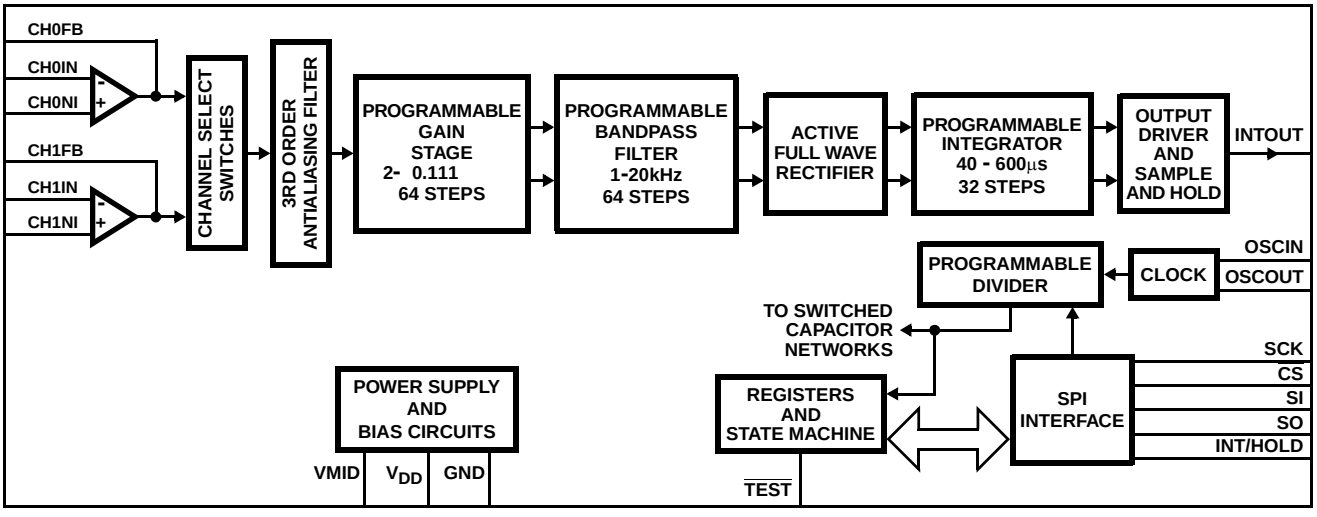
Features

- Two Sensor Inputs
- Microprocessor Programmable
- Accurate and Stable Filter Elements
- Digitally Programmable Gain
- Digitally Programmable Time Constants
- Digitally Programmable Filter Characteristics
- On-Chip Crystal Oscillator
- Programmable Frequency Divider
- External Clock Frequencies up to 24MHz
  - 4, 5, 6, 8, 10, 12, 16, 20, and 24MHz
- Operating Temperature Range -40°C to 125°C
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Engine Knock Detector Processor
- Analog Signal Processing Where Controllable Filter Characteristics are Required

Simplified Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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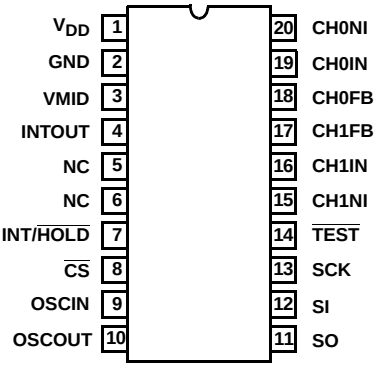
Pinout

HIP9011
(SOIC)
TOP VIEW



Pin Descriptions

PIN NUMBER	DESIGNATION	DESCRIPTION
1	V_{DD}	Five volt power input.
2	GND	This pin is tied to ground.
3	V_{MID}	This pin is connected to the internal mid-supply generator and is brought out for bypassing by a 0.022µF capacitor.
4	INTOUT	Buffered output of the integrator. Output signal is held by an internal Sample and Hold circuit when INT/$\overline{HOLD}$ is low.
5, 6	NC	These pins are not internally connected. Do Not Use.
7	INT/$\overline{HOLD}$	Selects whether the chip is in the Integrate Mode (Input High) or in the Hold Mode (Input Low). This pin has an internal pull down.
8	$\overline{CS}$	A low input on this pin enables the chip to communicate over the SPI bus. This pin has an internal pull-up.
9	OSCIN	Input to inverter used for the oscillator circuit. A 4MHz crystal or ceramic resonator is connected between this pin and pin 10. To bias the inverter, a 1.0MΩ to 10MΩ resistor is usually connected between this pin and pin 10.
10	OSCOUT	Output of the inverter used for the oscillator. See pin 9 above.
11	SO	Output of the chip SPI data bus. This is a three-state output that is controlled via the SPI bus. The output is placed in the high impedance state by setting $\overline{CS}$ high when the chip is not selected. This high impedance state can also be programmed by setting the LSB of the prescaler word to 1. This will take precedence over $\overline{CS}$. A 0 enables the active state. The Diagnostic Mode overrides these conditions.
12	SI	Input of the chip SPI data bus. Data length is eight bits. This pin has an internal pull-up.
13	SCK	Input from the SPI clock. Normally low, the data is transferred to the chip internal circuitry on the falling clock edge. This pin has an internal pull up.
14	$\overline{TEST}$	A low on this pin places the chip in the diagnostic mode. For normal operation this pin is tied high or left open. This pin has an internal pull up.
15	CH1NI	Non-inverting input of Channel one.
16	CH1IN	Inverting input to channel one amplifier. A resistor is tied from this summing input to the transducer. A second resistor is tied between this pin and pin 17, CH1FB to establish the gain of the amplifier.
17	CH1FB	Output of the channel one amplifier. This pin is used to apply feedback.
18	CH0FB	Output of the channel zero amplifier. This pin is used to apply feedback.
19	CH0IN	Inverting input to channel zero amplifier. Remainder same as channel one amplifier except feedback is applied from pin 18.
20	CH0NI	Non-inverting input of Channel 0. Remainder the same as pin 16, except feedback is applied from terminal 18.

Absolute Maximum Ratings

DC Logic Supply, V_{DD} . . . . . -0.5V to 7.0V
Output Voltage, V_O . . . . . -0.5V to 7.0V
Input Voltage, V_{IN} . . . . . 7V Max

Operating Conditions

Temperature Range . . . . . -40^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	120

Maximum Power Dissipation, P_D
For $T_A = -40^oC$ to 70^oC . . . . . 400mW Max
For $T_A = 70^oC$ to 125^oC, Derate Linearly at . . . . . 6mW/^oC
Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range, T_{STG} . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
At a Distance 1/16 ±1/32 inch, (1.59 ±0.79mm) from Case for 10s Max. (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V_{DD} = 5V ±5%, GND = 0V, Clock Frequency 4MHz ±0.1%, $T_A = -40^oC$ to 125^oC, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS						
Quiescent Supply Current	I_{DD}	V_{DD} = 5.25V, GND = 0V	-	5.0	8.0	mA
Midpoint Voltage, Pin 3	V_{MID}	V_{DD} = 5.0V, I_L = 2mA Source	2.3	2.45	2.55	V
Midpoint Voltage, Pin 3	V_{MID}	V_{DD} = 5.0V, I_L = 0mA	2.4	2.5	2.6	V
Low Input Voltage, Pins INT/$\overline{HOLD}$, $\overline{CS}$, SI, SCK	V_{IL}		-	-	30	% of V_{DD}
High Input Voltage, Pins INT/$\overline{HOLD}$, $\overline{CS}$, SI, SCK	V_{IH}		70	-	-	% of V_{DD}
Hysteresis voltage, Pins INT/$\overline{HOLD}$, $\overline{CS}$, SI, SCK	V_{HYST}		0.85	-	-	V
Internal Pull-Up Current	I Source $\overline{CS}$, SI, SCK, $\overline{TEST}$	V_{DD} = 5.0V, Measured at GND	-	50	-	µA
Internal Pull-Down Current	I Sink, INT/$\overline{HOLD}$	V_{DD} = 5.0V, Measured at V_{DD}	-	-50	-	µA
Low Level Output, Pin SO	V_{OL}	I_{SOURCE} = 1.6mA, V_{DD} = 5.0V	0.01	-	0.30	V
High Level Output, Pin SO	V_{OH}	I_{SINK} = 200µA, V_{DD} = 5.0V	4.8	4.9	5.0	V
Three-State Leakage Pin SO	I_L	Measured at GND; V_{DD} = 5.0V	-	-	±10	µA
Low Level Output, Pin 10, OSCOUT	V_{OL}	I_{SOURCE} = 500µA; V_{DD} = 5.0V	-	-	1.5	V
High Level Output, Pin 10, OSCOUT	V_{OH}	I_{SINK} = -500µA; V_{DD} = 5.0V	4.4	-	-	V
SPI BUS INTERFACE AC Parametrics						
CS Falling to SCLK Rising	t_{CCH}		10	-	-	ns
CS Rising to SCLK Falling	t_{CCL}		80	-	-	ns
SCLK Low	t_{PWL}		60	-	-	ns
SCLK High	t_{PWH}		60	-	-	ns
SCLK Falling to CS Rising	t_{SCCH}		60	-	-	ns
Data High Setup Time	t_{SUH}		20	-	-	ns
Data Low Setup Time	t_{SUL}		20	-	-	ns
Data High Hold Time	t_{HH}		10	-	-	ns
Data Low Hold Time	t_{HL}		10	-	-	ns
Min Time Between 2 Programmed Words	t_{CSH}		200	-	-	ns
CS Rising to INT/Hold Rising	t_{CIH}		8	-	-	µs

Electrical Specifications V_{DD} = 5V ±5%, GND = 0V, Clock Frequency 4MHz ±0.1%, T_A = -40°C to 125°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT AMPLIFIERS						
CH0 and CH1 High Output Voltage	$V_{OUT}HI$	I_{SINK} = 100µA, V_{DD} = 5.0V	4.7	4.9	-	V
CH0 and CH1 Low Output Voltage	$V_{OUT}LO$	I_{SOURCE} = 100µA; V_{DD} = 5.0V	-	15	200	mV
Voltage Gain	A_{CL}	Input R = 47.5K, Feedback R = 475kΩ	+18	+20	+21	dB
ANTIALIASING FILTER						
Response 1kHz to 20kHz, Referenced to 1kHz	BW	Test Mode	-	-0.5	-	dB
Attenuation at 180kHz, Referenced to 1kHz	ATTEN	Test Mode	-10	-15	-	dB
PROGRAMMABLE FILTERS						
Peak to Peak Voltage Output	V_{OUT}	Run Mode	3.5	4.0	-	V_{P-P}
Filters Q (Note 2)	Q	Run Mode	-	2.5	-	Q
PROGRAMMABLE GAIN AMPLIFIERS						
Percent Amplifier Gain Deviation	%G	Run Mode	-	±1	-	%
INTEGRATOR						
Integrator Reset Voltage	V_{RESET}	Pin 4 Voltage at Start of Integration Cycle; V_{DD} = 5.0V	75	125	175	mV
Integrator Droop after 500µs	V_{DROOP}	Hold Mode, Pin 7 = 0V, V_{DD} = 5.0V Pin 4 set to 20% to 80% of V_{DD}	-	±3	±50	mV
DIFFERENTIAL CONVERTER						
Differential to Single Ended Converter Offset Voltage	$DIFV_{IO}$	By Design	-	0.1	-	mV
Change In Converter Output	DIFOUT	Run Mode, 500µA Sinking Load to No Load Condition	-	±1	±10	mV
SYSTEM GAIN DEVIATION						
Gain Deviation from “Ideal Equation” Correlation Factor + 5.0% (Note 3)	V_{OUT} - V_{RESET}	Run Mode, maximum signal output from Input Amplifier <2.25V_{P-P}, Equation Output X 0.95 + Device Reset Voltage; For Total $V_{OUT} \leq$ 4.7V	-8%, ±100mV	Equation X 0.95 - V_{RESET}	8%, ±100mV	V

NOTES:

2. Q = fo/BW, where: fo = Center Frequency, BW = 3dB Bandwidth
3. Ideal Equation: INTOUT (Volts) = [V_{IN} * G_{IN} * G_{PR} * G_{BPF} * 1/π * (N/t_C(ms) * f_Q(kHz)) * G_{DSE}] + V_{RESET}
   Where: V_{IN} = input signal amplitude (V_{P-P})
   G_{IN} = External Input Gain; GIN = R_F/R_{IN}
   G_{PR} = Programmed Gain
   G_{BPF} = Gain of Bandpass Filter (2 for Ideal Case at Center)
   t_{INT} = Integration Time; t_{INT} = N/f_Q
   0.318 = 1/π
   N = Number of Cycles of Input Signal
   f_Q = Frequency of Input Signal
   R_F = Feedback Resistor Value
   R_{IN} = Signal Input Resistor Value
   t_C = Programmed Time Constant
   G_{DSE} = Gain of DSE Converter (2 for Ideal Case)
   V_{RESET} = Integrator Reset Voltage = 0.125V, Typ

Timing Diagrams

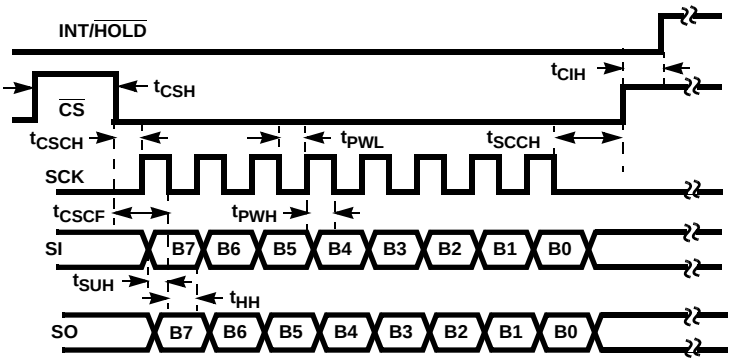


FIGURE 1. SPI TIMING

TABLE 1. SPI TIMING REQUIREMENTS

SYMBOL	REQUIREMENT	TIME
t_{CSCH}	Minimum time from $\overline{CS}$ falling edge to SCK rising edge.	10ns
t_{CSCF}	Minimum time from $\overline{CS}$ falling edge to SCK falling edge.	80ns
t_{PWL}	Minimum time for the SCK low.	60ns
t_{PWH}	Minimum time for the SCK high.	60ns
t_{SCCH}	Minimum time from SCK falling after 8 bits to CS raising edge.	80ns
t_{SUH}	Minimum time from data high to falling edge of spiclk.	20ns
t_{SUL}	Minimum time from data low to falling edge of spiclk.	20ns
t_{HH}	Minimum time for data high after the falling edge of the spiclk.	10ns
t_{HL}	Minimum time for data low after the falling edge of the spiclk.	10ns
t_{CIH}	Minimum time after $\overline{CS}$ raises until INT/$\overline{HOLD}$ goes high.	8µs
t_{CSH}	Minimum time between programming 2 internal registers.	200ns

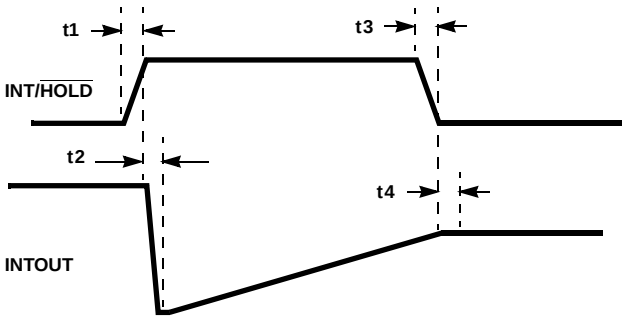
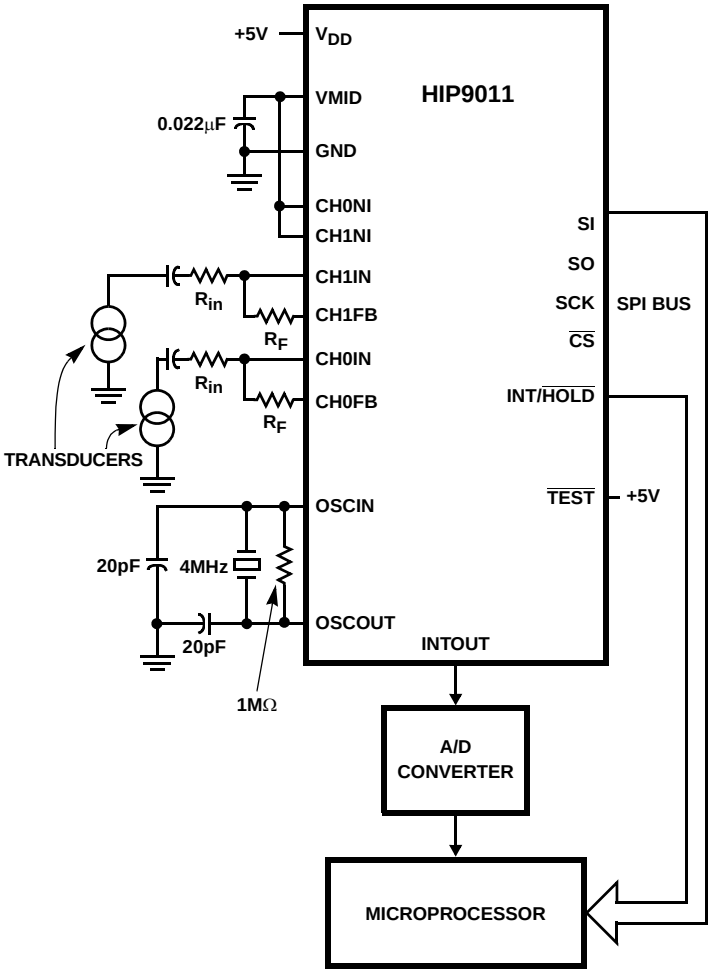


FIGURE 2. INTEGRATOR TIMING

TABLE 2. INTEGRATE/$\overline{HOLD}$ TIMING REQUIREMENTS

SYMBOL	REQUIREMENT	TIME
t1	Maximum rise time of the INT/$\overline{HOLD}$ signal.	45ns
t2	Maximum time after INT/$\overline{HOLD}$ rises for INTOUT to begin to integrate.	20µs
t3	Maximum fall time of INT/$\overline{HOLD}$ signal.	45ns
t4	Typical time after INT/$\overline{HOLD}$ goes low before chip goes into hold state.	20µs



EXAMPLE CASE USING IDEAL SYSTEM EQUATION

When the Input Signal is Present for the Period t_{INT}:

INTOUT (Volts) =

$$V_{IN} \times G_{IN} \times \left[\left(G_{BPR} \times G_{PR} \times \frac{1}{\pi} \times \frac{t_{int}}{t_c}\right) \times G_{DSE}\right] + V_{RESET}$$

Where:

V_{IN} = 200mV_{P-P}, Continuous AC Signal
G_{IN} = 1.0, Ratio of R_F to R_{IN}
G_{PR} = 0.190
G_{BPF} = 2.0 Ideal Gain Value
t_C = 200µs
t_{INT} = 2ms
G_{DSE} = 2.0 Ideal Gain Value
V_{RESET} = 0.125V, Typical Value

INTOUT (Volts) =

$200x10^{-3}*1*[2 * 0.19 * 0.318 * 2x10^{-3}/200x10^{-6}* 2]+0.125$
= 0.4833 + 0.125
= 0.608V

FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF THE HIP9011 IN AN AUTOMOTIVE APPLICATION

Description of the HIP9011 Operation

This IC is designed to be a universal digitally controlled, analog interface between engine acoustical sensors or accelerometers and internal combustion engine fuel management systems. Two wideband input amplifiers are provided which will allow the use of two sensors. These sensors be of the piezoelectric type, that can be mounted in optimum locations on either in-line or V type engine configurations.

Output from these input amplifiers are directed to a channel select mux switch and then into a 3rd order antialiasing filter. The output signal is then directed to two programmable gain stages, where one stage inverts or shifts the knock signal 180 degrees. The gain stage signals are outputted to two programmable bandpass filter stages. Outputs from the two BPF stages are then full wave rectified before being digitally integrated by the programmable integrator. The integrator output is applied to a line driver for further processing by the engine fuel management control system. The gain, bandpass filter and integrator stage settings are programmable from a microprocessor via the SPI Bus Interface

Broadband piezoelectric ceramic transducers used for the engine signal pickup have device capacitances in the order of 1100pF and output voltages that range from 5mV to 8V RMS. During normal engine operation, a single input channel is selected and applied to the HIP9011. The engine background noise is typically well below in amplitude than the pre-detonation noise. Therefore, the bandpass filter stages can be optimized to further discriminate between engine background and combustion noise and pre-detonation noise.

A basic approach to engine pre-detonation systems is to only observe engine background during the time interval that noise is expected and if detected, retard timing. This basic approach does not require the sensitivity and selectivity that is needed for a continuously adjustable solution. Enhanced fuel economy and performance is obtainable when this IC is coupled with a microprocessor controlled fuel management system.

Circuit Block Description

Input Amplifiers

Two amplifiers can be selected to interface to the engine sensors. These amplifiers have a typical open loop gain of 100dB, with a typical bandwidth of 2.6MHz. The common mode input voltage range extends to within 0.5V of either supply rail. The amplifier output has a similar output range.

Sufficient gain, bandwidth and output swing capability is provided to ensure that the amplifier can handle attenuation gain settings of 20 to 1 or -26dB. This would be needed when high peak output signals, in the range of $8V_{RMS}$ are obtained from the transducer. Gain settings of 10 times can also be needed when the transducers have output levels of $5mV_{RMS}$.

In a typical application the input signal frequency may vary from 1kHz to 20kHz. External capacitors are used to decouple the IC from the sensor (C1 and C2) refer to Figure 4. A typical value of the capacitor would be 3.3nF. Series input resistors, R1 and R2, are used to connect the inverting inputs of the amplifiers, (pins 19 and 16.) Feedback resistors, R3 and R4, in conjunction with R3 and R4 are used to set the gain of the amplifiers.

A mid voltage level is generated internally within the IC. This level is set to be half way between V_{DD} and ground. Throughout the IC this level is used as a quiet, DC reference for the signal processing circuits within the IC. This point is brought out for several reasons, it can be used as a reference voltage, and it must be bypassed to insure that it remains as a quiet reference for the internal circuitry.

The input amplifiers are designed with power down capability, which, when activated disables their bias circuit and their output goes into a three-state state condition. This is utilized during the diagnostic mode, in which the output terminals of the amplifiers are driven by the outside world with various test signals.

Antialiasing Filter

The IC has a 3rd order Butterworth filter with a 3dB point at 70kHz. Double poly capacitors and implanted resistors are used to set poles in the filter. This filter is required to have no more than 1dB attenuation at 20kHz (highest frequency off interest) and a minimum attenuation of 10dB at 180kHz. This filter precedes the switch capacitor filter stages which run at the system frequency of 200kHz.

Programmable Gain Stage

The gains for two identical programmable gain stages can be adjusted, so that the knock energies can be compensated if needed. This adjustment can be made with 64 different gain settings, ranging between 2 and 0.111. The signals can swing between 20 to 80 percent of V_{DD}. Programming is discussed in the SPI Communications Protocol section.

Programmable Bandpass Filter

Two identical programmable filters are used to detect the frequencies of interest. The Band Pass Filter (BPF) is programmed to pass the frequency component of the engine knock. The filter frequency is established by the characteristics of the particular engine and transducer. By integrating the rectified outputs from these two filters at the INTEGRATOR stage, a knock can be detected if it has occurred.

The filters have a nominal differential gain of 4. Their frequency is set by a programmable word (discussed in the SPI Communications Protocol section.) Center frequencies can be programed from 1.22kHz to 19.98kHz, in 64 steps. The filter Qs are typically 2.4.

Active Full Wave Rectifier

The output of the bandpass filters are unity gain buffered prior to full wave rectification using switch capacitor techniques. Each side of the rectifier circuit provides both negative and positive values of the knock frequency bandpass frequency filter outputs. The output is able to swing from 20 to 80 percent of V_{DD}. Care was taken to minimize the RMS variations from input to output of this stage.

Programmable Integrator Stage

The signals from the rectifier stage are separated into 2 output signal paths which are then integrated together. A differential system is used to minimize noise. One side integrates the positive energy value from the Knock Frequency Rectifier. The second side does the integration of the negative energy value. The positive and negative energy signals are opposite phase signals. Using this technique reduces system noise from affecting the actual signal.

The integrator time constant is software programmable by the Integrator Time Constant discussed in the Communications Protocol section. The time constant can be programmed from 40μs to 600μs, with a total of 32 steps. If for example, we program a time constant to 200μs, then with one volt difference between each channel, the output of the integrator will change by volt in 200μs.



FIGURE 4. INPUT AMPLIFIER CONNECTIONS

Integration is enabled by the rising edge of the input control signal INT/$\overline{HOLD}$. Within 20µs after the integrate input reaches a logic high level, the output of the integrator will fall to approximately V_{RESET}, 0.125V. The output of the integrator is an analog voltage.

Differential to Single-Ended Converter

This circuit takes the differential output of the integrators (through the test-multiplexer circuit) and provides a signal that is the sum of the two signals. This technique is used to improve the noise immunity of the system.

Output Buffer

This output amplifier is the same amplifier circuits as the input amplifier used to interface with the sensors. For diagnostic purposes when the output of the antialias filter is being evaluated, this amplifier is in the power down mode.

Test Multiplexer

This circuit receives the positive and negative outputs from the integrator, together with the outputs from different parts of the IC. The Test Mux output is controlled by the fifth programming word of the communications protocol. This multiplexes the switch capacitor filter output, the gain control output and the antialias filter output.

SPI Communications Protocol

Communicating to the Knock Sensor via the SPI Bus (MOSI). A chip select pin (CS) is used to enable the chip, which, in conjunction with the SPI clock (SCK), which moves an eight bit programming word. Five different programming words are used to set the following internal programmable registers: GAIN, BANDPASS FREQUENCY FILTER, INTEGRATOR TIME CONSTANT, CHANNEL SELECT, SO output mode, and TEST MODES.

When chip select ($\overline{CS}$) goes low, on the next falling edge of the SPI clock (SCK), data is latched into the SPI register. The data is shifted with the most significant bit first and least significant bit last. Each word is divided into two parts: first the address and then the value. Depending on the function being controlled, the address is 2 or 3 bits, and the value is either 5 or 6 bits long. All five programming words can be entered into the IC during the HOLD mode of operation. The integration or hold mode of operation is controlled by the INT/$\overline{HOLD}$ input signal.

Programming Words

1. Band Pass Filter Frequency: Defines the center frequency of the Band Pass Filter in the system. The first 2 bits are used for the address and the last 6 bits are used for its value. 00FFFFFF Example: 00001010 would be the Band Pass Filter at a center frequency of 1.78kHz (bit value of 10 in Table 3).
2. Gain Control: defines the value of the gain stage attenuation of gain setting. The first 2 bits are again used for the address and the last 6 bits for its value. 10GGGGGG Example: 10010100 would be the Gain Control (10 for the first two bits) with an attenuation of 0.739 (bit value of 20 in Table 3).
3. Integrator Time Constant: Defines the Integration Time Constant for the system. The first 3 bits are used for the address and the last 5 bits for the value. 110TTTTT Example: 11000011 would be the Integrator Time Constant (110 for the first 3 bits) and an Integration Time Constant of 55µs (bit value 3 in Table 3).
4. Test/Channel Select Control: Again the first three bits, 111 are the address for this function, and the last five bits define the functions that may be programmed. Example: 111B4B3B2B1B0; The options are:
   A) If B0 is “0”, than channel 0 is selected. If B0 is “1”; than channel 1 is selected as the input.
   B) The remaining bits are used for selection of the various diagnostic modes. $\overline{TEST}$ pin (14) = low. Not applicable in Run Mode.
5. Prescaler/SO terminal status: Defines the division ratio of the internal frequency prescaler and the status of the SO terminal, pin 11. P1 to P4 bits define the frequency that may be used with an external clock. The status of the three state SO pin is set by the last, Z bit. 01P5P4P3P2P1Z; Example: 0100000, Note, in this case bit P5 is not used. (01 for the first 2 bits sets the Prescaler/SO function) P1 to P4 set Prescaler for a clock frequency of 4MHz and the last bit sets the S0 terminal to an active state.

TABLE 3. FREQUENCY, GAIN, AND INTEGRATOR TIME CONSTANT

BIT VALUE PER FUNCTION	FREQUENCY (kHz)	GAIN	TIME CONSTANT (μs)	BIT VALUE PER FUNCTION	FREQUENCY (kHz)	GAIN
0	1.22	2.000	40	32	4.95	0.421
1	1.26	1.882	45	33	5.12	0.400
2	1.31	1.778	50	34	5.29	0.381
3	1.35	1.684	55	35	5.48	0.364
4	1.40	1.600	60	36	5.68	0.348
5	1.45	1.523	65	37	5.90	0.333
6	1.51	1.455	70	38	6.12	0.320
7	1.57	1.391	75	39	6.37	0.308
8	1.63	1.333	80	40	6.64	0.296
9	1.71	1.280	90	41	6.94	0.286
10	1.78	1.231	100	42	7.27	0.276
11	1.87	1.185	110	43	7.63	0.267
12	1.96	1.143	120	44	8.02	0.258
13	2.07	1.063	130	45	8.46	0.250
14	2.18	1.000	140	46	8.95	0.236
15	2.31	0.944	150	47	9.50	0.222
16	2.46	0.895	160	48	10.12	0.211
17	2.54	0.850	180	49	10.46	0.200
18	2.62	0.810	200	50	10.83	0.190
19	2.71	0.773	220	51	11.22	0.182
20	2.81	0.739	240	52	11.65	0.174
21	2.92	0.708	260	53	12.10	0.167
22	3.03	0.680	280	54	12.60	0.160
23	3.15	0.654	300	55	13.14	0.154
24	3.28	0.630	320	56	13.72	0.148
25	3.43	0.607	360	57	14.36	0.143
26	3.59	0.586	400	58	15.07	0.138
27	3.76	0.567	440	59	15.84	0.133
28	3.95	0.548	480	60	16.71	0.129
29	4.16	0.500	520	61	17.67	0.125
30	4.39	0.471	560	62	18.76	0.118
31	4.66	0.444	600	63	19.98	0.111

TABLE 4. PRESCALER

CLOCK FREQUENCY (MHz)	P5	P4	P3	P2	P1
4	X	0	0	0	0
5	X	0	0	0	1
6	X	0	0	1	0
8	X	0	0	1	1
10	X	0	1	0	0
12	X	0	1	0	1
16	X	0	1	1	0
20	X	0	1	1	1
24	X	1	0	0	0

NOTE: X = Don't care, P5 not used.

TABLE 5. SO TERMINAL STATUS

SO TERMINAL STATUS	Z
High Impedance	1
SO Terminal Active	0

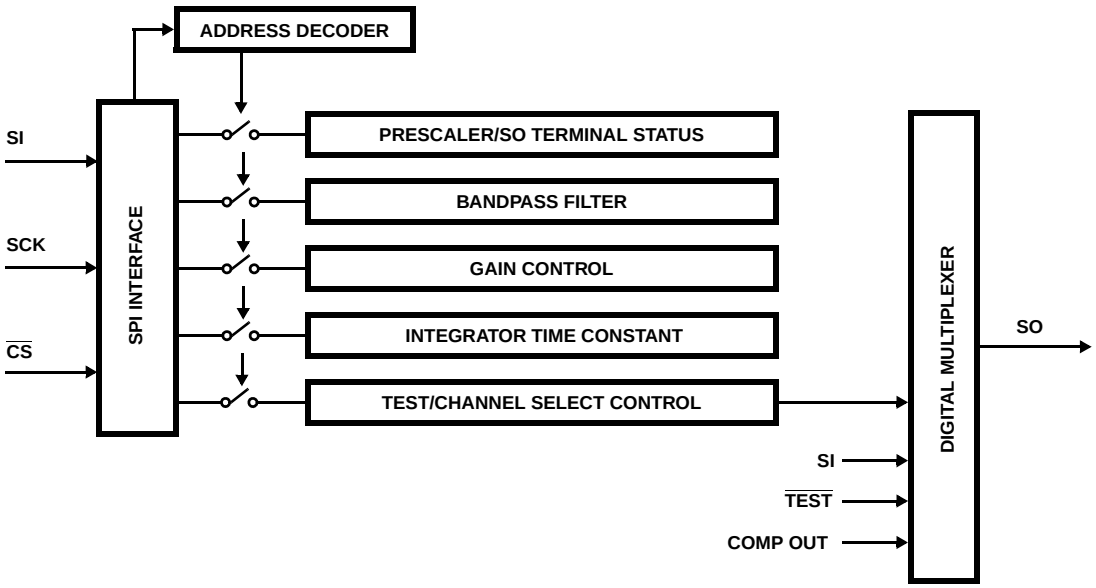


FIGURE 5. PROGRAMMABLE REGISTERS AND STATE MACHINE

The Digital SPI Block diagram in Figure 5 shows the programming flow of the chip. An eight bit word is received at the SI port. Data is shifted in by the SCK clock when the chip is enable by the $\overline{CS}$ pin. The word is decoded by the address decoding circuit, and the information is directed to one of 5 registers. These registers control the following chip functions:

1. Band Pass Filter frequency.
2. Gain control or attenuation.
3. Integration time constant of the rectified BPF output.
4. Prescaler.
5. Test/Channel Select.
   a) Test conditions of the part.
   b) Channel select to one of two input amplifiers.

A crystal oscillator circuit is provided. The chip requires at minimum a 4MHz crystal to be connected across OSCIN and OSCOUT pins. An external 4MHz signal may also be provided to the OSCIN Terminal Pin 9.

In the diagnostic mode, we can use the digital multiplexer to output one of the following results through the SO pin (11):

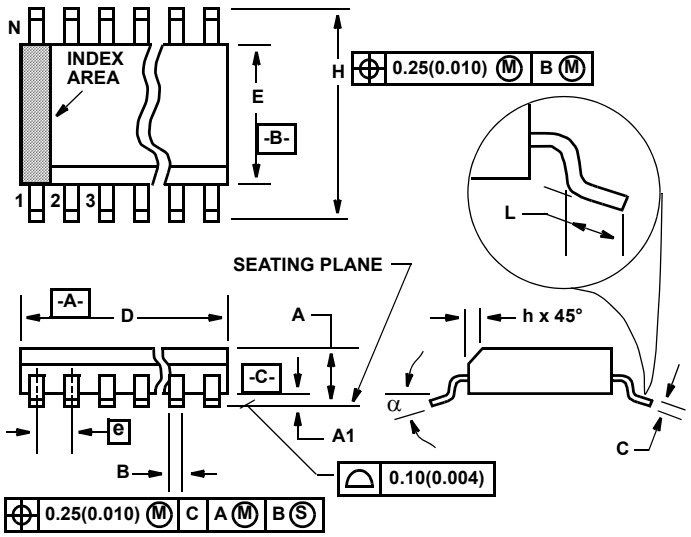
1. Value of one of the five registers in the chip
2. Buffered value of the SI pin (12).
3. Value of an internal comparator used to rectify the analog signal

A digital SPI filter is located in the SPI Block which provides a pseudo noise immunity characteristic.

The digital SPI filter operation requires that the SCK be low prior to the fall of $\overline{CS}$, followed by 8 SCK pulses (low-high-low transitions). With the SCK ending the pulse sequence in a logic low condition, the transition of $\overline{CS}$ from a low to high transition will cause the data-word in the SPI Buffer to be loaded into the proper addressed programmable register.

During the Integration mode, INT/$\overline{HOLD}$ pin is high, any single SPI byte that is entered will be acted upon if the conditions of the digital SPI filter are met. The digital SPI filter allows for only 8 bits per word to be accepted.

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.014	0.019	0.35	0.49	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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