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July 2000 File Number 4774.2

Multiple Linear Power Controller with ACPI Control Interface

The HIP6500 complements either an HIP6020 or an HIP6021 in ACPI-compliant designs for microprocessor and computer applications. The IC integrates two linear controllers and two regulators, switching, monitoring and control functions into a 20-pin SOIC package. One linear controller generates the $3.3V_{DUAL}$ voltage plane from the ATX supply's 5VSB output, powering the PCI slots through an external pass transistor during sleep states (S3, S4/S5). A second transistor is used to switch in the ATX 3.3V output for operation during S0 and S1/S2 (active) operating states. The second linear controller supplies the computer system's 2.5V/3.3V memory power through an external pass transistor in active states. During S3 state, an integrated pass transistor supplies the 2.5V/3.3V sleep power. A third controller powers up the $5V_{DUAL}$ plane by switching in the ATX 5V output in active states, and the ATX 5VSB in sleep states. The two internal regulators consist of a low current 3.3V sleep output and a dedicated, noise-free 2.5V clock chip supply. The HIP6500's operating mode (active outputs or sleep outputs) is selectable through two digital control pins, $\overline{S3}$ and $\overline{S5}$. Further control of the logic governing activation of different power states is offered through two configuration pins, $\overline{EN3VDL}$ and EN5VDL. In active state, the $3.3V_{DUAL}$ linear regulator uses an external N-Channel pass MOSFET to connect the output directly to the 3.3V input supplied by an ATX (or equivalent) power supply, for minimal losses. In sleep state, power delivery on the $3.3V_{DUAL}$ output is transferred to an NPN transistor, also external to the controller. Active state power delivery for the $2.5/3.3V_{MEM}$ output is performed through an external NPN transistor, or an NMOS switch for the 3.3V setting. In sleep state, conduction on this output is transferred to an internal pass transistor. The $5V_{DUAL}$ output is powered through two external MOS transistors. In sleep states, a PMOS (or PNP) transistor conducts the current from the ATX 5VSB output; while in active state, current flow is transferred to an NMOS transistor connected to the ATX 5V output. Similar to the $3.3V_{DUAL}$ output, the operation of the $5V_{DUAL}$ output is dictated not only by the status of the $\overline{S3}$ and $\overline{S5}$ pins, but that of the EN5VDL pin as well. The $3.3V_{SB}$ internal regulator is active for as long as the ATX 5VSB voltage is applied to the chip, and derives its output current from the 5VSB pin. The $2.5V_{CLK}$ output is only active during S0 and S1/S2, and uses the 3V3 pin as input source for its internal pass element.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HIP6500CB	0 to 70	20 Ld SOIC	M20.3
HIP6500EVAL1	Evaluation Board		

Features

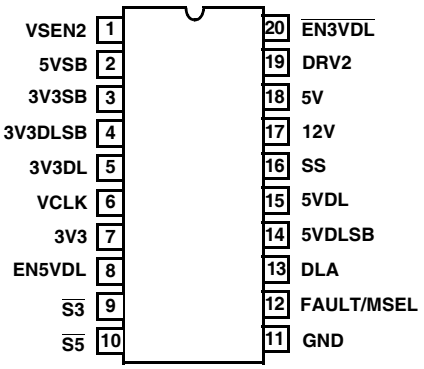
- Provides 5 ACPI-Controlled Voltages
  - 5V Active/Sleep ($5V_{DUAL}$)
  - 3.3V Active/Sleep ($3.3V_{DUAL}$)
  - 2.5V/3.3V Active/Sleep ($2.5V_{MEM}$)
  - 3.3V Always Present ($3.3V_{SB}$)
  - 2.5V Clock (Active Only) ($2.5V_{CLK}$)
- Excellent Output Voltage Regulation
  - $3.3V_{DUAL}$ Output: ±2.0% Over Temperature; Sleep State Only
  - $2.5V/3.3V_{MEM}$ Output: ±2.0% Over Temperature; Both Operational States (3.3V setting in sleep only)
  - $2.5V_{CLK}$ and $3.3V_{SB}$ Output: ±2.0% Over Temperature
- Small Size
  - Very Low External Component Count
- Selectable Memory Output Voltage Via FAULT/MSEL Pin
  - 2.5V for RDRAM Memory
  - 3.3V for SDRAM Memory
- Under-Voltage Monitoring of All Outputs with Centralized FAULT Reporting and Temperature Shutdown

Applications

- Motherboard Power Regulation for ACPI-Compliant Computers

Pinout

HIP6500
(SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Block Diagram

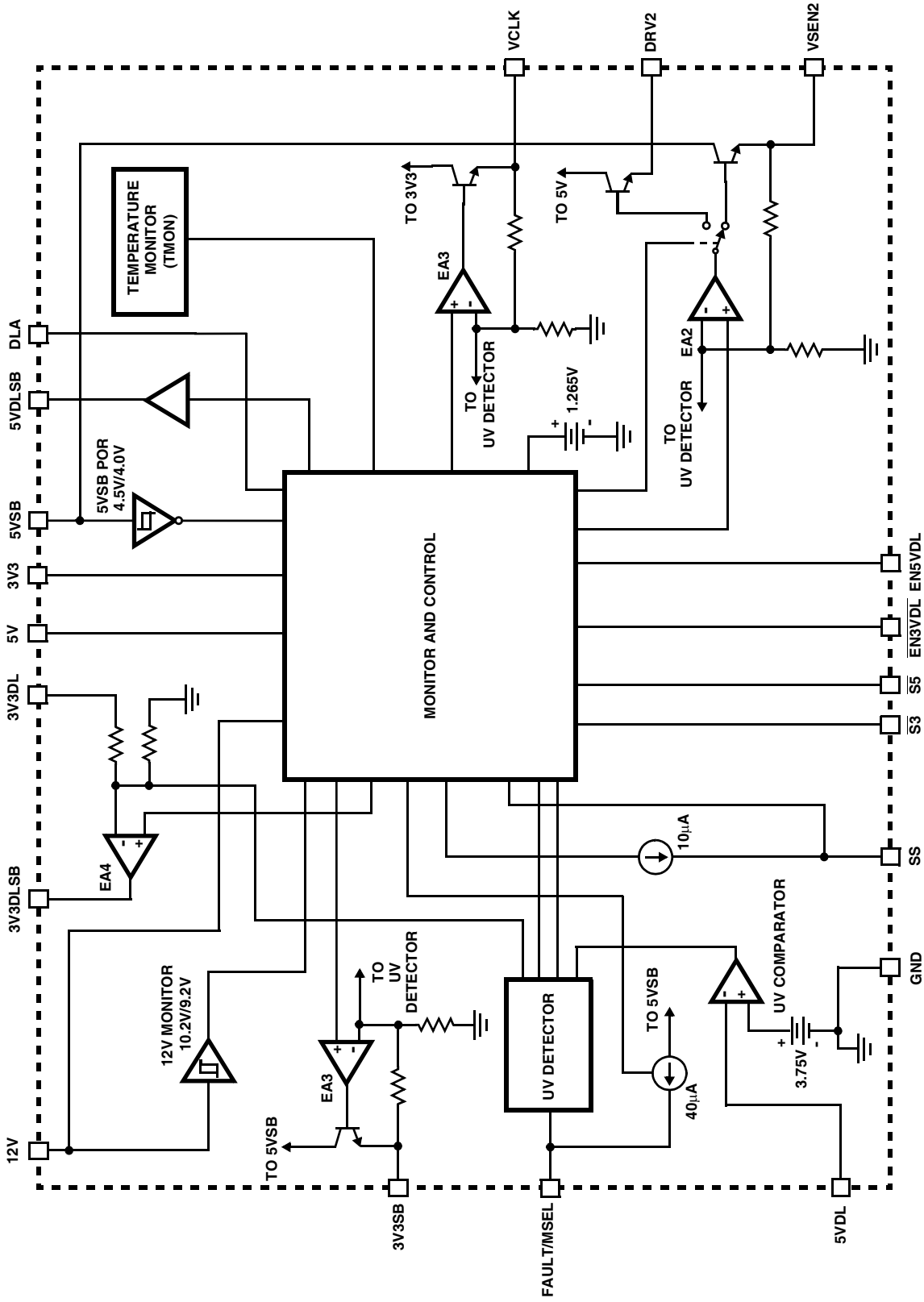


FIGURE 1.

Simplified Power System Diagram

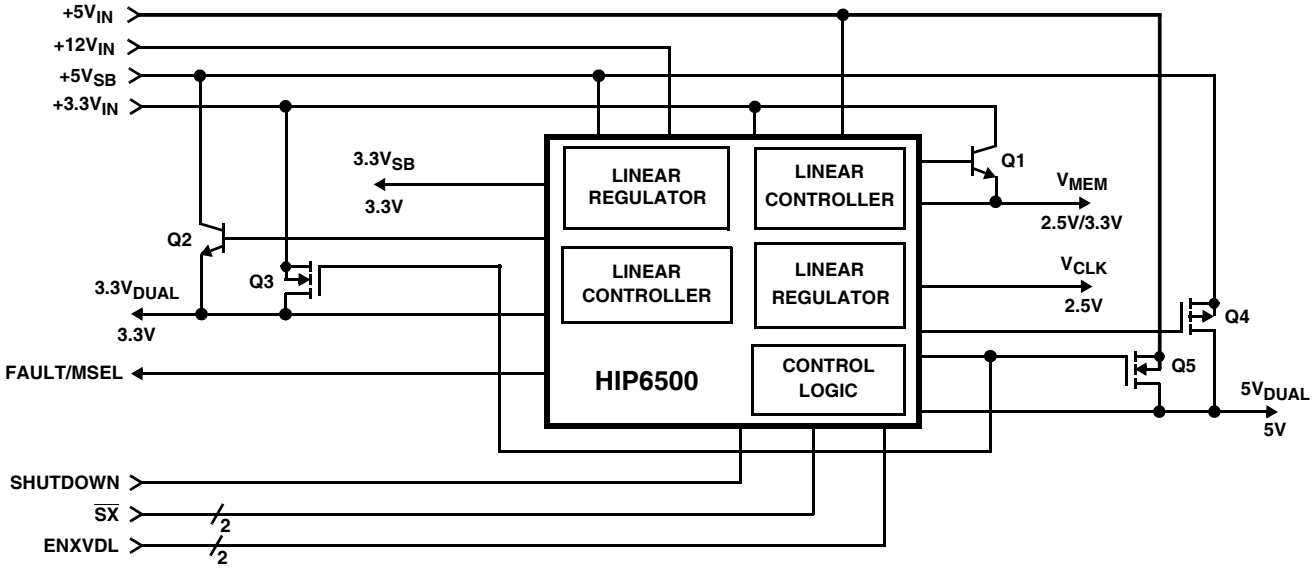


FIGURE 2.

Typical Application

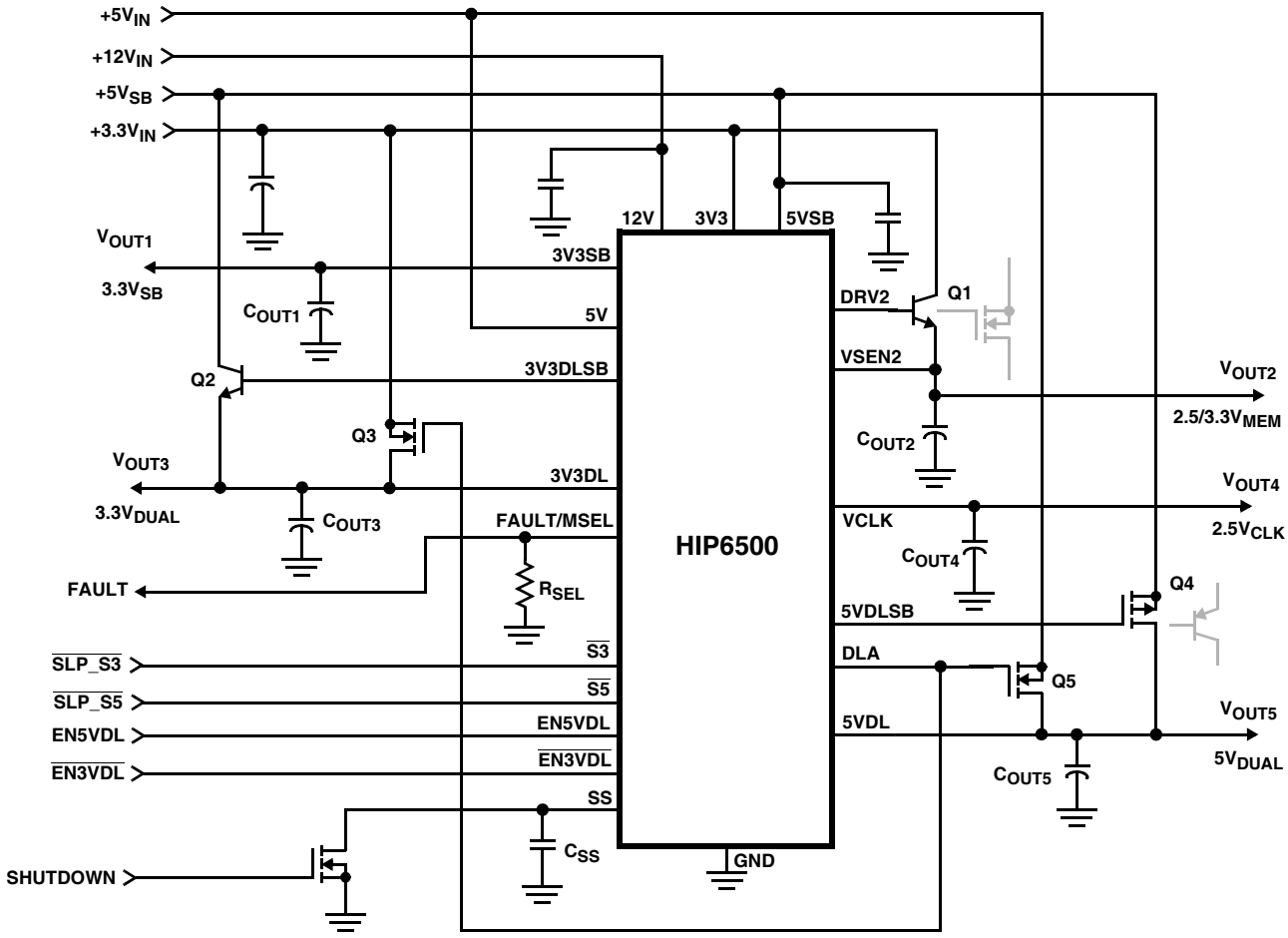


FIGURE 3.

Absolute Maximum Ratings

Supply Voltage, V_{5VSB} . . . . . +7.0V
12V. . . . . GND - 0.3V to +14.5V
DLA, DRV2 . . . . . GND - 0.3V to V_{12V} +0.3V
All Other Pins. . . . . GND - 0.3V to 5VSB + 0.3V
ESD Classification . . . . . Class 3

Recommended Operating Conditions

Supply Voltage, V_{5VSB} . . . . . +5V ±±5%
Digital Inputs, $V_{\overline{SX}}$, V_{EN5VDL}, $V_{\overline{EN3VDL}}$ . . . . . .0 to +5.25V
Ambient Temperature Range. . . . . 0^oC to 70^oC
Junction Temperature Range . . . . . 0^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	85

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted Refer to Figures 1, 2 and 3

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply Current	I_{5VSB}		-	30	-	mA
Shutdown Supply Current	$I_{5VSB(OFF)}$	V_{SS} = 0.8V	-	14	-	mA
POWER-ON RESET, SOFT-START, AND VOLTAGE MONITORS						
Rising 5VSB POR Threshold			-	-	4.5	V
5VSB POR Hysteresis			-	0.2	-	V
Rising 12V Threshold			-	-	10.2	V
12V Hysteresis			-	1.0	-	V
Rising 3V3 and 5V Thresholds			-	90	-	%
3V3 and 5V Hysteresis			-	5	-	%
Soft-Start Current	I_{SS}		-	10	-	µA
Shutdown Voltage Threshold	V_{SD}		-	-	0.8	V
3.3V_{SB} LINEAR REGULATOR (V_{OUT1})						
Regulation			-	-	2.0	%
3V3SB Nominal Voltage Level	V_{3V3SB}		-	3.3	-	V
3V3SB Undervoltage Rising Threshold			-	2.77	-	V
3V3SB Undervoltage Hysteresis			-	110	-	mV
3V3SB Output Current	I_{3V3SB}	5VSB = 5V	250	300	-	mA
2.5/3.3V_{MEM} LINEAR REGULATOR (V_{OUT2})						
Regulation			-	-	2.0	%
VSEN2 Nominal Voltage Level	V_{VSEN2}	R_{SEL} = 1kΩ	-	2.5	-	V
VSEN2 Nominal Voltage Level	V_{VSEN2}	R_{SEL} = 10kΩ	-	3.3	-	V
VSEN2 Undervoltage Rising Threshold			-	83	-	%
VSEN2 Undervoltage Hysteresis (Note 2)			-	3	-	%
VSEN2 Output Current	I_{VSEN2}	5VSB = 5V	250	300	-	mA
DRV2 Output Drive Current	I_{DRV2}	5VSB = 5V, R_{SEL} = 1kΩ	220	-	-	mA
DRV2 Output Impedance		R_{SEL} = 10kΩ	-	200	-	Ω

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted Refer to Figures 1, 2 and 3 **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
3.3V$_{DUAL}$ LINEAR REGULATOR (V$_{OUT3}$)						
Sleep State Regulation			-	-	2.0	%
3V3DL Nominal Voltage Level	V_{3V3DL}		-	3.3	-	V
3V3DL Undervoltage Rising Threshold			-	2.77	-	V
3V3DL Undervoltage Hysteresis			-	110	-	mV
3V3DLSB Output Drive Current	$I_{3V3DLSB}$	5VSB = 5V	5	8.5	-	mA
DLA Output Impedance			-	90	-	Ω
2.5V$_{CLK}$ LINEAR REGULATOR (V$_{OUT4}$)						
Regulation			-	-	2.0	%
VCLK Nominal Voltage Level	V_{VCLK}		-	2.5	-	V
VCLK Undervoltage Rising Threshold			-	2.10	-	V
VCLK Undervoltage Hysteresis			-	80	-	mV
VCLK Output Current (Note 3)	I_{VCLK}	V_{3V3} = 3.3V	500	800	-	mA
5V$_{DUAL}$ SWITCH CONTROLLER (V$_{OUT5}$)						
5VDL Undervoltage Rising Threshold			-	4.22	-	V
5VDL Undervoltage Hysteresis			-	170	-	mV
5VDLSB Output Drive Current	I_{5VDLSB}	5VDLSB = 4V, 5VSB = 5V	-20	-	-40	mA
5VDLSB Pull-up Impedance to 5VSB			-	350	-	Ω
TIMING INTERVALS						
Active State Assessment Past Input UV Thresholds (Note 4)			20	25	30	ms
Active-to-Sleep Control Input Delay			-	200	-	µs
CONTROL I/O ($\overline{S3}$, $\overline{S5}$, $\overline{EN3VDL}$, EN5VDL, FAULT/MSEL)						
High Level Input Threshold			-	-	2.2	V
Low Level Input Threshold			0.8	-	-	V
$\overline{S3}$, $\overline{S5}$ Internal Pull-Up Impedance to 5VSB			-	70	-	kΩ
FAULT Output Impedance		FAULT = high	-	100	-	Ω
TEMPERATURE MONITOR						
Fault-Level Threshold (Note 5)			140	-	-	°C
Shutdown-Level Threshold (Note 5)			-	155	-	°C

NOTES:

2. Valid for 3.3V setting only.
3. At ambient temperatures less than 50°C.
4. Guaranteed by correlation.
5. Guaranteed by design.

Functional Pin Description

3V3 (Pin 7)

Connect this pin to the ATX 3.3V output. This pin provides the output current for the 2V5CLK pin, and is monitored for power quality.

5VSB (Pin 2)

Provide a very well de-coupled 5V bias supply for the IC to this pin by connecting it to the ATX 5VSB output. This pin provides the output current for the 3V3SB and VSEN2 pins, as well as the base current for Q2. The voltage at this pin is monitored for power-on reset (POR) purposes.

5V (Pin 18)

Connect this pin to the ATX 5V output. This pin provides the base bias current for Q1, and is monitored for power quality.

12V (Pin 17)

Connect this pin to the ATX 12V output. This pin provides the gate bias voltage for Q3 and Q5, and is monitored for power quality.

GND (Pin 11)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

$\overline{S3}$ and $\overline{S5}$ (Pins 9 and 10)

These pins switch the IC's operating state from active (S0, S1/S2) to S3 and S4/S5 sleep states. These are digital inputs featuring internal 50kΩ (typical) resistor pull-ups to 5VSB. Internal circuitry de-glitches these pins for disturbances lasting as long as 2μs (typically). Additional circuitry blocks any illegal state transitions (such as S3 to S4/S5 or vice versa). Respectively, connect $\overline{S3}$ and $\overline{S5}$ to the computer system's $\overline{SLP_S3}$ and $\overline{SLP_S5}$ signals.

$\overline{EN3VDL}$ and EN5VDL (Pins 20 and 8)

These pins control the logic governing the dual outputs' behavior in response to S3 and S4/S5 requests. These are digital inputs whose status can only be changed during active states operation or during chip shutdown (SS pin grounded by external open-drain device or chip bias below POR level). The input information is latched-in when entering a sleep state, as well as following 5VSB POR release or exit from shutdown. $\overline{EN3VDL}$ features an internal 50kΩ pull-down resistor, while EN5VDL is internally pulled high through a similar resistor.

FAULT/MSEL (Pin 12)

This is a multiplexed function pin allowing the setting of the memory output voltage to either 2.5V or 3.3V (for RDRAM or SDRAM memory systems). In case of an undervoltage on any of the outputs or on any of the monitored ATX outputs, or in case of an overtemperature event, this pin is used to report the fault condition by being pulled to 5VSB.

SS (Pin 16)

Connect this pin to a small ceramic capacitor (no less than 5nF; 0.1μF recommended). The internal soft-start (SS) current source along with the external capacitor creates a voltage ramp used to control the ramp-up of the output voltages. Pulling this pin low with an open-drain device shuts down all the outputs as well as forces the FAULT pin low. The C_{SS} capacitor is also used to provide a controlled voltage slew rate during active-to-sleep transitions on the $3.3V_{DUAL}$, and V_{MEM} outputs.

VSEN2 (Pin 1)

Connect this pin to the memory output (V_{OUT2}). In sleep states, this pin is regulated to 2.5V or 3.3V (based on R_{SEL}) through an internal pass transistor capable of delivering 300mA (typically). When V_{OUT2} is programmed to 2.5V, the active-state voltage at this pin is regulated through an external NPN transistor connected at the DRV2 pin. For the 3.3V setting, the ATX 3.3V is passed to this pin through a fully on external N-MOS transistor. During all operating states, the voltage at this pin is monitored for under-voltage events.

DRV2 (Pin 19)

For the 2.5V RDRAM systems connect this pin to the base of a suitable NPN transistor. This pass transistor regulates the 2.5V output from the ATX 3.3V during active states operation. For 3.3V SDRAM systems connect this pin to the gate of a suitable N-MOS transistor; this transistor is used to switch in the ATX 3.3V output.

3V3DL (Pin 5)

Connect this pin to the 3.3V dual output (V_{OUT3}). In sleep states, the voltage at this pin is regulated to 3.3V; in active states, ATX 3.3V output is delivered to this node through a fully on N-MOS transistor. During all operating states, this pin is monitored for under-voltage events.

3V3DLSB (Pin 4)

Connect this pin to the base of a suitable NPN transistor. In sleep state, this transistor is used to regulate the voltage at the 3V3DL pin to 3.3V.

DLA (Pin 13)

Connect this pin to the gates of suitable N-MOSFETs, which in active state, switch in the ATX 3.3V and 5V outputs into the $3.3V_{DUAL}$ and $5V_{DUAL}$ outputs, respectively.

5VDL (Pin 15)

Connect this pin to the $5V_{DUAL}$ output (V_{OUT5}). In either operating state, the voltage at this pin is provided through a fully on MOS transistor. This pin is also monitored for under-voltage events.

5VDLSB (Pin 14)

Connect this pin to the gate of a suitable P-MOSFET or bipolar PNP. In sleep state, this transistor is switched on, connecting the ATX 5VSB output to the $5V_{DUAL}$ regulator output.

3V3SB (Pin 3)

This pin is the output of the internal $3.3V_{SB}$ regulator (V_{OUT1}). This internal regulator operates continuously for as long as the 5VSB bias voltage is applied to the HIP6500. This pin is monitored for under-voltage events.

VCLK (Pin 6)

This pin is the output of the internal 2.5V clock chip regulator (V_{OUT4}). This internal regulator operates only in active states (S0, S1/S2) and is shut off during any sleep state, regardless of the configuration of the chip. This pin is monitored for under-voltage events.

Description

Operation

The HIP6500 controls 5 output voltages (Refer to Figures 1, 2, and 3). It is designed for microprocessor computer applications with 3.3V, 5V, 5VSB, and 12V bias input from an ATX power supply. The IC is composed of two linear controllers supplying the PCI slots' $3.3V_{AUX}$ power (V_{OUT3}) and the 2.5V RDRAM or 3.3V SDRAM memory power (V_{OUT2}), two linear regulators providing an always-present $3.3V_{SB}$ (V_{OUT1}), and a dedicated 2.5V clock chip supply (V_{OUT4}), a dual switch controller supplying the $5V_{DUAL}$ voltage (V_{OUT5}), as well as all the control and monitoring functions necessary for complete ACPI implementation.

Initialization

The HIP6500 automatically initializes upon receipt of input power. The Power-On Reset (POR) function continually monitors the 5VSB input supply voltage, initiating $3.3V_{SB}$ soft-start operation after exceeding POR threshold. At 3ms (typically) after $3.3V_{SB}$ finishes its ramp-up, the ENxVDL status and the memory voltage (V_{MEM}) setting are latched in and the chip proceeds to ramp up the remainder of the voltages, as required.

Operational Truth Tables

The $\overline{\text{EN3VDL}}$ and EN5VDL pins offer a choice of 4 configurations in terms of the overall system architecture and supported features. Tables 1-3 describe the truth combinations pertaining to each of the three outputs.

TABLE 1. $3.3V_{DUAL}$ OUTPUT (V_{OUT3}) TRUTH TABLE

$\overline{\text{EN3VDL}}$	$\overline{\text{S5}}$	$\overline{\text{S3}}$	3V3DL	COMMENTS
0	1	1	3.3V	S0, S1 States (Active)
0	1	0	3.3V	S3
0	0	1	Note	Maintains Previous State
0	0	0	3.3V	S4/S5
1	1	1	3.3V	S0, S1 States (Active)
1	1	0	3.3V	S3
1	0	1	Note	Maintains Previous State
1	0	0	0V	S4/S5

NOTE: Combination Not Allowed.

As seen in Table 1, $\overline{\text{EN3VDL}}$ simply controls whether the 3.3VDUAL plane remains powered up during S4/S5 sleep state.

TABLE 2. $5V_{DUAL}$ OUTPUT (V_{OUT5}) TRUTH TABLE

EN5VDL	$\overline{\text{S5}}$	$\overline{\text{S3}}$	5VDL	COMMENTS
0	1	1	5V	S0, S1 States (Active)
0	1	0	0V	S3
0	0	1	Note	Maintains Previous State
0	0	0	0V	S4/S5
1	1	1	5V	S0, S1 States (Active)
1	1	0	5V	S3
1	0	1	Note	Maintains Previous State
1	0	0	5V	S4/S5

NOTE: Combination Not Allowed.

Similarly, Table 2 details the fact that EN5VDL status controls whether the $5V_{DUAL}$ plane supports the S3-S5 sleep states.

TABLE 3. $2.5/3.3V_{MEM}$ OUTPUT (V_{OUT2}) TRUTH TABLE

R_{SEL}	$\overline{\text{S5}}$	$\overline{\text{S3}}$	$2.5/3.3V_{MEM}$	COMMENTS
1kΩ	1	1	2.5V	S0, S1 States (Active)
1kΩ	1	0	2.5V	S3
1kΩ	0	1	Note	Maintains Previous State
1kΩ	0	0	0V	S5
10kΩ	1	1	3.3V	S0, S1 States (Active)
10kΩ	1	0	3.3V	S3
10kΩ	0	1	Note	Maintains Previous State
10kΩ	0	0	0V	S5

NOTE: Combination Not Allowed.

As seen in Table 3, $2.5/3.3V_{MEM}$ output is maintained in S3 (suspend to RAM) sleep state only. The dual-voltage support accommodates both SDRAM as well as RDRAM type memories.

Not shown in any of the tables are the $3.3V_{SB}$ and the $2.5V_{CLK}$ outputs. The $3.3V_{SB}$ output powers up as soon as the 5VSB ATX output is available. The $2.5V_{CLK}$ output operation is restricted by the chip's POR and is only available in active state (S0, S1). For additional information, see the soft-start sequence diagrams.

Additionally, the internal circuitry does not allow the transition from an S3 (suspend to RAM) state to an S4/S5 (suspend to disk/soft off) state or vice versa. The only 'legal' transitions are from an active state (S0, S1) to a sleep state (S3, S5) and vice versa.

Functional Timing Diagrams

Figures 4 through 8 are timing diagrams, detailing the power up/down sequences of all three outputs in response to the status of the enable ($\overline{EN3VDL}$, EN5VDL) and sleep-state pins ($\overline{S3}$, $\overline{S5}$), as well as the status of the ATX supply.

The status of the $\overline{EN3VDL}$ and EN5VDL pins can only be changed while in active (S0, S1) states, when the bias supply (5VSB pin) is below POR level, or during chip shutdown (SS pin shorted to GND); a status change of these two pins while in a sleep state is ignored.

Not shown in these diagrams is the deglitching feature used to protect against false sleep state tripping. Both $\overline{S3}$ and $\overline{S5}$ pins are protected against noise by a 2µs filter (typically 1 - 4µs). This feature is useful in noisy computer environments if the control signals have to travel over significant distances. Additionally, the $\overline{S3}$ pin features a 200µs delay in transitioning to sleep states. Once the $\overline{S3}$ pin goes low, an internal timer is activated. At the end of the 200µs interval, if the $\overline{S5}$ pin is low, the HIP6500 switches into S5 sleep state; if the $\overline{S5}$ pin is high, the HIP6500 goes into S3 sleep state.

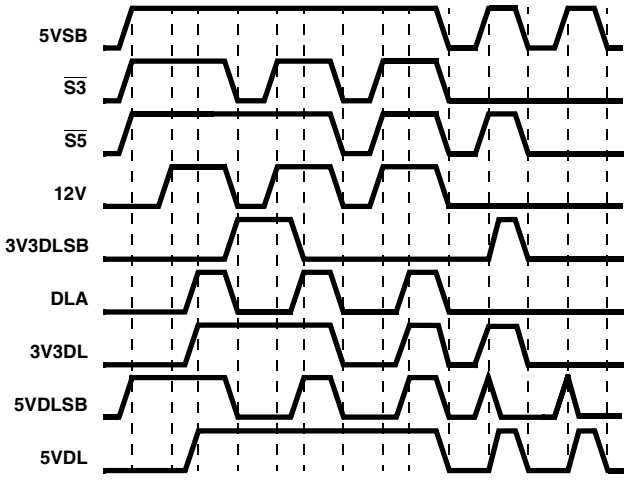


FIGURE 4. $3V_{DUAL}$ AND $5V_{DUAL}$ TIMING DIAGRAM FOR $\overline{EN3VDL}$ = 1, EN5VDL = 1

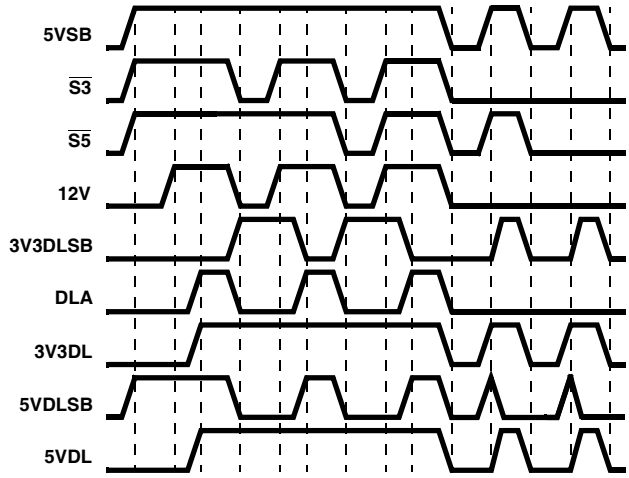


FIGURE 6. $3V_{DUAL}$ AND $5V_{DUAL}$ TIMING DIAGRAM FOR $\overline{EN3VDL}$ = 0, EN5VDL = 1

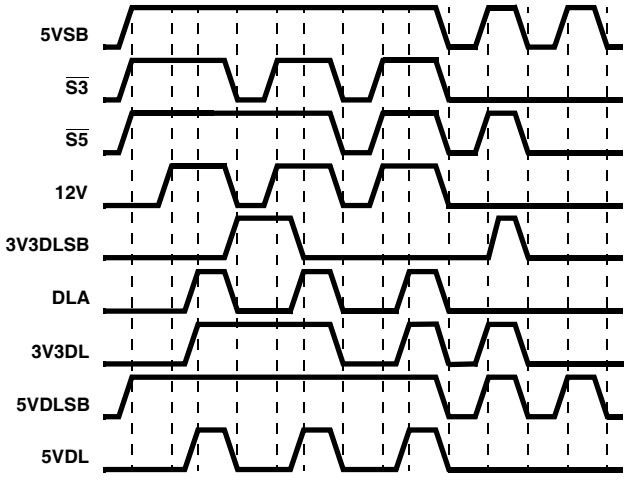


FIGURE 5. $3V_{DUAL}$ AND $5V_{DUAL}$ TIMING DIAGRAM FOR $\overline{EN3VDL}$ = 1, EN5VDL = 0

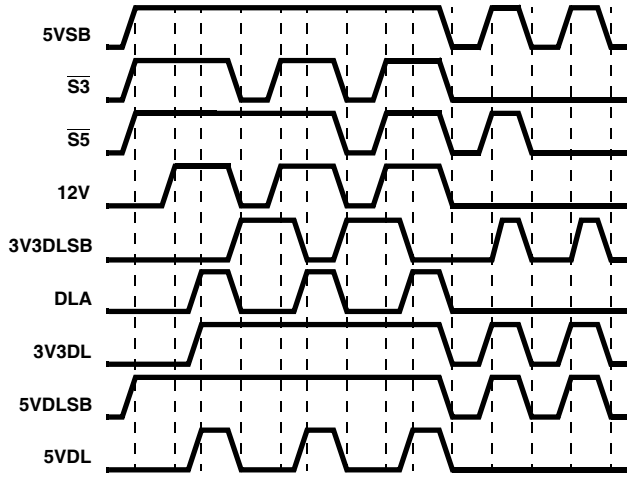


FIGURE 7. $3V_{DUAL}$ AND $5V_{DUAL}$ TIMING DIAGRAM FOR $\overline{EN3VDL}$ = 0, EN5VDL = 0

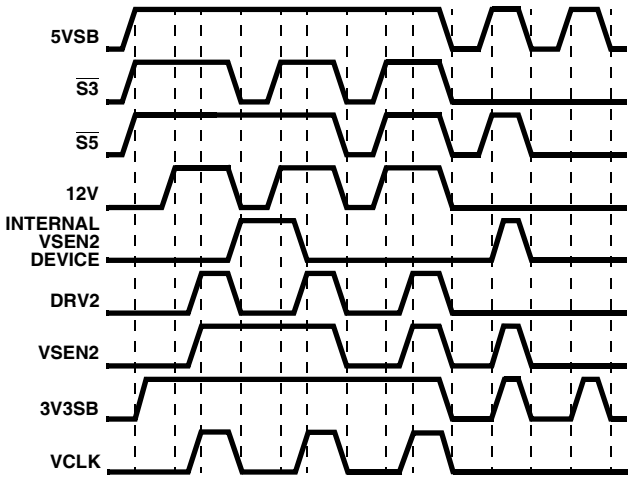


FIGURE 8. 2.5/3.3V_{MEM}, 3.3V_{SB} AND VCLK TIMING DIAGRAM

Soft-Start Circuit

SOFT-START INTO SLEEP STATES (S3, S4/S5)

The 5VSB POR function initiates the soft-start sequence. An internal 10µA current source charges an external capacitor. The error amplifiers reference inputs are clamped to a level proportional to the SS (soft-start) pin voltage. As the SS pin voltage slews from about 1.25V to 2.5V, the input clamp allows a rapid and controlled output voltage rise.

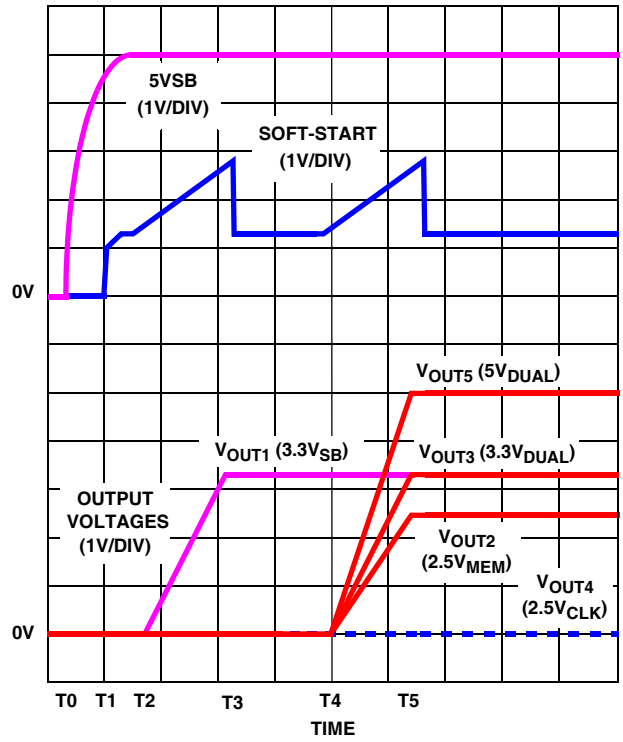


FIGURE 9. SOFT-START INTERVAL IN A SLEEP STATE (ALL OUTPUTS ENABLED)

Figure 9 shows the soft-start sequence for the typical application start-up in sleep state with all output voltages enabled. At time T0 5VSB (bias) is applied to the circuit. At time T1 the 5VSB surpasses POR level. An internal fast charge circuit quickly raises the SS capacitor voltage to approximately 1V, then the 10µA current source continues the charging. The soft-start capacitor voltage reaches approximately 1.25V at time T2, at which point the 3.3V_{SB} error amplifiers' reference input starts its transition, causing the output voltage to ramp up proportionally. The ramp-up continues until time T3 when the 3.3V_{SB} voltage reaches the set value. After the 3.3V_{SB} reached its set value, as the soft-start capacitor voltage reaches approximately 2.75V, the under-voltage monitoring circuit of this output is activated and the soft-start capacitor is quickly discharged to approximately 1.25V. Following the 3ms (typical) time-out between T3 and T4, the memory and enabling pins' selection are latched in, and the soft-start capacitor commences a second ramp-up designed to smoothly bring up the remainder of the voltages required by the system. At time T5 all voltages are within regulation limits, and as the SS voltage reaches 2.75V, all the UV monitors are activated and the SS capacitor is quickly discharged to 1.25V, where it remains until the next transition.

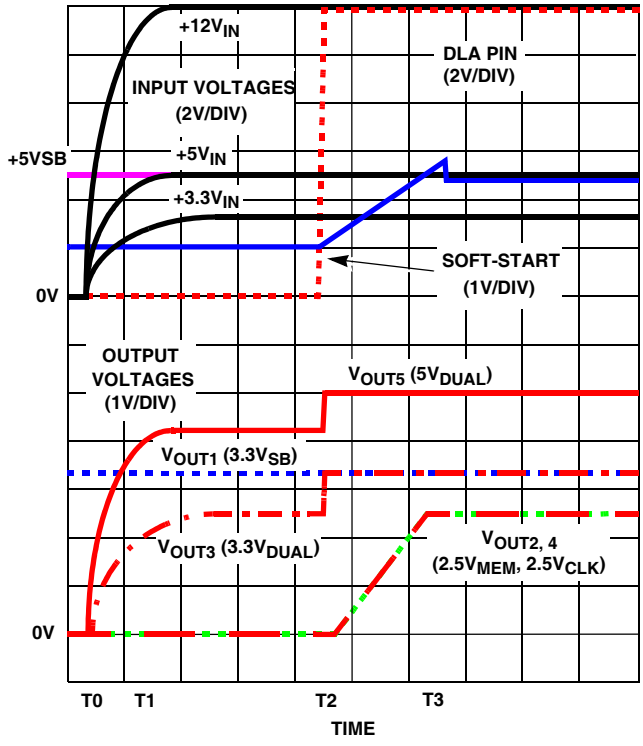


FIGURE 10. SOFT-START INTERVAL IN ACTIVE STATE (2.5/3.3V_{MEM} OUTPUT SHOWN IN 2.5V SETTING)

SOFT-START INTO ACTIVE STATES (S0, S1)

If both $\overline{S3}$ and $\overline{S5}$ are logic high at the time the 5VSB is applied, the HIP6500 will assume active state wake-up and keep off the controlled external transistors and the VCLK output until some time (typically 25ms) after the ATX's main outputs used by the application (3.3V, 5V, and 12V) exceed the set thresholds. This time-out feature is necessary in order to insure the main ATX outputs are stabilized. The time-out also assures smooth transitions from sleep into active when sleep states are being supported. $3.3V_{SB}$ output, whose operation is only dependent on 5VSB presence, will come up right as bias voltage reaches POR level.

During sleep to active state transitions from conditions where the outputs are initially 0V (such as S5 to S0 transition with $\overline{EN3VDL}$ = 1 and EN5VDL = 0, or simple power-up sequence directly into active state), the $3V_{DUAL}$ and $5V_{DUAL}$ outputs go through a quasi soft-start by being pulled high through the body diodes of the N-Channel MOSFETs connected between these outputs and the 3.3V and 5V ATX outputs. Figure 10 shows this start-up.

5VSB is already present when the main ATX outputs are turned on at time T0. As a result of $+3.3V_{IN}$ and $+5V_{IN}$ ramping up, the $3.3V_{DUAL}$ and $5V_{DUAL}$ output capacitors charge up through the body diodes of Q3 and Q5, respectively (see Figure 3). At time T1, all main ATX outputs exceed the HIP6500's undervoltage thresholds, and the internal 25ms (typical) timer is initiated. At T2 the time-out initiates a soft-start, and the memory and clock outputs are ramped-up, reaching regulation limits at time T3. Simultaneous with the beginning of the memory and clock voltage ramp-up, at time T2, the DLA pin is pulled high, turning on Q3 and Q5 in the process, and bringing the $3.3V_{DUAL}$ and $5V_{DUAL}$ outputs in regulation. Shortly after time T3, as the SS voltage reaches 2.75V, the soft-start capacitor is quickly discharged down to approximately 2.45V, where it remains until a valid sleep state request is received from the system.

Fault Protection

All the outputs are monitored against undervoltage events. A severe overcurrent caused by a failed load on any of the outputs, would, in turn, cause that specific output to suddenly drop. If any of the output voltages drop below 80% (typical) of their set value, such event is reported by having the FAULT/MSEL pin pulled to 5V. Additionally, exceeding the maximum current rating of an integrated regulator (output with pass regulator on chip) can lead to output voltage drooping; if excessive, this droop can ultimately trip the under-voltage detector and send a FAULT signal to the computer system.

A FAULT condition occurring on an output when controlled through an external pass transistor will only set off the FAULT flag, and it will not shut off or latch off any part of the circuit. A FAULT condition occurring on an output when controlled through an internal pass transistor, will set off the FAULT flag, and it will shut off the faulting regulator only. If shutdown or latch off of the entire circuit is desired in case of a fault, regardless of the cause, this can be achieved by externally pulling or latching the SS pin low. Pulling the SS pin low will also force the FAULT pin to go low and reset an internally latched-off output.

Special consideration is given to the initial start-up sequence. If, following a 5VSB POR event, the $3.3V_{SB}$ output is ramped up and is subject to an undervoltage event before the remainder of the controlled voltages have been brought up, then the FAULT output goes high and the entire IC latches off. Latch-off condition can be reset by cycling the bias power (5VSB). Undervoltage events on the $3.3V_{SB}$ output at any other times are handled according to the description found in the second paragraph under the current heading.

Another condition that could set off the FAULT flag is chip over-temperature. If the HIP6500 reaches an internal temperature of $140^{o}C$ (typical), the FAULT flag is set off, but the chip continues to operate until the temperature reaches $155^{o}C$ (typical), when unconditional shutdown of all outputs takes place. Operation resumes at $140^{o}C$ and the temperature cycling occurs until the fault-causing condition is removed.

Output Voltages

The output voltages are internally set and do not require any external components. Selection of the V_{MEM} memory voltage is done by means of an external resistor connected between the FAULT/MSEL pin and ground. An internal 40µA (typical) current source creates a voltage drop across this resistor. Following every $3.3V_{SB}$ ramp-up or chip reset (see Soft-Start Circuit), this voltage is compared with an internal reference and the setting is latched in. Based on this comparison, the output voltage is set at either 2.5V (R_{SEL} = 1kΩ), or 3.3V (R_{SEL} = 10kΩ). It is very important that no capacitor is connected to the FAULT/MSEL pin; the presence of a capacitive element at this pin can lead to false memory voltage selection. See Figure 11 for details.

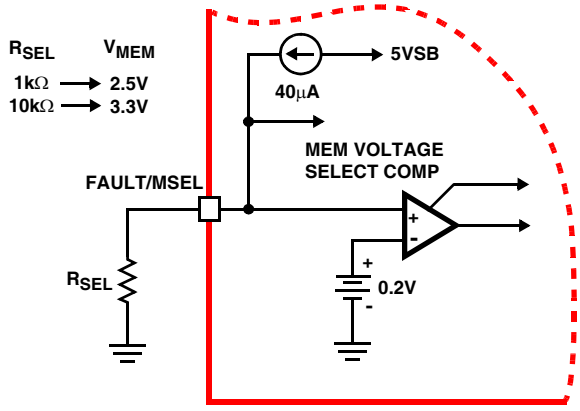


FIGURE 11. 2.5/3.3V_{MEM} OUTPUT VOLTAGE SELECTION CIRCUITRY DETAILS

Application Guidelines

Soft-Start Interval

The 5VSB output of a typical ATX supply is capable of 725mA. During power-up in a sleep state, it needs to provide sufficient current to charge up all the output capacitors and simultaneously provide some amount of current to the output loads. Drawing excessive amounts of current from the 5VSB output of the ATX can lead to voltage collapse and induce a pattern of consecutive restarts with unknown effects on the system's behavior or health.

The built-in soft-start circuitry allows tight control of the slew-up speed of the output voltages controlled by the HIP6500, thus enabling power-ups free of supply drop-off events. Since the outputs are ramped up in a linear fashion, the current dedicated to charging the output capacitors can be calculated with the following formula:

$$I_{COUT} = \frac{I_{SS}}{C_{SS} \times V_{BG}} \times \Sigma(C_{OUT} \times V_{OUT})$$, where

I_{SS} - soft-start current (typically 10µA)

C_{SS} - soft-start capacitor

V_{BG} - bandgap voltage (typically 1.26V)

$\Sigma(C_{OUT} \times V_{OUT})$ - sum of the products between the capacitance and the voltage of an output (total charge delivered to all outputs).

Due to the various system timing events, it is recommended that the soft-start interval not be set to exceed 30ms.

Shutdown

In case of a FAULT condition that might endanger the computer system, or at any other time, all the HIP6500 outputs can be shut down by pulling the SS pin below the specified shutdown level (typically 0.8V) with an open drain or open collector device capable of sinking a minimum of 2mA. Pulling the SS pin low effectively shuts down all the pass elements. Upon release of the SS pin, the HIP6500 undergoes a new soft-start cycle and resumes normal operation in accordance to the ATX supply and control pins status.

Layout Considerations

The typical application employing a HIP6500 is a fairly straight forward implementation. Like with any other linear regulator, attention has to be paid to the few potentially sensitive small signal components, such as those connected to sensitive nodes or those supplying critical by-pass current.

The power components (pass transistors) and the controller IC should be placed first. The controller should be placed in a central position on the motherboard, closer to the memory load if possible, but not excessively far from the clock chip or the processor. Insure the VSEN2 connection is properly sized to carry 250mA without significant resistive losses; similar guideline applies to the VCLK output, which can deliver as much as 800mA (typical). As the current for the VCLK output is provided from the ATX 3.3V, the connection from the 3V3 pin to the 3.3V plane should be sized to carry the maximum clock output current while exhibiting negligible voltage losses. Similarly, the current for the $3.3V_{SB}$ output is provided from the 5VSB pin, and the output current on pin DRV2 from the 5V pin - for best results, insure these pins are connected to their respective sources through adequate traces. The pass transistors should be placed on pads capable of heatsinking matching the device's power dissipation. Where applicable, multiple via connections to a large internal plane can significantly lower localized device temperature rise.

Placement of the decoupling and bulk capacitors should follow a placement reflecting their purpose. As such, the high-frequency decoupling capacitors should be placed as close as possible to the load they are decoupling; the ones decoupling the controller close to the controller pins, the ones decoupling the load close to the load connector or the load itself (if embedded). Even though bulk capacitance (aluminum electrolytics or tantalum capacitors) placement is not as critical as the high-frequency capacitor placement, having these capacitors close to the load they serve is preferable.

The only critical small signal component is the soft-start capacitor, C_{SS}. Locate this component close to SS pin of the control IC and connect to ground through a via placed close to the capacitor's ground pad. Minimize any leakage current paths from SS node, since the internal current source is only 10µA.

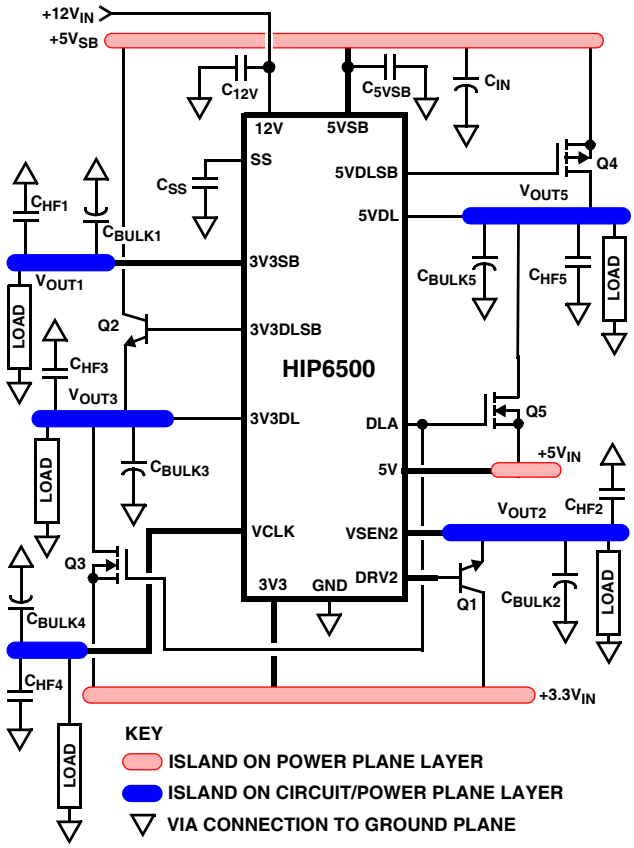


FIGURE 12. PRINTED CIRCUIT BOARD ISLANDS

A multi-layer printed circuit board is recommended. Figure 12 shows the connections of most of the components in the converter. Note that the individual capacitors each could represent numerous physical capacitors. Dedicate one solid layer for a ground plane and make all critical component ground connections through vias placed as close to the component terminal as possible. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Ideally, the power plane should support both the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers to create power islands connecting the filtering components (output capacitors) and the loads. Use the remaining printed circuit layers for small signal wiring.

Component Selection Guidelines

Output Capacitors Selection

The output capacitors for all outputs should be selected to allow the output voltage to meet the dynamic regulation requirements of active state operation (S0, S1). The load transient for the various microprocessor system's components may require high quality capacitors to supply the high slew rate (di/dt) current demands. Thus, it is recommended that the output capacitors be selected for transient load regulation, paying attention to their parasitic components (ESR, ESL).

Also, during the transition between active and sleep states, there is a short interval of time during which none of the power pass elements are conducting - during this time the output capacitors have to supply all the output current. The output voltage drop during this brief period of time can be easily approximated with the following formula:

$$\Delta V_{OUT} = I_{OUT} \times \left(ESR_{OUT} + \frac{t_t}{C_{OUT}} \right), \text{ where}$$

ΔV_{OUT} - output voltage drop

ESR_{OUT} - output capacitor bank ESR

I_{OUT} - output current during transition

C_{OUT} - output capacitor bank capacitance

t_t - active-to-sleep or sleep-to-active transition time (10µs typ.)

The output voltage drop is heavily dependent on the ESR (equivalent series resistance) of the output capacitor bank, the choice of capacitors should be such as to maintain the output voltage above the lowest allowable regulation level.

V_{CLK} (V_{OUT4}) Output Capacitors Selection

The output capacitor for the V_{CLK} linear regulator provides loop stability. Figure 13 outlines a capacitance vs. equivalent series resistance envelope. For stable operation and optimized performance, select a C_{OUT4} capacitor or combination of capacitors with characteristics within the shown envelope.

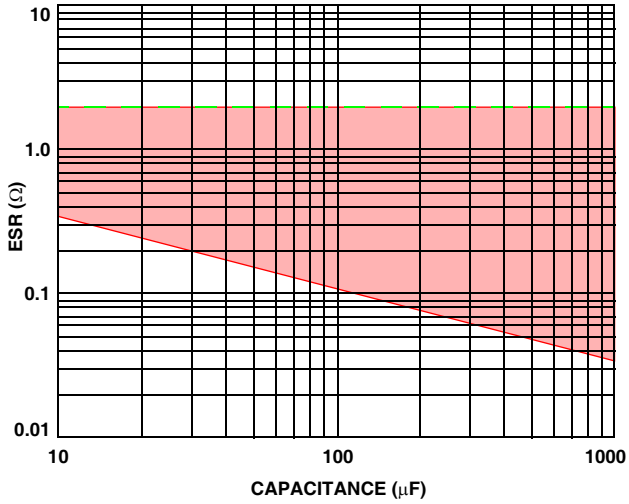


FIGURE 13. C_{OUT4} OUTPUT CAPACITOR

Input Capacitors Selection

The input capacitors for an HIP6500 application have to have a sufficiently low ESR as to not allow the input voltage to dip excessively when energy is transferred to the output capacitors. If the ATX supply does not meet the specifications, certain imbalances between the ATX's outputs and the HIP6500's regulation levels could have as a result a brisk transfer of energy from the input capacitors to

the supplied outputs. At the transition between active and sleep states, this phenomena could result in the 5VSB voltage dropping below the POR level (typically 4.1V) and temporarily disabling the HIP6500. The solution to a potential problem such as this is using larger input capacitors with a lower total combined ESR.

Transistor Selection/Considerations

The HIP6500 usually requires one P-Channel (or bipolar PNP), two N-Channel MOSFETs and two bipolar NPN transistors.

One important criteria for selection of transistors for all the linear regulators/switching elements is package selection for efficient removal of heat. The power dissipated in a linear regulator/switching element is

$$P_{LINEAR} = I_O \times (V_{IN} - V_{OUT})$$

Select a package and heatsink that maintains the junction temperature below the rating with the maximum expected ambient temperature.

Q1

The active element on the 2.5V/3.3V_{MEM} output has different requirements for each of the two voltage settings. In 2.5V systems utilizing RDRAM (or voltage-compatible) memory, Q1 has to be a bipolar NPN capable of conducting up to 7.5A and exhibit a current gain (h_{fe}) of minimum 40 at this current and 0.7V V_{CE}; in such systems the 2.5V output is actively regulated while in active state. In 3.3V systems (SDRAM or compatible) Q1 has to be an N-Channel MOSFET; in such systems the MOSFET is switched on during active state (S0, S1). The main criteria for the selection of this transistor is output voltage budgeting. The maximum $r_{DS(ON)}$ allowed at highest junction temperature can be expressed with the following equation:

$$r_{DS(ON)max} = \frac{V_{INmin} - V_{OUTmin}}{I_{OUTmax}}$$, where

V_{INmin} - minimum input voltage

V_{OUTmin} - minimum output voltage allowed

I_{OUTmax} - maximum output current

The gate bias available for this MOSFET is of the order of 8V.

Q5

If a P-Channel MOSFET is used to switch the 5VSB output of the ATX supply into the $5V_{DUAL}$ output during S3 and S5 states (as dictated by EN5VDL status), then, similar to the situation where Q1 is a MOSFET, the selection criteria of this device is also proper voltage budgeting. The maximum $r_{DS(ON)}$, however, has to be achieved with only 4.5V of V_{GS}, so a logic level MOSFET needs to be selected. If a PNP device is chosen to perform this function, it has to have a low saturation voltage while providing the maximum sleep current and have a current gain sufficiently high to be saturated using the minimum drive current (typically 20mA).

Q3,4

The two N-Channel MOSFETs are used to switch the 3.3V and 5V inputs provided by the ATX supply into the 3.3VDUAL and 5VDUAL outputs, respectively, while in active (S0, S1) state. Similar $r_{DS(ON)}$ criteria apply in these cases as well. Unlike the PMOS, however, these NMOS transistors get the benefit of an increased V_{GS} drive (approximately 8V and 7V, respectively).

Q2

The NPN transistor used as sleep state pass element (Q2) on the $3.3V_{DUAL}$ output has to have a minimum current gain of 100 at 1.5V V_{CE} and 500mA I_{CE} throughout the in-circuit operating temperature range.

HIP6500 Application Circuit

Figure 14 shows an application circuit of an ACPI-sanctioned power management system for a microprocessor computer system. The power supply provides the $3.3V_{SB}$ voltage (V_{OUT1}), the PCI $3.3V_{DUAL}$ voltage (V_{OUT3}), the RDRAM 2.5VMEM memory voltage (V_{OUT2}), the $2.5V_{CLK}$ clock voltage (V_{OUT4}), and the $5V_{DUAL}$ voltage (V_{OUT5}) from +3.3V, +5VSB, and +12VDC ATX supply outputs. For systems employing SDRAM memory, replace R1 with 10kΩ and Q1 with an HUF76113SK8. Q4 can also be a PNP, such as an MMBT2907AL. For detailed information on the circuit, including a Bill-of-Materials and circuit board description, see Application Note AN9862.

Also see Intersil Corporation's web page (http://www.intersil.com/tsc) for the latest information.

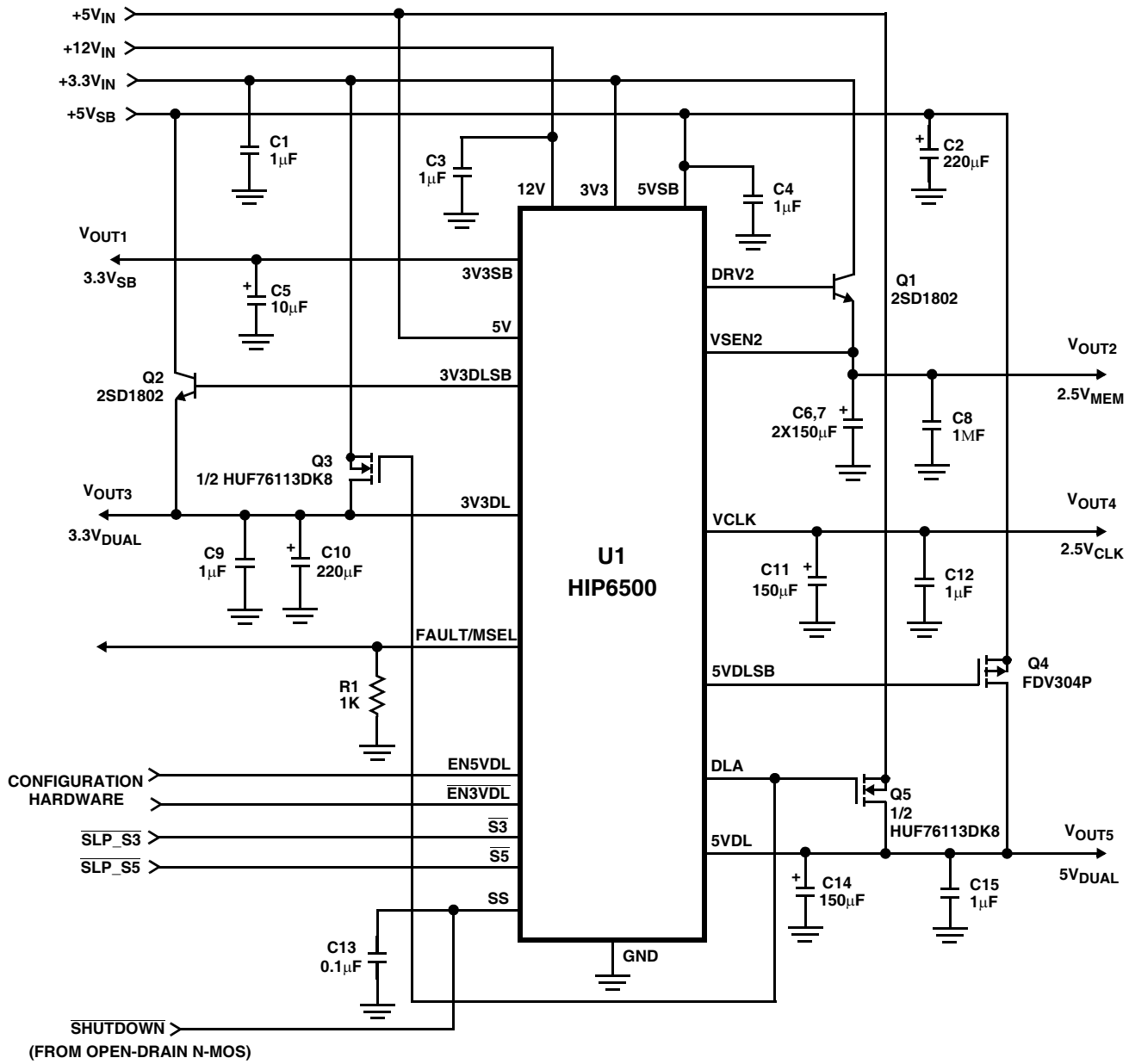
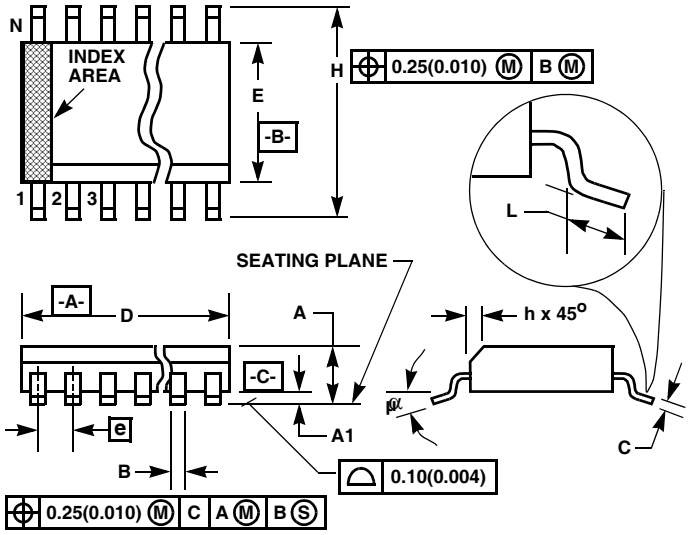


FIGURE 14. TYPICAL HIP6500 APPLICATION DIAGRAM

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M20.3 **(JEDEC MS-013-AC ISSUE C)**
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93