Data Sheet | April 1998 | File Number 4490.2

Advanced Dual PWM and Dual Linear Power Control

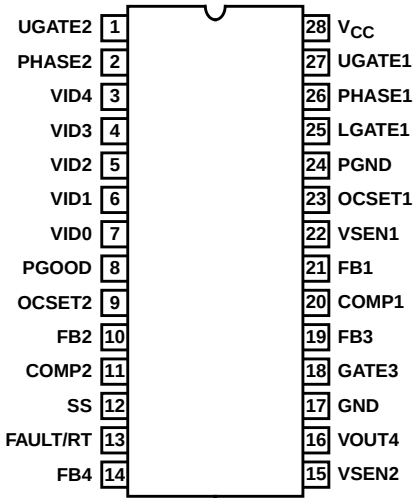
The HIP6019 provides the power control and protection for four output voltages in high-performance microprocessor and computer applications. The IC integrates two PWM controllers, a linear regulator and a linear controller as well as the monitoring and protection functions into a single 28 lead SOIC package. One PWM controller regulates the microprocessor core voltage with a synchronous-rectified buck converter, while the second PWM controller supplies the computer's 3.3V power with a standard buck converter. The linear controller regulates power for the GTL bus and the linear regulator provides power for the clock driver circuits.

The HIP6019 includes an Intel-compatible, TTL 5-input digital-to-analog converter (DAC) that adjusts the core PWM output voltage from $2.1V_{DC}$ to $3.5V_{DC}$ in 0.1V increments and from $1.8V_{DC}$ to $2.05V_{DC}$ in 0.05V steps. The precision reference and voltage-mode control provide ±1% static regulation. The second PWM controller is user-adjustable for output levels between 3.0V and 3.5V with ±2% accuracy. The adjustable linear regulator uses an internal pass device to provide 2.5V ±2.5%. The adjustable linear controller drives an external N-Channel MOSFET to provide 1.5V ±2.5%.

The HIP6019 monitors all the output voltages. A single Power Good signal is issued when the core is within ±10% of the DAC setting and the other levels are above their under- voltage levels. Additional built-in over-voltage protection for the core output uses the lower MOSFET to prevent output voltages above 115% of the DAC setting. The PWM controller's over-current functions monitor the output current by sensing the voltage drop across the upper MOSFET's $r_{DS(ON)}$, eliminating the need for a current sensing resistor.

Pinout

HIP6019 (SOIC)
TOP VIEW



Features

- Provides 4 Regulated Voltages
  - Microprocessor Core, I/O, Clock Chip and GTL Bus
- Drives N-Channel MOSFETs
- Operates from +5V and +12V Inputs
- Simple Single-Loop Control Designs
  - Voltage-Mode PWM Control
- Fast Transient Response
  - High-Bandwidth Error Amplifiers
  - Full 0% to 100% Duty Ratios
- Excellent Output Voltage Regulation
  - Core PWM Output: ±1% Over Temperature
  - I/O PWM Output: ±2% Over Temperature
  - Other Outputs: ±2.5% Over Temperature
- TTL-Compatible 5-Bit Digital-to-Analog Core Output Voltage Selection
  - Wide Range . . . . . $1.8V_{DC}$ to $3.5V_{DC}$
  - 0.1V Steps . . . . . $2.1V_{DC}$ to $3.5V_{DC}$
  - 0.05V Steps . . . . . $1.8V_{DC}$ to $2.05V_{DC}$
- Power-Good Output Voltage Monitor
- Microprocessor Core Voltage Protection Against Shorted MOSFET
- Over-Voltage and Over-Current Fault Monitors
  - Does Not Require Extra Current Sensing Element, Uses MOSFET's $r_{DS(ON)}$
- Small Converter Size
  - Constant Frequency Operation
  - 200kHz Free-Running Oscillator; Programmable from 50kHz to 1MHz

Applications

- Full Motherboard Power Regulation for Computers
- Low-Voltage Distributed Power Supplies

Ordering Information

PART NUMBER	TEMP. (^oC)	PACKAGE	PKG. NO.
HIP6019CB	0 to 70	28 Ld SOIC	M28.3
HIP6019EVAL1	Evaluation Board		

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Block Diagram

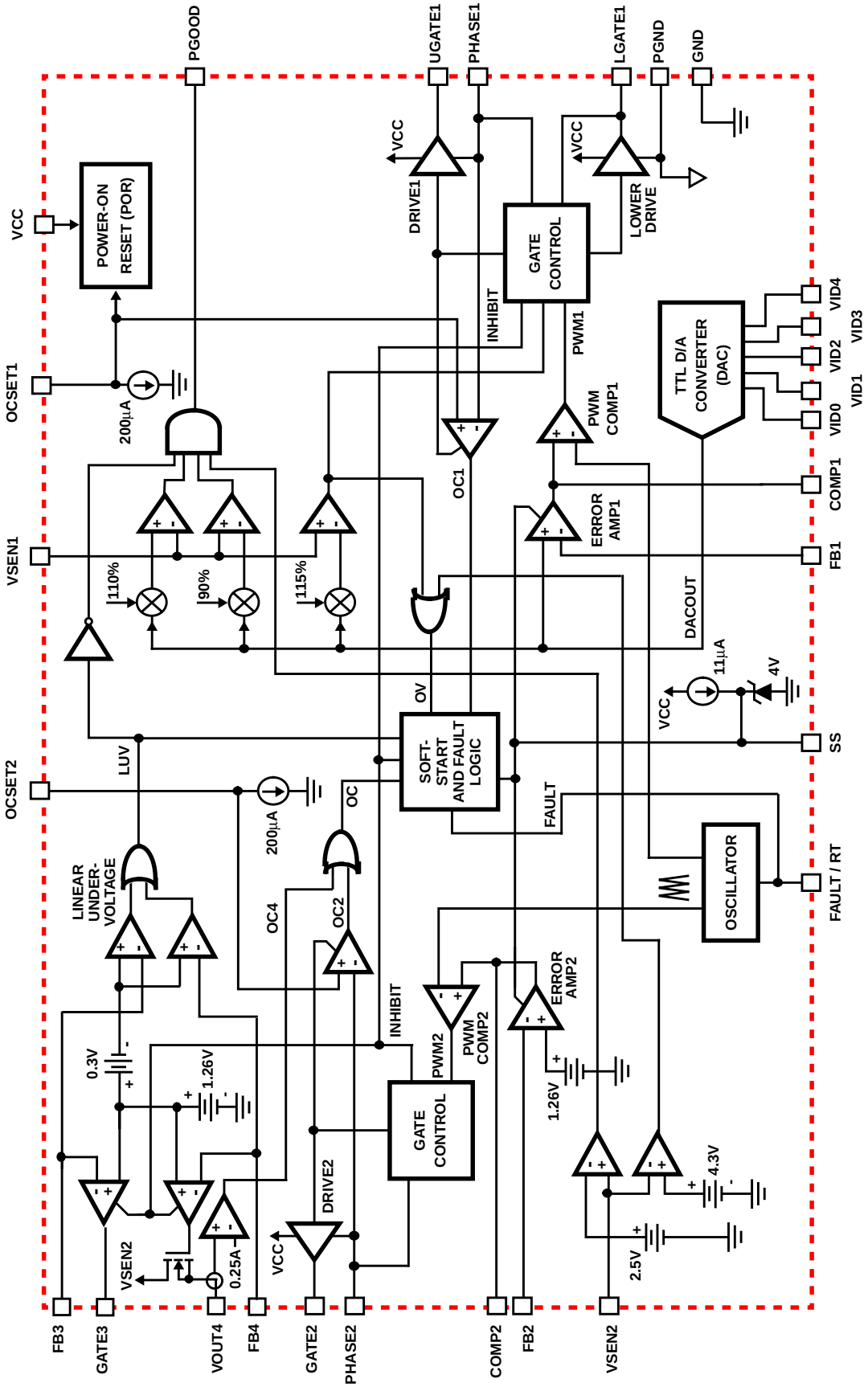


FIGURE 1.

Simplified Power System Diagram

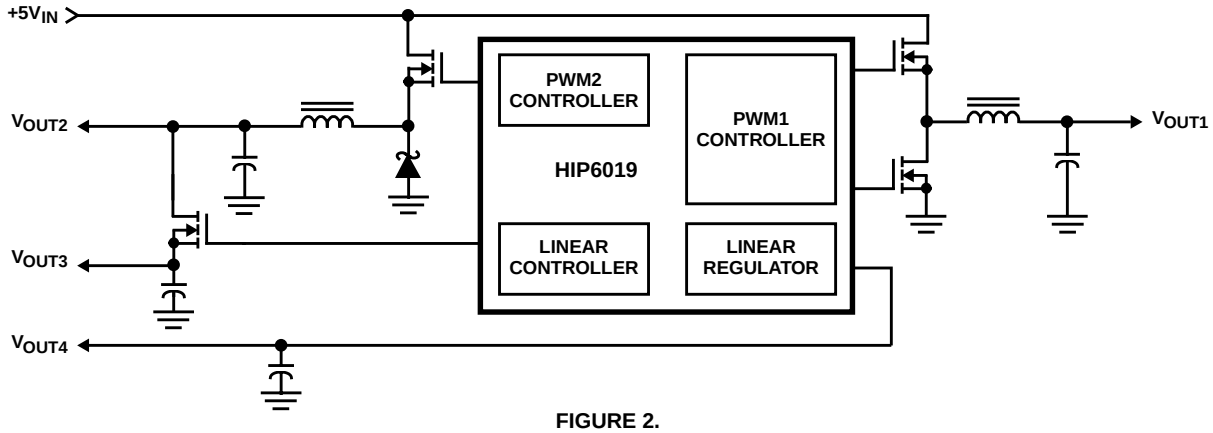


FIGURE 2.

Typical Application

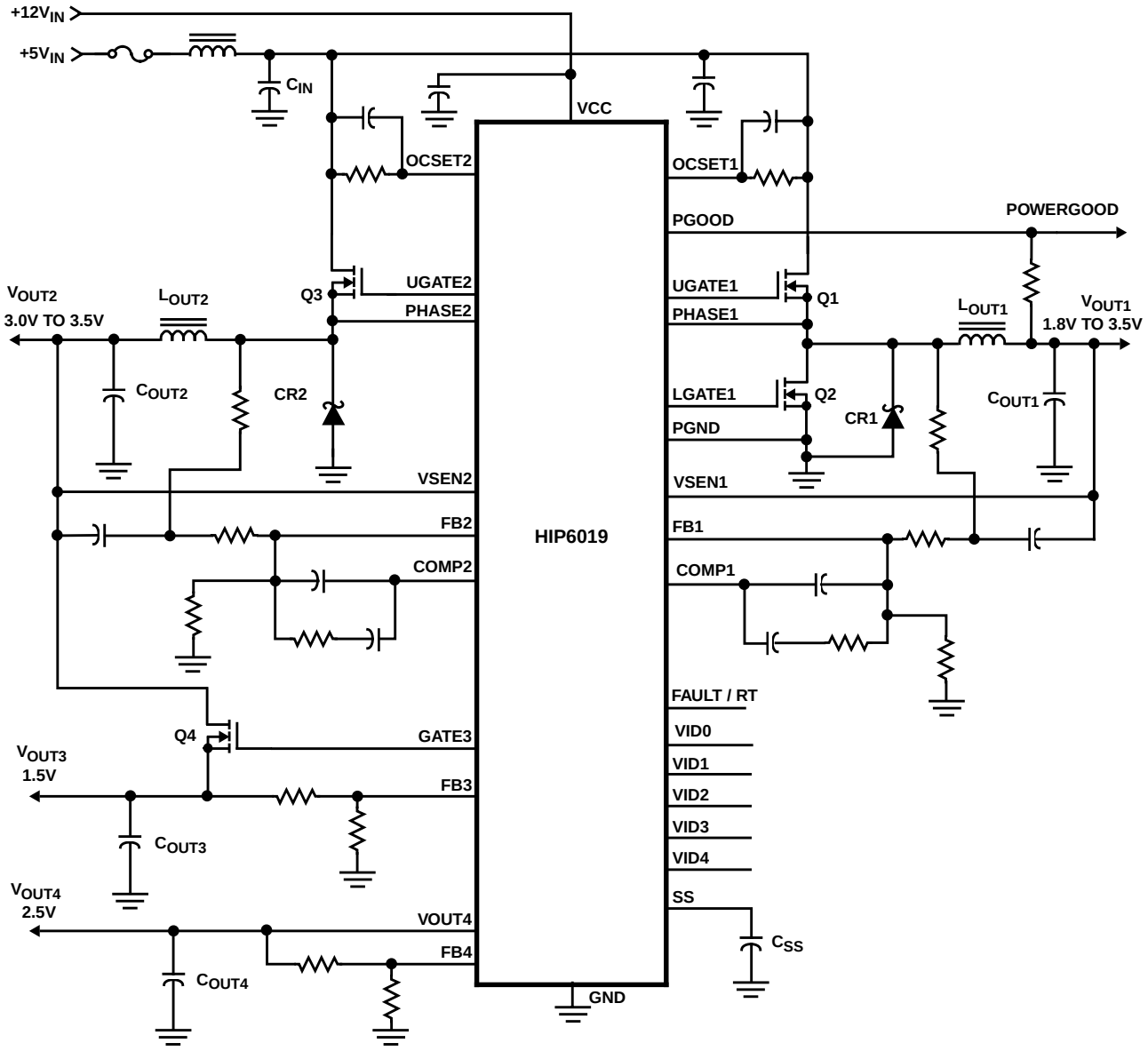


FIGURE 3.

Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . +15V
PGOOD, RT/FAULT, and GATE Voltage . . . . GND - 0.3V to V_{CC} + 0.3V
Input, Output or I/O Voltage . . . . . GND -0.3V to 7V
ESD Classification . . . . . Class 2

Operating Conditions

Supply Voltage, V_{CC} . . . . . +12V ±10%
Ambient Temperature Range . . . . . 0^oC to 70^oC
Junction Temperature Range . . . . . 0^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
SOIC Package 60
SOIC Package (with 3 in^2 of copper) 50
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted.
Refer to Figures 1, 2 and 3

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply	I_{CC}	UGATE1, GATE2, GATE3, LGATE1, and VOUT4 Open	-	10	-	mA
POWER-ON RESET						
Rising VCC Threshold		V_{OCSET} = 4.5V	8.6	-	10.4	V
Falling VCC Threshold		V_{OCSET} = 4.5V	8.2	-	10.2	V
Rising V_{OCSET1} Threshold			-	1.25	-	V
OSCILLATOR						
Free Running Frequency		RT = OPEN	185	200	215	kHz
Total Variation		6kΩ < RT to GND < 200kΩ	-15	-	+15	%
Ramp Amplitude	ΔV_{OSC}	RT = Open	-	1.9	-	V_{P-P}
REFERENCE AND DAC						
DAC(VID0-VID4) Input Low Voltage			-	-	0.8	V
DAC(VID0-VID4) Input High Voltage			2.0	-	-	V
DACOUT Voltage Accuracy			-1.0	-	+1.0	%
Reference Voltage (Pin FB2, FB3, and FB4)			1.240	1.265	1.290	V
LINEAR REGULATOR						
Regulation		10mA < I_{VOUT4} < 150mA	-2.5	-	2.5	%
Under-Voltage Level	$FB4_{UV}$	FB4 Rising	-	75	87	%
Under-Voltage Hysteresis			-	6	-	%
Over-Current Protection			180	230	-	mA
Over-Current Protection During Start-Up		C_{SS} Voltage < 4V	560	700	-	mA
LINEAR CONTROLLER						
Regulation		VSEN3 = GATE3	-2.5	-	2.5	%
Under-Voltage Level	$FB3_{UV}$	FB3 Rising	-	75	87	%
Under-Voltage Hysteresis			-	6	-	%

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Refer to Figures 1, 2 and 3 **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM CONTROLLER ERROR AMPLIFIERS						
DC Gain			-	88	-	dB
Gain-Bandwidth Product	GBWP		-	15	-	MHz
Slew Rate	SR	COMP = 10pF	-	6	-	V/µs
PWM CONTROLLER GATE DRIVERS						
Drive1 (and 2) Source	I_{UGATE}	VCC = 12V, V_{UGATE1} (or V_{GATE2}) = 6V	-	1	-	A
Drive1 (and 2) Sink	R_{UGATE}	$V_{GATE-PHASE}$ = 1V	-	1.7	3.5	Ω
Lower Gate Source	I_{LGATE}	VCC = 12V, V_{LGATE} = 1V	-	1	-	A
Lower Gate Sink	R_{LGATE}	V_{GATE} = 1V	-	1.4	3.0	Ω
PROTECTION						
V_{OUT1} Over-Voltage Trip		VSEN1 Rising	112	115	118	%
V_{OUT2} Over-Voltage Trip		VSEN2 Rising	4.1	4.3	4.5	V
VSEN2 Input Resistance			-	70	-	kΩ
FAULT Sourcing Current	I_{OVP}	$V_{FAULT/RT}$ = 10.0V	10	14	-	mA
OCSET1(and 2) Current Source	I_{OCSET}	V_{OCSET} = 4.5V_{DC}	170	200	230	µA
Soft-Start Current	I_{SS}		-	11	-	µA
Chip Shutdown Soft-Start Threshold			-	-	1.0	V
POWER GOOD						
V_{OUT1} Upper Threshold		VSEN1 Rising	108	-	110	%
V_{OUT1} Under-Voltage		VSEN1 Rising	92	-	94	%
V_{OUT1} Hysteresis		Upper/Lower Threshold	-	2	-	%
V_{OUT2} Under-Voltage		VSEN2 Rising	2.45	2.55	2.65	V
V_{OUT2} Under-Voltage Hysteresis			-	100	-	mV
PGOOD Voltage Low	V_{PGOOD}	I_{PGOOD} = -4mA	-	-	0.5	V

Typical Performance Curves

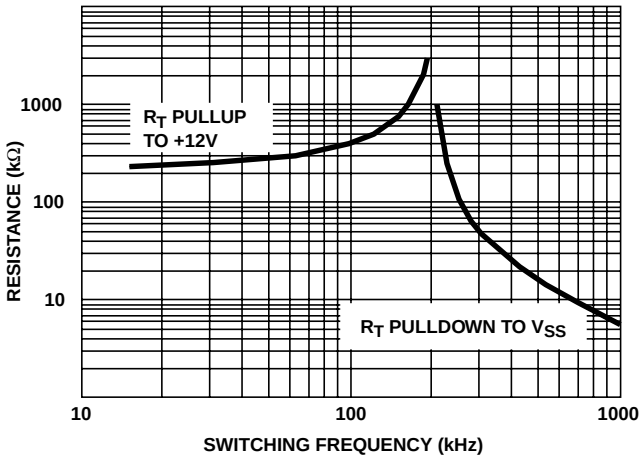


FIGURE 4. R_T RESISTANCE vs FREQUENCY

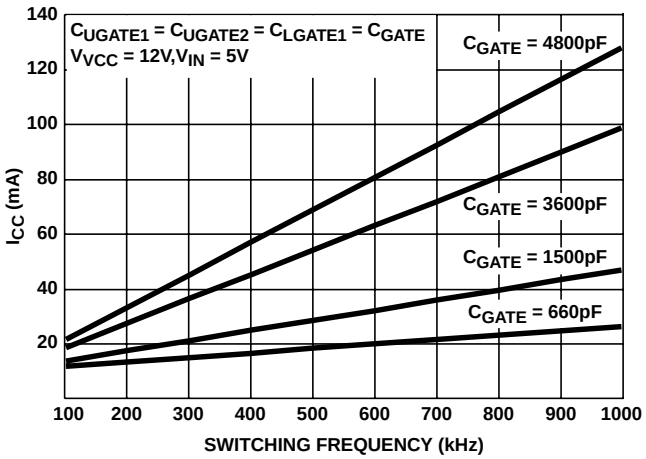


FIGURE 5. BIAS SUPPLY CURRENT vs FREQUENCY

Functional Pin Description

VSEN1, VSEN2 (Pins 22 and 15)

These pins are connected to the PWM converters' output voltages. The PGOOD and OVP comparator circuits use these signals to report output voltage status and for over-voltage protection. VSEN2 provides the input power to the integrated linear regulator.

OCSET1, OCSET2 (Pins 23 and 9)

Connect a resistor (R_{OCSET}) from this pin to the drain of the respective upper MOSFET. R_{OCSET}, an internal 200µA current source (I_{OCSET}), and the upper MOSFET on-resistance ($r_{DS(ON)}$) set the converter over-current (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

An over-current trip cycles the soft-start function. Sustaining an over-current for 2 soft-start intervals shuts down the controller.

Additionally, OCSET1 is an output for the inverted FAULT signal ($\overline{FAULT}$). If a fault condition causes FAULT to go high, OCSET1 will be simultaneously pulled to ground though an internal MOS device (typical $r_{DS(ON)} = 100\Omega$).

SS (Pin 12)

Connect a capacitor from this pin to ground. This capacitor, along with an internal 11µA current source, sets the soft-start interval of the converter.

Pulling this pin low (typically below 1.0V) with an open drain signal will shutdown the IC.

VID0, VID1, VID2, VID3, VID4 (Pins 7, 6, 5, 4 and 3)

VID0-4 are the input pins to the 5-bit DAC. The states of these five pins program the internal voltage reference (DACOUT). The level of DACOUT sets the core converter output voltage (V_{OUT1}). It also sets the core PGOOD and OVP thresholds.

COMP1, COMP2, and FB1, FB2 (Pins 20, 11, 21, and 10)

COMP1, 2 and FB1, 2 are the available external pins of the PWM error amplifiers. Both the FB pins are the inverting input of the error amplifiers. Similarly, the COMP pins are the error amplifier outputs. These pins are used to compensate the voltage-control feedback loops of the PWM converters.

GND (Pin 17)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

PGOOD (Pin 8)

PGOOD is an open collector output used to indicate the status of the PWM converter output voltages. This pin is pulled low when the core output is not within ±10% of the DACOUT reference voltage, or when any of the other outputs are below their under-voltage thresholds.

The PGOOD output is open for VID codes that inhibit operation. See Table 1.

PHASE1, PHASE2 (Pins 26 and 2)

Connect the PHASE pins to the respective PWM converter's upper MOSFET source. These pins are used to monitor the voltage drop across the upper MOSFETs for over-current protection.

UGATE1, UGATE2 (Pins 27 and 1)

Connect UGATE pins to the respective PWM converter's upper MOSFET gate. These pins provide the gate drive for the upper MOSFETs.

PGND (Pin 24)

This is the power ground connection. Tie the synchronous PWM converter's lower MOSFET source to this pin.

LGATE1 (Pin 25)

Connect LGATE1 to the synchronous PWM converter's lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.

VCC (Pin 28)

Provide a 12V bias supply for the IC to this pin. This pin also provides the gate bias charge for all the MOSFETs controlled by the IC.

FAULT/RT (Pin 13)

This pin provides oscillator switching frequency adjustment. By placing a resistor (R_T) from this pin to GND, the nominal 200kHz switching frequency is increased according to the following equation:

$$Fs \approx 200kHz + \frac{5 \times 10^6}{R_T(k\Omega)} \qquad (R_T \text{ to GND})$$

Conversely, connecting a pull-up resistor (R_T) from this pin to VCC reduces the switching frequency according to the following equation:

$$Fs \approx 200kHz - \frac{4 \times 10^7}{R_T(k\Omega)} \qquad (R_T \text{ to 12V})$$

Nominally, this pin voltage is 1.26V, but is pulled to VCC in the event of an over-voltage or over-current condition.

GATE3 (Pin 18)

Connect this pin to the gate of an external MOSFET. This pin provides the drive for the linear controller's pass transistor.

FB3 (Pin 19)

Connect this pin to a resistor divider to set the linear controller output.

VOUT4 (Pin 16)

Output of the linear regulator. Supplies current up to 230mA.

FB4 (Pin 14)

Connect this pin to a resistor divider to set the linear regulator output.

Description

Operation

The HIP6019 monitors and precisely controls 4 output voltage levels (Refer to Figures 1, 2, and 3). It is designed for microprocessor computer applications with 5V power and 12V bias input from a PS2 or ATX power supply. The IC has 2 PWM controllers, a linear controller, and a linear regulator. The first PWM controller (PWM1) is designed to regulate the microprocessor core voltage (V_{OUT1}). PWM1 controller drives 2 MOSFETs (Q1 and Q2) in a synchronous-rectified buck converter configuration and regulates the core voltage to a level programmed by the 5-bit digital-to-analog converter (DAC). The second PWM controller (PWM2) is designed to regulate the I/O voltage (V_{OUT2}). PWM2 controller drives a MOSFET (Q3) in a standard buck converter configuration and regulates the I/O voltage to a resistor programmable level between 3.0 and 3.5V_{DC}. An integrated linear regulator supplies the 2.5V clock generator power (V_{OUT4}). The linear controller drives an external MOSFET (Q4) to supply the GTL bus power (V_{OUT3}).

Initialization

The HIP6019 automatically initializes upon receipt of input power. Special sequencing of the input supplies is not necessary. The Power-On Reset (POR) function continually monitors the input supply voltages. The POR monitors the bias voltage (+12V_{IN}) at the VCC pin and the 5V input voltage (+5V_{IN}) at the OCSET1 pin. The normal level on OCSET1 is equal to +5V_{IN} less a fixed voltage drop (see over-current protection). The POR function initiates soft-start operation after both input supply voltages exceed their POR thresholds.

Soft-Start

The POR function initiates the soft-start sequence. Initially, the voltage on the SS pin rapidly increases to approximately 1V (this minimizes the soft-start interval). Then an internal 11µA current source charges an external capacitor (C_{SS}) on the SS pin to 4V. The PWM error amplifier reference inputs (+ terminal) and outputs (COMP1 and COMP2 pins) are clamped to a level proportional to the SS pin voltage. As the SS pin voltage ramps from 1V to 4V, the output clamp allows generation of PHASE pulses of increasing width that charge the output capacitor(s). After this initial stage, the reference input clamp slows the output voltage rate-of-rise and provides a smooth transition to the final set voltage. Additionally, both linear regulator's reference inputs are clamped to a voltage proportional to the SS pin voltage. This method provides a rapid and controlled output voltage rise.

Figure 6 shows the soft-start sequence for the typical application. At T0 the SS voltage rapidly increases to approximately 1V. At T1, the SS pin and error amplifier output voltage reach the valley of the oscillator's triangle wave. The oscillator's triangular waveform is compared to the clamped error amplifier output voltage. As the SS pin voltage increases, the pulse-width on the PHASE pin increases. The interval of increasing pulse-width continues until each output reaches sufficient voltage to transfer control to the input reference clamp. If we consider the 3.3V output (V_{OUT2}) in Figure 6, this time occurs at T2. During the interval between T2 and T3, the error amplifier reference ramps to the final value and the converter regulates the output to a voltage proportional to the SS pin voltage. At T3 the input clamp voltage exceeds the reference voltage and the output voltage is in regulation.

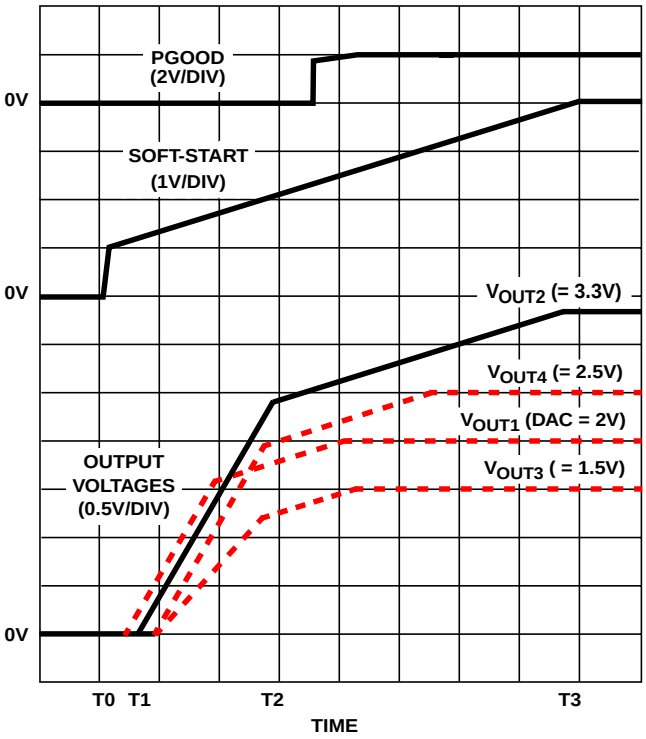


FIGURE 6. SOFT-START INTERVAL

The remaining outputs are also programmed to follow the SS pin voltage. Each linear output (V_{OUT3} and V_{OUT4}) initially follows the 3.3V output (V_{OUT2}). When each output reaches sufficient voltage the input reference clamp slows the rate of output voltage rise. The PGOOD signal toggles 'high' when all output voltage levels have exceeded their under-voltage levels. See the Soft-Start Interval section under Applications Guidelines for a procedure to determine the soft-start interval.

Fault Protection

All four outputs are monitored and protected against extreme overload. A sustained overload on any linear regulator output or an over-voltage on the PWM outputs disables all converters and drives the FAULT/RT pin to VCC.

Figure 7 shows a simplified schematic of the fault logic. An over-voltage detected on either VSEN1 or VSEN2

immediately sets the fault latch. A sequence of three over-current fault signals also sets the fault latch. A comparator indicates when C_{SS} is fully charged (UP signal), such that an under-voltage event on either linear output (FB3 or FB4) is ignored until after the soft-start interval (approximately T3 in Figure 6). At start-up, this allows V_{OUT3} and V_{OUT4} to slew up over increased time intervals, without generating a fault. Cycling the bias input voltage (+12V_{IN} on the VCC pin) off then on resets the counter and the fault latch.

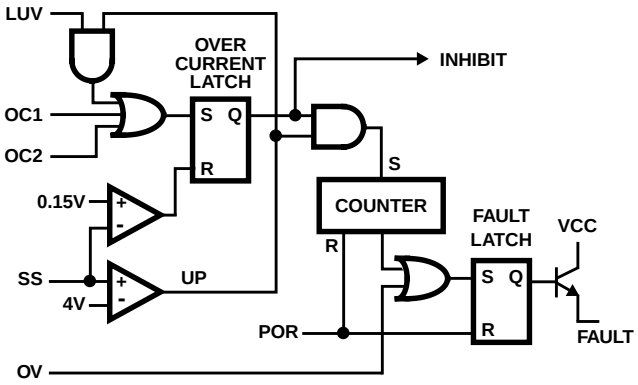


FIGURE 7. FAULT LOGIC - SIMPLIFIED SCHEMATIC

Over-Voltage Protection

During operation, a short on the upper MOSFET (Q1) causes V_{OUT1} to increase. When the output exceeds the over-voltage threshold of 115% of DACOUT, the over-voltage comparator trips to set the fault latch and turns Q2 on as required in order to regulate V_{OUT1} to 1.15 x DACOUT. This blows the input fuse and reduces V_{OUT1}. The fault latch raises the FAULT/RT pin close to VCC potential.

A separate over-voltage circuit provides protection during the initial application of power. For voltages on the VCC pin below the power-on reset (and above ~4V), V_{OUT1} is monitored for voltages exceeding 1.26V. Should VSEN1 exceed this level, the lower MOSFET (Q2) is driven on, as needed to regulate V_{OUT1} to 1.26V.

Over-Current Protection

All outputs are protected against excessive over-currents. Both PWM controllers use the upper MOSFET's on-resistance, $r_{DS(ON)}$ to monitor the current for protection against shorted outputs. The linear regulator monitors the current of the integrated power device and signals an over-current condition for currents in excess of 230mA. Additionally, both the linear regulator and the linear controller monitor FB3 and FB4 for under-voltage to protect against excessive currents.

Figures 8 and 9 illustrate the over-current protection with an overload on OUT2. The overload is applied at T0 and the current increases through the output inductor (L_{OUT2}). At time T1, the OVER-CURRENT2 comparator trips when the voltage across Q3 ($I_D \cdot r_{DS(ON)}$) exceeds the level programmed by R_{OCSET}. This inhibits all outputs, discharges the soft-start capacitor (C_{SS}) with a 11µA current sink, and increments the counter. C_{SS} recharges at T2 and initiates a soft-start cycle with the error amplifiers clamped by soft-start. With OUT2 still overloaded, the inductor current increases to trip the over-current comparator. Again, this inhibits all outputs, but the soft-start voltage continues increasing to 4V before discharging. The counter increments to 2. The soft-start cycle repeats at T3 and trips the over-current comparator. The SS pin voltage increases to 4V at T4 and the counter increments to 3. This sets the fault latch to disable the converter. The fault is reported on the FAULT/RT pin.

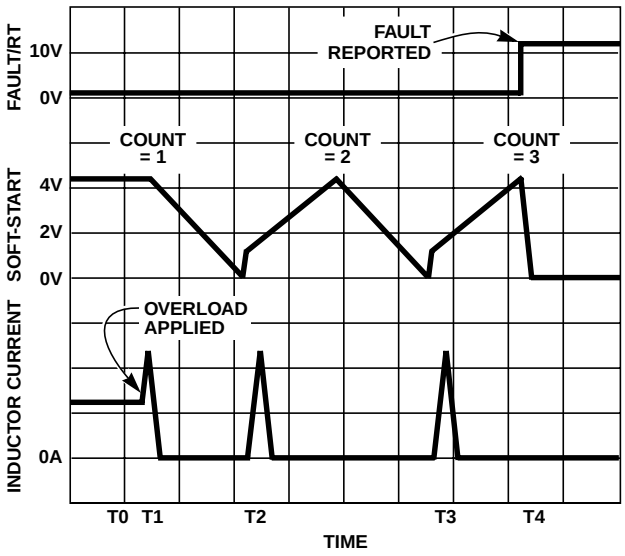


FIGURE 8. OVER-CURRENT OPERATION

The PWM1 controller and the linear regulator operate in the same way as PWM2 to over-current faults. Additionally, the linear regulator and linear controller monitor the feedback pins for an under-voltage. Should excessive currents cause FB3 or FB4 to fall below the linear under-voltage threshold, the LUV signal sets the over-current latch if C_{SS} is fully charged. Blanking the LUV signal during the C_{SS} charge interval allows the linear outputs to build above the under-voltage threshold during normal start-up. Cycling the bias input power off then on resets the counter and the fault latch.

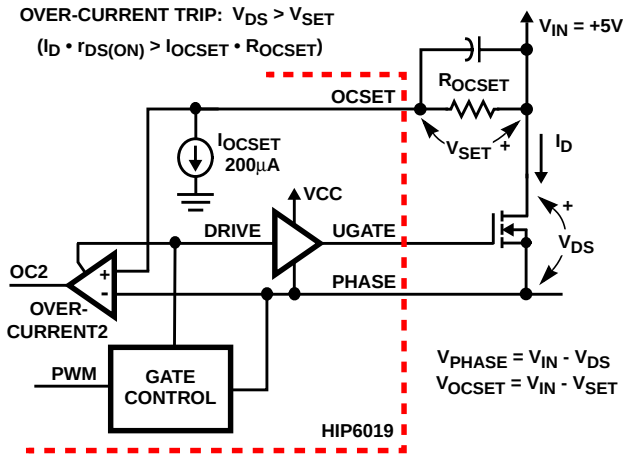


FIGURE 9. OVER-CURRENT DETECTION

Resistors (R_{OCSET1} and R_{OCSET2}) program the over-current trip levels for each PWM converter. As shown in Figure 9, the internal 200µA current sink develops a voltage across R_{OCSET} (V_{SET}) that is referenced to V_{IN}. The DRIVE signal enables the over-current comparator (OVER-CURRENT1 or OVER-CURRENT2). When the voltage across the upper MOSFET (V_{DS}) exceeds V_{SET}, the over-current comparator trips to set the over-current latch. Both V_{SET} and V_{DS} are referenced to V_{IN} and a small capacitor across R_{OCSET} helps V_{OCSET} track the variations of V_{IN} due to MOSFET switching. The over-current function will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

The OC trip point varies with MOSFET's temperature. To avoid over-current tripping in the normal operating load range, determine the R_{OCSET} resistor from the equation above with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature.
2. The minimum I_{OCSET} from the specification table.
3. Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + (\Delta I)/2$, where ΔI is the output inductor ripple current.

For an equation for the output inductor ripple current see the section under component guidelines titled 'Output Inductor Selection'.

OUT1 Voltage Program

The output voltage of the PWM1 converter is programmed to discrete levels between $1.8V_{DC}$ and $3.5V_{DC}$. This output is designed to supply the microprocessor core voltage. The voltage identification (VID) pins program an internal voltage reference (DACOUT) through a TTL-compatible 5-bit digital-to-analog converter. The level of DACOUT also sets the PGOOD and OVP thresholds. Table 1 specifies the DACOUT voltage for the different combinations of connections on the VID pins. The VID pins can be left open for a logic 1 input, because they are internally pulled up to +5V by a 10µA current source. Changing the VID inputs during operation is not recommended. The sudden change in the resulting reference voltage could toggle the PGOOD signal and exercise the over-voltage protection. All VID pin combinations resulting in an INHIBIT disable the IC and the open-collector at the PGOOD pin.

Application Guidelines

Soft-Start Interval

Initially, the soft-start function clamps the error amplifiers' output of the PWM converters. After the output voltage increases to approximately 80% of the set value, the reference input of the error amplifier is clamped to a voltage proportional to the SS pin voltage. The resulting output voltage sequence is shown in Figure 6.

The soft-start function controls the output voltage rate of rise to limit the current surge at start-up. The soft-start interval is programmed by the soft-start capacitor, C_{SS}. Programming a faster soft-start interval increases the peak surge current. The peak surge current occurs during the initial output voltage rise to 80% of the set value.

Shutdown

Neither PWM output switches until the soft-start voltage (V_{SS}) exceeds the oscillator's valley voltage. Additionally, the reference on each linear's amplifier is clamped to the soft-start voltage. Holding the SS pin low (with an open drain or collector signal) turns off all four regulators.

The VID codes resulting in an INHIBIT as shown in Table 1 also shut down the IC.

TABLE 1. V_{OUT1} VOLTAGE PROGRAM

PIN NAME					NOMINAL OUT1 VOLTAGE DACOUT
VID4	VID3	VID2	VID1	VID0	
0	1	X	X	X	INHIBIT
0	0	1	1	X	INHIBIT
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	INHIBIT
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6

TABLE 1. V_{OUT1} VOLTAGE PROGRAM (Continued)

PIN NAME					NOMINAL OUT1 VOLTAGE DACOUT
VID4	VID3	VID2	VID1	VID0	
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

NOTE: 0 = connected to GND or V_{SS}, 1 = open or connected to 5V through pull-up resistors, X = don't care.

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device over-voltage stress. Careful component layout and printed circuit design minimizes the voltage spikes in the converter. Consider, as an example, the turnoff transition of the upper MOSFET. Prior to turnoff, the upper MOSFET was carrying the full load current. During the turnoff, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET or Schottky diode. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes. Contact Intersil for evaluation board drawings of the component placement and printed circuit board.

There are two sets of critical components in a DC-DC converter using a HIP6019 controller. The power components are the most critical because they switch large amounts of energy. The critical small signal components connect to sensitive nodes or supply critical bypassing current.

The power components should be placed first. Locate the input capacitors close to the power switches. Minimize the length of the connections between the input capacitors and the power switches. Locate the output inductor and output capacitors between the MOSFETs and the load. Locate the PWM controller close to the MOSFETs.

The critical small signal components include the bypass capacitor for VCC and the soft-start capacitor, C_{SS}. Locate these components close to their connecting pins on the control IC. Minimize any leakage current paths from SS node because the internal current source is only 11µA.

A multi-layer printed circuit board is recommended. Figure 10 shows the connections of the critical components in the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the control IC to the MOSFET gate and source should be sized to carry 1A currents. The traces for OUT4 need only be sized for 0.2A. Locate C_{OUT4} close to the HIP6019 IC.

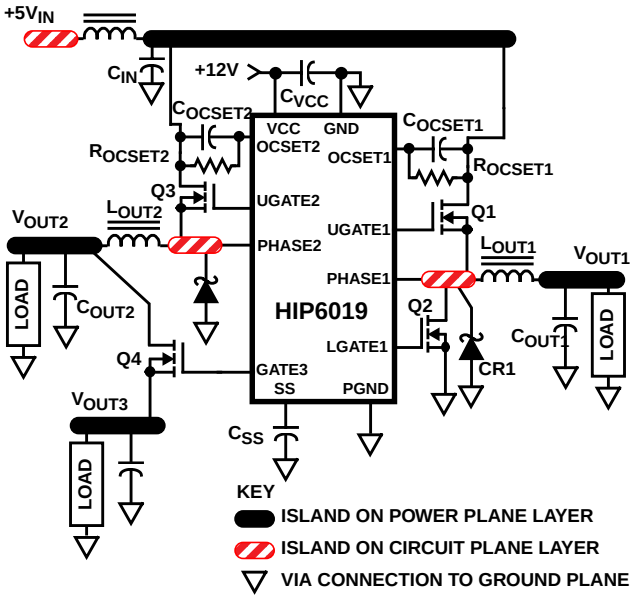


FIGURE 10. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

PWM Controller Feedback Compensation

Both PWM controllers use voltage-mode control for output regulation. This section highlights the design consideration for a voltage-mode controller. Apply the methods and considerations to both PWM controllers.

Figure 11 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage is regulated to the reference voltage level. The reference voltage level is the DAC output voltage for PWM1 and is 1.265V for PWM2. The error amplifier output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

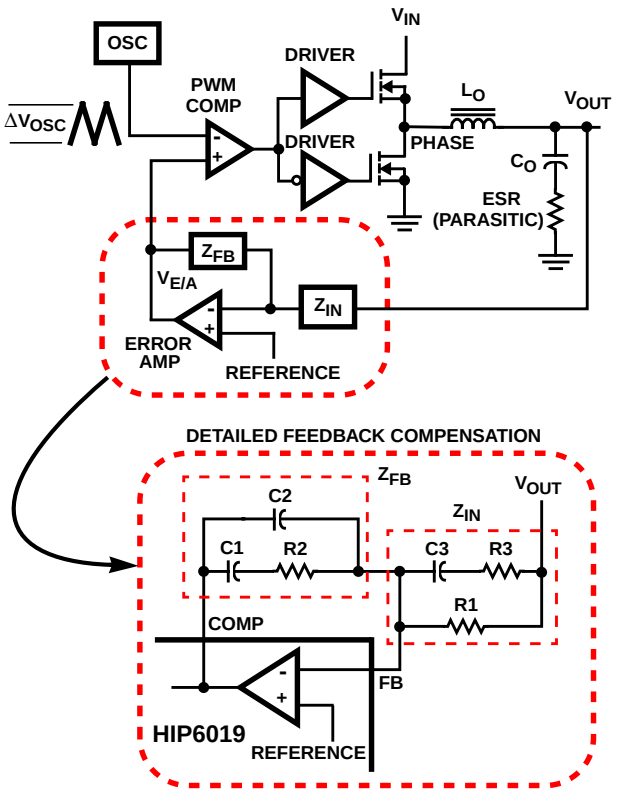


FIGURE 11. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC gain and the output filter, with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC gain of the modulator is simply the input voltage, V_{IN}, divided by the peak-to-peak oscillator voltage, ΔV_{OSC}.

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad F_{ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

The compensation network consists of the error amplifier internal to the HIP6019 and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with an acceptable 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 11. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R2/R1) for desired converter bandwidth.
2. Place 1ST Zero below filter's Double Pole (~75% F_{LC}).
3. Place 2ND Zero at filter's Double Pole.
4. Place 1ST Pole at the ESR Zero.
5. Place 2ND Pole at half the switching frequency.
6. Check Gain against Error Amplifier's Open-Loop Gain.
7. Estimate Phase Margin - repeat if necessary.

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C1} \qquad F_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C1 \times C2}{C1 + C2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R1 + R3) \times C3} \qquad F_{P2} = \frac{1}{2\pi \times R3 \times C3}$$

Figure 12 shows an asymptotic plot of the DC-DC converter's gain vs frequency. The actual modulator gain has a peak due to the high Q factor of the output filter at F_{LC}, which is not shown in Figure 12. Using the above guidelines should yield a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The closed loop gain is constructed on the log-log graph of Figure 12 by adding the modulator gain (in dB) to the compensation gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

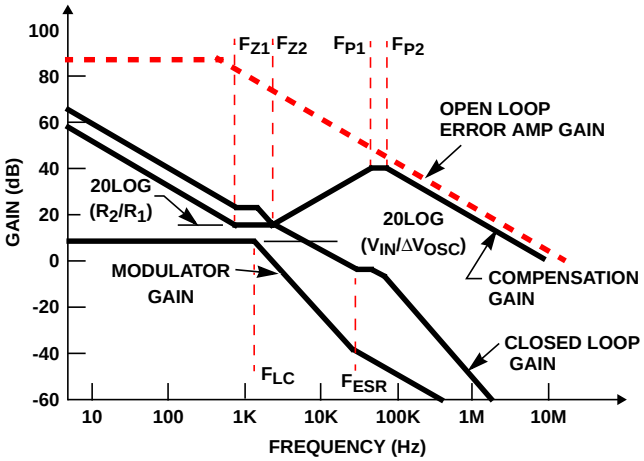


FIGURE 12. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth loop. A stable control loop has a 0dB gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

Oscillator Synchronization

The PWM controllers use a triangle wave for comparison with the error amplifier output to provide a pulse-width modulated wave. Should the output voltages of the two PWM converters be programmed close to each other, then cross-talk could cause nonuniform PHASE pulse-widths and increased output voltage ripple. The HIP6019 avoids this problem by synchronizing the two converters 180° out-of-phase for DAC

settings above, and including 2.5V. This is accomplished by inverting the triangle wave sent to PWM 2.

Component Selection Guidelines

Output Capacitor Selection

The output capacitors for each output have unique requirements. In general the output capacitors should be selected to meet the dynamic regulation requirements. Additionally, the PWM converters require an output capacitor to filter the current ripple. The linear regulator is internally compensated and requires an output capacitor that meets the stability requirements. The load transient for the microprocessor core requires high quality capacitors to supply the high slew rate (di/dt) current demands.

PWM Output Capacitors

Modern microprocessors produce transient load rates above 10A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and ESL (effective series inductance) parameters rather than actual capacitance.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching regulator applications for the bulk capacitors. The bulk capacitor's ESR determines the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select suitable components. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor. For a given transient load magnitude, the output voltage transient response due to the output capacitor characteristics can be approximated by the following equation:

$$V_{TRAN} = ESL \times \frac{dI_{TRAN}}{dt} + ESR \times I_{TRAN}$$

Linear Output Capacitors

The output capacitors for the linear regulator and the linear controller provide dynamic load current. The linear controller uses dominant pole compensation integrated in the error amplifier and is insensitive to output capacitor selection. Capacitor, C_{OUT3} should be selected for transient load regulation.

The output capacitor for the linear regulator provides loop stability. The linear regulator (OUT4) requires an output capacitor characteristic shown in Figure 13 The upper line plots the 45 phase margin with 150mA load and the lower line is the 45 phase margin limit with a 10mA load. Select a C_{OUT4} capacitor with characteristic between the two limits.

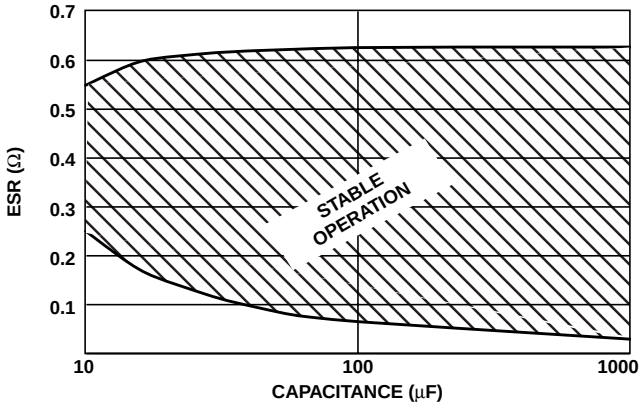


FIGURE 13. C_{OUT4} OUTPUT CAPACITOR

Output Inductor Selection

Each PWM converter requires an output inductor. The output inductor is selected to meet the output voltage ripple requirements and sets the converter's response time to a load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_S \times L_O} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the HIP6019 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time interval required to slew the inductor current from an initial current value to the post-transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitors. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following

equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. With a +5V input source, the worst case response time can be either at the application or removal of load and dependent upon the output voltage setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline.

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use ceramic capacitance for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors should be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

For a through hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Selection/Considerations

The HIP6019 requires 4 N-Channel power MOSFETs. Two MOSFETs are used in the synchronous-rectified buck topology of PWM1 converter. PWM2 converter uses a MOSFET as the buck switch and the linear controller drives a MOSFET as a pass transistor. These should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements.

PWM1 MOSFET Selection and Considerations

In high-current PWM applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to duty factor (see the equations below). The conduction losses are the only component of power dissipation for the lower MOSFETs. Only the upper MOSFET has switching losses, since the lower device turns on into near zero voltage.

The equations below assume linear voltage-current transitions and do not model power loss due to the reverse-recovery of the lower MOSFET's body diode. The gate-charge losses are proportional to the switching frequency (F_S) and are dissipated by the HIP6019, thus not contributing to the MOSFETs' temperature rise. However, large gate charge increases the switching interval, t_{SW} which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{UPPER} = \frac{I_O^2 \times r_{DS(ON)} \times V_{OUT}}{V_{IN}} + \frac{I_O \times V_{IN} \times t_{SW} \times F_S}{2}$$

$$P_{LOWER} = \frac{I_O^2 \times r_{DS(ON)} \times (V_{IN} - V_{OUT})}{V_{IN}}$$

The $r_{DS(ON)}$ is different for the two previous equations even if the type device is used for both. This is because the gate drive applied to the upper MOSFET is different than the lower MOSFET. Figure 14 shows the gate drive where the upper gate-to-source voltage is approximately V_{CC} less the input supply. For +5V main power and $+12V_{DC}$ for the bias, the gate-to-source voltage of Q1 is 7V. The lower gate drive voltage is $+12V_{DC}$. A logic-level MOSFET is a good choice for Q1 and a logic-level MOSFET can be used for Q2 if its absolute gate-to-source voltage rating exceeds the maximum voltage applied to V_{CC}.

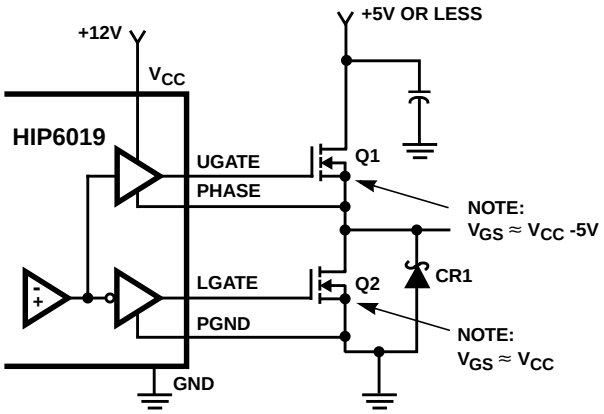


FIGURE 14. OUTPUT GATE DRIVERS

Rectifier CR1 is a clamp that catches the negative inductor swing during the dead time between the turn off of the lower MOSFET and the turn on of the upper MOSFET. The diode must be a Schottky type to prevent the lossy parasitic MOSFET body diode from conducting. It is acceptable to

omit the diode and let the body diode of the lower MOSFET clamp the negative inductor swing, but efficiency might drop one or two percent as a result. The diode's rated reverse breakdown voltage must be greater than twice the maximum input voltage.

PWM2 MOSFET and Schottky Selection

The power dissipation in PWM2 converter power devices is similar to PWM1 except that the power losses of the lower device are representative of a Schottky diode instead of a MOSFET. The transistor power losses follow the PWM1 upper MOSFET equation, so the selection process should be somewhat similar. The equation below describes the conduction power losses incurred by the Schottky diode.

$$P_{SCH} = \frac{I_O \times V_f \times (V_{IN} - V_{OUT})}{V_{IN}}$$

As it can be observed, conduction losses in the Schottky diode are proportional with the forward voltage drop (V_f).

Linear Controller MOSFET Selection

The main criteria for selection of MOSFET for the linear regulator is package selection for efficient removal of heat. The power dissipated in a linear regulator is:

$$P_{LINEAR} = I_O \times (V_{IN} - V_{OUT})$$

Select a package and heatsink that maintains the junction temperature below the maximum rating while operating at the highest expected ambient temperature.

HIP6019 DC-DC Converter Application Circuit

Figure 15 shows an application circuit of a power supply for a microprocessor computer system. The power supply provides the microprocessor core voltage (V_{OUT1}), the I/O voltage (V_{OUT2}), the GTL bus voltage (V_{OUT3}) and clock generator voltage (V_{OUT4}) from $+5V_{DC}$ and $+12V_{DC}$. For detailed information on the circuit, including a Bill-of-Materials and circuit board description, see Application Note AN9800. Also see Intersil's web page (http://www.intersil.com) or Intersil AnswerFAX (407-724-7800) document # 99800 for the latest information.

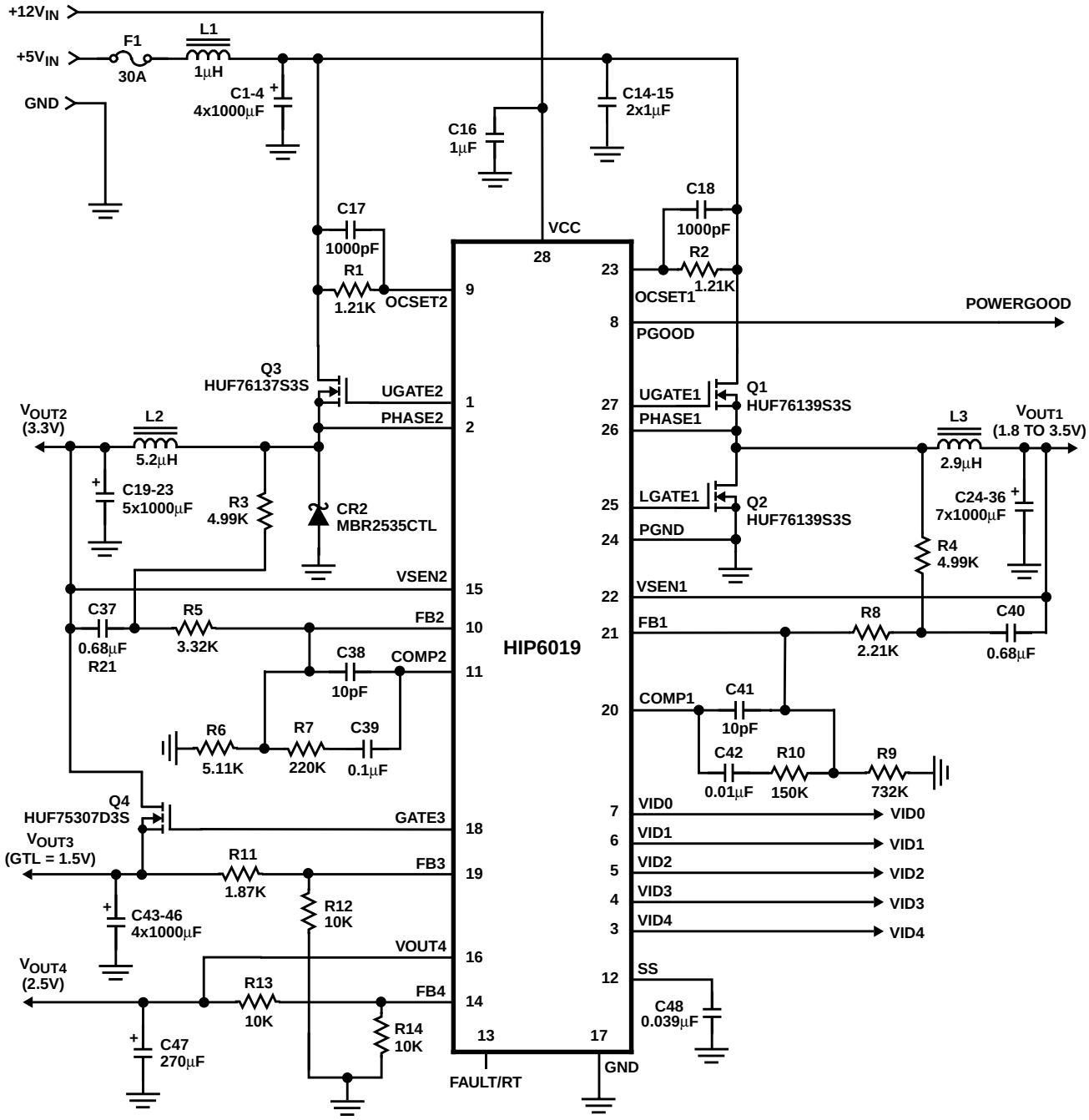


FIGURE 15. APPLICATION CIRCUIT

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