Data Sheet | January 30, 2006 | FN6059.2

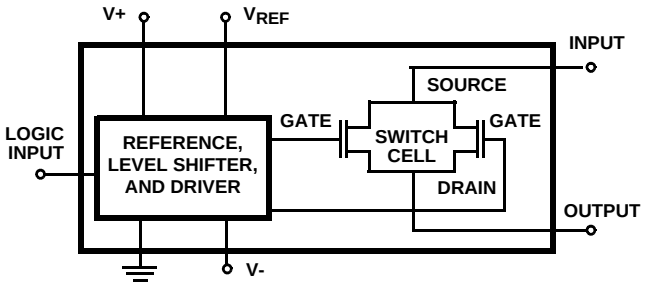
Dual SPST CMOS Analog Switch

The HI-200/883 is a monolithic device comprising two independently selectable SPST switchers which feature fast switching speeds (240ns typical) combined with low power dissipation (15mW typical @ +25°C).

Each switch provides low “ON” resistance operation for input signal voltages up to the supply rails and for signal currents up to 25mA continuous. Rugged DI construction eliminates latch-up and substrate SCR failure modes.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200/883 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuits, digital filters, and op amp gain switching networks.

Functional Diagram



Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low “On” Release . . . . . .100Ω Max
- Wide Analog Signal Range . . . . . .±15V
- TTL/CMOS Compatible . . . . . 2.4V (Logic “1”)
- Turn-On Time. 500ns
- Analog Current Range (Continuous) 25mA
- No Latch-Up
- Replaces DG200

Applications

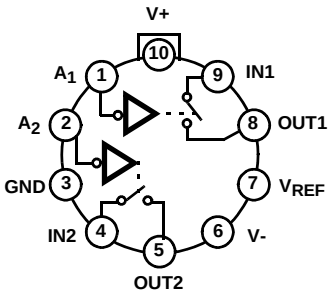
- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Op Amp Gain Switching Networks

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HI2-0200/883	-55 to 125	10 Pin Metal Can	T10.B

Pinout

HI2-200/883 (METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
$\pm V_{SUPPLY}$ to Ground (V+, V-) . . . . . $\pm$20V
Analog Input Voltage, ($+V_S$) . . . . . $+V_{SUPPLY}$ +2V
($-V_S$) . . . . . $-V_{SUPPLY}$ -2V
Digital Input Voltage, ($+V_A$) . . . . . $+V_{SUPPLY}$ +4V
($-V_A$) . . . . . $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current 25mA
Junction Temperature . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . $\leq$275°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	160	75

Package Power Dissipation at +75°C
Metal Can Package . . . . . 0.62W/°C
Package Power Dissipation Derating Factor above +75°C
Metal Can Package . . . . . 8.24mW/°C

Recommended Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage Range ($\pm V_{SUPPLY}$) . . . . . $\pm$15V
Analog Input Voltage (V_S) . . . . . $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) . . . . . 0V to 0.8V
Logic High Level (V_{AH}) . . . . . 2.4V to $+V_{SUPPLY}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = –15V, V_{REF} = OPEN, GND = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Switch "ON" Resistance	r_{DS}	V_A = 0.8V, V_S = 10V, I_D = -1mA, All Unused Channels V_A = 0.8V	1	25	-	70	Ω
			2, 3	-55 to 125	-	100	Ω
		V_A = 0.8V, V_S = -10V, I_D = 1mA, All Unused Channels V_A = 0.8V	1	25	-	70	Ω
			2, 3	-55 to 125	-	100	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_A = 2.4V, All Unused Channels V_A = 2.4V, V_D = +14V, V_S = -14V	1	25	-5	5	nA
			2, 3	-55 to 125	-500	500	nA
		V_S = -14V, V_D = +14V, V_A = 2.4V, All Unused Channels V_A = 2.4V, V_D = -14V, V_S = +14V	1	25	-5	5	nA
			2, 3	-55 to 125	-500	500	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -14V, V_S = +14V, V_A = 2.4V, All Unused Channels V_A = 2.4V, V_D = +14V, V_S = -14V	1	25	-5	5	nA
			2, 3	-55 to 125	-500	500	nA
		V_D = +14V, V_S = -14V, V_A = 2.4V, All Unused Channels V_A = 2.4V, V_D = -14V, V_S = +14V	1	25	-5	5	nA
			2, 3	-55 to 125	-500	500	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_A = 0.8V, All Unused Channels V_A = 0.8V, V_D = V_S = -14V	1	25	-5	5	nA
			2, 3	-55 to 125	-500	500	nA
		V_D = V_S = -14V, V_A = 0.8V, All Unused Channels V_A = 0.8V, V_D = V_S = +14V	1	25	-5	5	nA
			2, 3	-55 to 125	-500	500	nA
Low Level Input Current	I_{AL}	V_{AL} = 0.8V All Channels V_A = 2.4V	1	25	-1.0	1.0	µA
			2, 3	-55 to 125	-1.0	1.0	µA
High Level Input Current	I_{AH}	V_{AH} = 2.4V All Channels V_{AH} = 4.0V	1	25	-1.0	1.0	µA
			2, 3	-55 to 125	-1.0	1.0	µA
Supply Current	$+I_{CC}$	All Channels V_A = 0V	1	25	-	2.0	µA
			2, 3	-55 to 125	-	2.0	µA
		All Channels V_A = 3V	1	25	-	2.0	mA
			2, 3	-55 to 125	-	2.0	mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, V_{REF} = OPEN, GND = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Supply Current	$-I_{CC}$	All Channels V_A = 0V	1	25	-2.0	-	µA
			2, 3	-55 to 125	-2.0	-	µA
		All Channels V_A = 3V	1	25	-2.0	-	µA
			2, 3	-55 to 125	-2.0	-	µA

TABLE 2. A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, V_{REF} = OPEN, GND = 0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Turn “ON” Time	t_{ON}	C_L = 35pF, R_L = 1kΩ	9	25	-	500	ns
			10, 11	55 to 125	-	800	ns
Turn “OFF” Time	t_{OFF}	C_L = 33pF, R_L = 1kΩ	9	25	-	500	ns
			10, 11	55 to 125	-	650	ns

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (NOTE 1)

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, V_{REF} = OPEN, GND = 0V

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE (°C)	MIN	MAX	UNITS
Address Capacitance	C_A	f = 1MHz, V_{AL} = 0V	1	25	-	20	pF
Switches Input Capacitance	$C_{S\ (OFF)}$	f = 1MHz, V_{AH} = 5V, Measured Source to GND	1	25	-	20	pF
Switch Output Capacitance	$C_{D\ (OFF)}$	f = 1MHz, V_{AH} = 5V, Measured Output to Ground	1	25	-	20	pF
	$C_{D\ (ON)}$	f = 1MHz, V_{AL} = 0V, Measured Output to Ground	1	25	-	30	pF
Drain to Source Capacitance	C_{DS}	f = 1MHz, V_{AH} = 5V	1	25	-	2.0	pF
Off Isolation	V_{ISO}	f = 200kHz, V_A = 2.4, R_L = 1K, V_{GEN} = $1V_{P-P}$, C_L = 10pF	1	25	55	-	dB
Cross Talk	V_{CT}	f = 200kHz, V_A = 2.4, R_L = 1K, V_{GEN} = $1V_{P-P}$, C_L = 10pF	1	25	60	-	dB
Charge Transfer Error	V_{CTE}	f = 200kHz, V_A = 0 to 4V, C_L = 0.01µF	1	25	-10	10	mV

NOTE:

1. Parameters listed in Table 2 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	**SUBGROUPS** (Tables 1 and 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1 (Note 2), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

NOTE:

2. PDA applies to Subgroup 1 only.

Test Circuits

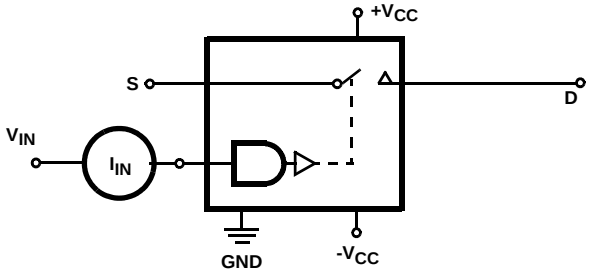


FIGURE 1. INPUT LEAKAGE CURRENT

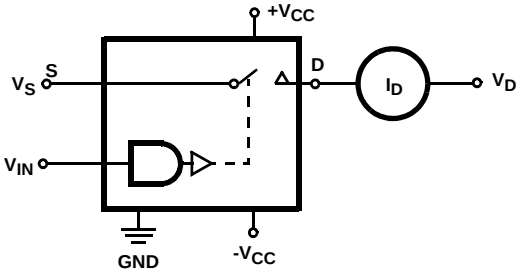


FIGURE 2. $I_{D\ (OFF)}$

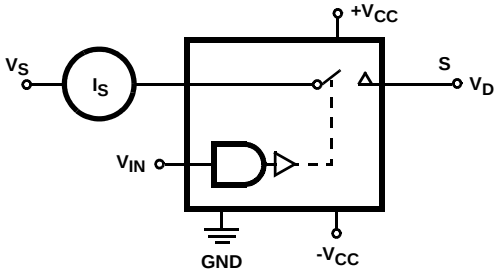


FIGURE 3. $I_{S\ (OFF)}$

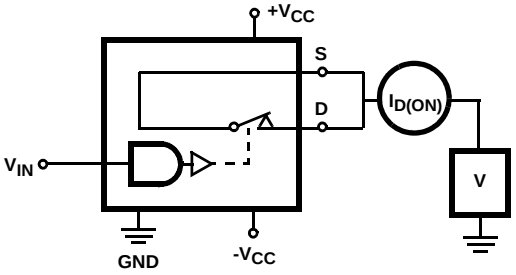


FIGURE 4. $I_{D\ (ON)}$

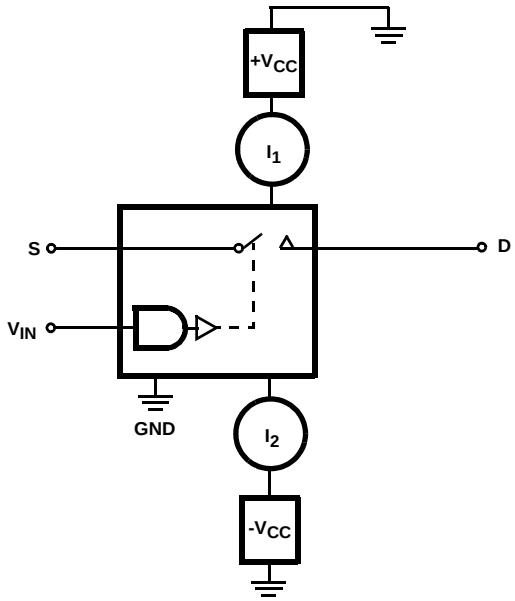


FIGURE 5. SUPPLY CURRENTS

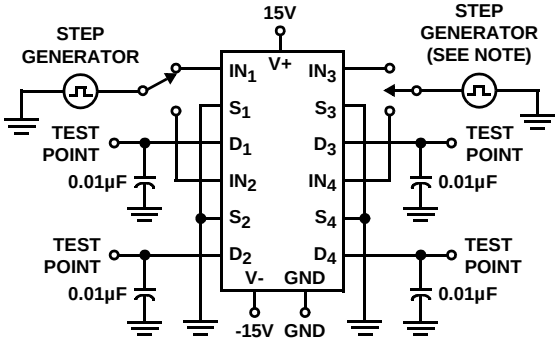


FIGURE 6. CHARGE TRANSFER ERROR

Test Circuits (Continued)

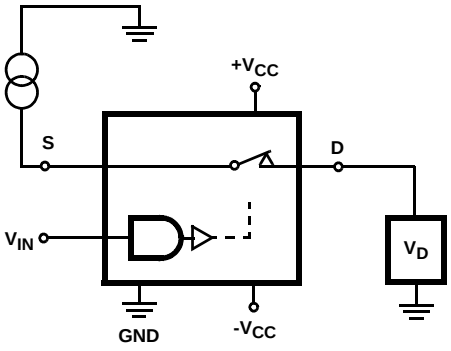


FIGURE 7. R_{DS}

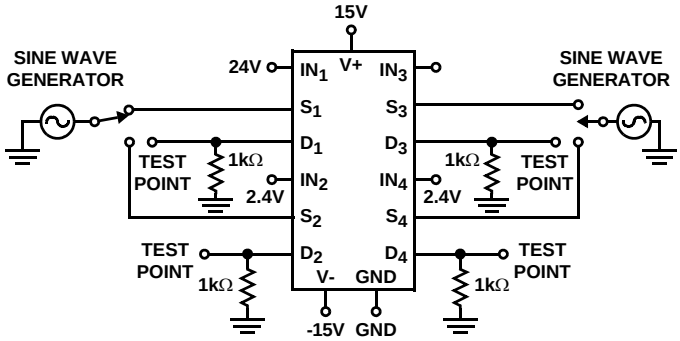


FIGURE 8. OFF CHANNEL ISOLATION

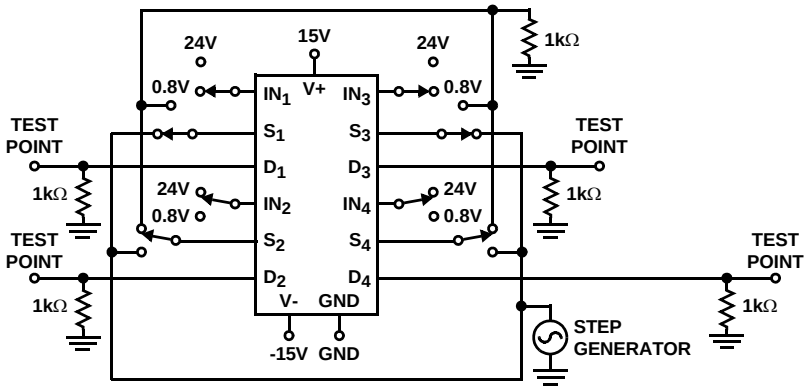


FIGURE 9. CROSSTALK BETWEEN CHANNELS

Switching Waveforms

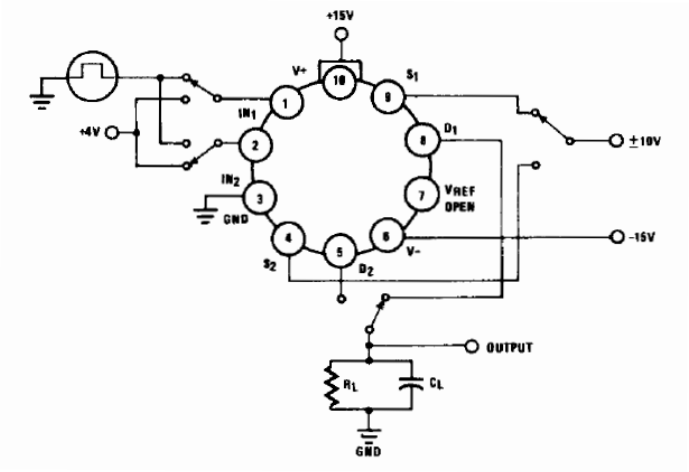


FIGURE 10.

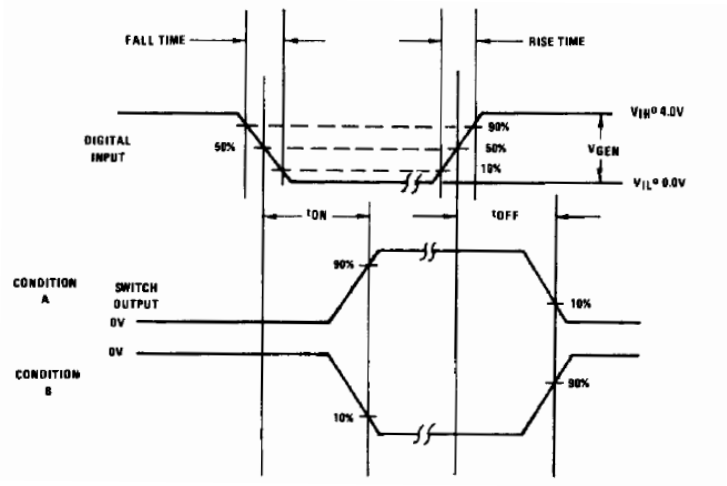


FIGURE 11.

Burn-In Circuit

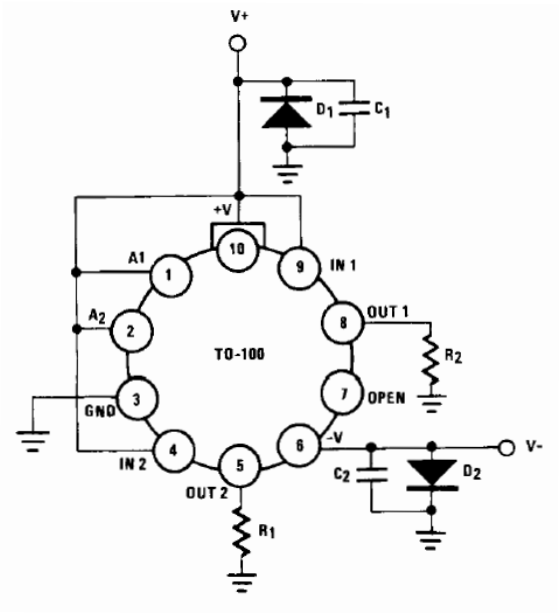


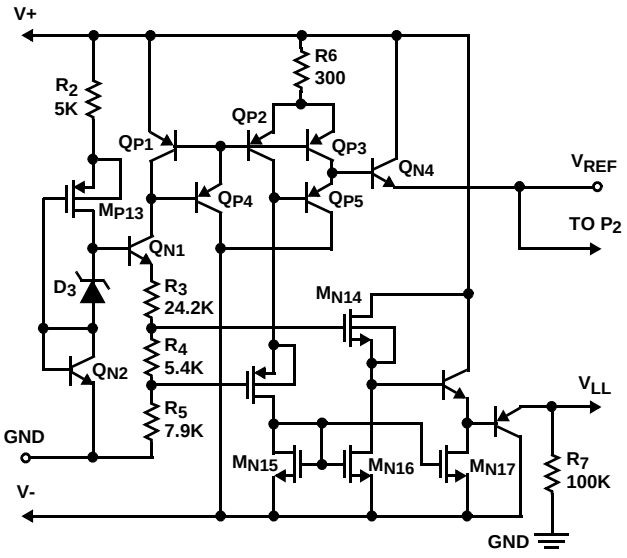
FIGURE 12. HI-200/883 METAL CAN (TO-99)

NOTES:

3. $R_1 = R_2 = 10k\Omega$
4. $C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
5. $D_1 = D_2$ = IN4002 or equivalent
6. $|(V+) - (V-)| = 30V$

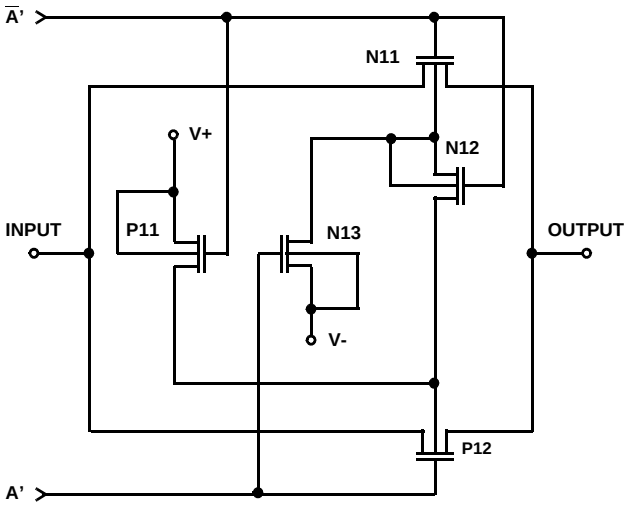
Schematic Diagrams

TTL/CMOS REFERENCE CIRCUIT V_{REF} CELL

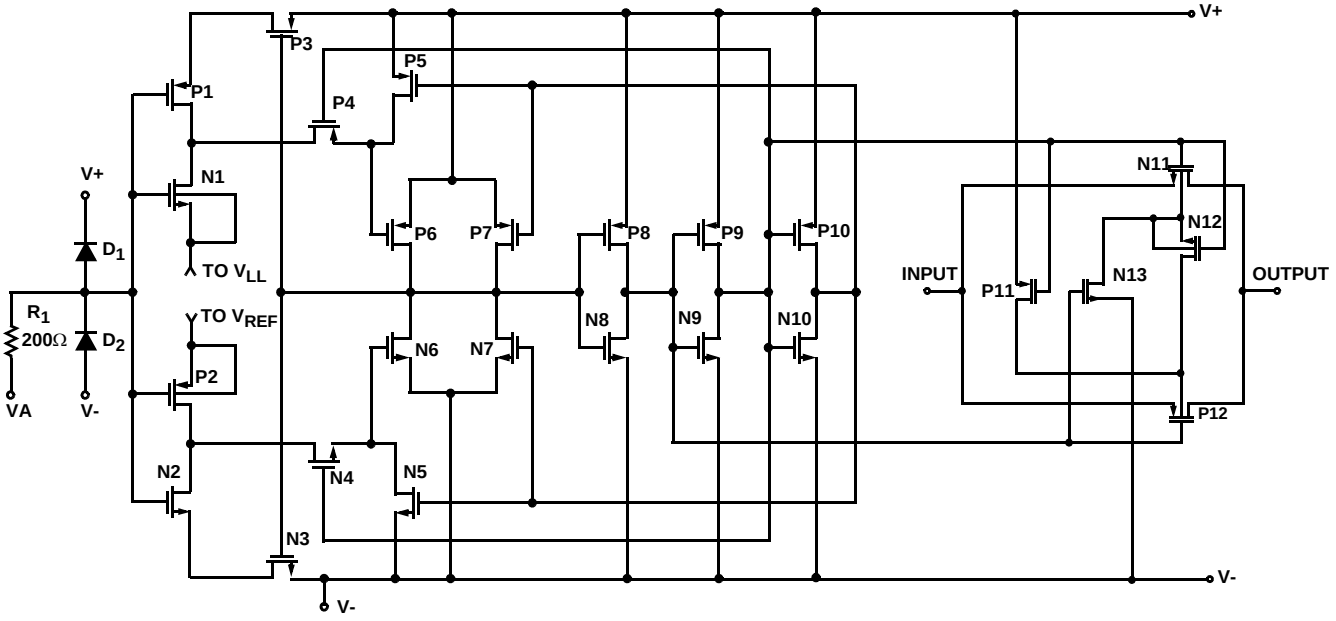


Schematic Diagrams (Continued)

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Test Circuits and Waveforms $T_A = 25°C$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$ and V_{REF} = Open

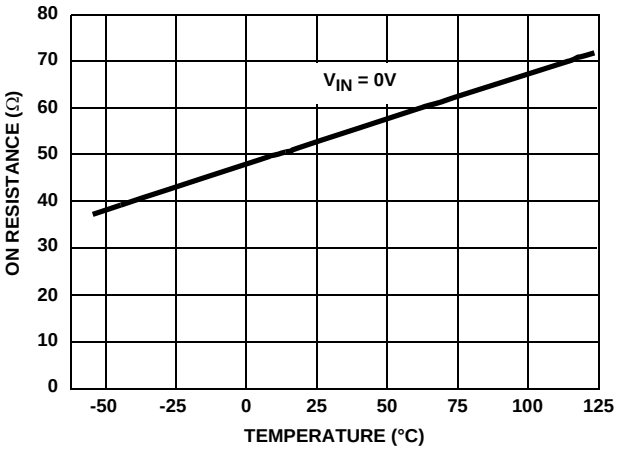


FIGURE 13. ON RESISTANCE vs TEMPERATURE

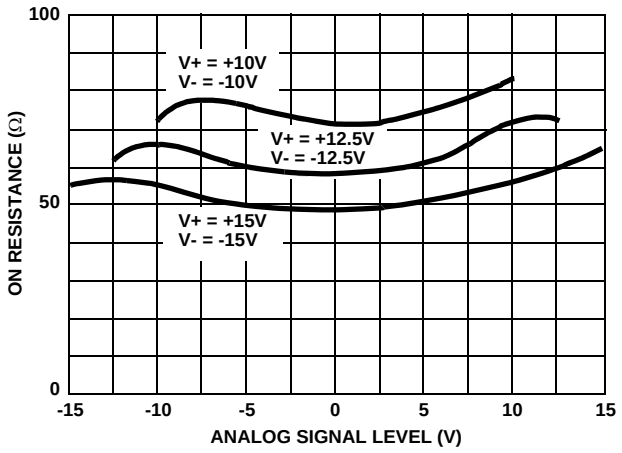


FIGURE 14. ON RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

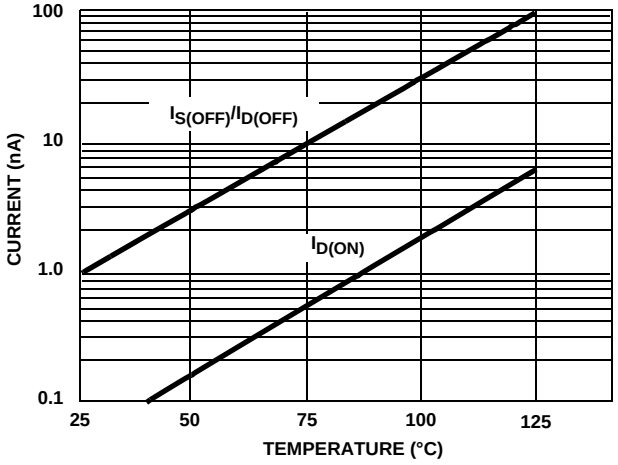


FIGURE 15. LEAKAGE CURRENT vs TEMPERATURE

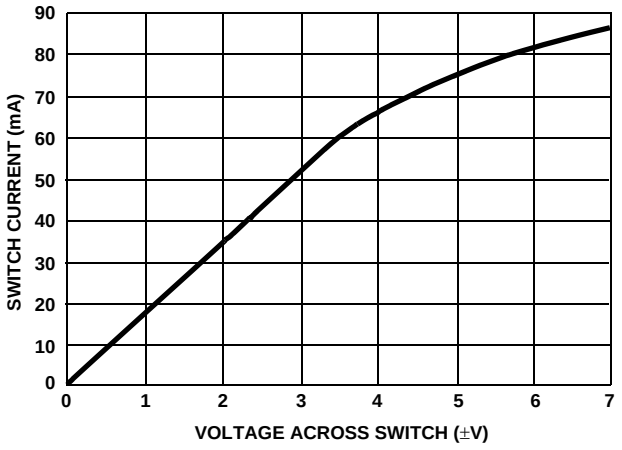


FIGURE 16. SWITCH CURRENT vs VOLTAGE

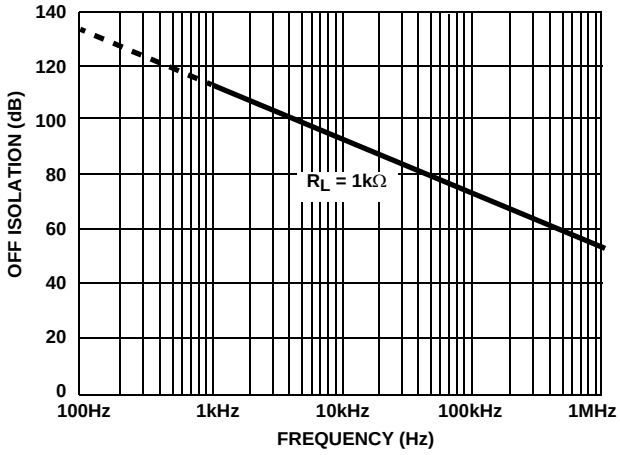


FIGURE 17. OFF ISOLATION vs FREQUENCY

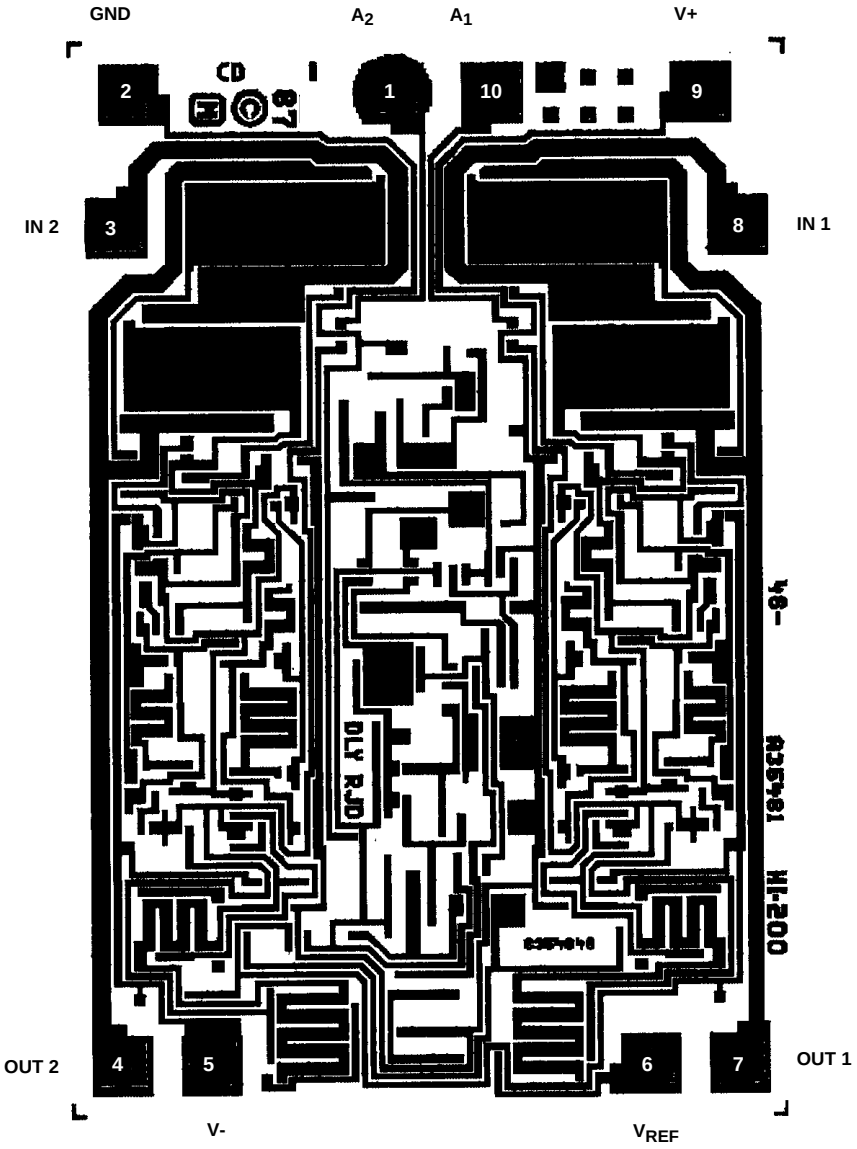
Die Characteristics

DIE ATTACH:

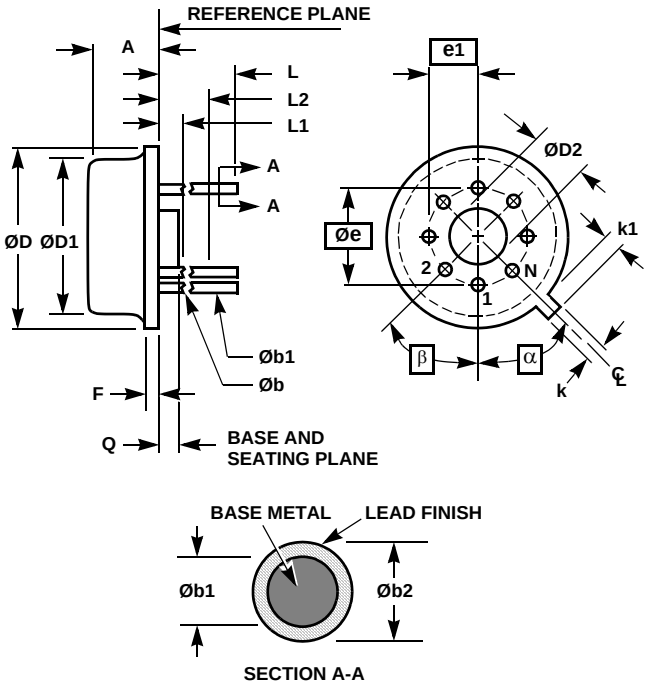
Material: Gold/Silicon Eutectic Alloy
Temperature: Metal Can - 420°C (Max)

Metallization Mask Layout

HI-200



Metal Can Packages (Can)



T10.B MIL-STD-1835 MACY1-X10 (A2)
10 LEAD METAL CAN PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.52	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	0.110	0.160	2.79	4.06	-
e	0.230 BSC		5.84 BSC		-
e1	0.115 BSC		2.92 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	36^{o} BSC		36^{o} BSC		3
β	36^{o} BSC		36^{o} BSC		3
N	10		10		4

Rev. 0 5/18/94

NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.

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