HEF4069UB

Hex inverter

Rev. 8 — 16 November 2011 Product data sheet

1. General description

The HEF4069UB is a general purpose hex inverter. Each inverter has a single stage.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from −40 °C to +85 °C and −40 °C to +125 °C
- Complies with JEDEC standard JESD 13-B

3. Applications

- Oscillator

4. Ordering information

Table 1. Ordering information

All types operate from −40 °C to +125 °C.

Type number	Package		
	Name	Description	Version
HEF4069UBP	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
HEF4069UBT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
HEF4069UBTT	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

5. Functional diagram

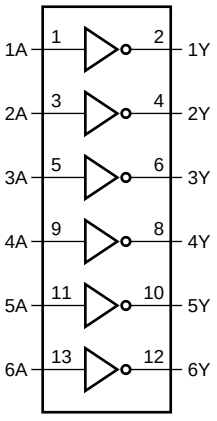


Fig 1. Functional diagram

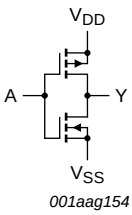


Fig 2. Schematic diagram (one inverter)

6. Pinning information

6.1 Pinning

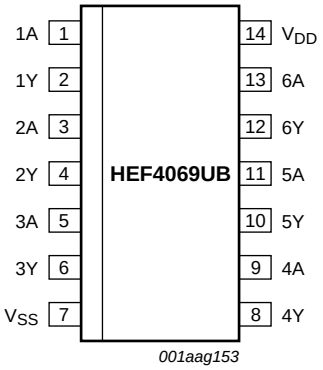


Fig 3. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 6A	1, 3, 5, 9, 11, 13	input
1Y to 6Y	2, 4, 6, 8, 10, 12	output
V_{SS}	7	ground (0 V)
V_{DD}	14	supply voltage

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7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+18	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{DD} + 0.5$ V		-	±10	mA
V_I	input voltage			–0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{DD} + 0.5$ V		-	±10	mA
$I_{I/O}$	input/output current			-	±10	mA
I_{DD}	supply current			-	50	mA
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature			–40	+125	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C				
		DIP14	[1]	-	750	mW
		SO14	[2]	-	500	mW
		TSSOP14	[3]	-	500	mW
P	power dissipation	per output		-	100	mW

[1] For DIP14 packages: above T_{amb} = 70 °C, P_{tot} derates linearly with 12 mW/K.

[2] For SO14 packages: above T_{amb} = 70 °C, P_{tot} derates linearly with 8 mW/K.

[3] For TSSOP14 packages: above T_{amb} = 60 °C, P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	–40	-	+125	°C

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9. Static characteristics

Table 5. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = –40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		T_{amb} = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 μA	5 V	4	-	4	-	4	-	4	-	V
			10 V	8	-	8	-	8	-	8	-	V
			15 V	12.5	-	12.5	-	12.5	-	12.5	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 μA	5 V	-	1	-	1	-	1	-	1	V
			10 V	-	2	-	2	-	2	-	2	V
			15 V	-	2.5	-	2.5	-	2.5	-	2.5	V
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 μA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 μA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	–1.7	-	–1.4	-	–1.1	-	–1.1	mA
		V_O = 4.6 V	5 V	-	–0.64	-	–0.5	-	–0.36	-	–0.36	mA
		V_O = 9.5 V	10 V	-	–1.6	-	–1.3	-	–0.9	-	–0.9	mA
		V_O = 13.5 V	15 V	-	–4.2	-	–3.4	-	–2.4	-	–2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V_O = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I_{DD}	supply current	all valid input combinations; I_O = 0 A	5 V	-	0.25	-	0.25	-	7.5	-	7.5	μA
			10 V	-	0.5	-	0.5	-	15.0	-	15.0	μA
			15 V	-	1.0	-	1.0	-	30.0	-	30.0	μA
C_I	input capacitance	digital inputs		-	-	-	7.5	-	-	-	-	pF

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10. Dynamic characteristics

Table 6. Dynamic characteristics

T_{amb} = 25 °C; for waveforms see Figure 4; for test circuit see Figure 5.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	nA to nY;	5 V	18 ns + (0.55 ns/pF)C_L	-	45	90	ns
			10 V	9 ns + (0.23 ns/pF)C_L	-	20	40	ns
			15 V	7 ns + (0.16 ns/pF)C_L	-	15	25	ns
t_{PLH}	LOW to HIGH propagation delay	nA to nY	5 V	13 ns + (0.55 ns/pF)C_L	-	40	80	ns
			10 V	9 ns + (0.23 ns/pF)C_L	-	20	40	ns
			15 V	7 ns + (0.16 ns/pF)C_L	-	15	30	ns
t_{THL}	HIGH to LOW output transition time	output nY	5 V	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C_L	-	20	40	ns
t_{TLH}	LOW to HIGH output transition time	output nY	5 V	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C_L	-	20	40	ns

[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

Table 7. Dynamic power dissipation

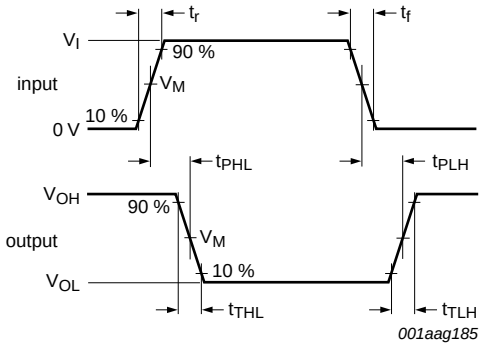
V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula	Where
P_D	dynamic power dissipation	5 V	$P_D = 600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	f_i = input frequency in MHz;
		10 V	$P_D = 4000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	f_o = output frequency in MHz;
		15 V	$P_D = 22000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	C_L = output load capacitance in pF; $\Sigma(f_o \times C_L)$ = sum of the outputs; V_{DD} = supply voltage in V.

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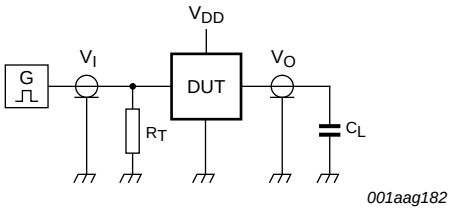
11. Waveforms



Measurement points: $V_M = 0.5V_{DD}$.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. Propagation delay and transition times



Definitions for test circuit:

C_L = load capacitance including jig and probe capacitance;

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator;

For test data refer to Table 8.

Fig 5. Test circuit for measuring switching times

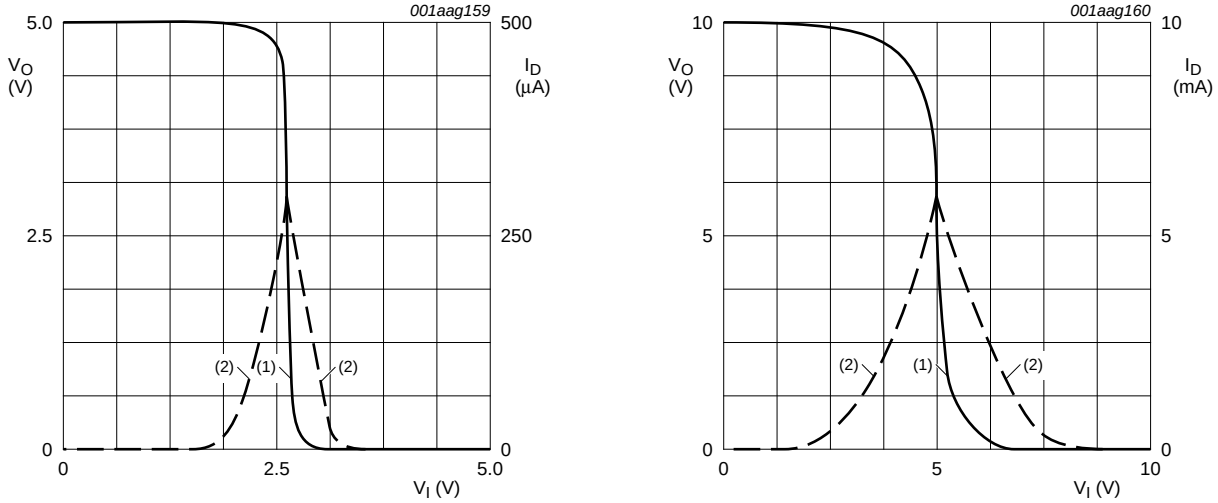
Table 8. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

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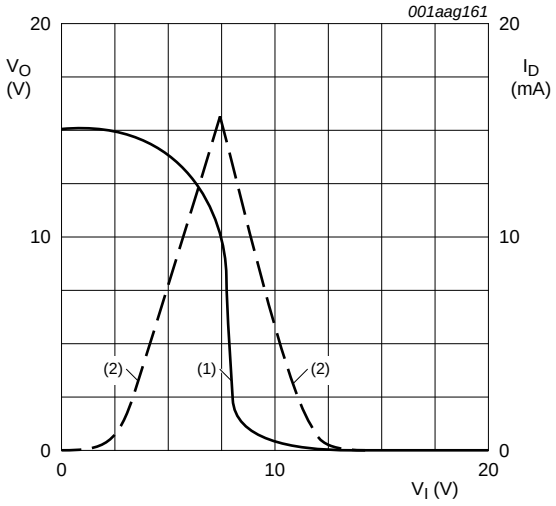
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11.1 Transfer characteristics



a. V_{DD} = 5 V; I_O = 0 A

b. V_{DD} = 10 V; I_O = 0 A



c. V_{DD} = 15 V; I_O = 0 A

(1) V_O = output voltage.

(2) I_D = drain current.

Fig 6. Typical transfer characteristics

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12. Application information

Some examples of applications for the HEF4069UB.

Figure 7 shows an astable relaxation oscillator using two HEF4069UB inverters and 2 BAW62 diodes. The oscillation frequency is mainly determined by R1 × C1, provided R1 << R2 and R2 × C2 << R1 × C1.

The function of R2 is to minimize the influence of the forward voltage across the protection diodes on the frequency; C2 is a stray (parasitic) capacitance.

The period T_p is given by $T_p = T_1 + T_2$,

where:

$$T_1 = R1C1In\frac{V_{DD} + V_{ST}}{V_{ST}}$$

$$T_2 = R1C1In\frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}}$$

V_{ST} = the signal threshold level of the inverter.

The period is fairly independent of V_{DD}, V_{ST} and temperature. The duty factor, however, is influenced by V_{ST}.

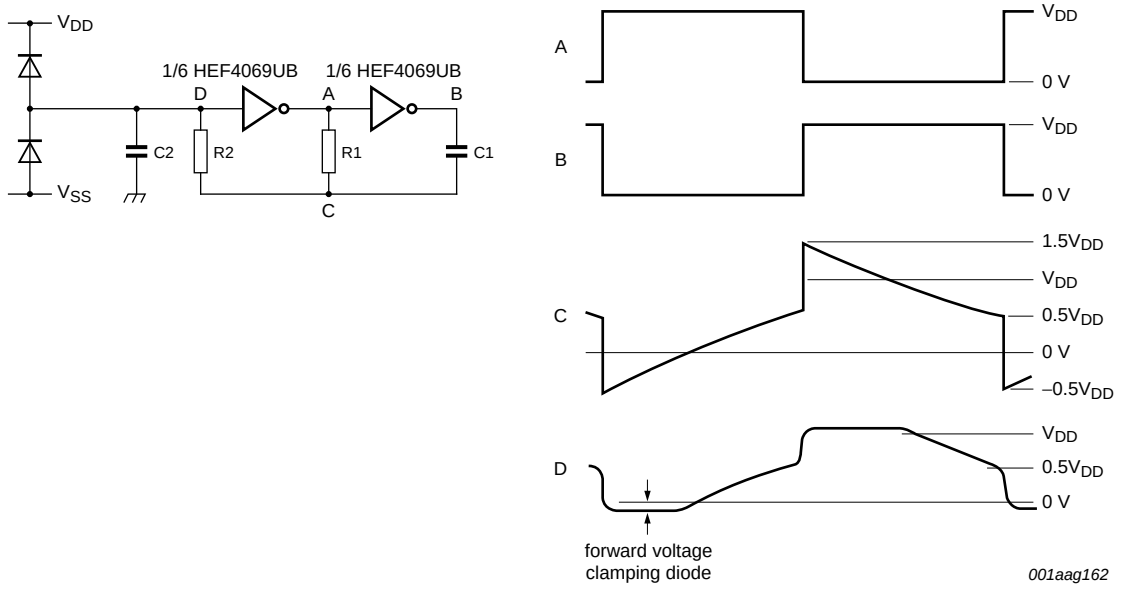
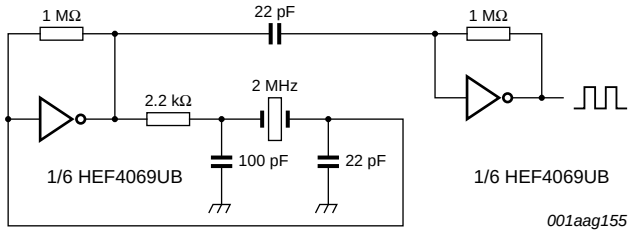


Fig 7. Astable relaxation oscillator

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Figure 8 shows a crystal oscillator for frequencies up to 10 MHz using two HEF4069UB inverters. The second inverter amplifies the oscillator output voltage to a level sufficient to drive other Local Oxidation CMOS (LOCMOS) circuits.



The output inverter is used to amplify the oscillator output voltage to a level sufficient to drive other LOCMOS circuits.

Fig 8. Crystal oscillator

Figure 9 and Figure 10 show voltage gain and supply current. Figure 11 shows the test set-up and an example of an analog amplifier using one HEF4069UB.

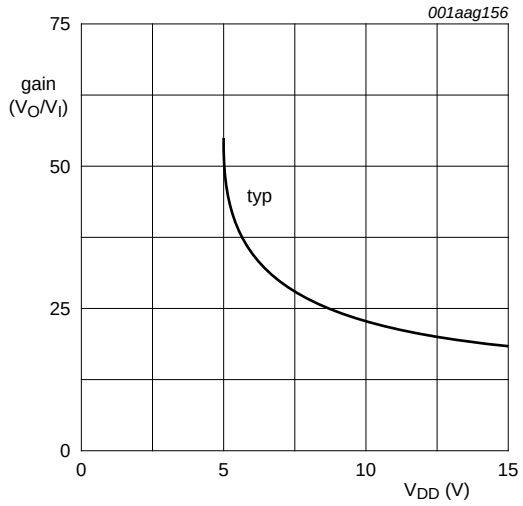


Fig 9. Typical voltage gain as a function of supply voltage

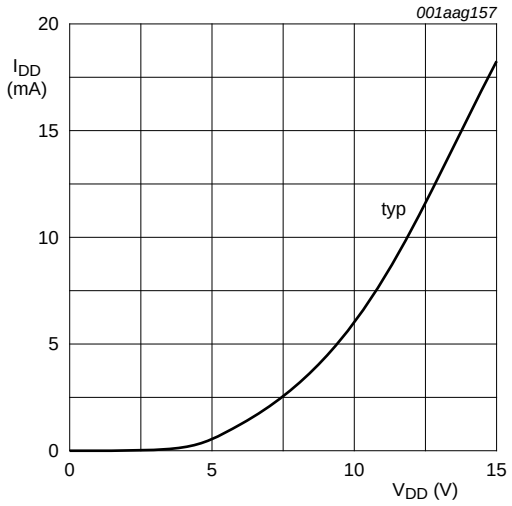


Fig 10. Typical supply current as a function of supply voltage

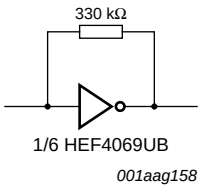
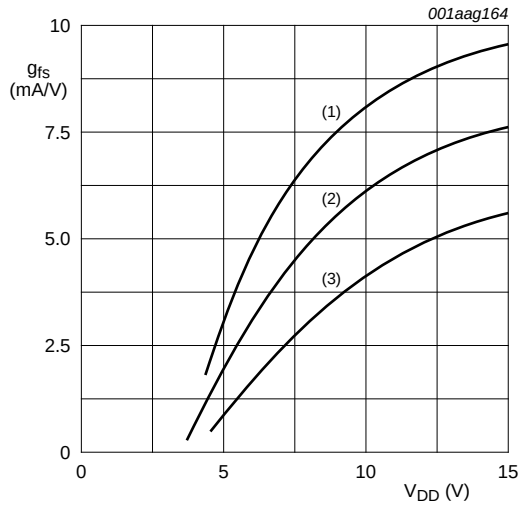


Fig 11. Test set-up

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Figure 12 shows typical forward transconductance and Figure 13 shows the test set-up.

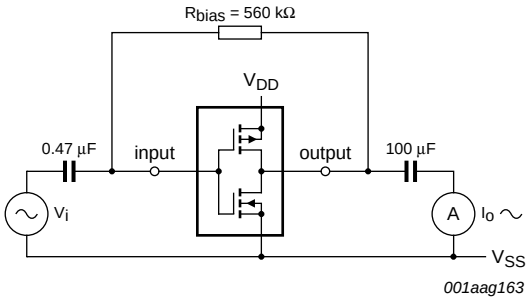


(1) Average +2σ; where: 'σ' is the standard deviation.

(2) Average.

(3) Average −2σ; where: 'σ' is the standard deviation.

Fig 12. Typical forward transconductance as a function of supply voltage at T_{amb} = 25 °C



$$g_{fs} = \frac{dI_o}{dV_i}$$ at V_O is constant.

f_i = 1 kHz

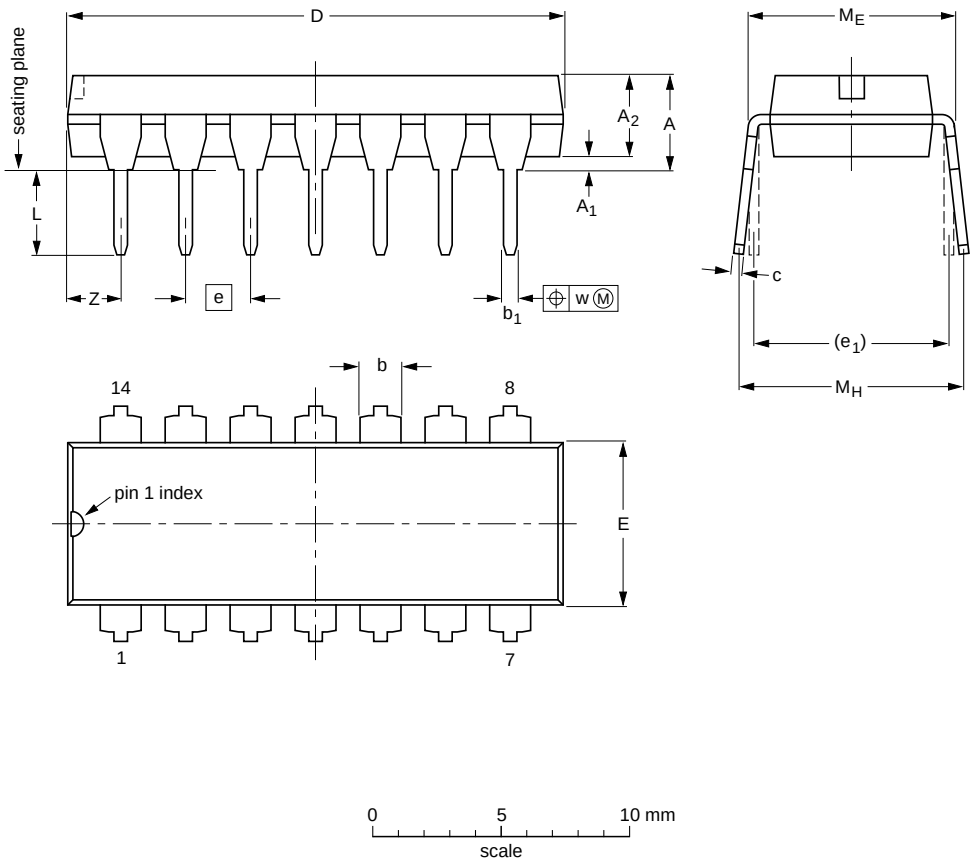
Fig 13. Test set-up

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13. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

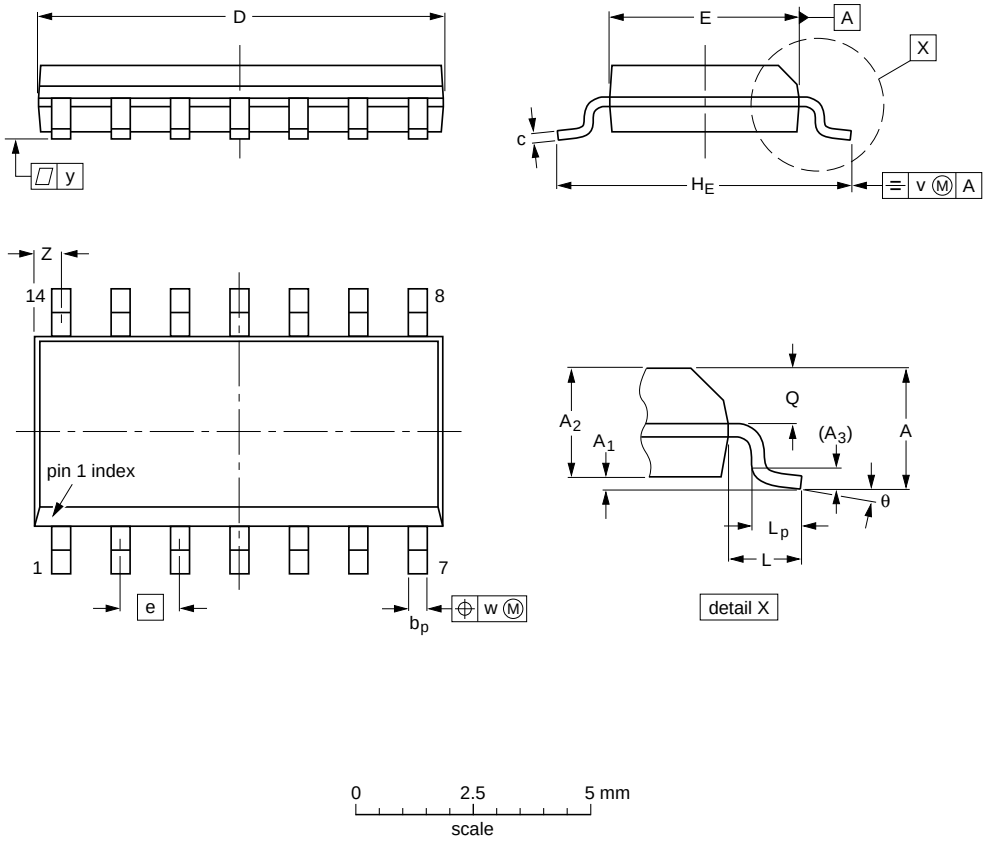
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 14. Package outline SOT27-1 (DIP14)

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SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

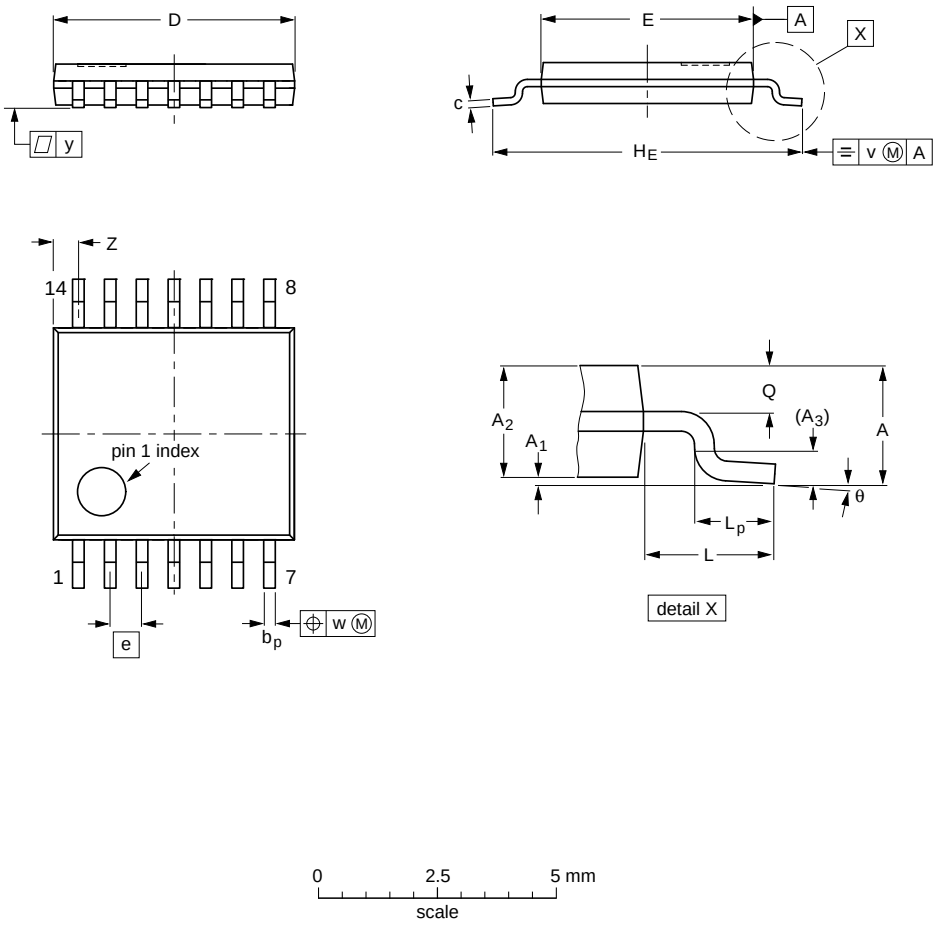
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 15. Package outline SOT108-1 (SO14)

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 16. Package outline SOT402-1 (TSSOP14)

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14. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4069UB v.8	20111116	Product data sheet	-	HEF4069UB v.7
Modifications:	• Legal pages updated. • Changes in “General description”, “Features and benefits” and “Applications”.			
HEF4069UB v.7	20110511	Product data sheet	-	HEF4069UB v.6
HEF4069UB v.6	20091208	Product data sheet	-	HEF4069UB v.5
HEF4069UB v.5	20090723	Product data sheet	-	HEF4069UB v.4
HEF4069UB v.4	20080704	Product data sheet	-	HEF4069UB_CNV v.3
HEF4069UB_CNV v.3	19950101	Product specification	-	HEF4069UB_CNV v.2
HEF4069UB_CNV v.2	19950101	Product specification	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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