HD74LVC533

Octal D-type Transparent Latches with 3-state Outputs

REJ03D0356–0400Z
(Previous ADE-205-070B (Z))
Rev.4.00
Jul. 27, 2004

Description

The HD74LVC533 has eight D type latches with three state outputs in a 20 pin package. When the latch enable input is high, the Q outputs will follow the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. Low voltage and high-speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- V_{CC} = 2.0 V to 5.5 V
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.0 V (@V_{CC} = 3.3 V, Ta = 25°C)
- High output current ±24 mA (@V_{CC} = 3.0 V to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LVC533FPEL	SOP–20 pin (JEITA)	FP–20DAV	FP	EL (2,000 pcs/reel)
HD74LVC533TELL	TSSOP–20 pin	TTP–20DAV	T	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

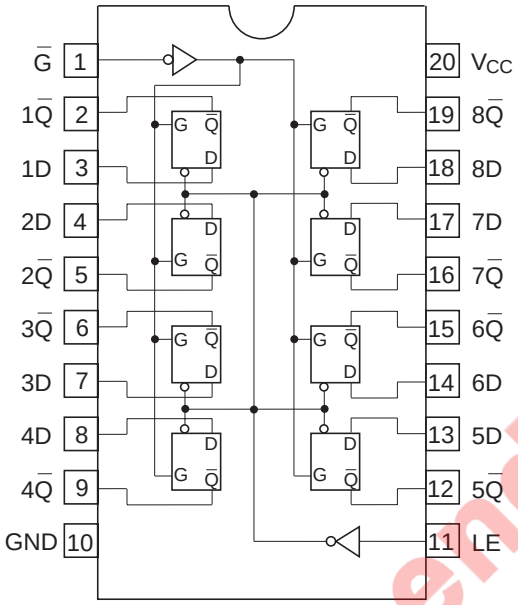
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Function Table

Inputs			
$\overline{G}$	LE	D	Output $\overline{Q}$
H	X	X	Z
L	H	L	H
L	H	H	L
L	L	X	Q_0

H: High level
L: Low level
X: Immaterial
Z: High impedance
Q_0: Level of $\overline{Q}$ before the indicated steady input conditions were established.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to 6.0	V	
Input diode current	I_{IK}	–50	mA	V_I = –0.5 V
Input voltage	V_I	–0.5 to 6.0	V	
Output diode current	I_{OK}	–50	mA	V_O = –0.5 V
		50		V_O = V_{CC}+0.5 V
Output voltage	V_O	–0.5 to V_{CC} +0.5	V	
Output current	I_O	±50	mA	
V_{CC}, GND current / pin	I_{CC} or I_{GND}	100	mA	
Storage temperature	Tstg	–65 to +150	°C	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

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Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	1.5 to 5.5	V	Data retention
		2.0 to 5.5		At operation
Input / output voltage	V_I	0 to 5.5	V	$\overline{G}$, LE, D
	V_O	0 to V_{CC}	V	$\overline{Q}$
Operating temperature	Ta	–40 to 85	°C	
Output current	I_{OH}	–12	mA	V_{CC} = 2.7 V
		–24 *2		V_{CC} = 3.0 V to 5.5 V
	I_{OL}	12	mA	V_{CC} = 2.7 V
		24 *2		V_{CC} = 3.0 V to 5.5 V
Input rise / fall time *1	t_r, t_f	10	ns/V	

Notes: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.
2. Duty cycle ≤ 50%

Electrical Characteristics

			Ta = –40 to 85°C			
Item	Symbol	V_{CC} (V)	Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.7 to 3.6	2.0	—	V	
		4.5 to 5.5	V_{CC}×0.7	—		
	V_{IL}	2.7 to 3.6	—	0.8	V	
		4.5 to 5.5	—	V_{CC}×0.3		
Output voltage	V_{OH}	2.7 to 5.5	V_{CC}–0.2	—	V	I_{OH} = –100 µA
		2.7	2.2	—		I_{OH} = –12 mA
		3.0	2.4	—		
		3.0	2.0	—		I_{OH} = –24 mA
		4.5	3.8	—		
	V_{OL}	2.7 to 5.5	—	0.2	V	I_{OL} = 100 µA
		2.7	—	0.4		I_{OL} = 12 mA
		3.0	—	0.55		I_{OL} = 24 mA
		4.5	—	0.55		
Input current	I_{IN}	0 to 5.5	—	±5.0	µA	V_{IN} = 5.5 V or GND
Off state output current	I_{OZ}	5.5	—	±10	µA	V_{IN} = V_{CC}, GND V_{OUT} = V_{CC} or GND
Quiescent supply current	I_{CC}	5.5	—	20	µA	V_{IN} = V_{CC} or GND
	ΔI_{CC}	3.0 to 3.6	—	500	µA	V_{IN} = one input at(V_{CC}–0.6)V, other inputs at V_{CC} or GND

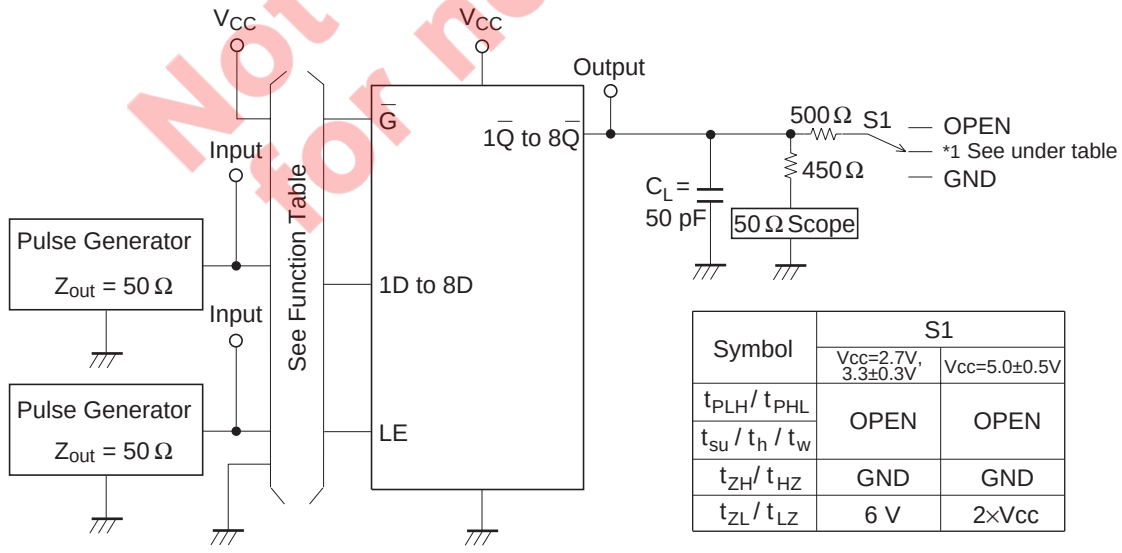
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Switching Characteristics

Item	Symbol	V_{CC} (V)	Ta = –40 to 85°C Min	Typ	Max	Unit	From (Input)	To (Output)
Propagation delay time	t_{PLH}	2.7	—	7.0	9.0	ns	D	$\overline{Q}$
	t_{PHL}	3.3±0.3	1.5	5.0	8.0			
		5.0±0.5	—	4.0	6.5			
	t_{PLH}	2.7	—	7.5	10.5	ns	LE	$\overline{Q}$
	t_{PHL}	3.3±0.3	1.5	5.5	9.5			
		5.0±0.5	—	4.0	8.0			
Output enable time	t_{ZH}	2.7	—	7.5	9.5	ns	$\overline{G}$	$\overline{Q}$
	t_{ZL}	3.3±0.3	1.5	5.5	8.5			
		5.0±0.5	—	4.0	7.0			
Output disable time	t_{HZ}	2.7	—	5.0	8.5	ns	$\overline{G}$	$\overline{Q}$
	t_{LZ}	3.3±0.3	1.5	4.5	7.5			
		5.0±0.5	—	3.5	6.5			
Setup time	t_{su}	2.7	2.0	—	—	ns		
		3.3±0.3	2.0	—	—			
		5.0±0.5	2.0	—	—			
Hold time	t_h	2.7	2.0	—	—	ns		
		3.3±0.3	2.0	—	—			
		5.0±0.5	2.0	—	—			
Pulse width	t_w	2.7	4.0	—	—	ns		
		3.3±0.3	4.0	—	—			
		5.0±0.5	4.0	—	—			
Input capacitance	C_{IN}	2.7	—	3.0	—	pF		
Output capacitance	C_O	2.7	—	15.0	—	pF		

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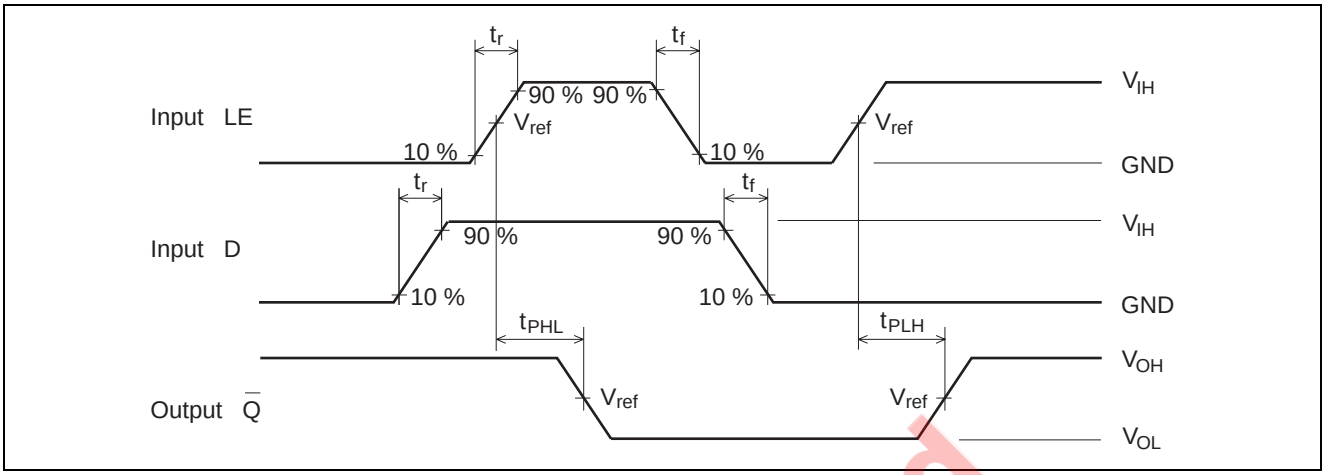
Test Circuit



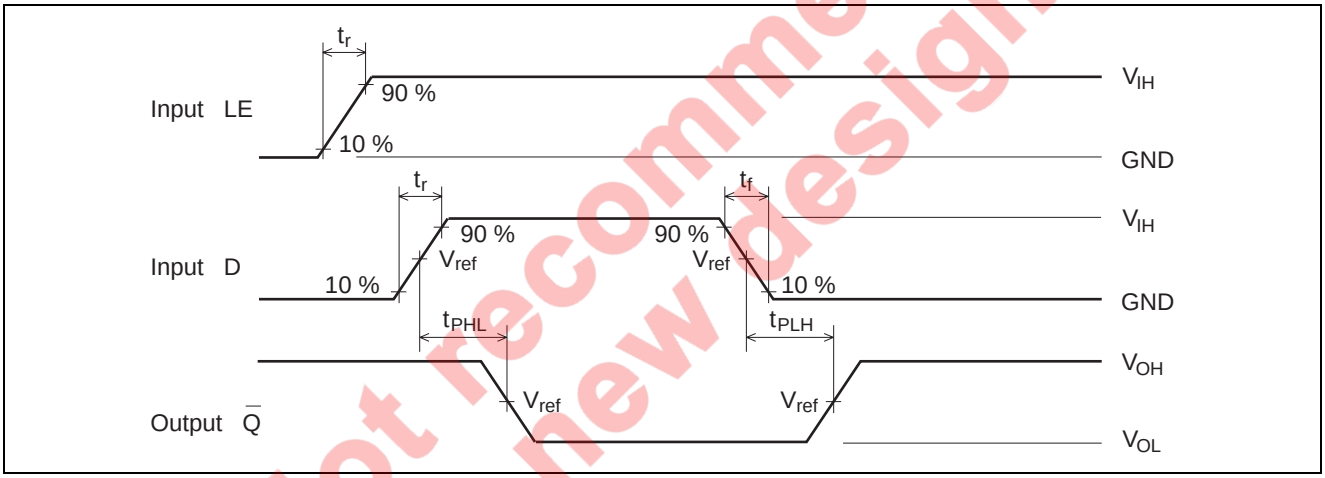
Symbol	S1 Vcc=2.7V, 3.3±0.3V	S1 Vcc=5.0±0.5V
t_{PLH} / t_{PHL}	OPEN	OPEN
t_{su} / t_h / t_w		
t_{ZH} / t_{HZ}	GND	GND
t_{ZL} / t_{LZ}	6 V	2×Vcc

Note: 1. C_L includes probe and jig capacitance.

Waveforms – 1

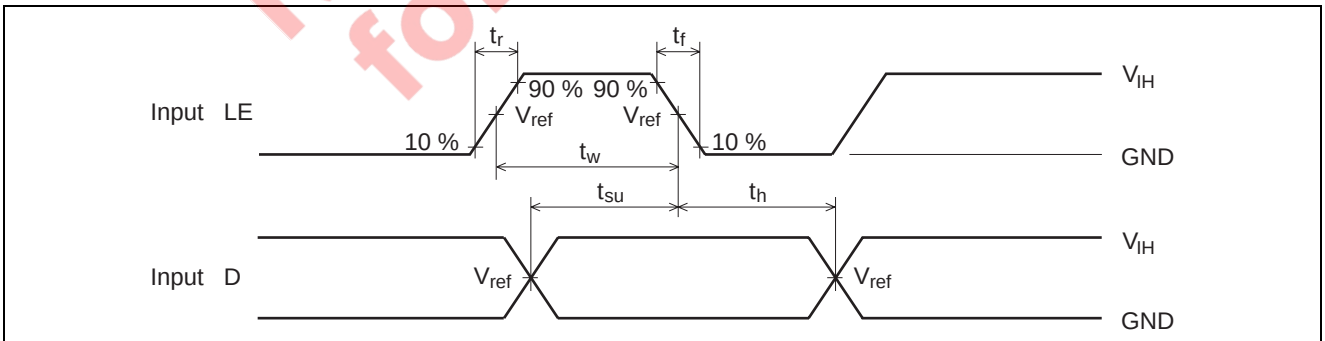


Waveforms – 2



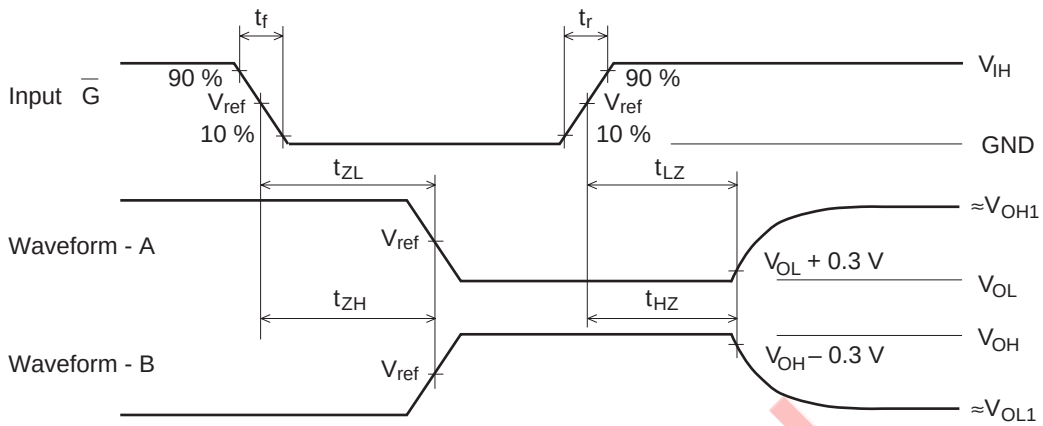
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Waveforms – 3



Notes: 1. t_r = 2.5 ns, t_f = 2.5 ns
2. Input waveform : PRR = 10 MHz, duty cycle 50%

Waveforms – 4



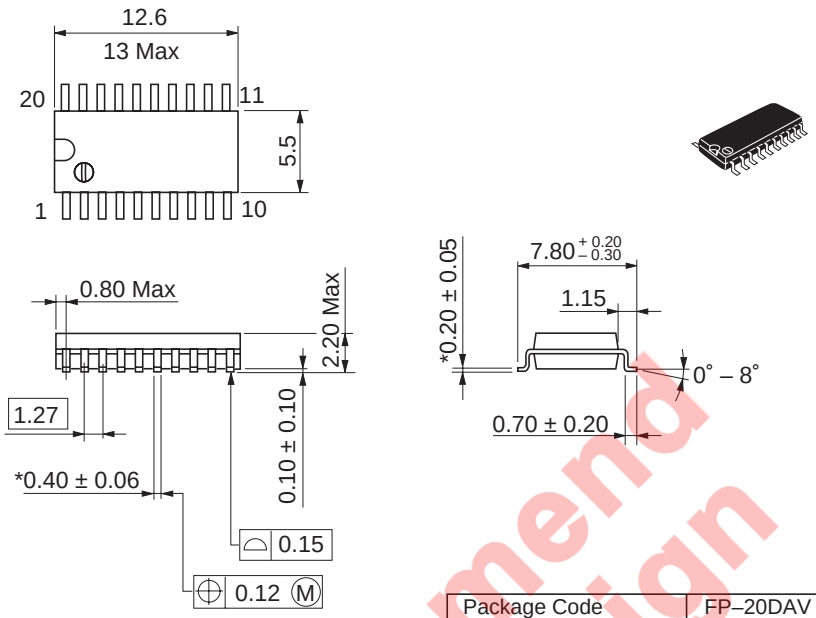
TEST	Vcc=2.7V, 3.3±0.3V	Vcc=5.0±0.5V
V_{IH}	2.7 V	Vcc
V_{ref}	1.5 V	50%Vcc
V_{OH1}	3 V	Vcc
V_{OL1}	GND	GND

Notes:
1. t_r = 2.5 ns, t_f = 2.5 ns
2. Input waveform : PRR = 10 MHz, duty cycle 50%
3. Waveform – A shows input conditions such that the output is "L" level when enable by the output control.
4. Waveform – B shows input conditions such that the output is "H" level when enable by the output control.

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Package Dimensions

As of January, 2002
Unit: mm

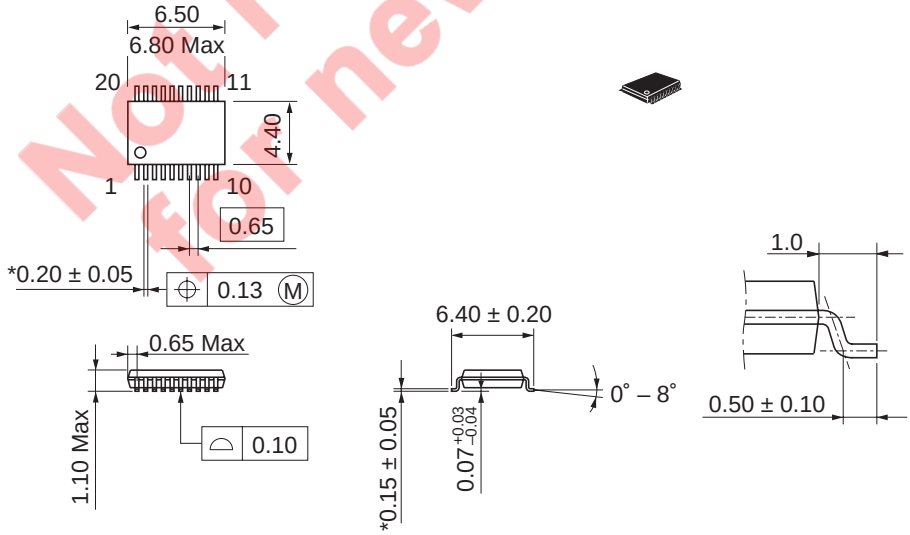


Package Code	FP–20DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.31 g

*Pd plating

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As of January, 2002
Unit: mm



Package Code	TTP–20DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.07 g

*Pd plating

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