

HD74LV4053A

Triple 2-channel Analog Multiplexer / Demultiplexer

REJ03D0339-0300Z
(Previous ADE-205-284A (Z))
Rev.3.00
Jul. 21, 2004

Description

The HD74LV4053A handles both analog and digital signals, and enables signals of either type with amplitudes of up to 5.5 V (peak) to be transmitted in either direction (at $V_{CC} = 0$ V to 5.5 V).

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Features

- $V_{CC} = 2.0$ V to 5.5 V operation
- All control inputs V_{IH} (Max.) = 5.5 V (@ $V_{CC} = 0$ V to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV4053AFPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74LV4053ARPEL	SOP-16 pin (JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)
HD74LV4053ATELL	TSSOP-16 pin	TTP-16DAV	T	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

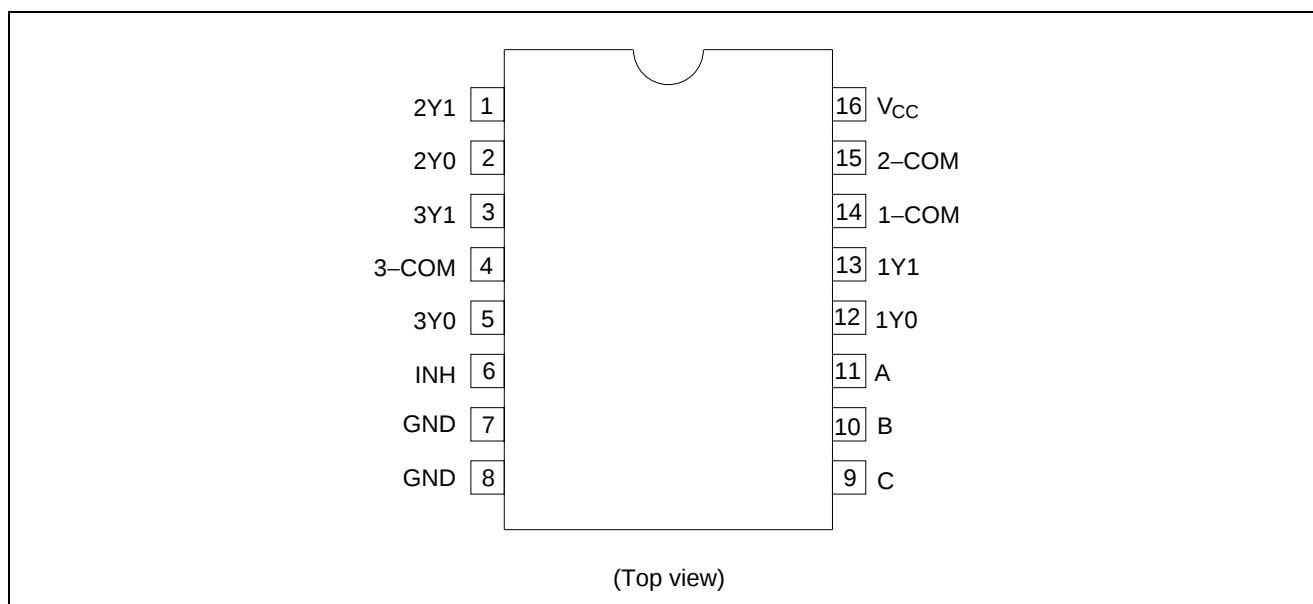
Function Table

Inputs

INH	C	B	A	On Channel
L	L	L	L	1Y0, 2Y0, 3Y0
L	L	L	H	1Y1, 2Y0, 3Y0
L	L	H	L	1Y0, 2Y1, 3Y0
L	L	H	H	1Y1, 2Y1, 3Y0
L	H	L	L	1Y0, 2Y0, 3Y1
L	H	L	H	1Y1, 2Y0, 3Y1
L	H	H	L	1Y0, 2Y1, 3Y1
L	H	H	H	1Y1, 2Y1, 3Y1
H	X	X	X	NONE

Note: H: High level
L: Low level
X: Immaterial

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range* ¹	V_I	-0.5 to 7.0	V	
Output voltage range* ^{1, 2}	V_O	-0.5 to $V_{CC} + 0.5$	V	Output: H or L
Input clamp current	I_{IK}	-20	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±25	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±50	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* ³	P_T	785	mW	SOP
		500		TSSOP
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

1. The input and output voltage ratings may be exceeded even if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

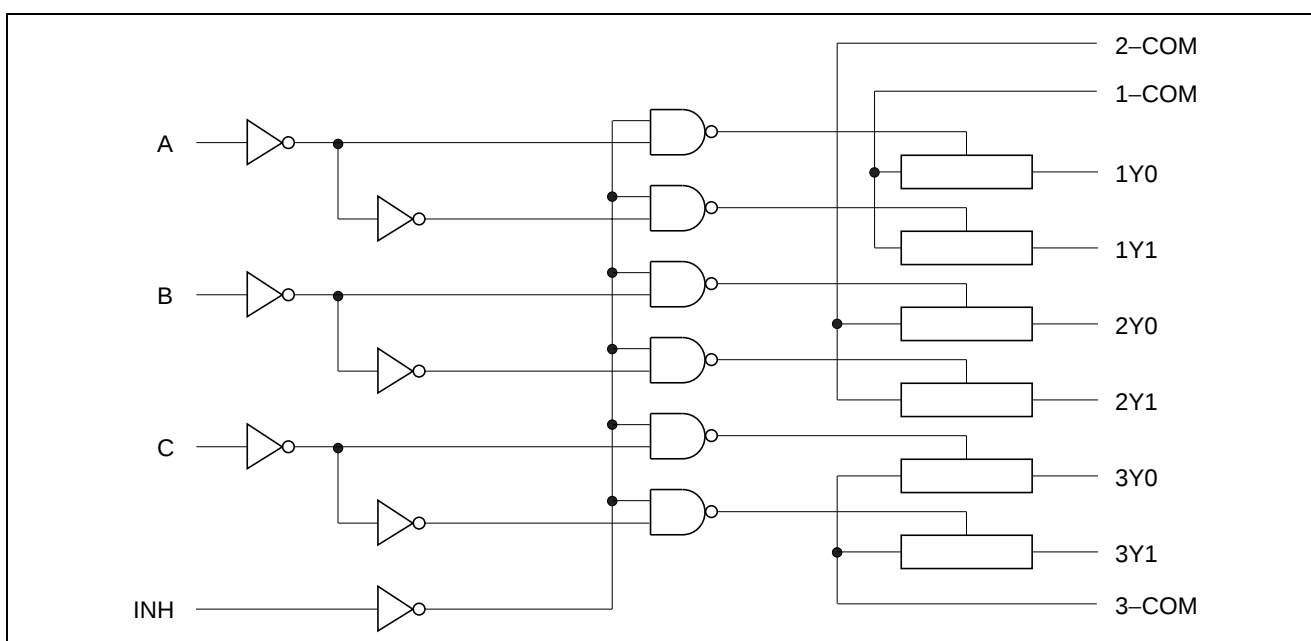
Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0* ¹	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_{IO}	0	V_{CC}	V	
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3 \text{ to } 2.7 \text{ V}$
		0	100		$V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$
		0	20		$V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$
Operating free-air temperature	T_a	-40	85	°C	

Notes: Unused or floating control inputs must be held high or low.

1. With the supply voltage at or around 2 V, the analog switch on-state resistance loses linearity significantly. It is recommended that only digital signals be transmitted at these low supply voltages.

Logic Diagram



DC Electrical Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Input voltage	V _{IH}	2.0	—	—	—	1.5	—	V	Control input only
		2.3 to 2.7	—	—	—	V _{CC} × 0.7	—		
		3.0 to 3.6	—	—	—	V _{CC} × 0.7	—		
		4.5 to 5.5	—	—	—	V _{CC} × 0.7	—		
	V _{IL}	2.0	—	—	—	—	0.5		
		2.3 to 2.7	—	—	—	—	V _{CC} × 0.3		
		3.0 to 3.6	—	—	—	—	V _{CC} × 0.3		
		4.5 to 5.5	—	—	—	—	V _{CC} × 0.3		
On-state switch resistance	R _{ON}	2.3	—	60	180	—	225	Ω	V _{IN} = V _{CC} or GND
		3.0	—	50	150	—	190		V _{INH} = V _{IL}
		4.5	—	40	75	—	100		I _T = 2 mA
Peak on resistance	R _{ON (P)}	2.3	—	200	500	—	600	Ω	V _{IN} = V _{CC} to GND
		3.0	—	90	180	—	225		V _{INH} = V _{IL}
		4.5	—	50	100	—	125		I _T = 2 mA
Difference of on-state resistance between switches	ΔR _{ON}	2.3	—	20	30	—	40	Ω	V _{IN} = V _{CC} to GND
		3.0	—	10	20	—	30		V _{INH} = V _{IL}
		4.5	—	7	15	—	20		I _T = 2 mA
Off-state switch leakage current	I _s (OFF)	5.5	—	—	±0.1	—	±1.0	μA	V _{IN} = V _{CC} , V _{OUT} = GND or V _{IN} = GND, V _O = V _{CC} , V _{INH} = V _{IH}
On-state switch leakage current	I _s (ON)	5.5	—	—	±0.1	—	±1.0	μA	V _{IN} = V _{CC} or GND V _{INH} = V _{IL}
Input current	I _{IN}	0 to 5.5	—	—	±0.1	—	±1.0	μA	V _{IN} = 5.5 V or GND
Quiescent supply current	I _{CC}	5.5	—	—	—	—	20	μA	V _{IN} = V _{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

$$V_{CC} = 2.5 \pm 0.2 \text{ V}$$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	2.5	10.0	—	16.0	ns	C _L = 15 pF	COM or Yn	Yn or COM
	t _{PHL}	—	5.0	12.0	—	18.0		C _L = 50 pF		
Enable time	t _{ZH}	—	7.0	18.0	—	23.0	ns	R _L = 1 kΩ C _L = 15 pF	INH	COM or Yn
	t _{ZL}	—	9.0	28.0	—	35.0				
Disable time	t _{HZ}	—	9.0	18.0	—	23.0	ns	R _L = 1 kΩ C _L = 15 pF	INH	COM or Yn
	t _{LZ}	—	13.0	28.0	—	35.0				

$$V_{CC} = 3.3 \pm 0.3 \text{ V}$$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	2.0	6.0	—	10.0	ns	C _L = 15 pF	COM or Yn	Yn or COM
	t _{PHL}	—	4.0	9.0	—	12.0		C _L = 50 pF		
Enable time	t _{ZH}	—	5.0	12.0	—	15.0	ns	R _L = 1 kΩ C _L = 15 pF	INH	COM or Yn
	t _{ZL}	—	7.0	20.0	—	25.0				
Disable time	t _{HZ}	—	7.0	12.0	—	15.0	ns	R _L = 1 kΩ C _L = 15 pF	INH	COM or Yn
	t _{LZ}	—	10.0	20.0	—	25.0				

$$V_{CC} = 5.0 \pm 0.5 \text{ V}$$

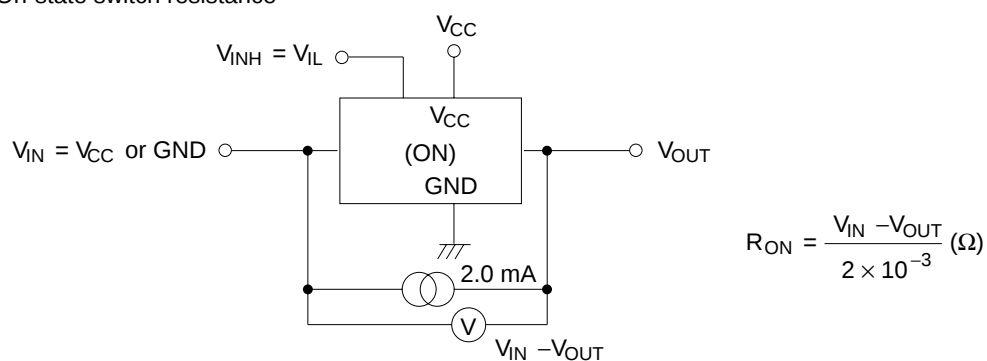
Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	1.5	4.0	—	7.0	ns	C _L = 15 pF	COM or Yn	Yn or COM
	t _{PHL}	—	3.0	6.0	—	8.0		C _L = 50 pF		
Enable time	t _{ZH}	—	4.0	8.0	—	10.0	ns	R _L = 1 kΩ C _L = 15 pF	INH	COM or Yn
	t _{ZL}	—	5.0	14.0	—	18.0				
Disable time	t _{HZ}	—	5.0	8.0	—	10.0	ns	R _L = 1 kΩ C _L = 15 pF	INH	COM or Yn
	t _{LZ}	—	8.0	14.0	—	18.0				

Switching Characteristics (cont.)

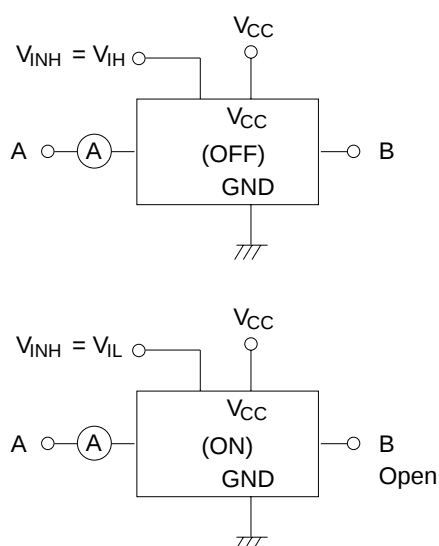
Item	Symbol	V _{CC} (V)	Ta = 25°C			Unit	Test Conditions	FROM (Input)	TO (Output)
			Min	Typ	Max				
Control input capacitance	C _{IC}	—	—	4.5	—	pF			
Common terminal capacitance	C _{IS}	—	—	12.5	—	pF			
Switch terminal capacitance	C _{I/O}	—	—	7.0	—	pF			
Feedthrough capacitance	C _T	—	—	0.5	—	pF			
Power dissipation capacitance	C _{PD}	—	—	9.0	—	pF			
Frequency response (Switch ON)		2.3	—	30.0	—	MHz	C _L = 50 pF, R _L = 600 Ω Adjust f _{in} voltage to obtain 0 dBm at output when f _{in} is 1 MHz (sine wave). Increase f _{in} frequency until the dB-meter reads -3 dBm. 20 log (V _O /V _I) = -3 dBm	COM or Yn	Yn or COM
		3.0	—	35.0	—				
		4.5	—	50.0	—				
Crosstalk (Between any switches)		2.3	—	-45.0	—	dB	C _L = 50 pF, R _L = 600 Ω Adjust f _{in} voltage to obtain 0 dBm at input when f _{in} is 1 MHz (sine wave).	COM	Yn
		3.0	—	-45.0	—				
		4.5	—	-45.0	—				
Crosstalk (Control input to signal output)		2.3	—	20.0	—	mV	C _L = 50 pF, R _L = 600 Ω Adjust R _L value to obtain 0 A at I _{IN/OUT} when f _{in} is 1 MHz (square wave).	INH	COM or Yn
		3.0	—	35.0	—				
		4.5	—	65.0	—				
Feedthrough attenuation (Switch OFF)		2.3	—	-45	—	dB	C _L = 50 pF, R _L = 600 Ω Adjust f _{in} voltage to obtain 0 dBm at input when f _{in} is 1 MHz (sine wave).	COM or Yn	Yn or COM
		3.0	—	-45	—				
		4.5	—	-45	—				
Sine-wave distortion		2.3	—	0.1	—	%	C _L = 50 pF, R _L = 10 kΩ f _{IN} = 1 kHz (sine wave) V _I = 2 V _{P-P} , V _{CC} = 2.3 V V _I = 2.5 V _{P-P} , V _{CC} = 3.0 V V _I = 4 V _{P-P} , V _{CC} = 4.5 V	COM or Yn	Yn or COM
		3.0	—	0.1	—				
		4.5	—	0.1	—				

Test Circuits

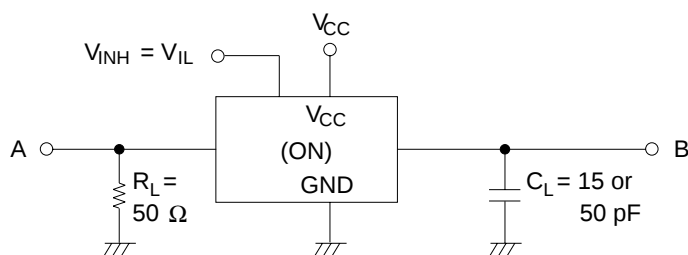
R_{ON} : On-state switch resistance



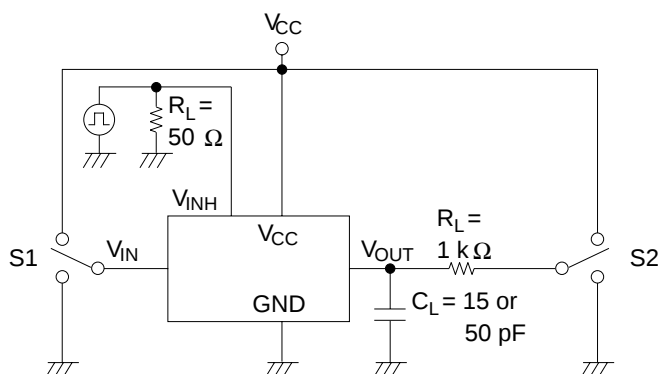
I_s (OFF): Off-state switch leakage current, I_s (ON): On-state switch leakage current



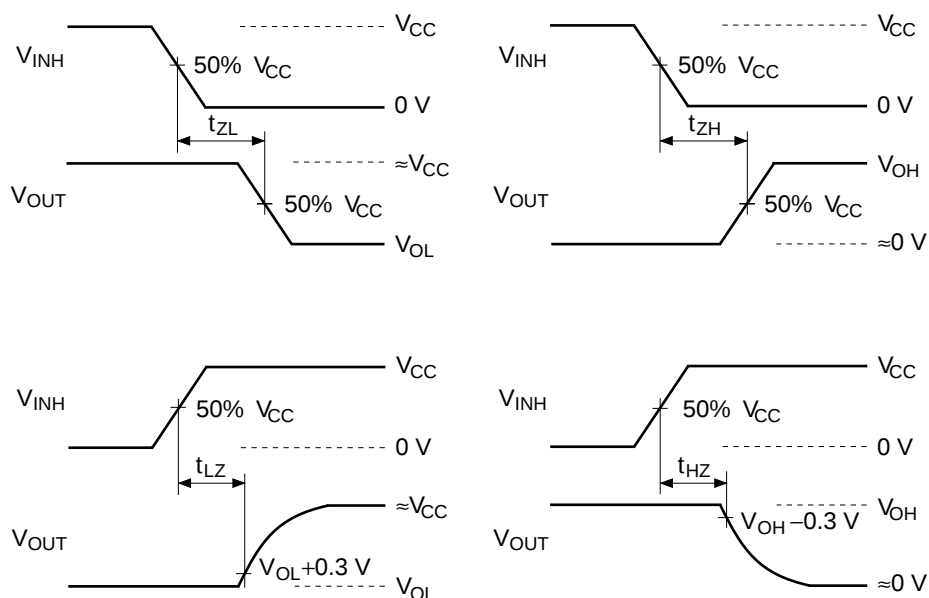
t_{PLH} , t_{PHL} : Propagation delay time (from switch input to switch output)



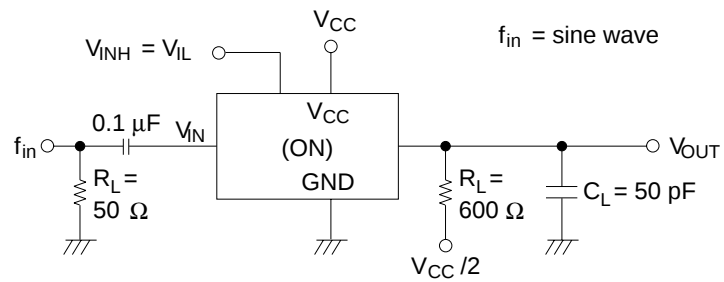
Switching time



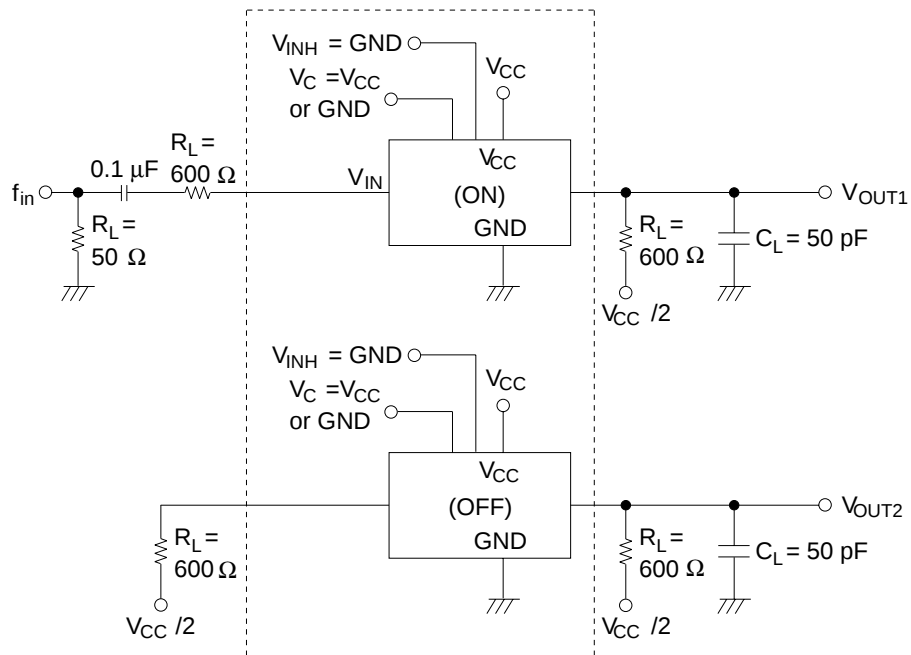
TEST	S1	S2
t_{LZ}/t_{ZL}	GND	V _{CC}
t_{HZ}/t_{ZH}	V _{CC}	GND



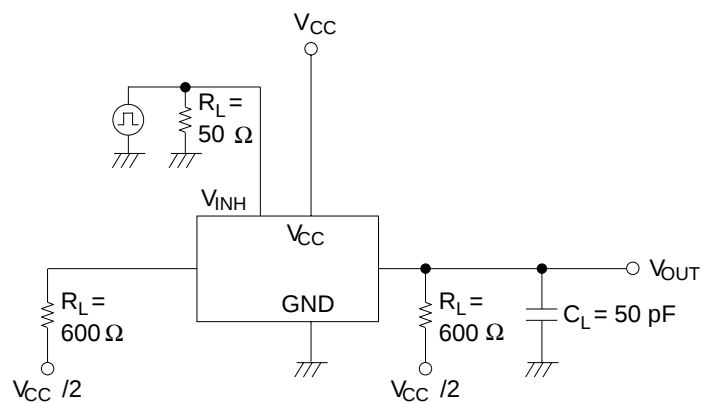
Frequency response (Switch ON)



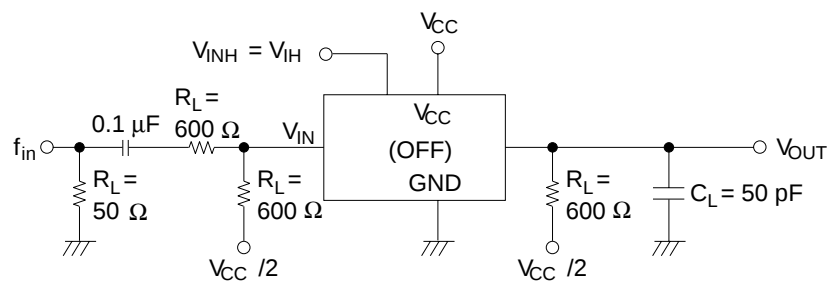
Crosstalk (Between any switches)



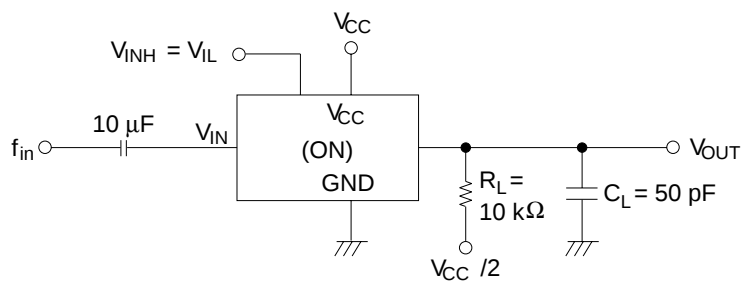
Crosstalk (Control input to signal output)



Feedthrough attenuation (Switch OFF)



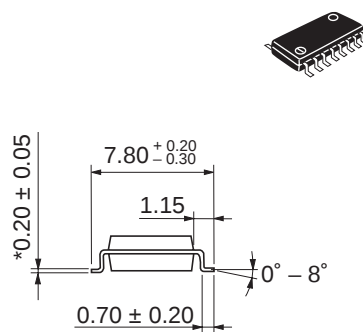
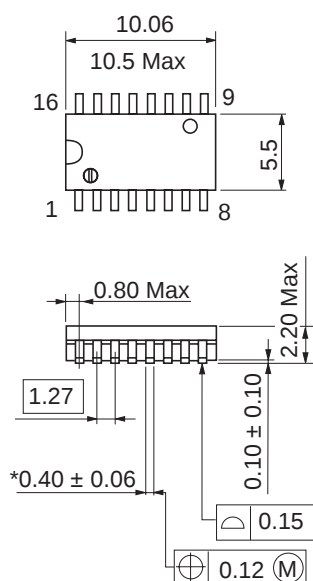
Sine-wave distortion



Package Dimensions

As of January, 2003

Unit: mm

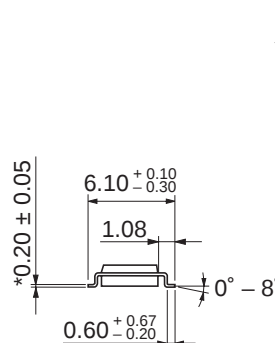
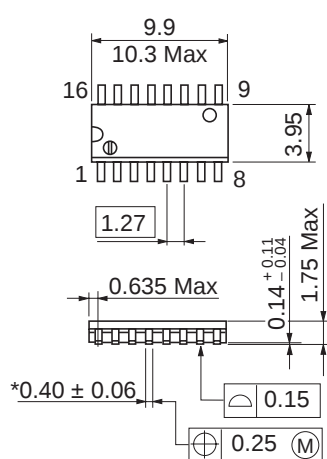


Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

*Ni/Pd/Au plating

As of January, 2003

Unit: mm

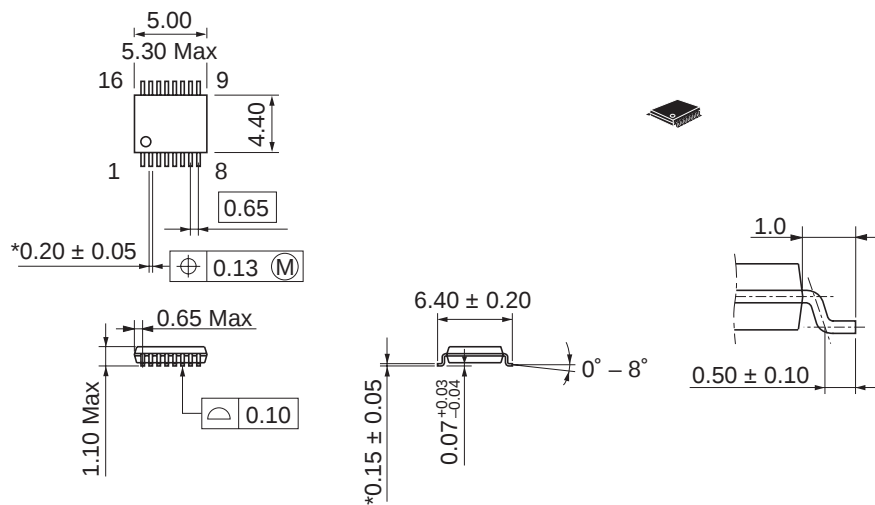


Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

*Ni/Pd/Au plating

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-16DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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