# HD74LV20A

## Dual 4-input Positive NAND Gates

REJ03D0236–0300Z
(Previous ADE-205-254A (Z))
Rev.3.00
May 31, 2004

### Description

The HD74LV20A performs the Boolean functions $Y = \overline{A \bullet B \bullet C \bullet D}$ or $Y = \overline{A}+\overline{B}+\overline{C}+\overline{D}$ in positive logic.

Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

### Features

- $V_{CC}$ = 2.0 V to 5.5 V operation
- All inputs $V_{IH}$ (Max.) = 5.5 V (@$V_{CC}$ = 0 V to 5.5 V)
- All outputs $V_O$ (Max.) = 5.5 V (@$V_{CC}$ = 0 V)
- Typial $V_{OL}$ ground bounce < 0.8 V (@$V_{CC}$ = 3.3 V, Ta = 25°C)
- Typial $V_{OH}$ undershoot > 2.3 V (@$V_{CC}$ = 3.3 V, Ta = 25°C)
- Output current ±6 mA (@$V_{CC}$ = 3.0 V to 3.6 V), ±12 mA (@$V_{CC}$ = 4.5 V to 5.5 V)
- Ordering Information

| Part Name | Package Type | Package Code | Package Abbreviation | Taping Abbreviation (Quantity) |
|---|---|---|---|---|
| HD74LV20AFPEL | SOP–14 pin(JEITA) | FP–14DAV | FP | EL (2,000 pcs/reel) |
| HD74LV20ARPEL | SOP–14 pin(JEDEC) | FP–14DNV | RP | EL (2,500 pcs/reel) |
| HD74LV20ATELL | TSSOP–14 pin | TTP–14DV | T | ELL (2,000 pcs/reel) |

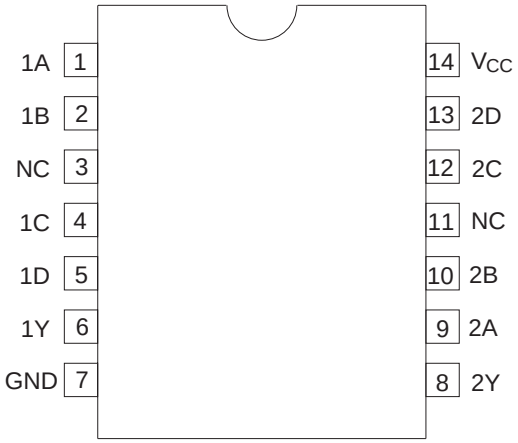
Note: Please consult the sales office for the above package availability.

### Function Table

| Inputs | | | | |
|---|---|---|---|---|
| **A** | **B** | **C** | **D** | **Output Y** |
| H | H | H | H | L |
| L | X | X | X | H |
| X | L | X | X | H |
| X | X | L | X | H |
| X | X | X | L | H |

Note: H: High level
L: Low level
X: Immaterial

## Pin Arrangement




(Top view)

## Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit | Conditions |
|---|---|---|---|---|
| Supply voltage range | $V_{CC}$ | –0.5 to 7.0 | V | |
| Input voltage range*[1] | $V_I$ | –0.5 to 7.0 | V | |
| Output voltage range*[1, 2] | $V_O$ | –0.5 to $V_{CC}$ + 0.5 | V | Output: H or L |
| | | –0.5 to 7.0 | | $V_{CC}$: OFF |
| Input clamp current | $I_{IK}$ | –20 | mA | $V_I$ < 0 |
| Output clamp current | $I_{OK}$ | ±50 | mA | $V_O$ < 0 or $V_O$ > $V_{CC}$ |
| Continuous output current | $I_O$ | ±25 | mA | $V_O$ = 0 to $V_{CC}$ |
| Continuous current through $V_{CC}$ or GND | $I_{CC}$ or $I_{GND}$ | ±50 | mA | |
| Maximum power dissipation at Ta = 25°C (in still air)*[3] | $P_T$ | 785 | mW | SOP |
| | | 500 | | TSSOP |
| Storage temperature | Tstg | –65 to 150 | °C | |

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

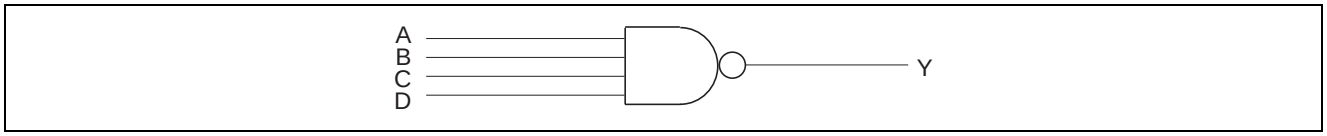
1. The input and output voltage ratings may be exceeded even if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

## Recommended Operating Conditions

| Item | Symbol | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| Supply voltage range | $V_{CC}$ | 2.0 | 5.5 | V | |
| Input voltage range | $V_I$ | 0 | 5.5 | V | |
| Output voltage range | $V_O$ | 0 | $V_{CC}$ | V | |
| Output current | $I_{OH}$ | — | –50 | µA | $V_{CC}$ = 2.0 V |
| | | — | –2 | mA | $V_{CC}$ = 2.3 to 2.7 V |
| | | — | –6 | | $V_{CC}$ = 3.0 to 3.6 V |
| | | — | –12 | | $V_{CC}$ = 4.5 to 5.5 V |
| | $I_{OL}$ | — | 50 | µA | $V_{CC}$ = 2.0 V |
| | | — | 2 | mA | $V_{CC}$ = 2.3 to 2.7 V |
| | | — | 6 | | $V_{CC}$ = 3.0 to 3.6 V |
| | | — | 12 | | $V_{CC}$ = 4.5 to 5.5 V |
| Input transition rise or fall rate | Δt /Δv | 0 | 200 | ns/V | $V_{CC}$ = 2.3 to 2.7 V |
| | | 0 | 100 | | $V_{CC}$ = 3.0 to 3.6 V |
| | | 0 | 20 | | $V_{CC}$ = 4.5 to 5.5 V |
| Operating free-air temperature | Ta | –40 | 85 | °C | |

Note: Unused or floating inputs must be held high or low.

## Logic Diagram



## DC Electrical Characteristics

Ta = –40 to 85°C

| Item | Symbol | $V_{CC}$ (V)* | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | 2.0 | 1.5 | — | — | V | |
| | | 2.3 to 2.7 | $V_{CC} \times 0.7$ | — | — | | |
| | | 3.0 to 3.6 | $V_{CC} \times 0.7$ | — | — | | |
| | | 4.5 to 5.5 | $V_{CC} \times 0.7$ | — | — | | |
| | $V_{IL}$ | 2.0 | — | — | 0.5 | | |
| | | 2.3 to 2.7 | — | — | $V_{CC} \times 0.3$ | | |
| | | 3.0 to 3.6 | — | — | $V_{CC} \times 0.3$ | | |
| | | 4.5 to 5.5 | — | — | $V_{CC} \times 0.3$ | | |
| Output voltage | $V_{OH}$ | Min to Max | $V_{CC}$ – 0.1 | — | — | V | $I_{OH}$ = –50 µA |
| | | 2.3 | 2.0 | — | — | | $I_{OH}$ = –2 mA |
| | | 3.0 | 2.48 | — | — | | $I_{OH}$ = –6 mA |
| | | 4.5 | 3.8 | — | — | | $I_{OH}$ = –12 mA |
| | $V_{OL}$ | Min to Max | — | — | 0.1 | | $I_{OL}$ = 50 µA |
| | | 2.3 | — | — | 0.4 | | $I_{OL}$ = 2 mA |
| | | 3.0 | — | — | 0.44 | | $I_{OL}$ = 6 mA |
| | | 4.5 | — | — | 0.55 | | $I_{OL}$ = 12 mA |
| Input current | $I_{IN}$ | 0 to 5.5 | — | — | ±1 | µA | $V_{IN}$ = 5.5 V or GND |
| Quiescent supply current | $I_{CC}$ | 5.5 | — | — | 20 | µA | $V_{IN}$ = $V_{CC}$ or GND, $I_O$ = 0 |
| Output leakage current | $I_{OFF}$ | 0 | — | — | 5 | µA | $V_I$ or $V_O$ = 0 V to 5.5 V |
| Input capacitance | $C_{IN}$ | 3.3 | — | 3.5 | — | pF | $V_I$ = $V_{CC}$ or GND |

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

## Switching Characteristics

$V_{CC}$ = 2.5 ± 0.2 V

| Item | Symbol | Ta = 25°C Min | Typ | Max | Ta = –40 to 85°C Min | Max | Unit | Test Conditions | FROM (Input) | TO (Output) |
|---|---|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | — | 7.8 | 11.6 | 1.0 | 13.5 | ns | $C_L$ = 15 pF | A, B, C, or D | Y |
| | $t_{PHL}$ | — | 10.1 | 15.3 | 1.0 | 18.5 | | $C_L$ = 50 pF | | |

$V_{CC}$ = 3.3 ± 0.3 V

| Item | Symbol | Ta = 25°C Min | Typ | Max | Ta = –40 to 85°C Min | Max | Unit | Test Conditions | FROM (Input) | TO (Output) |
|---|---|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | — | 4.6 | 6.6 | 1.0 | 8.0 | ns | $C_L$ = 15 pF | A, B, C, or D | Y |
| | $t_{PHL}$ | — | 7.7 | 10.1 | 1.0 | 11.5 | | $C_L$ = 50 pF | | |

$V_{CC}$ = 5.0 ± 0.5 V

| Item | Symbol | Ta = 25°C Min | Typ | Max | Ta = –40 to 85°C Min | Max | Unit | Test Conditions | FROM (Input) | TO (Output) |
|---|---|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | — | 3.3 | 5.0 | 1.0 | 6.0 | ns | $C_L$ = 15 pF | A, B, C, or D | Y |
| | $t_{PHL}$ | — | 4.8 | 7.0 | 1.0 | 8.0 | | $C_L$ = 50 pF | | |

## Operating Characteristics

$C_L$ = 50 pF

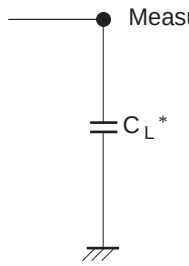
| Item | Symbol | $V_{CC}$ (V) | Ta = 25°C Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Power dissipation capacitance | $C_{PD}$ | 3.3 | — | 9.5 | — | pF | f = 10 MHz |
| | | 5.0 | — | 11.0 | — | | |

## Noise Characteristics

$C_L$ = 50 pF

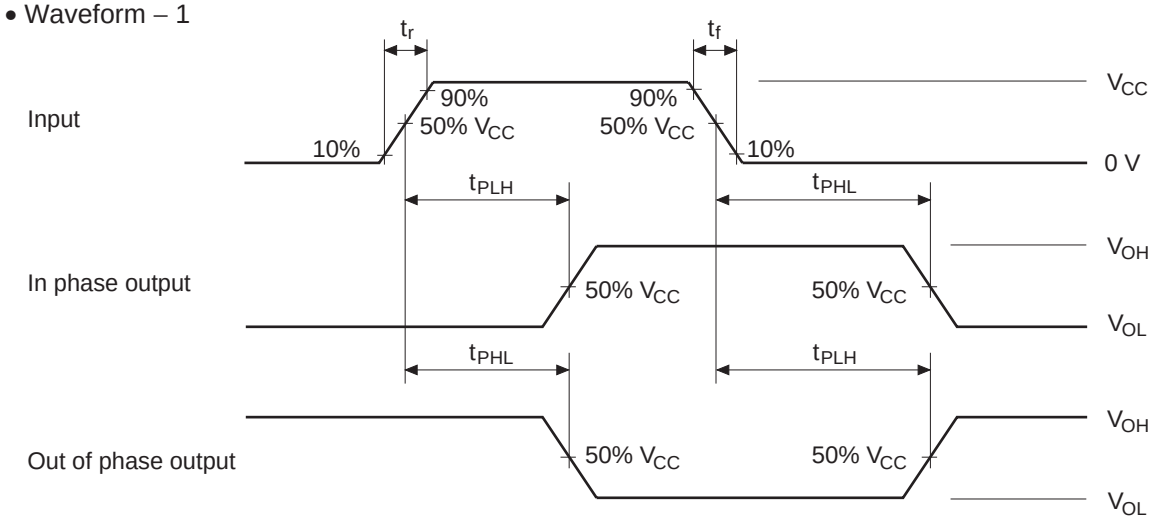
| Item | Symbol | $V_{CC}$ (V) | Ta = 25°C Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Quiet output, maximum dynamic $V_{OL}$ | $V_{OL (P)}$ | 3.3 | — | 0.2 | 0.8 | V | |
| Quiet output, minimum dynamic $V_{OL}$ | $V_{OL (V)}$ | 3.3 | — | –0.1 | –0.8 | V | |
| Quiet output, minimum dynamic $V_{OH}$ | $V_{OH (V)}$ | 3.3 | — | 3.2 | — | V | |
| High-level dyamic input voltage | $V_{IH (D)}$ | 3.3 | 2.31 | — | — | V | |
| Low-level dynamic inout voltage | $V_{IL (D)}$ | 3.3 | — | — | 0.99 | V | |

## Test Circuit




Note: $C_L$ includes the probe and jig capacitance.

• Waveform – 1

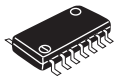


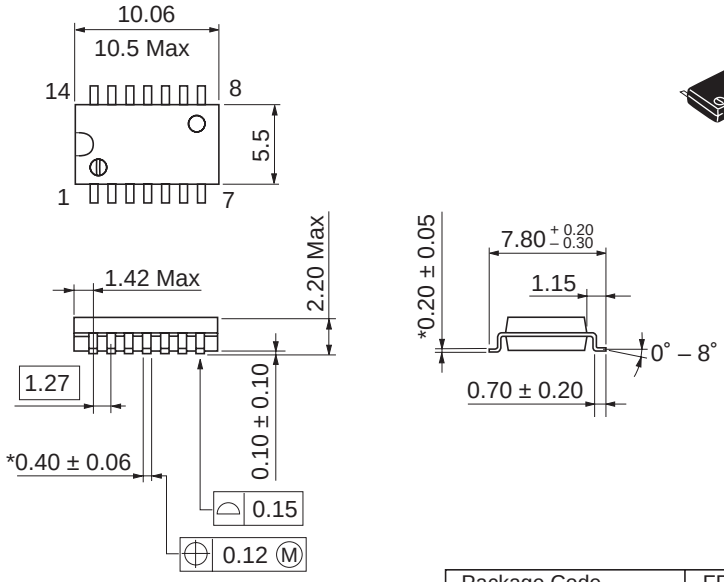

Notes: 1. Input waveform: PRR ≤ 1 MHz, Zo = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns
2. The output are measured one at a time with one transition per measurement.

## Package Dimensions

As of January, 2003

Unit: mm





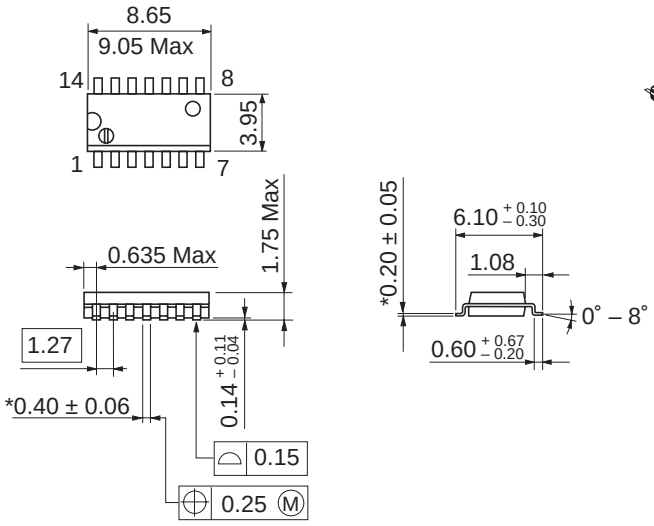

*Ni/Pd/Au plating

| | |
|---|---|
| Package Code | FP-14DAV |
| JEDEC | — |
| JEITA | Conforms |
| Mass (reference value) | 0.23 g |

As of January, 2003

Unit: mm



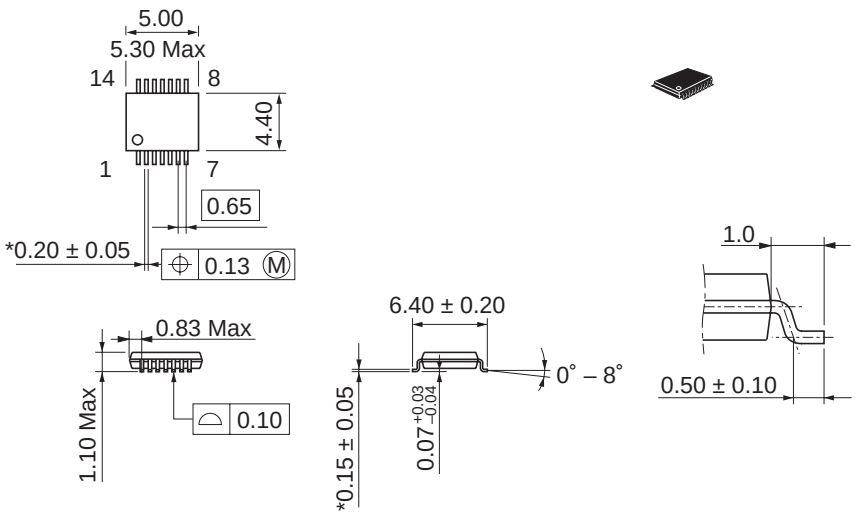



*Ni/Pd/Au plating

| | |
|---|---|
| Package Code | FP-14DNV |
| JEDEC | Conforms |
| JEITA | Conforms |
| Mass (reference value) | 0.13 g |

As of January, 2003

Unit: mm




*Ni/Pd/Au plating

| | |
|---|---|
| Package Code | TTP-14DV |
| JEDEC | — |
| JEITA | — |
| Mass (reference value) | 0.05 g |

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