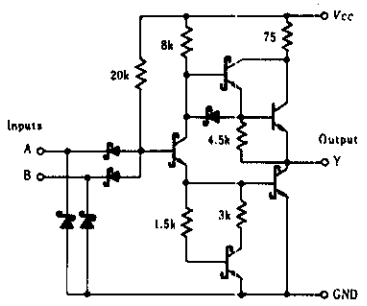
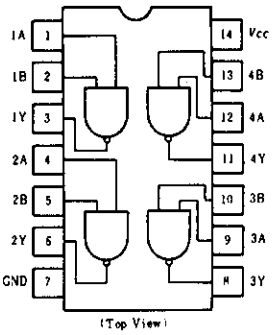
# HD74LS00 ●Quadruple 2-input Positive NAND Gates

## ■CIRCUIT SCHEMATIC(¼)




## ■PIN ARRANGEMENT




## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75℃$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$ | $I_{OL}=8mA$ | – | – | 0.5 | V |
| | | | $I_{OL}=4mA$ | – | – | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 0.8 | 1.6 | mA |
| | $I_{CCL}$ | $V_{CC}=5.25V$ | | – | 2.4 | 4.4 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25℃$ )

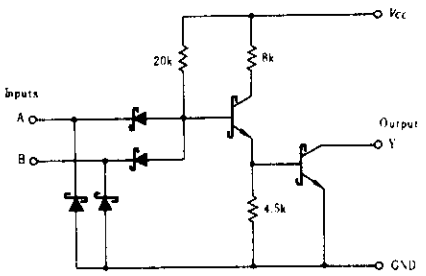
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | – | 9 | 15 | ns |
| | $t_{PHL}$ | | – | 10 | 15 | ns |

Note) Refer to Test Circuit and Waveform of the Common Item

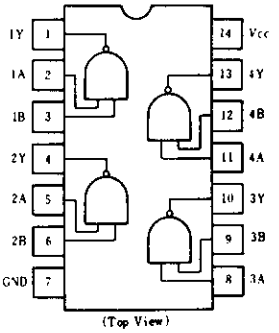
Home Print

# HD74LS01 ●Quadruple 2-input Positive NAND Gates(with Open Collector Outputs)

## ■CIRCUIT SCHEMATIC(¼)




## ■PIN ARRANGEMENT



(Top View)

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output voltage | $V_{OH}$ | – | – | 5.5 | V |
| Low level output current | $I_{OL}$ | – | – | 8 | mA |

## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$ | $I_{OL}=8mA$ | – | – | 0.5 | V |
| | | | $I_{OL}=4mA$ | – | – | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Output current | $I_{OH}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$ | | – | – | 100 | μA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 0.8 | 1.6 | mA |
| | $I_{CCL}$ | $V_{CC}=5.25V$ | | – | 2.4 | 4.4 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | – | 17 | 32 | ns |
| | $t_{PHL}$ | | – | 15 | 28 | ns |

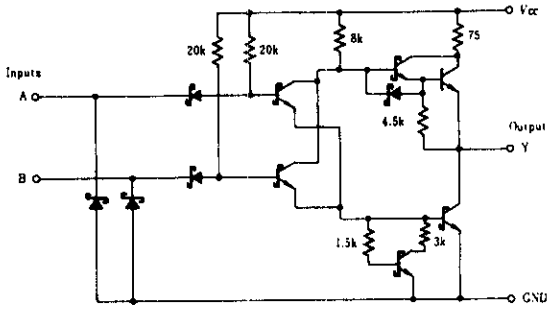
Note) Refer to Test Circuit and Waveform of the Common Item



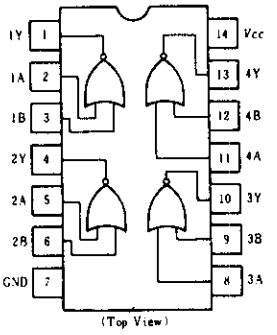
Home Print

# HD74LS02 ●Quadruple 2-input Positive NOR Gates

## ■CIRCUIT SCHEMATIC(¼)




## ■PIN ARRANGEMENT




## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$ | $I_{OL}=8mA$ | – | – | 0.5 | V |
| | | | $I_{OL}=4mA$ | – | – | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 1.6 | 3.2 | mA |
| | $I_{CCL}$ | $V_{CC}=5.25V$ | | – | 2.8 | 5.4 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

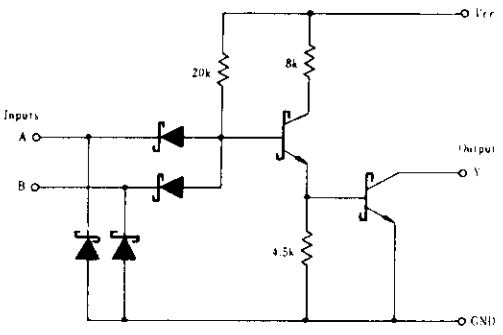
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | – | 10 | 15 | ns |
| | $t_{PHL}$ | | – | 10 | 15 | ns |

Note) Refer to Test Circuit and Waveform of the Common Item

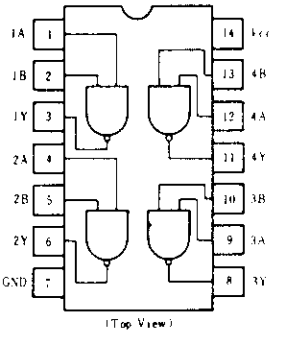
Home Print

# HD74LS03 ●Quadruple 2-input Positive NAND Gates (with Open Collector Outputs)

## ■CIRCUIT SCHEMATIC(¼)




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output voltage | $V_{OH}$ | – | – | 5.5 | V |
| Low level output current | $I_{OL}$ | – | – | 8 | mA |

## ■ELECTRICAL CHARACTERISTICS ( $Ta$=−20～+75℃ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V | $I_{OL}$=8mA | – | – | 0.5 | V |
| | | | $I_{OL}$=4mA | – | – | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V $V_I$=0.4V | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.1 | mA |
| Output current | $I_{OH}$ | $V_{CC}$=4.75V, $V_{IL}$=0.8V, $V_{OH}$=5.5V | | – | – | 100 | μA |
| Supply current | $I_{CCH}$ | $V_{CC}$=5.25V | | – | 0.8 | 1.6 | mA |
| | $I_{CCL}$ | $V_{CC}$=5.25V | | – | 2.4 | 4.4 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$=15pF, $R_L$=2kΩ | – | 17 | 32 | ns |
| | $t_{PHL}$ | | – | 15 | 28 | ns |

Note) Refer to Test Circuit and Waveform of the Common Item

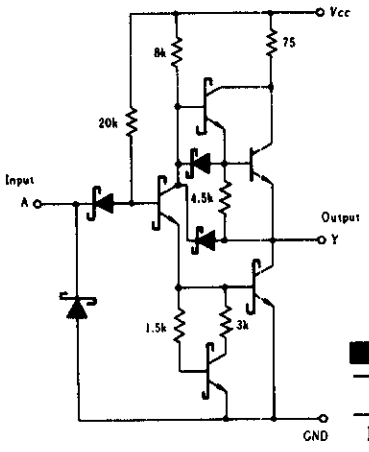


Home Print

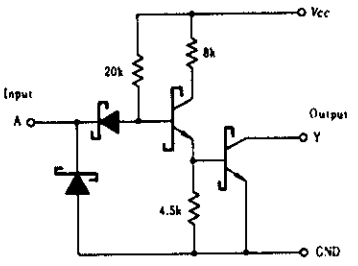
# HD74LS04/HD74LS05 ●Hex Inverters ●Hex Inverters (with Open Collector Outputs)

## ■CIRCUIT SCHEMATIC(1/6)

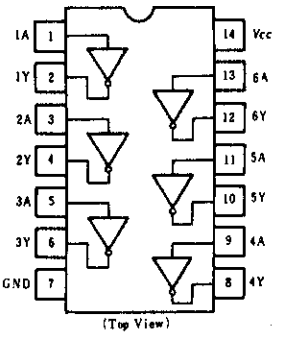
HD74LS04




HD74LS05




## ■PIN ARRANGEMENT




## ■HD74LS05 RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output voltage | $V_{OH}$ | – | – | 5.5 | V |
| Low level output current | $I_{OL}$ | – | – | 8 | mA |

## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75℃)

| Item | Symbol | Test Conditions | | HD74LS04 min | HD74LS04 typ* | HD74LS04 max | HD74LS05 min | HD74LS05 typ* | HD74LS05 max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | | 2.7 | – | – | – | – | – | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V | $I_{OL}$=8mA | – | – | 0.5 | – | – | 0.5 | V |
| | | | $I_{OL}$=4mA | – | – | 0.4 | – | – | 0.4 | |
| Output current | $I_{OH}$ | $V_{CC}$=4.75V, $V_{IL}$=0.8V, $V_{OH}$=5.5V | | – | – | – | – | – | 100 | μA |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | – | – | 20 | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | – | – | −0.4 | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.1 | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | – | −100 | – | – | – | mA |
| Supply current | $I_{CCH}$ | $V_{CC}$=5.25V | | – | 1.2 | 2.4 | – | 1.2 | 2.4 | mA |
| | $I_{CCL}$ | | | – | 3.6 | 6.6 | – | 3.6 | 6.6 | |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

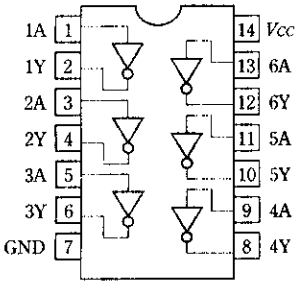
## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25℃)

| Item | Symbol | Test Conditions | HD74LS04 min | HD74LS04 typ | HD74LS04 max | HD74LS05 min | HD74LS05 typ | HD74LS05 max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$=15pF, $R_L$=2kΩ | – | 9 | 15 | – | 17 | 32 | ns |
| | $t_{PHL}$ | | – | 10 | 15 | – | 15 | 28 | |

Note) Refer to Test Circuit and Waveform of the Common Item

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## ■ PIN ARRANGEMENT




(Top View)

## ■ ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | *Vcc* | 7.0 | V |
| Input voltage | *VIN* | 7.0 | V |
| Output voltage | *Vout* | 30 | V |
| Operating temperature range | *Topr* | –20 ~ +75 | °C |
| Storage temperature range | *Tstg* | –65 ~ +150 | °C |

## ■ RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Supply voltage | *Vcc* | 4.75 | 5.00 | 5.25 | V |
| High level output voltage | *VOH* | – | – | 30 | V |
| Low level output current | *IOL* | – | – | 48 | mA |
| Operating temperature range | *Topr* | –20 | 25 | 75 | °C |



Home Print

## ■ ELECTRICAL CHARACTERISTICS ($Ta$ = –20 ~ +75°C)

| Item | Symbol | Test Conditions | | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | | – | – | 0.8 | V |
| Output voltage | $V_{OL}$ | $V_{CC}$ = 4.75V, | $V_{IH}$ = 2V | $I_{OL}$ = 24mA | – | – | 0.4 | V |
| | | | | $I_{OL}$ = 48mA | – | – | 0.5 | V |
| Input current | $I_{IH}$ | $V_{CC}$ = 5.25V | $V_I$ = 2.7V | | – | – | 20 | µA |
| | $I_{IL}$ | $V_{CC}$ = 5.25V, | $V_I$ = 0.4V | | – | – | –0.4 | mA |
| | $I_I$ | $V_{CC}$ = 5.25V, | $V_I$ = 7V | | – | – | 0.1 | mA |
| Output current | $I_{OH}$ | $V_{CC}$ = 4.75V, | $V_{IL}$ = 0.8V, | $V_{OH}$ = 30V | – | – | 250 | µA |
| Supply current | $I_{CCH}$ | $V_{CC}$ = 5.25V | | | – | 23 | 48 | mA |
| | $I_{CCL}$ | $V_{CC}$ = 5.25V | | | – | 21 | 51 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$ = 4.75V, | $I_{IN}$ = –18mA | | – | – | –1.5 | V |

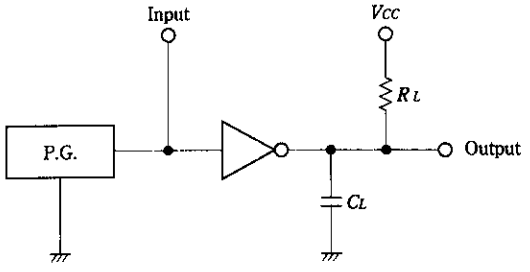
*$V_{CC}$ = 5V, $Ta$ = 25°C

## ■ SWITCHING CHARACTERISTICS ($V_{CC}$ = 5V, $Ta$ = 25°C)

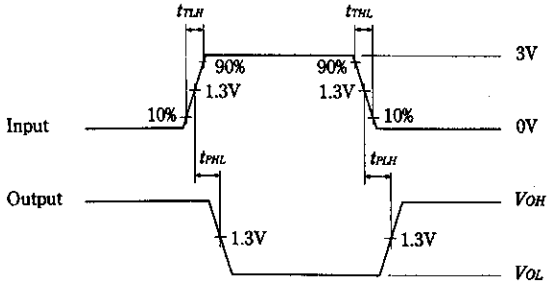
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$ = 15pF, $R_L$ = 110Ω | – | 10 | 15 | ns |
| | $t_{PHL}$ | | – | 15 | 23 | ns |

## ■ TESTING METHOD

Test Circuit

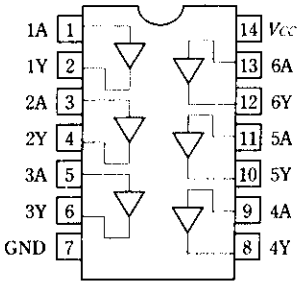



Waveform




Notes) 1. Input pulse: PRR = 1MHz, duty cycle 50%, Zout = 50Ω, $t_{TLH}$≤15ns, $t_{THL}$≤6ns
2. $C_L$ includes probe and jig capacitance.
3. All diodes are 1S2074Ⓗ

## ■ PIN ARRANGEMENT




(Top View)

## ■ ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | *Vcc* | 7.0 | V |
| Input voltage | *VIN* | 7.0 | V |
| Output voltage | *Vout* | 30 | V |
| Operating temperature range | *Topr* | −20 ~ +75 | °C |
| Storage temperature range | *Tstg* | −65 ~ +150 | °C |

## ■ RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Supply voltage | *Vcc* | 4.75 | 5.00 | 5.25 | V |
| High level output voltage | *VOH* | – | – | 30 | V |
| Low level output current | *IOL* | – | – | 48 | mA |
| Operating temperature range | *Topr* | −20 | 25 | 75 | °C |



Home Print

## ■ ELECTRICAL CHARACTERISTICS ($Ta$ = –20 ~ +75°C)

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OL}$ | $V_{CC}$ = 4.75V, $V_{IL}$ = 0.8V | $I_{OL}$ = 24mA | – | – | 0.4 | V |
| | | | $I_{OL}$ = 48mA | – | – | 0.5 | V |
| Input current | $I_{IH}$ | $V_{CC}$ = 5.25V $V_I$ = 2.7V | | – | – | 20 | µA |
| | $I_{IL}$ | $V_{CC}$ = 5.25V, $V_I$ = 0.4V | | – | – | –0.4 | mA |
| | $I_I$ | $V_{CC}$ = 5.25V, $V_I$ = 7V | | – | – | 0.1 | mA |
| Output current | $I_{OH}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, | $V_{OH}$ = 30V | – | – | 250 | µA |
| Supply current | $I_{CCH}$ | $V_{CC}$ = 5.25V | | – | 22 | 41 | mA |
| | $I_{CCL}$ | $V_{CC}$ = 5.25V | | – | 17 | 30 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$ = 4.75V, $I_{IN}$ = –18mA | | – | – | –1.5 | V |

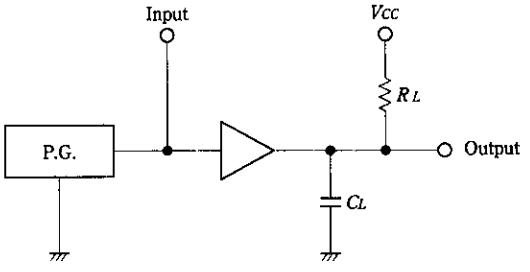
*$V_{CC}$ = 5V, $Ta$ = 25°C

## ■ SWITCHING CHARACTERISTICS ($V_{CC}$ = 5V, $Ta$ = 25°C)

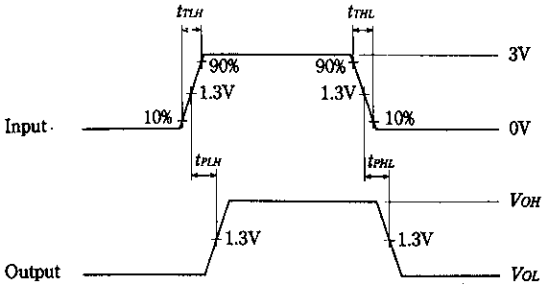
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$ = 15pF, $R_L$ = 110Ω | – | 10 | 15 | ns |
| | $t_{PHL}$ | | – | 20 | 30 | ns |

## ■ TESTING METHOD

Test Circuit



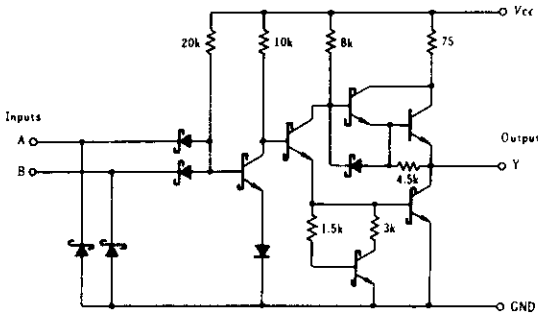

Waveform



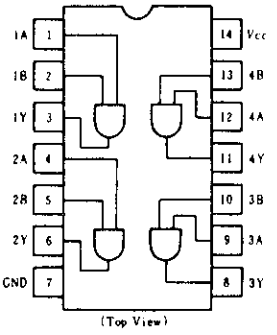

Notes) 1. Input pulse: PRR = 1MHz, duty cycle 50%, Zout = 50Ω, $t_{TLH} \leq 15$ns. $t_{THL} \leq 6$ns
2. $C_L$ includes probe and jig capacitance.
3. All diodes are 1S2074Ⓗ

# HD74LS08 ●Quadruple 2-input Positive AND Gates

## ■CIRCUIT SCHEMATIC(¼)




## ■PIN ARRANGEMENT




## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$ | $I_{OL}=8mA$ | – | – | 0.5 | V |
| | | | $I_{OL}=4mA$ | – | – | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 2.4 | 4.8 | mA |
| | $I_{CCL}$ | | | – | 4.4 | 8.8 | |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | – | 8 | 15 | ns |
| | $t_{PHL}$ | | – | 10 | 20 | |

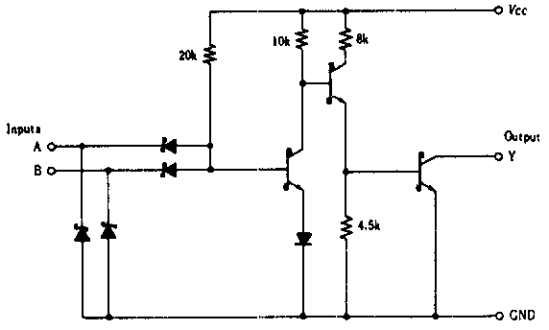
Note) Refer to Test Circuit and Waveform of the Common Item



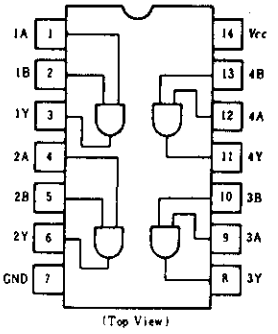
Home Print

# HD74LS09 ●Quadruple 2-input Positive AND Gates (with Open Collector Outputs)

## ■CIRCUIT SCHEMATIC(¼)




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output voltage | $V_{OH}$ | – | – | 5.5 | V |
| Low level output current | $I_{OL}$ | – | – | 8 | mA |

## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$ | $I_{OL}=8mA$ | – | – | 0.5 | V |
| | | | $I_{OL}=4mA$ | – | – | 0.4 | |
| Output current | $I_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{OH}=5.5V$ | | – | – | 100 | μA |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 2.4 | 4.8 | mA |
| | $I_{CCL}$ | $V_{CC}=5.25V$ | | – | 4.4 | 8.8 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

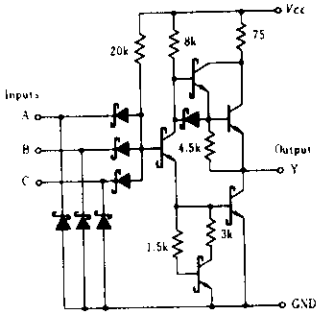
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | – | 20 | 35 | ns |
| | $t_{PHL}$ | | – | 17 | 35 | ns |

Note) Refer to Test Circuit and Waveform of the Common Item

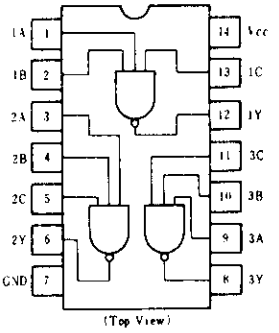
Home Print

# HD74LS10 ●Triple 3-input Positive NAND Gates

## ■CIRCUIT SCHEMATIC(⅓)




## ■PIN ARRANGEMENT




## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75℃$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$ | $I_{OL}=8mA$ | – | – | 0.5 | V |
| | | | $I_{OL}=4mA$ | – | – | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 0.6 | 1.2 | mA |
| | $I_{CCL}$ | | | – | 1.8 | 3.3 | |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25℃$ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | – | 9 | 15 | ns |
| | $t_{PHL}$ | | – | 10 | 15 | |

Note) Refer to Test Circuit and Waveform of the Common Item



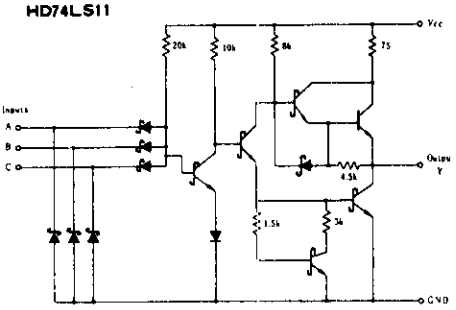
Home Print

# HD74LS11/HD74LS15

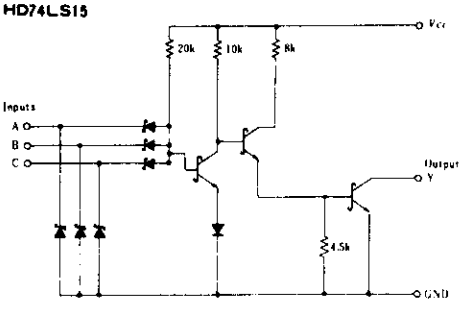
●Triple 3-input Positive AND Gates
●Triple 3-input Positive AND Gates (with Open Collector Outputs)

## ■CIRCUIT SCHEMATIC(⅓)

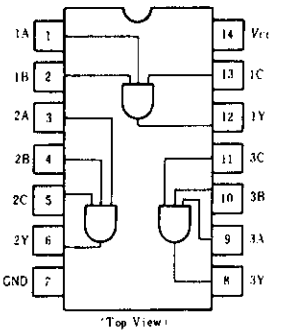
HD74LS11



HD74LS15



## ■PIN ARRANGEMENT




(Top View)

## ■HD74LS15 RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output voltage | $V_{OH}$ | – | – | 5.5 | V |
| Low level output current | $I_{OL}$ | – | – | 8 | mA |

## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20~+75℃)

| Item | Symbol | Test Conditions | | HD74LS11 | | | HD74LS15 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | min | typ* | max | min | typ* | max | |
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $I_{OH}$=−400μA | | 2.7 | – | – | – | – | – | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IL}$=0.8V | $I_{OL}$=8mA | – | – | 0.5 | – | – | 0.5 | V |
| | | | $I_{OL}$=4mA | – | – | 0.4 | – | – | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | – | – | 20 | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | – | – | −0.4 | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.1 | – | – | 0.1 | mA |
| Output current | $I_{OH}$ | $V_{CC}$=4.75V, $V_{OH}$=5.5V | | – | – | – | – | – | 100 | μA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | – | −100 | – | – | – | mA |
| Supply current | $I_{CCH}$ | $V_{CC}$=5.25V | | – | 1.8 | 3.6 | – | 1.8 | 3.6 | mA |
| | $I_{CCL}$ | $V_{CC}$=5.25V | | – | 3.3 | 6.6 | – | 3.3 | 6.6 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25℃)

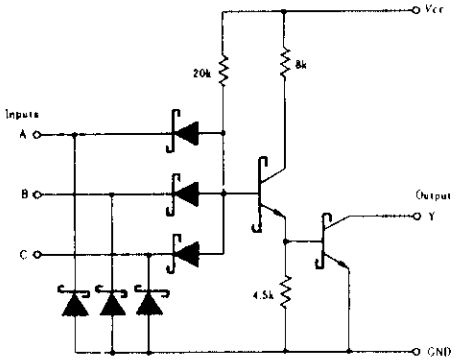
| Item | Symbol | Test Conditions | HD74LS11 | | | HD74LS15 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | min | typ | max | min | typ | max | |
| Propagation delay time | $t_{PLH}$ | $C_L$=15pF, $R_L$=2kΩ | – | 8 | 15 | – | 20 | 35 | ns |
| | $t_{PHL}$ | | – | 10 | 20 | – | 17 | 35 | ns |

Note) Refer to Test Circuit and Waveform of the Common Item

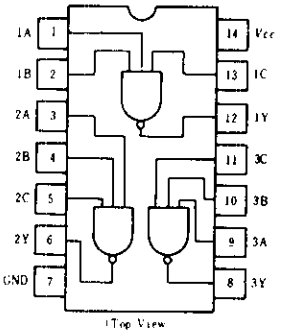
Home Print

# HD74LS12 ●Triple 3-input Positive NAND Gates (with Open Collector Outputs)

## ■CIRCUIT SCHEMATIC(⅓)




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output voltage | $V_{OH}$ | – | – | 5.5 | V |
| Low level output current | $I_{OL}$ | – | – | 8 | mA |

## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$ | $I_{OL}=8mA$ | – | – | 0.5 | V |
| | | | $I_{OL}=4mA$ | – | – | 0.4 | |
| Output current | $I_{OH}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$ | | – | – | 100 | μA |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 0.7 | 1.4 | mA |
| | $I_{CCL}$ | | | – | 1.8 | 3.3 | |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | – | 17 | 32 | ns |
| | $t_{PHL}$ | | – | 15 | 28 | |

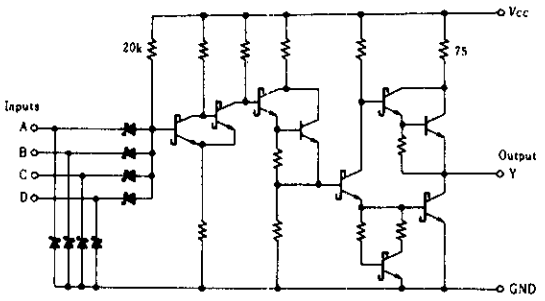
Note) Refer to Test Circuit and Waveform of the Common Item



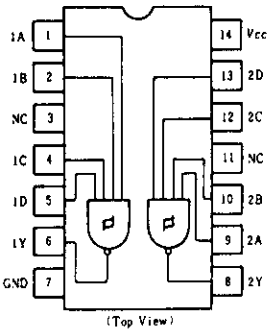
Home Print

# HD74LS13 ●Dual 4-input Positive NAND Schmitt Triggers

## ■CIRCUIT SCHEMATIC(½)




## ■PIN ARRANGEMENT




## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75℃$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input threshold voltage | $V_{T^+}$ | $V_{CC}=5V$ | | 1.4 | 1.6 | 1.9 | V |
| | $V_{T^-}$ | $V_{CC}=5V$ | | 0.5 | 0.7 | 1.0 | V |
| Hysteresis | $V_{T^+}-V_{T^-}$ | $V_{CC}=5V$ | | 0.4 | 0.9 | – | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $I_{OH}=-400\mu A$, $V_I=0.5V$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_I=1.9V$ | $I_{OL}=8mA$ | – | – | 0.5 | V |
| | | | $I_{OL}=4mA$ | – | – | 0.4 | |
| Input threshold current | $I_{T^+}$ | $V_{CC}=5V$, $V_I=V_{T^+}$ | | – | −0.14 | – | mA |
| | $I_{T^-}$ | $V_{CC}=5V$, $V_I=V_{T^-}$ | | – | −0.18 | – | mA |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 2.9 | 6 | mA |
| | $I_{CCL}$ | $V_{CC}=5.25V$ | | – | 4.1 | 7 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25℃$ )

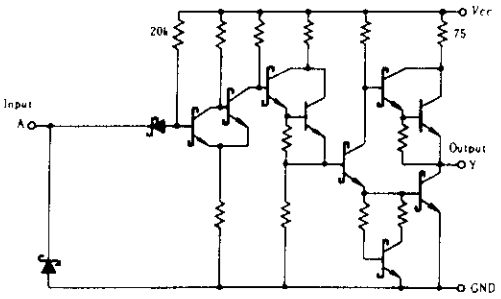
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | – | 15 | 22 | ns |
| | $t_{PHL}$ | | – | 18 | 27 | ns |

Note) Refer to Test Circuit and Waveform of the Common Item

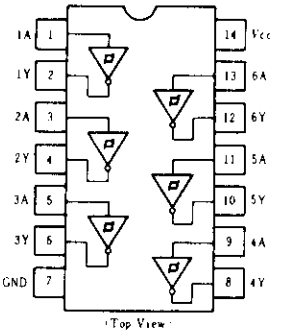
Home Print

# HD74LS14 ●Hex Schmitt Trigger Inverters

## ■CIRCUIT SCHEMATIC(1/6)




## ■PIN ARRANGEMENT




## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input threshold voltage | $V_{T^+}$ | $V_{CC}=5V$ | | 1.4 | 1.6 | 1.9 | V |
| | $V_{T^-}$ | $V_{CC}=5V$ | | 0.5 | 0.7 | 1.0 | V |
| Hysteresis | $V_{T^+}-V_{T^-}$ | $V_{CC}=5V$ | | 0.4 | 0.9 | – | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_I=0.5V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_I=1.9V$ | $I_{OL}=8mA$ | – | | 0.50 | V |
| | | | $I_{OL}=4mA$ | – | – | 0.40 | |
| Input threshold current | $I_{T^+}$ | $V_{CC}=5V$, $V_I=V_{T^+}$ | | – | −0.14 | – | mA |
| | $I_{T^-}$ | $V_{CC}=5V$, $V_I=V_{T^-}$ | | – | −0.18 | – | mA |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 8.6 | 16 | mA |
| | $I_{CCL}$ | $V_{CC}=5.25V$ | | – | 12 | 21 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

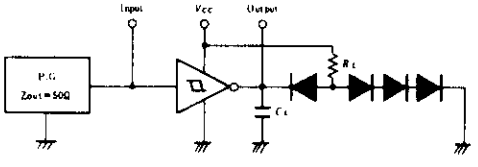
* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

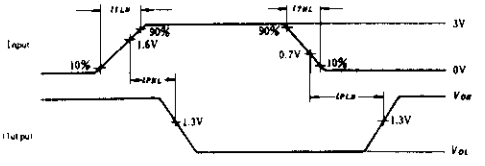
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | – | 15 | 22 | ns |
| | $t_{PHL}$ | | – | 15 | 22 | ns |

## ■TESTING METHOD

1. Test Circuit




Waveform



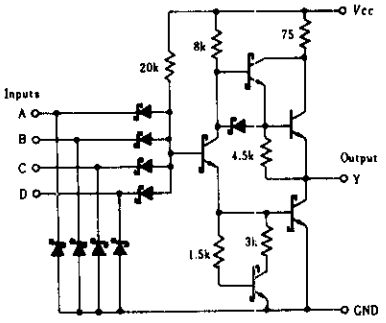

Notes) 1. Input pulse; $t_{TLH}\leqq15ns$, $t_{THL}\leqq6ns$, $PRR$=1MHz, duty cycle=50%
2. $C_L$ includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ.



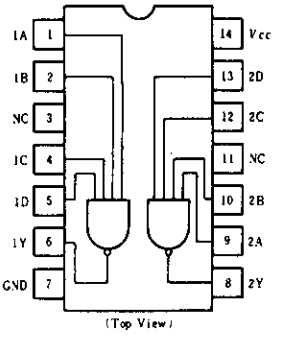
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# HD74LS20 ●Dual 4-input Positive NAND Gates

## ■CIRCUIT SCHEMATIC(½)




## ■PIN ARRANGEMENT




## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$ | $I_{OL}=8mA$ | – | – | 0.5 | V |
| | | | $I_{OL}=4mA$ | – | – | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 0.4 | 0.8 | mA |
| | $I_{CCL}$ | $V_{CC}=5.25V$ | | – | 1.2 | 2.2 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

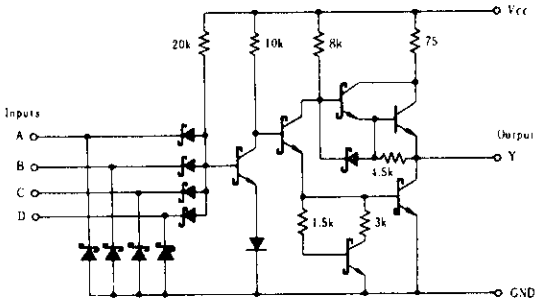
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | – | 9 | 15 | ns |
| | $t_{PHL}$ | | – | 10 | 15 | ns |

Note) Refer to Test Circuit and Waveform of the Common Item

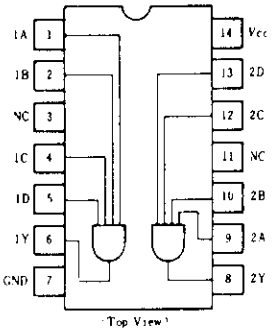
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# HD74LS21 ●Dual 4-input Positive AND Gates

## ■CIRCUIT SCHEMATIC(½)




## ■PIN ARRANGEMENT




## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$ | $I_{OL}=8mA$ | — | — | 0.5 | V |
| | | | $I_{OL}=4mA$ | — | — | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | — | 1.2 | 2.4 | mA |
| | $I_{CCL}$ | | | — | 2.2 | 4.4 | |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | — | 8 | 15 | ns |
| | $t_{PHL}$ | | — | 10 | 20 | |

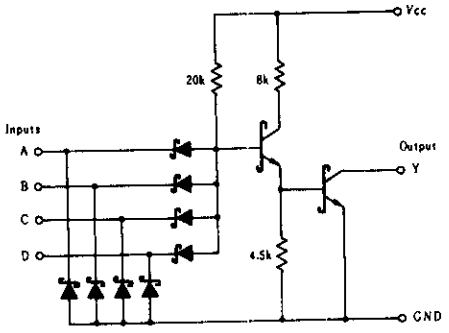
Note) Refer to Test Circuit and Waveform of the Common Item



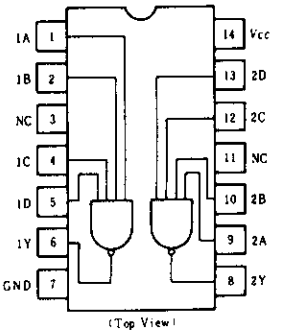
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# HD74LS22 ●Dual 4-input Positive NAND Gates (with Open Collector Outputs)

## ■CIRCUIT SCHEMATIC(½)




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output voltage | $V_{OH}$ | — | — | 5.5 | V |
| Low level output current | $I_{OL}$ | — | — | 8 | mA |

## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$ | $I_{OL}=8mA$ | — | — | 0.5 | V |
| | | | $I_{OL}=4mA$ | — | — | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | μA |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| Output current | $I_{OH}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$ | | — | — | 100 | μA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | — | 0.4 | 0.8 | mA |
| | $I_{CCL}$ | $V_{CC}=5.25V$ | | — | 1.2 | 2.2 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

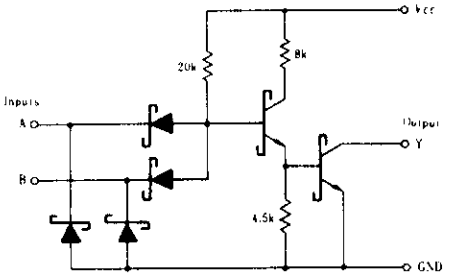
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | — | 17 | 32 | ns |
| | $t_{PHL}$ | | — | 15 | 28 | ns |

Note) Refer to Test Circuit and Waveform of the Common Item

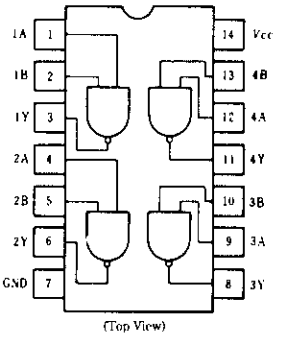
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# HD74LS26 ●Quadruple 2-input High-voltage Interface Positive NAND Gates

## ■CIRCUIT SCHEMATIC(¼)




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output voltage | $V_{OH}$ | – | – | 15 | V |
| Low level output current | $I_{OL}$ | – | – | 8 | mA |

## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Output current | $I_{OH}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$ | $V_{OH}=12V$ | – | – | 50 | μA |
| | | | $V_{OH}=15V$ | – | – | 1 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 0.8 | 1.6 | mA |
| | $I_{CCL}$ | | | – | 2.4 | 4.4 | |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | – | 17 | 32 | ns |
| | $t_{PHL}$ | | – | 15 | 28 | |

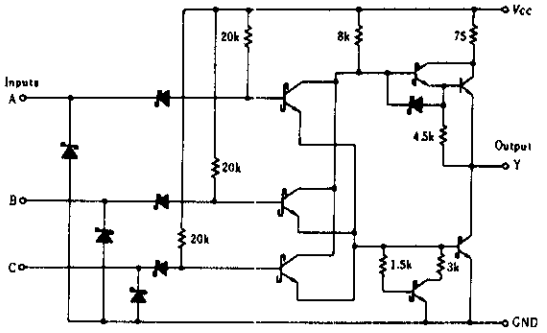
Note) Refer to Test Circuit and Waveform of the Common Item



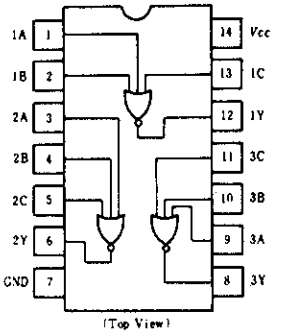
Home Print

# HD74LS27 ●Triple 3-input Positive NOR Gates

## ■CIRCUIT SCHEMATIC(⅓)




## ■PIN ARRANGEMENT




## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$ | $I_{OL}=4mA$ | – | – | 0.4 | |
| | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 2.0 | 4.0 | mA |
| | $I_{CCL}$ | $V_{CC}=5.25V$ | | – | 3.4 | 6.8 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

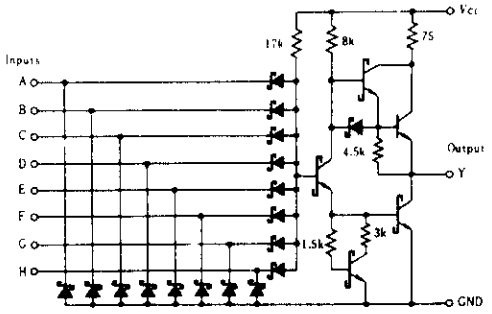
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | – | 10 | 15 | ns |
| | $t_{PHL}$ | | – | 10 | 15 | |

Note) Refer to Test Circuit and Waveform of the Common Item

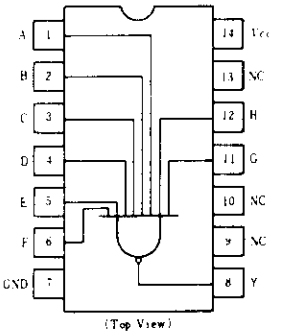
Home Print

# HD74LS30 ●8-input Positive NAND Gate

## ■CIRCUIT SCHEMATIC




## ■PIN ARRANGEMENT




## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$ | $I_{OL}=8mA$ | — | — | 0.5 | V |
| | | | $I_{OL}=4mA$ | — | — | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | — | 0.35 | 0.5 | mA |
| | $I_{CCL}$ | | | — | 0.6 | 1.1 | |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | — | 8 | 15 | ns |
| | $t_{PHL}$ | | — | 13 | 20 | |

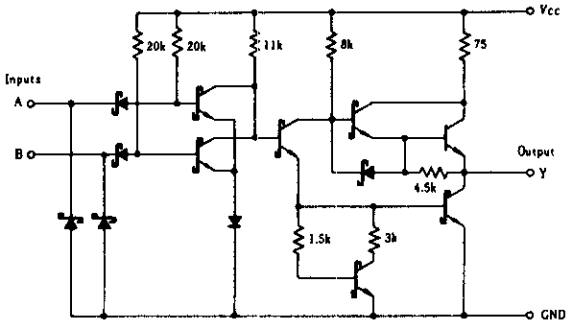
Note) Refer to Test Circuit and Waveform of the Common Item



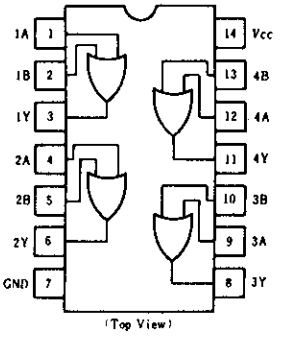
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# HD74LS32 ●Quadruple 2-input Positive OR Gates

## ■CIRCUIT SCHEMATIC(¼)




## ■PIN ARRANGEMENT




## ■ELECTRICAL CHARACTERISTICS ( $Ta$=−20～+75℃ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $I_{OH}$=−400μA | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IL}$=0.8V | $I_{OL}$=8mA | – | – | 0.5 | V |
| | | | $I_{OL}$=4mA | – | – | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | – | −100 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}$=5.25V | | – | 3.1 | 6.2 | mA |
| | $I_{CCL}$ | $V_{CC}$=5.25V | | – | 4.9 | 9.8 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

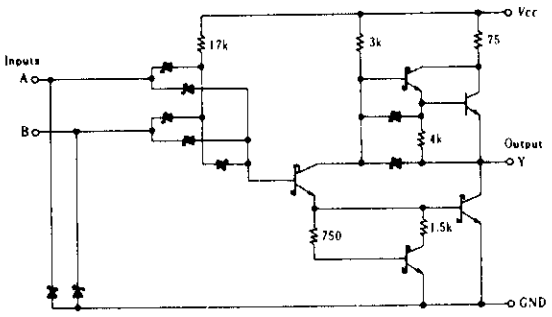
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$=15pF, $R_L$=2kΩ | – | 14 | 22 | ns |
| | $t_{PHL}$ | | – | 14 | 22 | ns |

Note) Refer to Test Circuit and Waveform of the Common Item

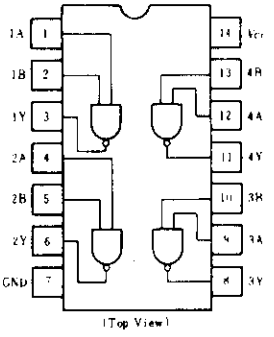
Home Print

# HD74LS37 ●Quadruple 2-input Positive NAND Buffers

## ■CIRCUIT SCHEMATIC(¼)




## ■PIN ARRANGEMENT



(Top View)

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output current | $I_{OH}$ | – | – | −1.2 | mA |
| Low level output current | $I_{OL}$ | – | – | 24 | mA |

## ■ELECTRICAL CHARACTERISTICS ( $Ta$=−20～+75℃ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IL}$=0.8V, $I_{OH}$=−1.2mA | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V | $I_{OL}$=24mA | – | – | 0.5 | V |
| | | | $I_{OL}$=12mA | – | – | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −30 | – | −130 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}$=5.25V | | – | 0.9 | 2.0 | mA |
| | $I_{CCL}$ | $V_{CC}$=5.25V | | – | 6 | 12 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$=45pF, $R_L$=667Ω | – | 12 | 24 | ns |
| | $t_{PHL}$ | | – | 12 | 24 | ns |

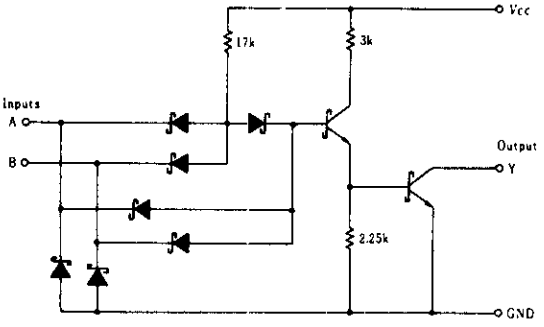
Note) Refer to Test Circuit and Waveform of the Common Item



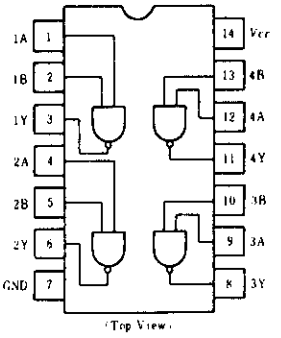
Home Print

# HD74LS38 ●Quadruple 2-input Positive NAND Buffers (with Open Collector Outputs)

## ■CIRCUIT SCHEMATIC(¼)




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output voltage | $V_{OL}$ | – | – | 5.5 | V |
| Low level output current | $I_{OL}$ | – | – | 24 | mA |

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$ | $I_{OL}=24mA$ | – | – | 0.5 | V |
| | | | $I_{OL}=12mA$ | – | – | 0.4 | |
| Output current | $I_{OH}$ | $V_{CC}=4.75V$, $V_I=0.8V$, $V_{OH}=5.5V$ | | – | – | 250 | μA |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 0.9 | 2.0 | mA |
| | $I_{CCL}$ | $V_{CC}=5.25V$ | | – | 6 | 12 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

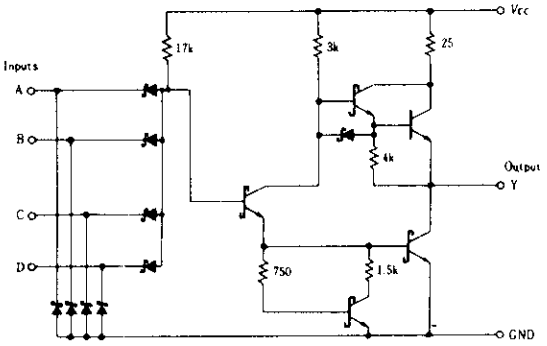
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=45pF$, $R_L=667\Omega$ | – | 20 | 32 | ns |
| | $t_{PHL}$ | | – | 18 | 28 | ns |

Note) Refer to Test Circuit and Waveform of the Common Item

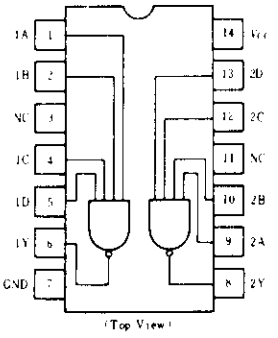
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# HD74LS40 ●Dual 4-input Positive NAND Buffers

## ■CIRCUIT SCHEMATIC(½)




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output current | $I_{OH}$ | – | – | −1.2 | mA |
| Low level output current | $I_{OL}$ | – | – | 24 | mA |

## ■ELECTRICAL CHARACTERISTICS ( $Ta$ = −20 ~ +75℃ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$ = 4.75V, $V_{IL}$ = 0.8V, $I_{OH}$ = −1.2mA | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V | $I_{OL}$ = 24mA | – | – | 0.5 | V |
| | | | $I_{OL}$ = 12mA | – | – | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}$ = 5.25V, $V_I$ = 2.7V | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}$ = 5.25V, $V_I$ = 0.4V | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}$ = 5.25V, $V_I$ = 7V | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$ = 5.25V | | −30 | – | −130 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}$ = 5.25V | | – | 0.45 | 1.0 | mA |
| | $I_{CCL}$ | $V_{CC}$ = 5.25V | | – | 3 | 6 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$ = 4.75V, $I_{IN}$ = −18mA | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$ = 5V, $Ta$ = 25℃ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$ = 45pF, $R_L$ = 667Ω | – | 12 | 24 | ns |
| | $t_{PHL}$ | | – | 12 | 24 | ns |

Note) Refer to Test Circuit and Waveform of the Common Item

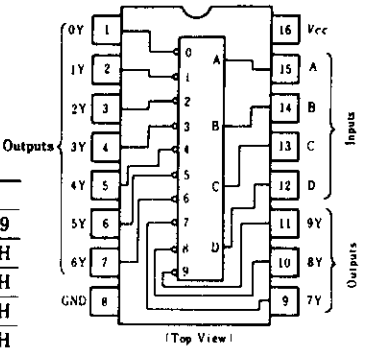


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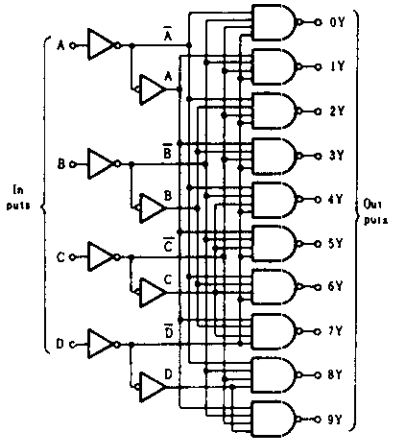
# HD74LS42 ●BCD-to-Decimal Decoder

This monolithic decimal decoder consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■FUNCTION TABLE

| No. | BCD Input | | | | Decimal Output | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | L | L | L | L | L | H | H | H | H | H | H | H | H | H |
| 1 | L | L | L | H | H | L | H | H | H | H | H | H | H | H |
| 2 | L | L | H | L | H | H | L | H | H | H | H | H | H | H |
| 3 | L | L | H | H | H | H | H | L | H | H | H | H | H | H |
| 4 | L | H | L | L | H | H | H | H | L | H | H | H | H | H |
| 5 | L | H | L | H | H | H | H | H | H | L | H | H | H | H |
| 6 | L | H | H | L | H | H | H | H | H | H | L | H | H | H |
| 7 | L | H | H | H | H | H | H | H | H | H | H | L | H | H |
| 8 | H | L | L | L | H | H | H | H | H | H | H | H | L | H |
| 9 | H | L | L | H | H | H | H | H | H | H | H | H | H | L |
| INVALID | H | L | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

H; high level, L; low level

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=8mA$ | – | – | 0.5 | V |
| | | | $I_{OL}=4mA$ | – | – | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current | $I_{CC}$** | $V_{CC}=5.25V$ | | – | 7 | 13 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC} = 5V$, $Ta = 25°C$
** $I_{CC}$ is measured with all outputs open and all inputs grounded.

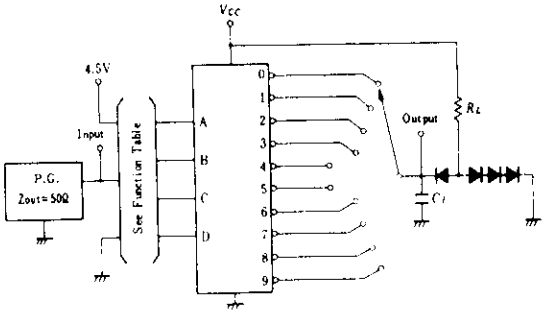
Home Print

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

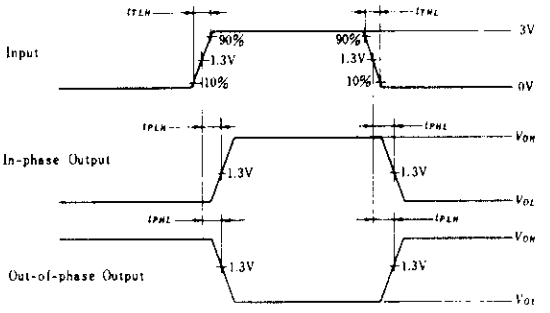
| Item | | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| Propagation delay time | 2 Stage | $t_{PLH}$ | $C_L$= 15pF, $R_L$=2kΩ | – | 15 | 25 | ns |
| | 3 Stage | | | – | 20 | 30 | |
| | 2 Stage | $t_{PHL}$ | | – | 15 | 25 | ns |
| | 3 Stage | | | – | 20 | 30 | |

## ■TESTING METHOD

### 1) Test Circuit




### Waveform




Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz, duty cycle 50%.

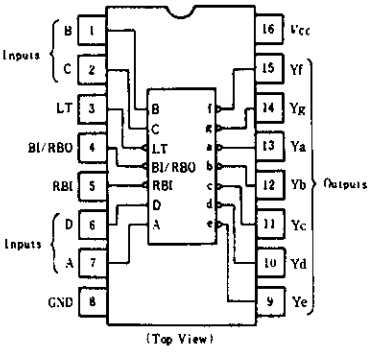


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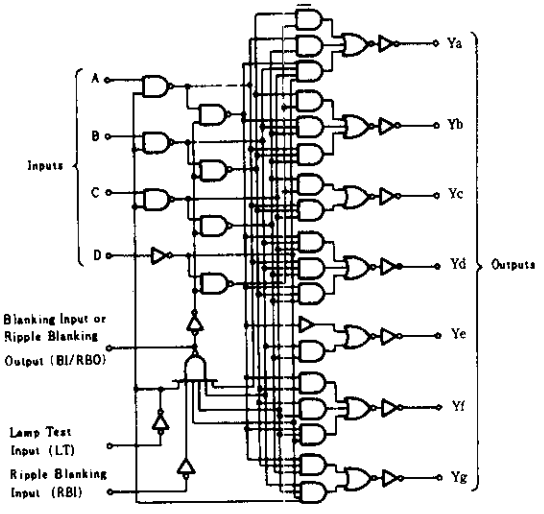
# HD74LS47 ●BCD-to-Seven-Segment Decoder/Driver (with 15V Outputs)

HD74LS47 features active-low outputs designed for driving incandescent indicators directly. This device has full ripple-blanking input/output controls and a lamp test input. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions. This circuit incorporates automatic leading and/or tailling-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. It contains an overriding blanking input (BI) which can be used to control the lamp intensity of pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7.0 | V |
| Input voltage | $V_{IN}$ | 7.0 | V |
| Output current ($t_W \leqq 1$ms, duty cycle $\leqq 10\%$) | $I_{O(peak)}$ | 200 | mA |
| Output current (off-state) | $I_{O(off)}$ | 1 | mA |
| Operating temperature range | $T_{opr}$ | −20 ~ +75 | ℃ |
| Storage temperature range | $T_{stg}$ | −65 ~ +150 | ℃ |

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## ■FUNCTION TABLE

| Decimal or Function | Inputs | | | | | | BI/RBO | Outputs | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LT | RBI | D | C | B | A | | a | b | c | d | e | f | g | |
| 0 | H | H | L | L | L | L | H | ON | ON | ON | ON | ON | ON | OFF | 1 |
| 1 | H | × | L | L | L | H | H | OFF | ON | ON | OFF | OFF | OFF | OFF | |
| 2 | H | × | L | L | H | L | H | ON | ON | OFF | ON | ON | OFF | ON | |
| 3 | H | × | L | L | H | H | H | ON | ON | ON | ON | OFF | OFF | ON | |
| 4 | H | × | L | H | L | L | H | OFF | ON | ON | OFF | OFF | ON | ON | |
| 5 | H | × | L | H | L | H | H | ON | OFF | ON | ON | OFF | ON | ON | |
| 6 | H | × | L | H | H | L | H | OFF | OFF | ON | ON | ON | ON | ON | |
| 7 | H | × | L | H | H | H | H | ON | ON | ON | OFF | OFF | OFF | OFF | |
| 8 | H | × | H | L | L | L | H | ON | ON | ON | ON | ON | ON | ON | |
| 9 | H | × | H | L | L | H | H | ON | ON | ON | OFF | OFF | ON | ON | |
| 10 | H | × | H | L | H | L | H | OFF | OFF | OFF | ON | ON | OFF | ON | |
| 11 | H | × | H | L | H | H | H | OFF | OFF | ON | ON | OFF | OFF | ON | |
| 12 | H | × | H | H | L | L | H | OFF | ON | OFF | OFF | OFF | ON | ON | |
| 13 | H | × | H | H | L | H | H | ON | OFF | OFF | ON | OFF | ON | ON | |
| 14 | H | × | H | H | H | L | H | OFF | OFF | OFF | ON | ON | ON | ON | |
| 15 | H | × | H | H | H | H | H | OFF | OFF | OFF | OFF | OFF | OFF | OFF | |
| BI | × | × | × | × | × | × | L | OFF | OFF | OFF | OFF | OFF | OFF | OFF | 2 |
| RBI | H | L | L | L | L | L | L | OFF | OFF | OFF | OFF | OFF | OFF | OFF | 3 |
| LT | L | × | × | × | × | × | H | ON | ON | ON | ON | ON | ON | ON | 4 |

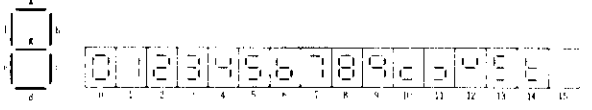
H; high level, L; low level, X; irrelevant

Notes: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.

3. When ripple-blanking input (RBI) and inputs A, B, C, and D are a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).

4. When a blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.



## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | V |
| Off-state output voltage * | $V_{O(off)}$ | | | 15 | V |
| On-state output current * | $I_{O(on)}$ | | | 24 | mA |
| High level output current ** | $I_{OH}$ | — | | −50 | μA |
| Low level output current ** | $I_{OL}$ | | | 3.2 | mA |
| Operating temperature range | $T_{opr}$ | −20 | 25 | 75 | °C |

* Applied to the a through g outputs.
** BI/RBO terminal.



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## ■ELECTRICAL CHARACTERISTICS ( $Ta$=−20～+75℃ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | BI/RBO | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−50μA | | 2.4 | – | – | V |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=1.6mA | – | – | 0.4 | V |
| | | | | $I_{OL}$=3.2mA | – | – | 0.5 | V |
| | a～g | $V_{O(on)}$ | $V_{CC}$=5.25V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{O(on)}$=12mA | – | – | 0.4 | V |
| | | | | $I_{O(on)}$=24mA | – | – | 0.5 | V |
| Output current | a～g | $I_{O(off)}$ | $V_{CC}$=5.25V, $V_{IH}$=2V, $V_{IL}$=0.8V, $V_{O(off)}$=15V | | – | – | 250 | μA |
| Input current | | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | – | – | 20 | μA |
| | All input except BI/RBO | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | – | – | −0.4 | mA |
| | BI/RBO | | | | – | – | −1.2 | mA |
| | | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.1 | mA |
| Short-circuit output current | BI/RBO | $I_{OS}$ | $V_{CC}$=5.25V | | −0.3 | – | −2 | mA |
| Supply current ** | | $I_{CC}$ | $V_{CC}$=5.25V | | – | 7 | 13 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | V |

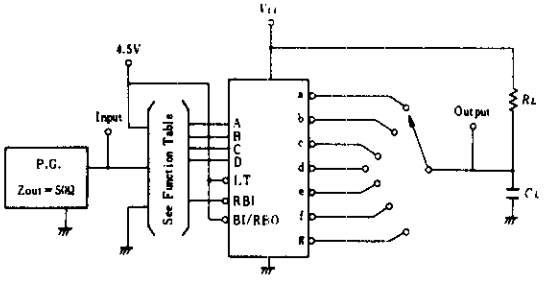
* $V_{CC}$=5V, $Ta$=25°C
** $I_{CC}$ is measured with all outputs open and all inputs at 4.5V.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

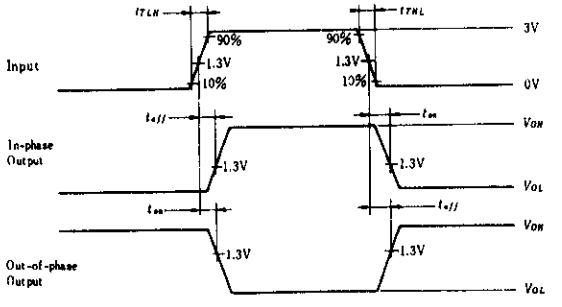
| Item | Symbol | Input | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| Turn-on time | $t_{on}$ | A | $C_L$=15pF, $R_L$=665Ω | – | – | 100 | ns |
| | | RBI | | – | – | 100 | ns |
| Turn-off time | $t_{off}$ | A | | – | – | 100 | ns |
| | | RBI | | – | – | 100 | ns |

## ■TESTING METHOD

### 1) Test Circuit




### Waveform




### 2) Testing Table

| Item | Inputs | | | | | Outputs | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RBI | D | C | B | A | a | b | c | d | e | f | g |
| | 4.5V | GND | GND | GND | IN | OUT | – | – | OUT | OUT | OUT | – |
| $t_{on}$ | 4.5V | GND | GND | 4.5V | IN | – | – | OUT | – | OUT | – | – |
| $t_{off}$ | 4.5V | GND | 4.5V | 4.5V | IN | OUT | OUT | – | OUT | OUT | OUT | OUT |
| | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | OUT | OUT | – |

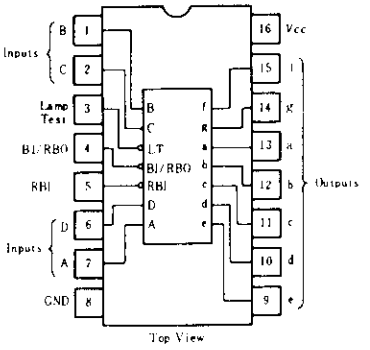
Input pulse; $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz, duty cycle 50%.

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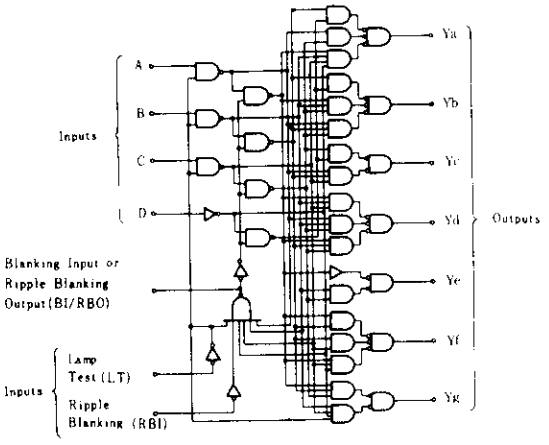
# HD74LS48 ● BCD-to-Seven-Segment Decoder Driver (Internal Pull-up outputs)

The HD74LS48 features active high outputs for driving lamp buffers. This circuit has full ripple blanking input/output controls and a lamp test input. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions. This circuit incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. It contains an overriding blanking input (BI) which can be used to control the lamp intensity be pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■RECOMMENDED OPERATING CONDITIONS

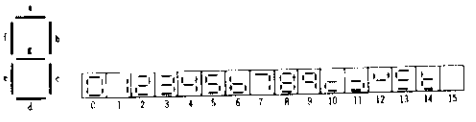
| Item | Symbol | | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| High level output current | $I_{OH}$ | a ~ g | — | — | −100 | μA |
| | | BI/RBO | — | — | −50 | μA |
| Low level output current | $I_{OL}$ | a ~ g | — | — | 6 | mA |
| | | BI/RBO | — | — | 3.2 | mA |

## ■FUNCTION TABLE

| Decimal or Function | Inputs LT | RBI | D | C | B | A | BI/RBO | Outputs a | b | c | d | e | f | g | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | H | H | L | L | L | L | H | H | H | H | H | H | H | L | 1 |
| 1 | H | × | L | L | L | H | H | L | H | H | L | L | L | L | |
| 2 | H | × | L | L | H | L | H | H | H | L | H | H | L | H | |
| 3 | H | × | L | L | H | H | H | H | H | H | H | L | L | H | |
| 4 | H | × | L | H | L | L | H | L | H | H | L | L | H | H | |
| 5 | H | × | L | H | L | H | H | H | L | H | H | L | H | H | |
| 6 | H | × | L | H | H | L | H | L | L | H | H | H | H | H | |
| 7 | H | × | L | H | H | H | H | H | H | H | L | L | L | L | |
| 8 | H | × | H | L | L | L | H | H | H | H | H | H | H | H | |
| 9 | H | × | H | L | L | H | H | H | H | H | L | L | H | H | |
| 10 | H | × | H | L | H | L | H | L | L | L | H | H | L | H | |
| 11 | H | × | H | L | H | H | H | L | L | H | H | L | L | H | |
| 12 | H | × | H | H | L | L | H | L | H | L | L | L | H | H | |
| 13 | H | × | H | H | L | H | H | H | L | L | H | L | H | H | |
| 14 | H | × | H | H | H | L | H | L | L | L | H | H | H | H | |
| 15 | H | × | H | H | H | H | H | L | L | L | L | L | L | L | |
| BI | × | × | × | × | × | × | L | L | L | L | L | L | L | L | 2 |
| RBI | H | L | L | L | L | L | L | L | L | L | L | L | L | L | 3 |
| LT | L | × | × | × | × | × | H | H | H | H | H | H | H | H | 4 |

H; high level, L; low level, X; irrelevant

Notes: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When a blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.





Home Print

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | a~g / BI/RBO | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OH}=-100\mu A$ / $I_{OH}=-50\mu A$ | 2.4 | – | – | V |
| | a~g | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=2mA$ | – | – | 0.4 | V |
| | BI/RBO | | | $I_{OL}=6mA$ | – | – | 0.5 | |
| | | | | $I_{OL}=1.6mA$ | – | – | 0.4 | |
| | | | | $I_{OL}=3.2mA$ | – | – | 0.5 | |
| Output current ** | a~g | $I_O$ | $V_{CC}=4.75V$, $V_O=0.85V$ | | −1.3 | – | – | mA |
| Input current | except BI/RBO | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | BI/RBO | | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −1.2 | |
| | except BI/RBO | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | BI/RBO | $I_{OS}$ | $V_{CC}=5.25V$ | | −0.3 | – | −2 | mA |
| Supply current *** | | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 25 | 38 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

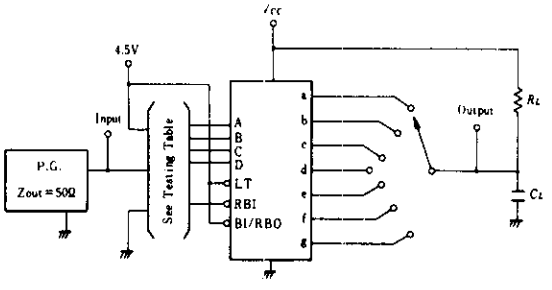
* $V_{CC}=5V$, $Ta=25°C$
** Input condition as for $V_{OH}$
*** $I_{CC}$ is measured with all outputs open and all inputs at 4.5V.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

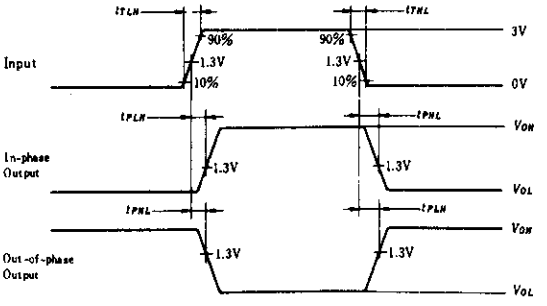
| Item | Symbol | Input | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PHL}$ | A | $C_L=15pF$, $R_L=4k\Omega$ | – | – | 100 | ns |
| | $t_{PLH}$ | | | – | – | 100 | |
| | $t_{PHL}$ | RBI | $C_L=15pF$, $R_L=6k\Omega$ | – | – | 100 | ns |
| | $t_{PLH}$ | | | – | – | 100 | |

## ■TESTING METHOD

### 1) Test Circuit




### Waveform




### 2) Testing Table

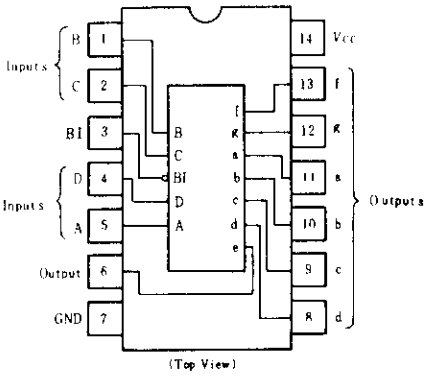
| Item | Inputs | | | | | Outputs | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RBI | D | C | B | A | a | b | c | d | e | f | g |
| | 4.5V | GND | GND | GND | IN | OUT | – | – | OUT | OUT | OUT | – |
| $t_{PLH}$ | 4.5V | GND | GND | 4.5V | IN | – | – | OUT | – | OUT | – | – |
| $t_{PHL}$ | 4.5V | GND | 4.5V | 4.5V | IN | OUT | OUT | – | OUT | OUT | OUT | OUT |
| | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | OUT | OUT | – |

Home Print

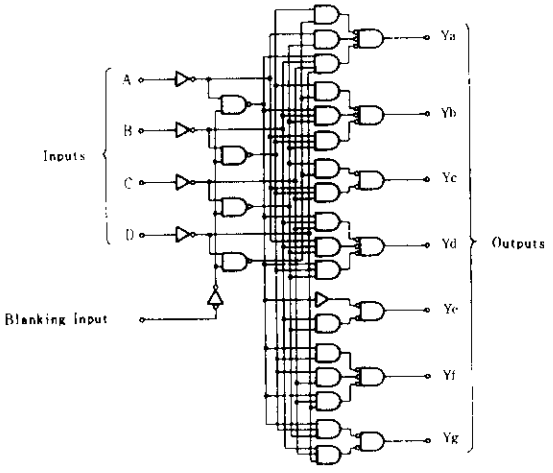
# HD74LS49 ●BCD-to-Seven Segment Decoder Driver (with Open collector outputs)

The HD74LS49 features active-high outputs for driving lamp buffer. This circuit incorporates a direct blanking input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions. It contains an over-riding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the output. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7.0 | V |
| Input voltage | $V_{IN}$ | 7.0 | V |
| Output current (off state) | $I_{O(off)}$ | 1 | mA |
| Operating temperature range | $T_{opr}$ | − 20 ~ + 75 | ℃ |
| Storage temperature range | $T_{stg}$ | 65 ~ + 150 | ℃ |

## ■FUNCTION TABLE

| Decimal or Function | Inputs | | | | | Outputs | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D | C | B | A | BI | a | b | c | d | e | f | g | |
| 0 | L | L | L | L | H | H | H | H | H | H | H | L | |
| 1 | L | L | L | H | H | L | H | H | L | L | L | L | |
| 2 | L | L | H | L | H | H | H | L | H | H | L | H | |
| 3 | L | L | H | H | H | H | H | H | H | L | L | H | |
| 4 | L | H | L | L | H | L | H | H | L | L | H | H | |
| 5 | L | H | L | H | H | H | L | H | H | L | H | H | |
| 6 | L | H | H | L | H | L | L | H | H | H | H | H | |
| 7 | L | H | H | H | H | H | H | H | L | L | L | L | |
| 8 | H | L | L | L | H | H | H | H | H | H | H | H | 1 |
| 9 | H | L | L | H | H | H | H | H | L | L | H | H | |
| 10 | H | L | H | L | H | L | L | L | H | H | L | H | |
| 11 | H | L | H | H | H | L | L | H | H | L | L | H | |
| 12 | H | H | L | L | H | L | H | L | L | L | H | H | |
| 13 | H | H | L | H | H | H | L | L | H | L | H | H | |
| 14 | H | H | H | L | H | L | L | L | H | H | H | H | |
| 15 | H | H | H | H | H | L | L | L | L | L | L | L | |
| BI | × | × | × | × | L | L | L | L | L | L | L | L | 2 |

H; high level, L; low level, X; irrelevant

Notes: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.





Home Print

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output current | $I_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$ | | – | – | 250 | μA |
| Output voltage | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Supply current ** | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 8 | 15 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

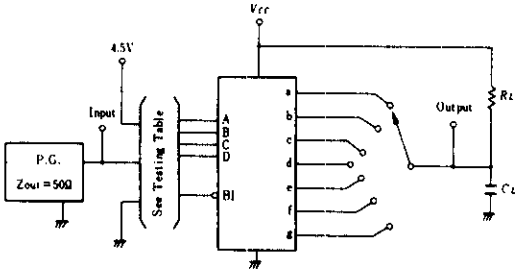
** $I_{CC}$ is measured with all outputs open and all inputs at 4.5V.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

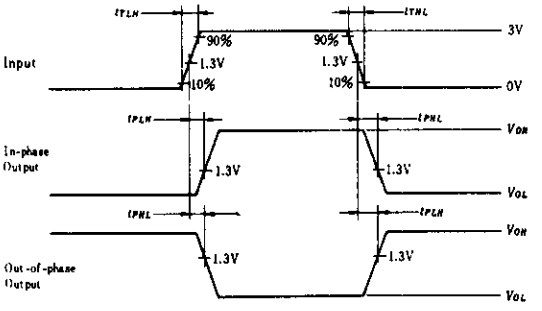
| Item | Symbol | Input | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PHL}$ | A | $C_L=15pF$, $R_L=2k\Omega$ | – | – | 100 | ns |
| | $t_{PLH}$ | | | – | – | 100 | |
| | $t_{PHL}$ | BI | $C_L=15pF$, $R_L=6k\Omega$ | – | – | 100 | ns |
| | $t_{PLH}$ | | | – | – | 100 | |

## ■TESTING METHOD

### 1) Test Circuit




### Waveform

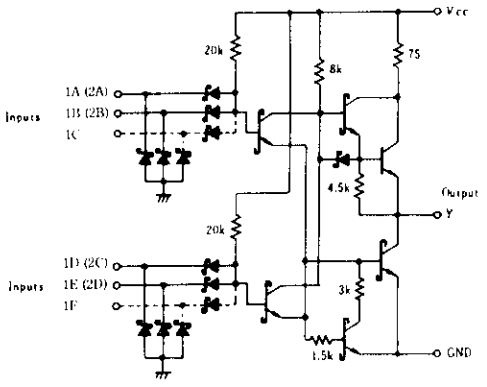



### 2) Testing Table

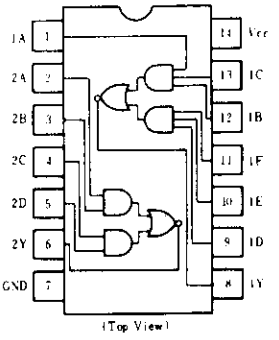
| Item | Inputs | | | | | Outputs | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | BI | D | C | B | A | a | b | c | d | e | f | g |
| | 4.5V | GND | GND | GND | IN | OUT | – | – | OUT | OUT | OUT | – |
| $t_{PLH}$ | 4.5V | GND | GND | 4.5V | IN | – | – | OUT | – | OUT | – | – |
| $t_{PHL}$ | 4.5V | GND | 4.5V | 4.5V | IN | OUT | OUT | – | OUT | OUT | OUT | OUT |
| | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | OUT | OUT | – |

# HD74LS51 ●2-wide 2-input, 2-wide 3-input AND-OR-INVERT Gates

## ■CIRCUIT SCHEMATIC(½)




## ■PIN ARRANGEMENT




## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$ | $I_{OL}=8mA$ | – | – | 0.5 | V |
| | | | $I_{OL}=4mA$ | – | – | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.2 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 0.8 | 1.6 | mA |
| | $I_{CCL}$ | | | – | 1.4 | 2.8 | |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | – | 12 | 20 | ns |
| | $t_{PHL}$ | | – | 12.5 | 20 | |

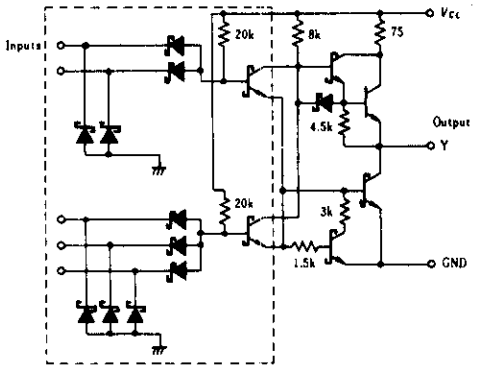
Note) Refer to Test Circuit and Waveform of the Common Item



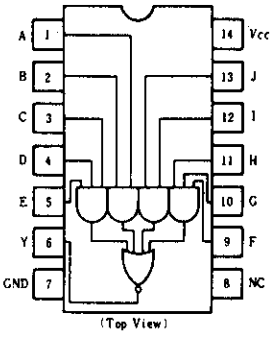
Home Print

# HD74LS54 ●4-wide 2-input, 3-input AND-OR-INVERT Gates

## ■CIRCUIT SCHEMATIC




## ■PIN ARRANGEMENT




Note) The schematic within the dashed line is included the half input terminals of HD74LS54.

## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$ | $I_{OL}=8mA$ | – | – | 0.5 | V |
| | | | $I_{OL}=4mA$ | – | – | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 0.8 | 1.6 | mA |
| | $I_{CCL}$ | | | – | 1.0 | 2.0 | |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

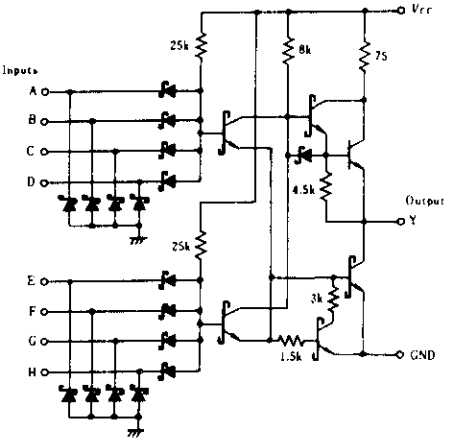
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=15pF$, $R_L=2k\Omega$ | – | 12 | 20 | ns |
| | $t_{PHL}$ | | – | 12.5 | 20 | |

Note) Refer to Test Circuit and Waveform of the Common Item

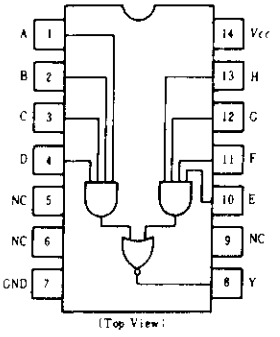
Home Print

# HD74LS55 ●2-wide 4-input AND-OR-INVERT Gates

## ■CIRCUIT SCHEMATIC




## ■PIN ARRANGEMENT




## ■ELECTRICAL CHARACTERISTICS ( $Ta$=−20～+75℃ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V | $I_{OL}$=8mA | – | – | 0.5 | V |
| | | | $I_{OL}$=4mA | – | – | 0.4 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | – | −100 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}$=5.25V | | – | 0.4 | 0.8 | mA |
| | $I_{CCL}$ | | | – | 0.7 | 1.3 | |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$=15pF, $R_L$=2kΩ | – | 12 | 20 | ns |
| | $t_{PHL}$ | | – | 12.5 | 20 | |

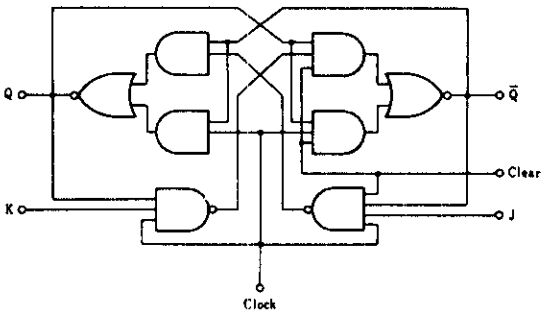
Note) Refer to Test Circuit and Waveform of the Common Item



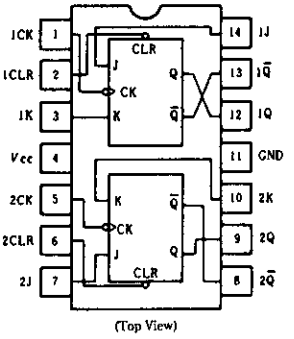
Home Print

# HD74LS73A ●Dual J-K Flip-Flops (with Clear)

## ■BLOCK DIAGRAM(½)




## ■PIN ARRANGEMENT




(Top View)

## ■FUNCTION TABLE

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| Clear | Clock | J | K | Q | $\bar{Q}$ |
| L | × | × | × | L | H |
| H | ↓ | L | L | $Q_0$ | $\bar{Q}_0$ |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | Toggle | |
| H | H | × | × | $Q_0$ | $\bar{Q}_0$ |

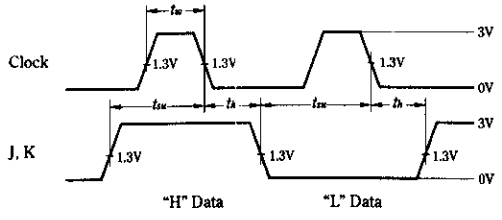
Notes) H; high level, L; low level, X; irrelevant
↓; transition from high to low level
$Q_0$; level of Q before the indicated steady-state input conditions were established.
$\bar{Q}_0$; complement of $\bar{Q}0$ or level of Q before the indicated steady-state input conditions were established.
Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

## ■RECOMMENDED OPERATING CONDITION

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | | $f_{clock}$ | 0 | — | 30 | MHz |
| Pulse width | Clock High | $t_w$ | 20 | — | — | ns |
| | Clear Low | | 25 | — | — | |
| Setup time | "H" Data | $t_{su}$ | 20↓ | — | — | ns |
| | "L" Data | | 20↓ | — | — | |
| Hold time | | $t_h$ | 0↓ | — | — | ns |

Note) ↓; The arrow indicates the falling edge.

## ■TIMING DEFINITION




Home Print

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=8mA$ | — | — | 0.5 | V |
| | | | | $I_{OL}=4mA$ | — | — | 0.4 | |
| Input current | J, K | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | $\mu A$ |
| | Clear | | | | — | — | 60 | |
| | Clock | | | | — | — | 80 | |
| | J, K | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| | Clear | | | | — | — | 0.8 | |
| | Clock | | | | — | — | −0.8 | |
| | J, K | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| | Clear | | | | — | — | 0.3 | |
| | Clock | | | | — | — | 0.4 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current ** | | $I_{CC}$ | $V_{CC}=5.25V$ | | — | 4 | 6 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

** With all outputs open, $I_{CC}$ is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

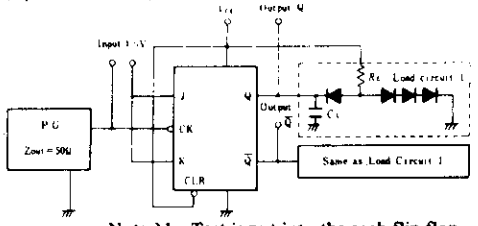
## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | | | $C_L=15pF$, $R_L=2k\Omega$ | 30 | 45 | — | MHz |
| Propagation delay time | $t_{PLH}$ | Clear | Q, $\bar{Q}$ | | — | 15 | 20 | ns |
| | $t_{PHL}$ | Clock | | | — | 15 | 20 | ns |

## ■TESTING METHOD

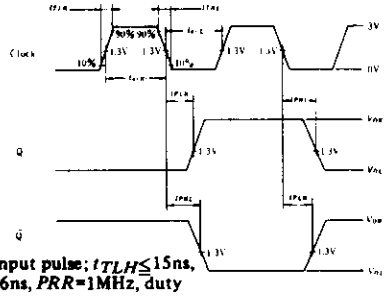
1) Test Circuit

1.1) $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Clock→Q, $\bar{Q}$)



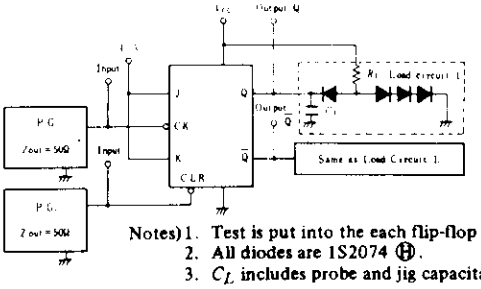

Notes) 1. Test is put into the each flip flop
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

Waveform



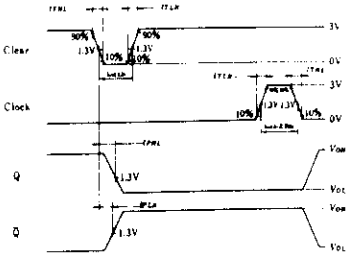

Note) Clock input pulse; $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$, $PRR=1MHz$, duty cycle=50% and: for $f_{max}$, $t_{TLH}=t_{THL} \leq 2.5ns$.

1.2) $t_{PHL}$ (Clear →Q), $t_{PLH}$ (Clear→$\bar{Q}$)




Notes) 1. Test is put into the each flip-flop
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

Waveform




Note) Clear and clock input pulse; $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$, $PRR=1MHz$



Home Print

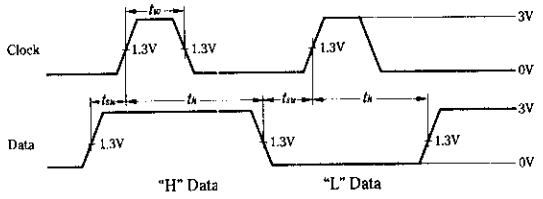
# HD74LS74A ●Dual D-type Positive Edge-triggered Flip-Flops (with Preset and Clear)

## ■FUNCTION TABLE

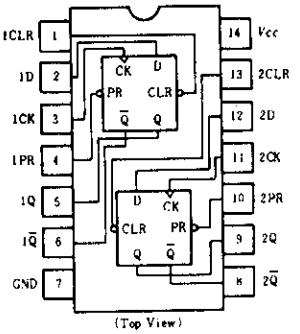
| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| Preset | Clear | Clock | D | Q | $\overline{Q}$ |
| L | H | × | × | H | L |
| H | L | × | × | L | H |
| L | L | × | × | H* | H* |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | × | $Q_0$ | $\overline{Q}_0$ |

Notes) H; high level, L; low level, X; irrelevant
↑; transition from low to high level
$Q_0$; level of Q before the indicated steady-state conditions were established.
$\overline{Q}_0$; complement of $Q_0$ or level of $\overline{Q}$ before the indicated steady-state input conditions were established.
*; This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

## ■TIMING DEFINITION




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | | $f_{clock}$ | 0 | — | 25 | MHz |
| Pulse width | Clock High | $t_W$ | 25 | — | — | ns |
| | Clear Preset | | 25 | — | — | |
| Setup time | "H" Data | $t_{su}$ | 20↑ | — | — | ns |
| | "L" Data | | 20↑ | — | — | |
| Hold time | | $t_h$ | 5↑ | — | — | ns |

Note) ↑; The arrow indicates the rising edge.

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$, $V_{IH}=2V$ | $I_{OL}=8mA$ | — | — | 0.5 | V |
| | | | | $I_{OL}=4mA$ | — | — | 0.4 | |
| Input current | D | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | μA |
| | Clear | | | | — | — | 40 | |
| | Preset | | | | — | — | 40 | |
| | Clock | | | | — | — | 20 | |
| | D | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| | Clear | | | | — | — | −0.8 | |
| | Preset | | | | — | — | −0.8 | |
| | Clock | | | | — | — | −0.4 | |
| | D | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| | Clear | | | | — | — | 0.2 | |
| | Preset | | | | — | — | 0.2 | |
| | Clock | | | | — | — | 0.1 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current | | $I_{CC}$** | $V_{CC}=5.25V$ | | — | 4 | 8 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$
** With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Home Print

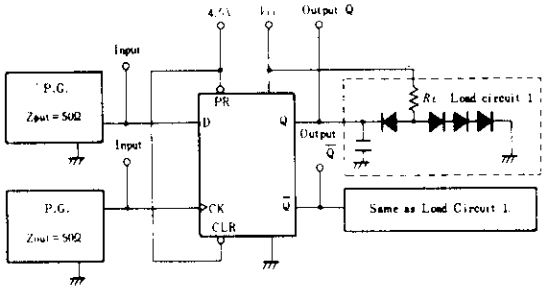
## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

| Item | Symbol | Inputs | Outputs | Test Condition | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | | | $C_L$=15pF, $R_L$=2kΩ | 25 | 33 | – | MHz |
| Propagation delay time | $t_{PLH}$ | Clock, Clear or Preset | Q, $\bar{Q}$ | | – | 13 | 25 | ns |
| | $t_{PHL}$ | | | | – | 25 | 40 | ns |

## ■TESTING METHOD

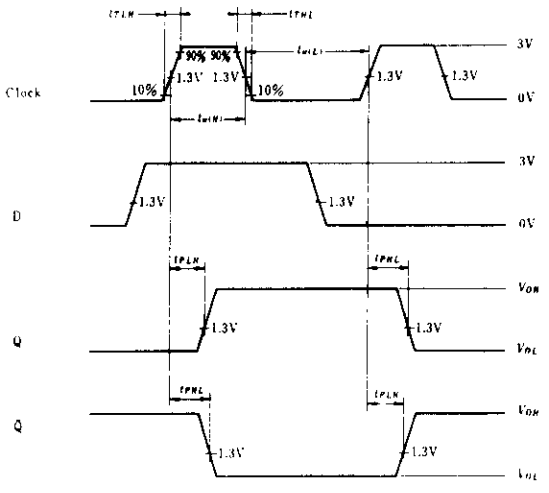
1) Test Circuit

1.1) $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Clock→Q,$\bar{Q}$)



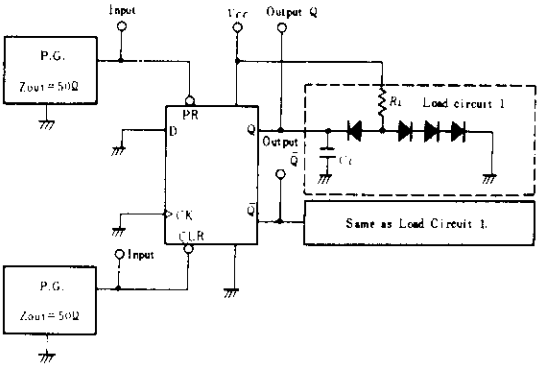

Notes) 1. Test is put into the each flip-flop
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

Waveform



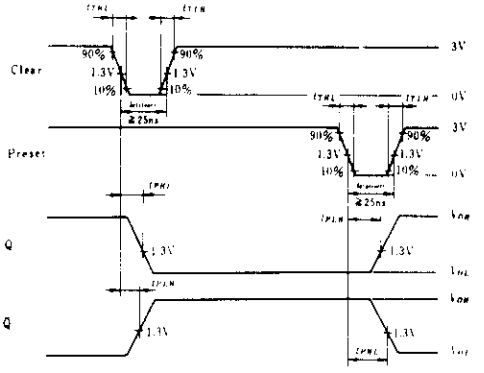

Note) Clock input pulse; $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz, duty cycle=50% and: for $f_{max}$, $t_{TLH}$=$t_{THL}$≦2.5ns.

1.2) $t_{PHL}$, $t_{PLH}$ (Clear or Preset→Q,$\bar{Q}$)




Notes) 1. Test is put into the each flip-flop
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

Waveform




Note) Clear and preset input pulse; $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz

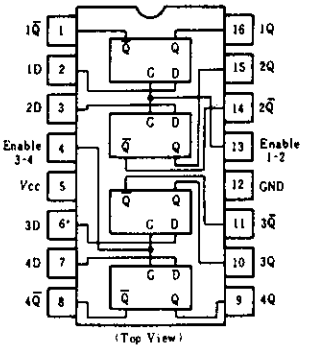


Home Print

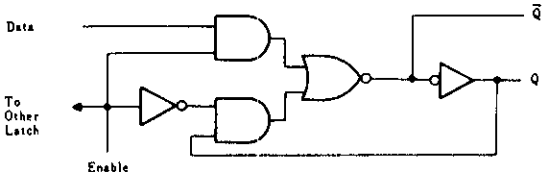
# HD74LS75 ●Quadruple Bistable Latches

The HD74LS75 is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data(D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high. This device features complementary Q and $\bar{Q}$ outputs from a 4-bit latch.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM(¼)




## ■FUNCTION TABLE

| Inputs | | Outputs | |
|---|---|---|---|
| D | G | Q | $\bar{Q}$ |
| L | H | L | H |
| H | H | H | L |
| × | L | $Q_0$ | $\bar{Q}_0$ |

Notes) H; high level, L; low level, X; irrelevant
$Q_0$; level of Q before the indicated steady-state input conditions were established.
$\bar{Q}_0$; complement of $Q_0$ or level of $\bar{Q}$ before the indicated steady-state input conditions were established.

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Pulse width | $t_w$ | 20 | – | – | ns |
| Setup time | $t_{su}$ | 15 | – | – | ns |
| Hold time | $t_h$ | 5 | – | – | ns |

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | D input | – | – | 20 | μA |
| | | | G input | – | – | 80 | |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | D input | – | – | −0.4 | mA |
| | | | G input | – | – | −1.6 | |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | D input | – | – | 0.1 | mA |
| | | | G input | – | – | 0.4 | |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current ** | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 6.3 | 12 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C
** $I_{CC}$ is measured with all outputs open and all inputs grounded.

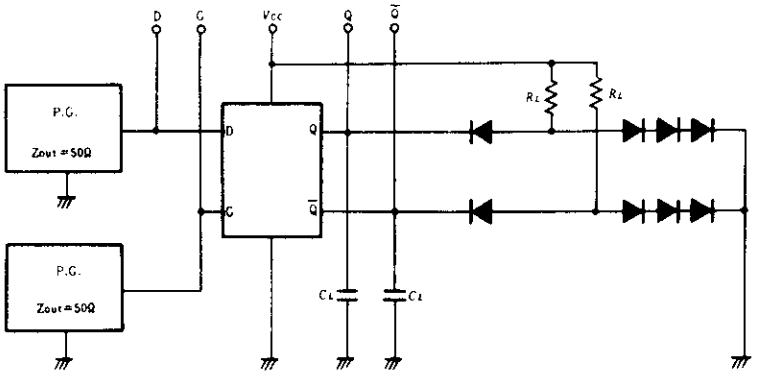
Home Print

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

| Item | Symbol | Input | Output | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | D | Q | $C_L$=15pF, $R_L$=2kΩ | — | 15 | 27 | ns |
| | $t_{PHL}$ | | | | — | 9 | 17 | |
| | $t_{PLH}$ | D | $\overline{Q}$ | | — | 12 | 20 | ns |
| | $t_{PHL}$ | | | | — | 7 | 15 | |
| | $t_{PLH}$ | G | Q | | — | 15 | 27 | ns |
| | $t_{PHL}$ | | | | — | 14 | 25 | |
| | $t_{PLH}$ | G | $\overline{Q}$ | | — | 16 | 30 | ns |
| | $t_{PHL}$ | | | | — | 7 | 15 | |

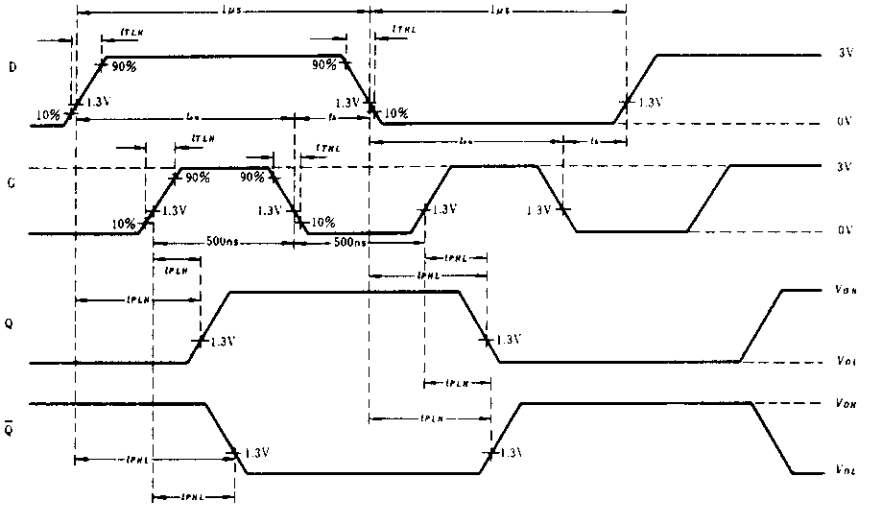
## ■TESTING METHOD

1) Test Circuit




Notes) 1. Test is put into the each latch
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

Waveform



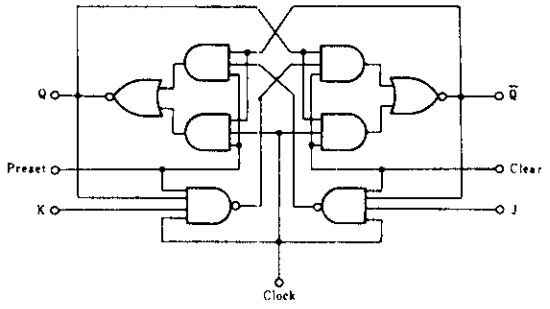

Notes) 1. Input pulse; D input; $PRR$=500kHz, G input; $PRR$=1MHz, $t_{THL} \leqq 10$ns, $t_{TLH} \leqq 10$ns.
2. When measuring propagation delay times from the D input, the corresponding $\overline{G}$ input must be held high.



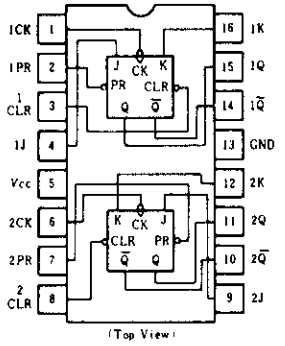
Home Print

# HD74LS76A ●Dual J-K Flip-Flops (with Preset and Clear)

## ■BLOCK DIAGRAM(½)




## ■PIN ARRANGEMENT

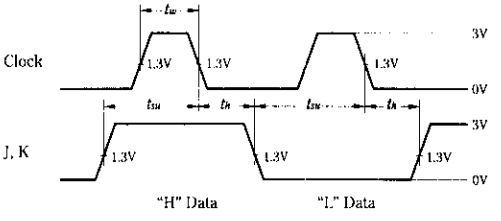



## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | | $f_{clock}$ | 0 | – | 30 | MHz |
| Pulse width | Clock High | $t_W$ | 20 | – | – | ns |
| | Clear Preset Low | | 25 | – | – | |
| Setup time | "H"Data | $t_{su}$ | 20↓ | – | – | ns |
| | "L"Data | | 20↓ | – | – | |
| Hold time | | $t_h$ | 0↓ | – | – | ns |

Note) ↓; The arrow indicates the falling edge.

## ■TIMING DEFINITION




## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=8mA$ | – | – | 0.5 | V |
| | | | | $I_{OL}=4mA$ | – | – | 0.4 | |
| Input current | J, K | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | Clear | | | | – | – | 60 | |
| | Preset | | | | – | – | 60 | |
| | Clock | | | | – | – | 80 | |
| | J, K | $I_{IL}$** | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | Clear | | | | – | – | −0.8 | |
| | Preset | | | | – | – | −0.8 | |
| | Clock | | | | – | – | −0.8 | |
| | J, K | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| | Clear | | | | – | – | 0.3 | |
| | Preset | | | | – | – | 0.3 | |
| | Clock | | | | – | – | 0.4 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current *** | | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 4 | 6 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$
** $I_{IL}$ should not be measured when preset and clear inputs are low at same time.
*** With all outputs open, $I_{CC}$ is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Home Print

## ■FUNCTION TABLE

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| Preset | Clear | Clock | J | K | Q | $\bar{Q}$ |
| L | H | × | × | × | H | L |
| H | L | × | × | × | L | H |
| L | L | × | × | × | H* | H* |
| H | H | ↓ | L | L | $Q_0$ | $\bar{Q}_0$ |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | Toggle | |
| H | H | H | × | × | $Q_0$ | $\bar{Q}_0$ |

Notes) H; high level, L; low level, X; irrelevant
↓; transition from high to low level
$Q_0$; level of Q before the indicated steady-state input conditions were established.
$\bar{Q}_0$; complement of $Q_0$ or level of $\bar{Q}$ before the indicated steady-state input conditions were established.
Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.
*; This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

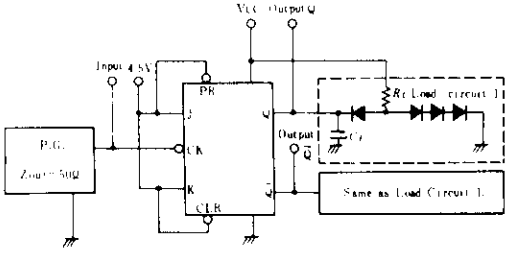
## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25℃$ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | | | $C_L=15pF$, $R_L=2k\Omega$ | 30 | 45 | – | MHz |
| Propagation delay time | $t_{PLH}$ | Clear Preset Clock | Q, $\bar{Q}$ | | | 15 | 20 | ns |
| | $t_{PHL}$ | | | | | 15 | 20 | ns |

## ■TESTING METHOD

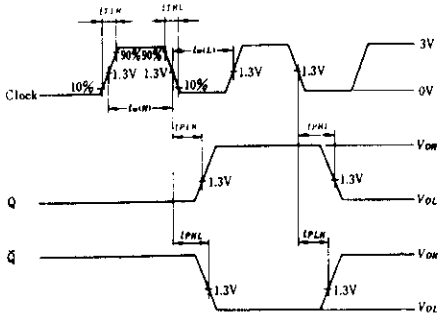
1) Test Circuit

1.1) $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Clock→Q,$\bar{Q}$)



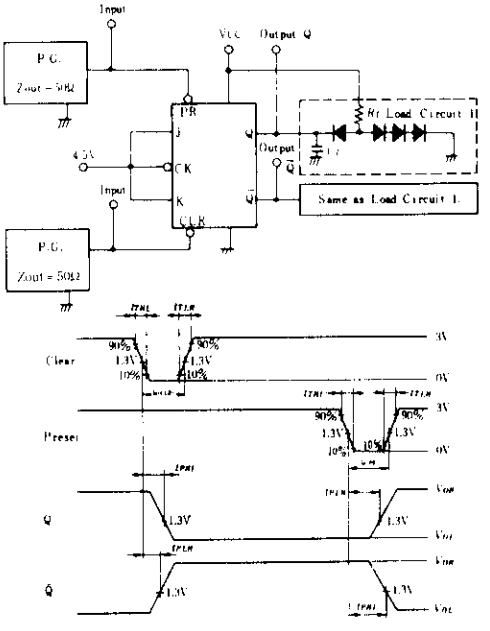

Notes) 1. Test is put into the each flip-flop
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

Waveform




Note) Clock input pulse; $t_{TLH}\leqq 15ns$, $t_{THL}\leqq 6ns$, $PRR=1MHz$, duty cycle=50% and: for $f_{max}$, $t_{TLH}=t_{THL}\leqq 2.5ns$.

1.2) $t_{PHL}$, $t_{PLH}$ (Clear,Preset→Q,$\bar{Q}$)




Note) Clear and preset input pulse; $t_{TLH}\leqq 15ns$, $t_{THL}\leqq 6ns$, $PRR=1MHz$

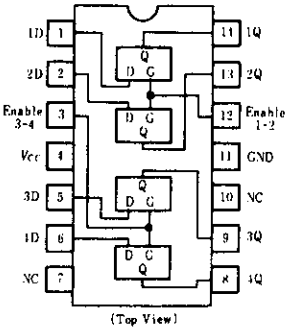


Home Print

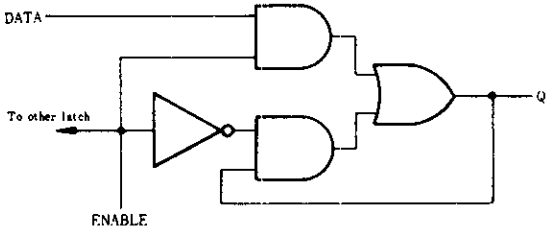
# HD74LS77 ●4-bit Bistable Latches

The HD74LS77 is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data(D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| D | G | Q |
| L | H | L |
| H | H | H |
| X | L | $Q_0$ |

Notes) H; high level, L; low level, X; irrelevant
$Q_0$; level of Q before the indicated steady-state input conditions were established.

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Pulse width | $t_w$ | 20 | — | — | ns |
| Setup time | $t_{su}$ | 20 | — | — | ns |
| Hold time | $t_h$ | 5 | — | — | ns |

## ■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | — | — | 0.4 | V |
| | | | | $I_{OL}=8mA$ | — | — | 0.5 | |
| Input current | D | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | $\mu A$ |
| | G | | | | — | — | 80 | |
| | D | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| | G | | | | — | — | −1.6 | |
| | D | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| | G | | | | — | — | 0.4 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current ** | | $I_{CC}$ | $V_{CC}=5.25V$ | | — | 6.9 | 13 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$
** $I_{CC}$ is measured with all outputs open and all inputs grounded.

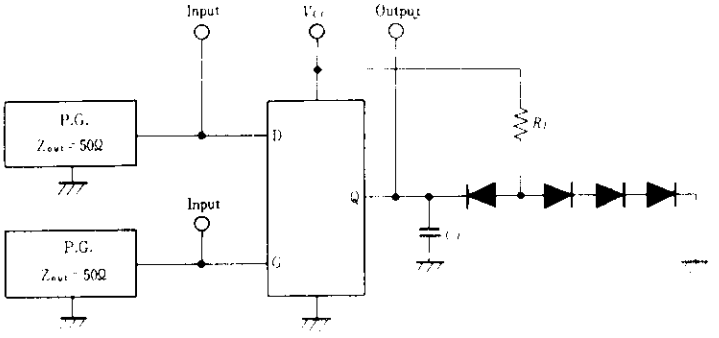
Home Print

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Input | Output | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | D | Q | $C_L$ 15pF<br>$R_L$ 2kΩ | - | 11 | 19 | ns |
| | $t_{PHL}$ | | | | - | 9 | 17 | |
| | $t_{PLH}$ | G | Q | | | 10 | 18 | |
| | $t_{PHL}$ | | | | | 10 | 18 | |

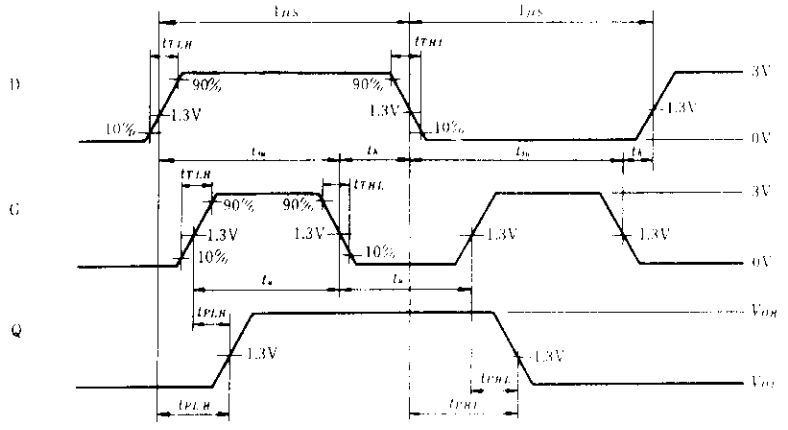
## ■TESTING METHOD

1) Test Circuit




Notes) 1. Test is put into the each latch
2. All diodes are 1S2074 (H).
3. $C_L$ includes probe and jig capacitance.

Waveform



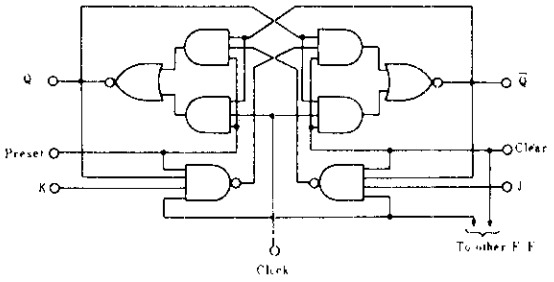

Notes) 1. Input pulse; $t_{TLH}\leqq 15ns$, $t_{THL}\leqq 6ns$.
2. When measuring propagation delay times from the D input, the corresponding G input must be held high.



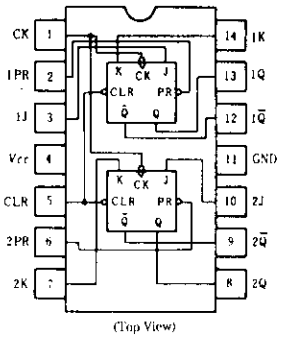
Home Print

# HD74LS78A ●Dual J-K Flip-Flops (with Preset, Common Clear, and Common Clock)

## ■BLOCK DIAGRAM(½)




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | | $f_{clock}$ | 0 | – | 30 | MHz |
| Pulse width | Clock High | $t_w$ | 20 | – | – | ns |
| | Preset Clear Low | | 25 | – | – | ns |
| Setup time | "H" Data | $t_{su}$ | 20↓ | – | – | ns |
| | "L" Data | | 20↓ | – | – | ns |
| Hold time | | $t_h$ | 0↓ | – | – | ns |

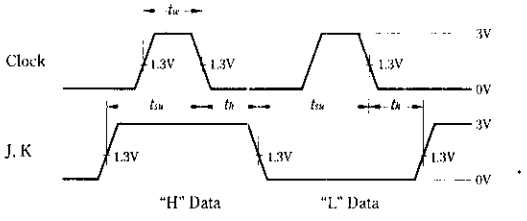
Note) ↓; The arrow indicates the falling edge.

## ■FUNCTION TABLE

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| Preset | Clear | Clock | J | K | Q | $\overline{Q}$ |
| L | H | × | × | × | H | L |
| H | L | × | × | × | L | H |
| L | L | × | × | × | H* | H* |
| H | H | ↓ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | Toggle | |
| H | H | H | × | × | $Q_0$ | $\overline{Q}_0$ |

Notes) H; high level, L; low level, X; irrelevant
↓; transition from high to low level
$Q_0$; level of Q before the indicated steady-state input conditions were established.
$\overline{Q}_0$; complement of $Q_0$ or level of $\overline{Q}$ before the indicated steady-state input conditions were established.
Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.
*; This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

## ■TIMING METHOD




## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2.7V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=8mA$ | – | – | 0.5 | V |
| | | | | $I_{OL}=4mA$ | – | – | 0.4 | |
| Input current | J, K | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | Clear | | | | – | – | 120 | |
| | Preset | | | | – | – | 60 | |
| | Clock | | | | – | – | 160 | |
| | J, K | $I_{IL}$** | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | Clear | | | | – | – | −1.6 | |
| | Preset | | | | – | – | −0.8 | |
| | Clock | | | | – | – | −1.6 | |
| | J, K | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| | Clear | | | | – | – | 0.6 | |
| | Preset | | | | – | – | 0.3 | |
| | Clock | | | | – | – | 0.8 | |
| Short circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current *** | | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 4 | 6 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}$ = 5V, $Ta$ = 25°C
** $I_{IL}$ should not be measured when preset and clear inputs are low at same time.
*** With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Home Print

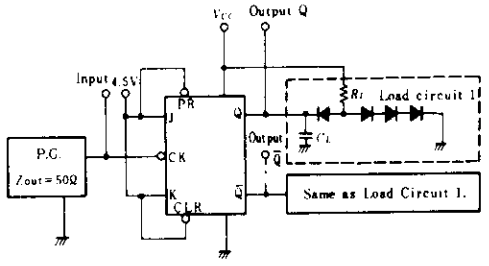
## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25°C )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | | | $C_L$ = 15pF, $R_L$ = 2kΩ | 30 | 45 | | MHz |
| Propagation delay time | $t_{PLH}$ | Clear Preset Clock | Q, $\bar{Q}$ | | – | 15 | 20 | ns |
| | $t_{PHL}$ | | | | – | 15 | 20 | ns |

## ■TESTING METHOD

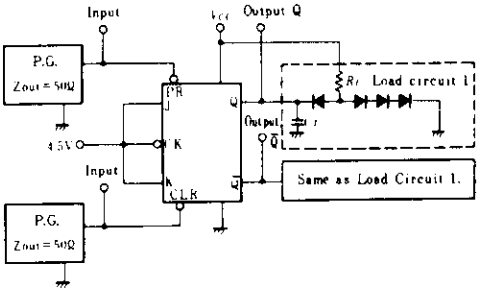
1) Test Circuit

1.1) $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Clock→Q,$\bar{Q}$)

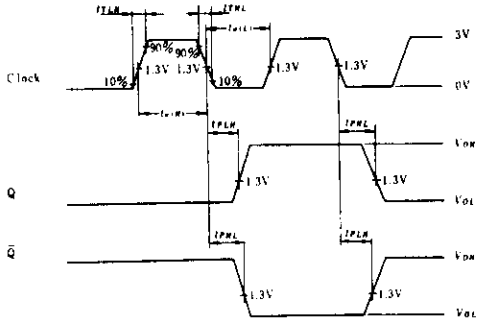



Notes) 1. Test is put into the each flip-flop
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

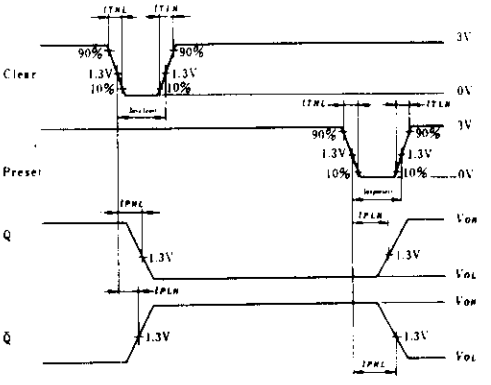
1.2) $t_{PHL}$, $t_{PLH}$ (Clear, Preset→Q,$\bar{Q}$)




Notes) 1. Test is put into the each flip-flop
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.




Note) Clock input pulse; $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz, duty cycle=50% and: for $f_{max}$, $t_{TLH}$=$t_{THL}$≦2.5ns.




Note) Clear and preset input pulse; $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz



Home Print

# HD74LS83A ●4-Bit Binary Full Adders (with Fast Carry)

This improved full addrer performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. This adder features full internal look ahead across all four bit generating the carry term in ten nanoseconds typically. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

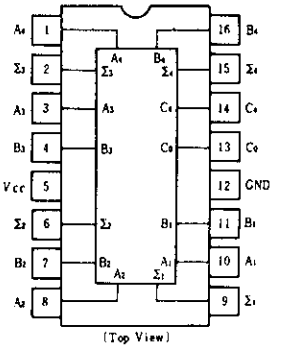
## ■FUNCTION TABLE

| Inputs | | | | Outputs | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | When C0 = L | | | When C0 = H | | |
| | | | | When C2 = L | | | When C2 = H | | |
| $A_1$ / $A_3$ | $B_1$ / $B_3$ | $A_2$ / $A_4$ | $B_2$ / $B_4$ | $\Sigma_1$ / $\Sigma_3$ | $\Sigma_2$ / $\Sigma_4$ | $C_2$ / $C_4$ | $\Sigma_1$ / $\Sigma_3$ | $\Sigma_2$ / $\Sigma_4$ | $C_2$ / $C_4$ |
| L | L | L | L | L | L | L | H | L | L |
| H | L | L | L | H | L | L | L | H | L |
| L | H | L | L | H | L | L | L | H | L |
| H | H | L | L | L | H | L | H | H | L |
| L | L | H | L | L | H | L | H | H | L |
| H | L | H | L | H | H | L | L | L | H |
| L | H | H | L | H | H | L | L | L | H |
| H | H | H | L | L | L | H | H | L | H |
| L | L | L | H | L | H | L | H | H | L |
| H | L | L | H | H | H | L | L | L | H |
| L | H | L | H | H | H | L | L | L | H |
| H | H | L | H | L | L | H | H | L | H |
| L | L | H | H | L | L | H | H | L | H |
| H | L | H | H | H | L | H | L | H | H |
| L | H | H | H | H | L | H | L | H | H |
| H | H | H | H | L | H | H | H | H | H |

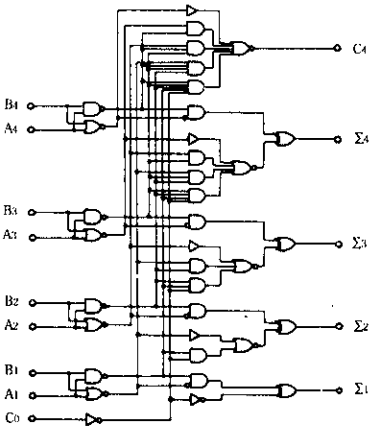
H; high level, L; low level, X; irrelevant

Note) Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The value at C2, A3, B3, A4, and B4 are than used to determine outputs Σ3, Σ4 and C4.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




Home Print

## ■ELECTRICAL CHARACTERISTICS ( $Ta$ = − 20 ~ + 75°C )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | | — | V |
| | | $V_{IL}$ | | | — | | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OH}$ = −400μA | | 2.7 | | — | V |
| | | $V_{OL}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V | $I_{OL}$ = 4mA | — | | 0.4 | V |
| | | | | $I_{OL}$ = 8mA | — | | 0.5 | |
| Input current | except C0 | $I_{IH}$ | $V_{CC}$ = 5.25V, $V_I$ = 2.7V | | — | | 40 | μA |
| | C0 | | | | — | | 20 | |
| | except C0 | $I_{IL}$ | $V_{CC}$ = 5.25V, $V_I$ = 0.4V | | — | | −0.8 | mA |
| | C0 | | | | | | 0.4 | |
| | except C0 | $I_I$ | $V_{CC}$ = 5.25V, $V_I$ = 7V | | — | | 0.2 | mA |
| | C0 | | | | — | | 0.1 | |
| Short circuit output current | | $I_{OS}$ | $V_{CC}$ = 5.25V | | −20 | | −100 | mA |
| Supply current | | $I_{CC}$ | $V_{CC}$ = 5.25V | All inputs = 0V | — | 22 | 39 | mA |
| | | | | B input 0.8V, Other inputs 4.5V | — | 19 | 34 | |
| | | | | All inputs 4.5V | — | 19 | 34 | |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$ = 4.75V, $I_{IN}$ = −18mA | | — | | −1.5 | V |

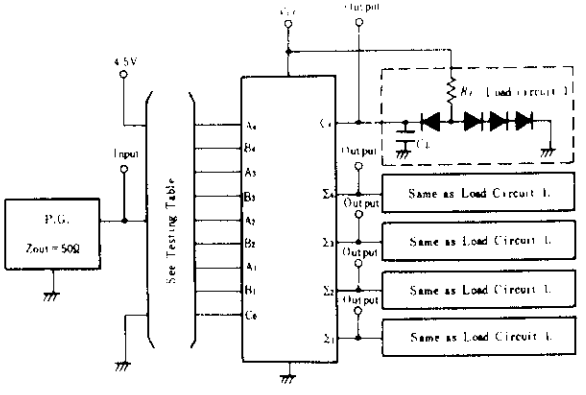
* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$ = 5V, $Ta$ = 25°C )

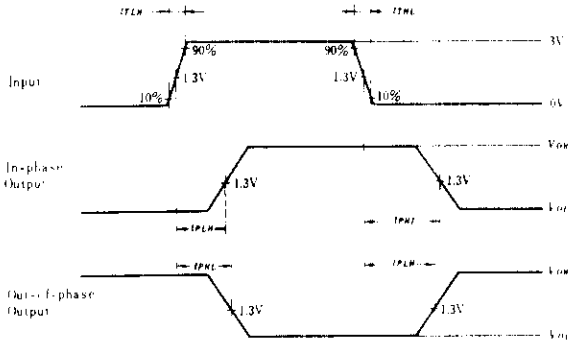
| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_0$ | $\Sigma_0$ | $C_L$ = 15pF, $R_L$ = 2kΩ | | 16 | 24 | ns |
| | $t_{PHL}$ | | | | | 15 | 24 | ns |
| | $t_{PLH}$ | $A_0$, $B_0$ | $\Sigma_0$ | | — | 15 | 24 | ns |
| | $t_{PHL}$ | | | | — | 15 | 24 | ns |
| | $t_{PLH}$ | $C_0$ | $C_4$ | | — | 11 | 17 | ns |
| | $t_{PHL}$ | | | | | 15 | 22 | ns |
| | $t_{PLH}$ | $A_3$, $B_3$ | $C_4$ | | | 11 | 17 | ns |
| | $t_{PHL}$ | | | | — | 12 | 17 | ns |

## ■TESTING METHOD

1) Test Circuit




Waveform




Notes) 1. Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz, duty cycle=50%
2. $C_L$ includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ.



Home Print

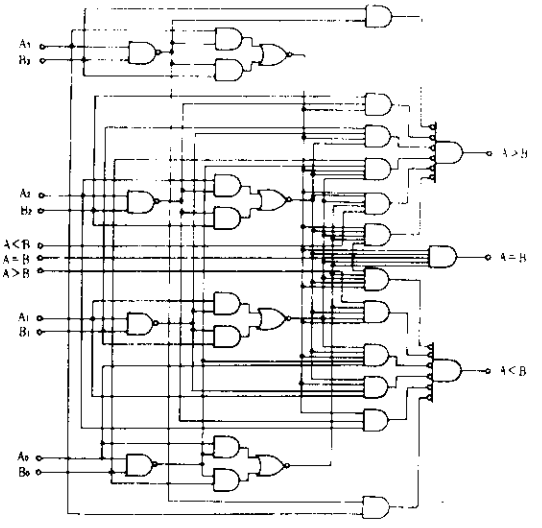
2) Testing Table

| Item | From input to output | Inputs | | | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $B_4$ | $A_4$ | $B_3$ | $A_3$ | $B_2$ | $A_2$ | $B_1$ | $A_1$ | $C_0$ | $C_4$ | $\Sigma_4$ | $\Sigma_3$ | $\Sigma_2$ | $\Sigma_1$ |
| | $C_0$ | GND | GND | GND | GND | GND | GND | GND | GND | IN | —— | —— | —— | —— | OUT |
| | →$\Sigma_i$ or $C_4$ | GND | 4.5V | GND | 4.5V | GND | 4.5V | GND | 4.5V | IN | OUT | OUT | OUT | OUT | OUT |
| | | GND | GND | GND | GND | GND | GND | GND / IN | IN / GND | GND | —— | —— | —— | —— | OUT |
| | | GND | GND | GND | GND | GND / IN | IN / GND | GND | GND | GND | —— | —— | —— | OUT | —— |
| | | GND | GND | GND / IN | IN / GND | GND | GND | GND | GND | GND | —— | —— | OUT | —— | —— |
| $t_{PLH}$ | | GND / IN | IN / GND | GND | GND | GND | GND | GND | GND | GND | —— | OUT | —— | —— | —— |
| $t_{PHL}$ | $A_i$ or $B_i$ | GND | GND | GND | GND | GND | GND | 4.5V / IN | IN / 4.5V | GND | —— | —— | —— | OUT | OUT |
| | →$\Sigma_i$ or $C_4$ | GND | GND | GND | GND | 4.5V / IN | IN / 4.5V | GND | GND | GND | —— | —— | OUT | OUT | —— |
| | | GND | GND | 4.5V / IN | IN / 4.5V | GND | GND | GND | GND | GND | —— | OUT | OUT | —— | —— |
| | | 4.5V / IN | IN / 4.5V | GND | GND | GND | GND | GND | GND | GND | OUT | OUT | —— | —— | —— |

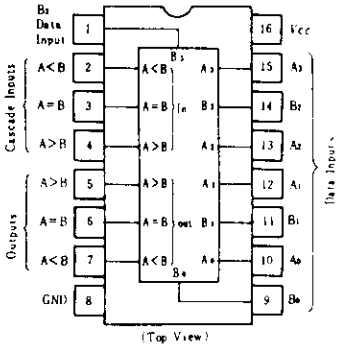
# HD74LS85 ●4-bit Magnitude Comparators

This four bit magnitude comparator performs comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. This device is fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A>B, A<B, and A=B outputs of a stage handling less-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the AßB input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

## ■BLOCK DIAGRAM



## ■PIN ARRANGEMENT




## ■FUNCTION TABLE

| Inputs | | | | Cascading inputs | | | Outputs | | |
|---|---|---|---|---|---|---|---|---|---|
| $A_3$, $B_3$ | $A_2$, $B_2$ | $A_1$, $B_1$ | $A_0$, $B_0$ | A < B | A < B | A = B | A > B | A < B | A = B |
| $A_3 > B_3$ | × | × | × | × | × | × | H | L | L |
| $A_3 < B_3$ | × | × | × | × | × | × | L | H | L |
| $A_3 = B_3$ | $A_2 > B_2$ | × | × | × | × | × | H | L | L |
| $A_3 = B_3$ | $A_2 < B_2$ | × | × | × | × | × | L | H | L |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 > B_1$ | × | × | × | × | H | L | L |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 < B_1$ | × | × | × | × | L | H | L |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1$ | $A_0 > B_0$ | × | × | × | H | L | L |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1$ | $A_0 < B_0$ | × | × | × | L | H | L |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1$ | $A_0 = B_0$ | H | L | L | H | L | L |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1$ | $A_0 = B_0$ | L | H | L | L | H | L |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1$ | $A_0 = B_0$ | × | × | H | L | L | H |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1$ | $A_0 = B_0$ | H | H | L | L | L | L |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1$ | $A_0 = B_0$ | L | L | L | H | H | L |

H; high level, L; low level, X; irrelevant



Home Print

## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75℃$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | A<B, A>B Inputs | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | Other inputs | | | | – | – | 60 | |
| | A<B, A>B Inputs | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | Other inputs | | | | – | – | −1.2 | |
| | A<B, A>B Inputs | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| | Other inputs | | | | – | – | 0.3 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current ** | | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 10.4 | 20 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

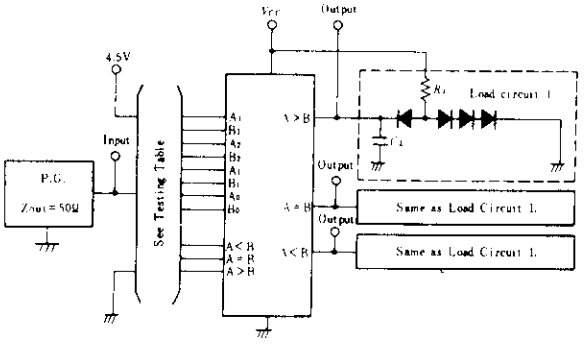
* $V_{CC}$=5V, $Ta$=25°C
** $I_{CC}$ is measured with outputs open, A=B grounded, and all other inputs at 4.5V.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25℃$ )

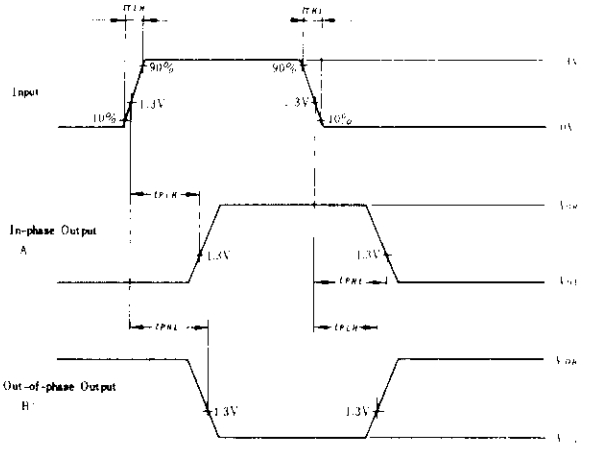
| Item | Symbol | Inputs | Outputs | Number of gate levels | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | Any A or B data Input | A<B, A>B | 1 | $C_L=15pF$, $R_L=2k\Omega$ | – | 14 | – | ns |
| | | | | 2 | | – | 19 | – | |
| | | | | 3 | | – | 24 | 36 | |
| | | | A=B | 4 | | – | 27 | 45 | |
| | $t_{PHL}$ | Any A or B data Input | A<B, A>B | 1 | | – | 11 | – | ns |
| | | | | 2 | | – | 15 | – | |
| | | | | 3 | | – | 20 | 30 | |
| | | | A=B | 4 | | – | 23 | 45 | |
| | $t_{PLH}$ | A<B or A=B | A>B | 1 | | – | 14 | 22 | ns |
| | $t_{PHL}$ | A<B or A=B | A>B | 1 | | – | 11 | 17 | ns |
| | $t_{PLH}$ | A=B | A=B | 2 | | – | 13 | 20 | ns |
| | $t_{PHL}$ | A=B | A=B | 2 | | – | 13 | 26 | ns |
| | $t_{PLH}$ | A>B or A=B | A<B | 1 | | – | 14 | 22 | ns |
| | $t_{PHL}$ | A>B or A=B | A<B | 1 | | – | 11 | 17 | ns |

## ■TESTING METHOD

1) Test Circuit




Waveform




Notes) 1. Input pulse; $t_{TLH} \leq 15$ns, $t_{THL} \leq 6$ns, $PRR = 1$MHz, duty cycle=50%
2. $C_L$ includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ.

2) Testing Table

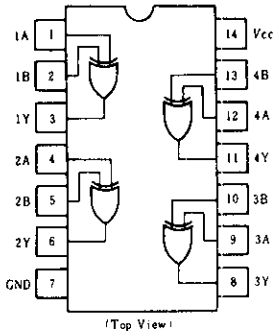
| Item | Inputs | | | | | | | | | | | Output Waveforms | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $A_3$ | $B_3$ | $A_2$ | $B_2$ | $A_1$ | $B_1$ | $A_0$ | $B_0$ | A > B | A = B | A < B | A > B | A = B | A < B |
| | IN | 4.5V | 4.5V | GND | GND | GND | GND | GND | GND | GND | GND | A | | B |
| | 4.5V | IN | GND | 4.5V | GND | GND | GND | GND | GND | GND | GND | B | | A |
| | GND | GND | IN | 4.5V | 4.5V | GND | GND | GND | GND | GND | GND | A | | B |
| | GND | GND | 4.5V | IN | GND | 4.5V | GND | GND | GND | GND | GND | B | | A |
| | GND | GND | GND | GND | IN | 4.5V | 4.5V | GND | GND | GND | GND | A | | B |
| | GND | GND | GND | GND | 4.5V | IN | GND | 4.5V | GND | GND | GND | B | | A |
| $t_{PLH}$ | GND | GND | GND | GND | GND | GND | IN | 4.5V | 4.5V | GND | GND | A | | B |
| $t_{PHL}$ | GND | GND | GND | GND | GND | GND | 4.5V | IN | GND | GND | 4.5V | B | | A |
| | GND | GND | GND | GND | GND | GND | IN | 4.5V | GND | 4.5V | GND | | A | B |
| | GND | GND | GND | GND | GND | GND | 4.5V | IN | GND | 4.5V | GND | B | A | |
| | GND | GND | GND | GND | GND | GND | GND | GND | IN | GND | GND | | | B |
| | GND | GND | GND | GND | GND | GND | GND | GND | GND | IN | GND | B | A | B |
| | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | IN | B | | |



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# HD74LS86 ●Quadruple 2-input Exclusive-OR Gates

## ■PIN ARRANGEMENT




## ■FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

H; high level, L; low level

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75$℃ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | – | – | 0.4 | V |
| | | | $I_{OL}$=8mA | – | – | 0.5 | |
| Input current | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.2 | mA |
| | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | – | – | 40 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | – | – | −0.8 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | – | −100 | mA |
| Supply current ** | $I_{CC}$ | $V_{CC}$=5.25V | | – | 6.1 | 10 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** $I_{CC}$ is measured with all outputs open and all inputs grounded.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

| Item | Symbol | Inputs | Test Conditions | | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A or B | $C_L$=15pF, $R_L$=2kΩ | Other inputs=0V | – | 12 | 23 | ns |
| | $t_{PHL}$ | | | | – | 10 | 17 | ns |
| | $t_{PLH}$ | A or B | | Other inputs=4.5V | – | 20 | 30 | ns |
| | $t_{PHL}$ | | | | – | 13 | 22 | ns |

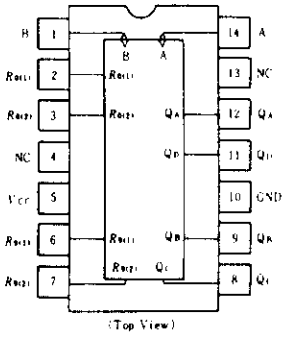
Note) Refer to Test Circuit and Waveform of the Common Item

Home Print

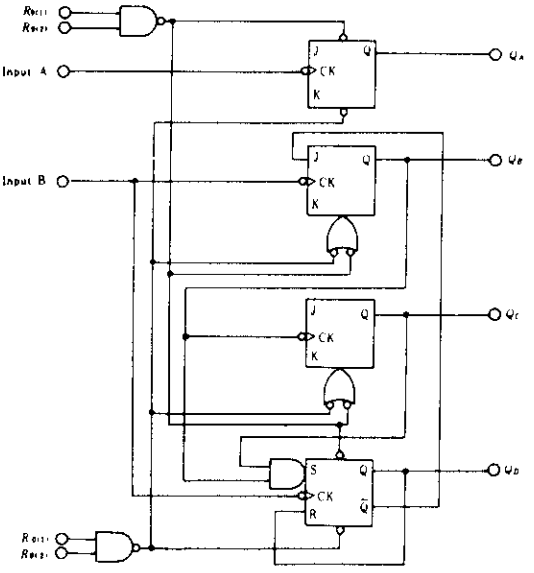
# HD74LS90 ●Decade Counters

The HD74LS90 contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and three-stage binary counter for divide-by-five. This device has a gated zero reset and also has gated set-to-nine inputs for use in BCD nine's complement applications. To use this maximum count length of this counter the B input is connected to the $Q_A$ output. The input count pulses are applied to input A and the outputs are descrived in the appropriate function table. A symmetrical divide-by-ten count can be obtained from HD-74LS90 counter by connecting the $Q_D$ output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output $Q_A$.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■ABSOLUTE MAXIMUM RATINGS

| Item | | Symbol | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 7.0 | V |
| Input voltage | R Inputs | $V_{IN}$ | 7.0 | V |
| | A, B Inputs | | 5.5 | V |
| Operating temperature range | | $T_{opr}$ | −20～+75 | ℃ |
| Storage temperature range | | $T_{stg}$ | −65～+150 | ℃ |

## ■FUNCTION TABLE

### Reset/Count Function Table

| Reset Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| $R_{0(1)}$ | $R_{0(2)}$ | $R_{9(1)}$ | $R_{9(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | × | L | L | L | L |
| H | H | × | L | L | L | L | L |
| × | × | H | H | H | L | L | H |
| × | L | × | L | Count | | | |
| L | × | L | × | Count | | | |
| L | × | × | L | Count | | | |
| × | L | L | × | Count | | | |

### BCD Count Sequence(Notes1)

| Count | Outputs | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

### Bi-Quinary Count Sequence(Notes2)

| Count | Outputs | | | |
|---|---|---|---|---|
| | $Q_A$ | $Q_D$ | $Q_C$ | $Q_B$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

Notes) 1. Output $Q_A$ is connected to input B for BCD count.
2. Output $Q_D$ is connected to input A for Bi-quinary count.
3. H; high level, L; low level, X; irrelevant.

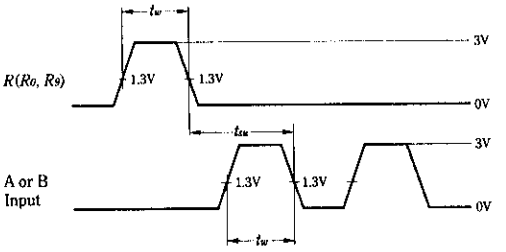


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## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Count frequency | A input | $f_{count}$ | 0 | — | 32 | MHz |
| | B input | | 0 | — | 16 | |
| Pulse width | A input | $t_w$ | 15 | — | — | ns |
| | B input | | 30 | — | — | |
| | Reset inputs | | 15 | — | — | |
| Setup time | | $t_{su}$ | 25 | — | — | ns |

## ■TIMING DEFINITION




## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$** | — | — | 0.4 | V |
| | | | | $I_{OL}=8mA$** | — | — | 0.5 | |
| Input current | Any Reset | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| | A input | | | | — | — | −2.4 | |
| | B input | | | | — | — | −3.2 | |
| | Any Reset | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | μA |
| | A input | | | | — | — | 40 | |
| | B input | | | | — | — | 80 | |
| | Any Reset | $I_I$ | $V_{CC}=5.25V$ | $V_I=7V$ | — | — | 0.1 | mA |
| | A input | | | $V_I=5.5V$ | — | — | 0.2 | |
| | B input | | | | — | — | 0.4 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current *** | | $I_{CC}$ | $V_{CC}=5.25V$ | | — | 9 | 15 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

** $Q_A$ output is tested at specified $I_{OL}$ plus the limit value of $I_{IL}$ for the B input. This permits driving the B input while maintaining full fan out capability.

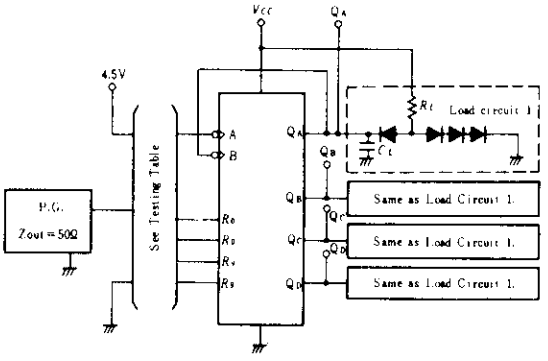
*** $I_{CC}$ is measured with all outputs open, both $R_0$ inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum count frequency | $f_{max}$ | A | $Q_A$ | $C_L=15pF$, $R_L=2k\Omega$ | 32 | 42 | — | MHz |
| | | B | $Q_B$ | | 16 | — | — | |
| Propagation delay time | $t_{PLH}$ | A | $Q_A$ | | — | 10 | 16 | ns |
| | $t_{PHL}$ | | | | — | 12 | 18 | |
| | $t_{PLH}$ | B | $Q_D$ | | — | 32 | 48 | ns |
| | $t_{PHL}$ | | | | — | 34 | 50 | |
| | $t_{PLH}$ | B | $Q_B$ | | — | 10 | 16 | ns |
| | $t_{PHL}$ | | | | — | 14 | 21 | |
| | $t_{PLH}$ | B | $Q_C$ | | — | 21 | 32 | ns |
| | $t_{PHL}$ | | | | — | 23 | 35 | |
| | $t_{PLH}$ | B | $Q_D$ | | — | 21 | 32 | ns |
| | $t_{PHL}$ | | | | — | 23 | 35 | |
| | $t_{PHL}$ | Set-to-0 | $Q_A\sim Q_D$ | | — | 26 | 40 | ns |
| | $t_{PLH}$ | Set-to-9 | $Q_A$, $Q_D$ | | — | 20 | 30 | ns |
| | $t_{PHL}$ | | $Q_B$, $Q_C$ | | — | 26 | 40 | |

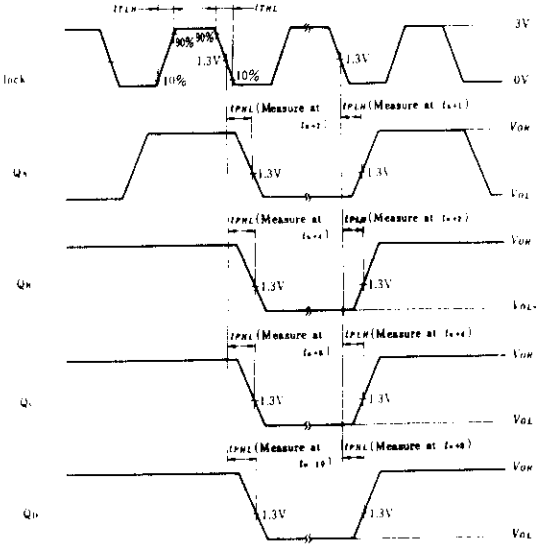
## ■TESTING METHOD

### 1) Test Circuit




Notes) 1. Input pulse; $t_{TLH} \leqq 15$ns. $t_{THL} \leqq 6$ns, $PRR = 1$MHz, duty cycle=50%
2. $C_L$ includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ.

### Waveform-1 $f_{max}$, $t_{PLH}$, $t_{PHL}$(Clock→Q)



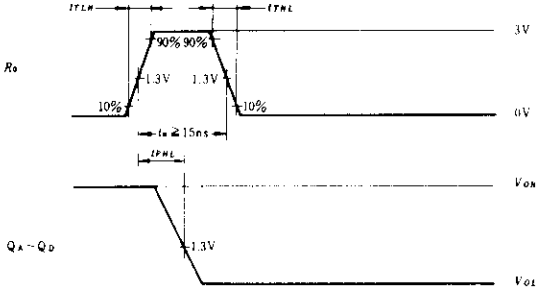

Notes) 1. Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 5$ns, $PRR = 1$MHz, duty cycle=50% and: for $f_{max}$, $t_{TLH} = t_{THL} \leqq 2.5$ns.
2. $t_n$ is reference bit time when all outputs are low.

### 2) Testing Table

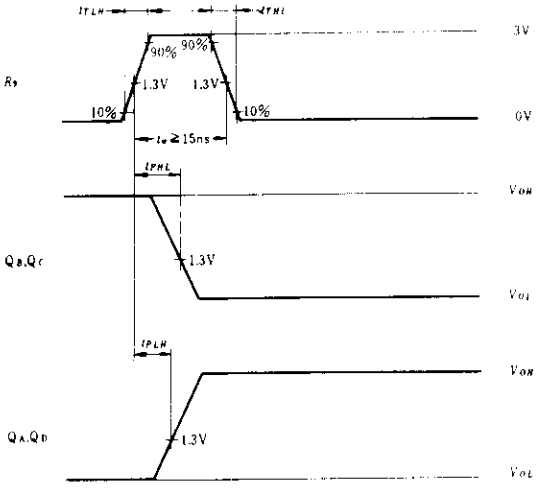
| Item | From input to output | Inputs A | B | R0 | R9 | Outputs QA | QB | QC | QD |
|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | A→Q | IN | to QA | GND | GND | Out | Out | Out | Out |
| | B→Q | 4.5V | IN | GND | GND | – | Out | Out | Out |
| $t_{PLH}$ $t_{PHL}$ | A→QA | IN | to QA | GND | GND | Out | – | – | – |
| | A→QD | IN | to QA | GND | GND | – | – | – | Out |
| | B→QB | 4.5V | IN | GND | GND | – | Out | – | – |
| | B→QC | 4.5V | IN | GND | GND | – | – | Out | – |
| | B→QD | 4.5V | IN | GND | GND | – | – | – | Out |
| | R0*→Q | IN* | to QA | IN | GND | Out | Out | Out | Out |
| | R9*→Q | IN* | to QA | GND | IN | Out | Out | Out | Out |

*; For initialized
**; Measured with each input and unused inputs at 4.5V.

### Waveform-2 $t_{PHL}(R_0 \rightarrow Q)$




### Waveform-3 $t_{PLH}$, $t_{PHL}(R_9 \rightarrow Q)$




Notes) 1. $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 5$ns.



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# HD74LS91 ●8-bit Shift Registers

This serial-in, serial-out, 8-bit shift register is composed of eight R-S master-slave flip-flops, input gating, and a clock drive. Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes these circuits to shift information one bit on the positive edge of an input clock pulse.

## ■FUNCTION TABLE

| Inputs | | Outputs | |
|---|---|---|---|
| $t_n$ | | $t_{n+8}$ | |
| A | B | $Q_H$ | $\overline{Q}_H$ |
| H | H | H | L |
| L | X | L | H |
| X | L | L | H |

Notes) H; high level, L; low level, X; irrelevant
$t_n$; Reference bit time, clock low
$t_{n+8}$; Bit time after 8 low-to-high clock transitions.

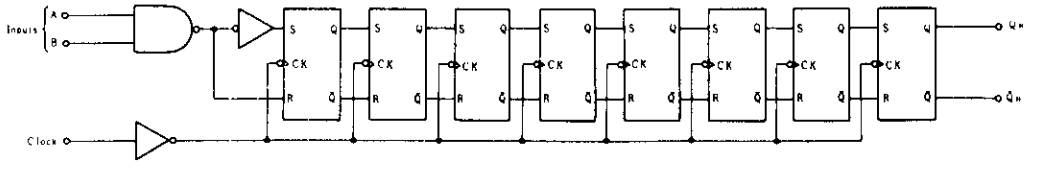
## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | max | Unit |
|---|---|---|---|---|
| Clock pulse width | $t_w$ | 25 | — | ns |
| Setup time | $t_{su}$ | 25 | — | ns |
| Hold time | $t_h$ | 5 | — | ns |

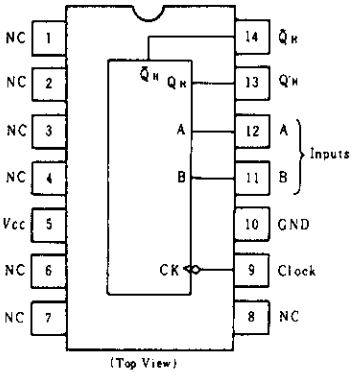
## ■TIMING CHART




## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




Home Print

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | | — | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | — | — | 0.4 | V |
| | | | $I_{OL}=8mA$ | — | | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | | | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| Short circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current | $I_{CC}$** | $V_{CC}=5.25V$ | | — | 12 | 20 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

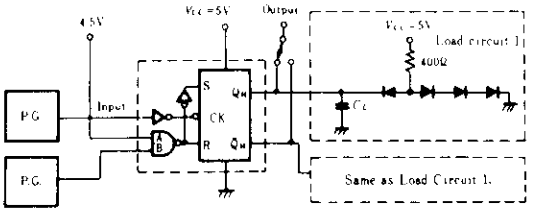
** $I_{CC}$ is measured after the eighth clock pulse with the output open and A and B inputs grounded.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | $C_L=15pF$, $R_L=2k\Omega$ | 10 | 18 | — | MHz |
| Propagation delay time | $t_{PLH}$ | | — | 24 | 40 | ns |
| | $t_{PHL}$ | | — | 27 | 40 | ns |

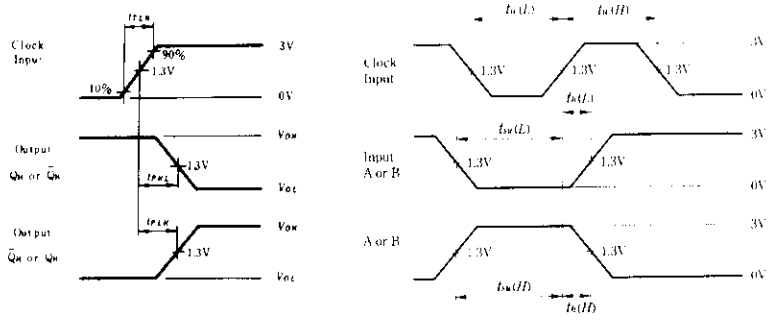
## ■TESTING METHOD

### 1) Test Circuit




Notes) 1. Input pulse; $t_{TLH} \leqq 15ns$, $t_{THL} \leqq 6ns$, $PRR=1MHz$, duty cycle=50%
2. $C_L$ includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ.

### Waveform



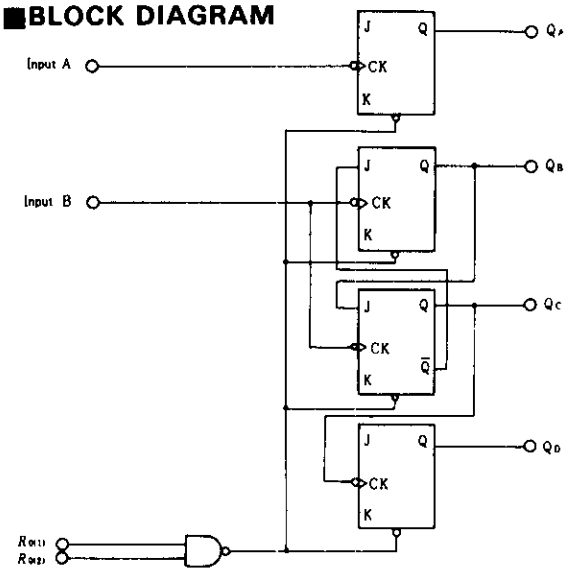



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# HD74LS92 ●Divide-by-Twelve Counters

The HD74LS92 contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and three-stage binary counter for divide-by-six. To use this maximum count length of this counter, the B input is connected to the $Q_A$ output. The input count pulses are applied to input A and the outputs are described in the appropriate function table.

## ■BLOCK DIAGRAM




## ■FUNCTION TABLE

### Reset/Count Function Table

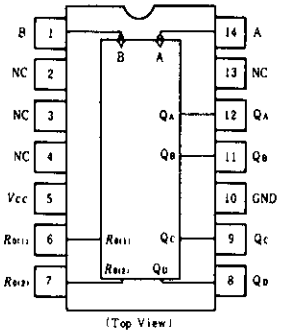
| Reset Inputs | | Outputs | | | |
|---|---|---|---|---|---|
| $R_{0(1)}$ | $R_{0(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | L | L | L |
| L | × | Count | | | |
| × | L | Count | | | |

### BCD Count Sequence (Notes 1)

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | H | L | L | L |
| 7 | H | L | L | H |
| 8 | H | L | H | L |
| 9 | H | L | H | H |
| 10 | H | H | L | L |
| 11 | H | H | L | H |

Notes) 1. Output $Q_A$ is connected to input B for BCD count.
3. H; high level, L; low level, X; irrelevant

## ■PIN ARRANGEMENT



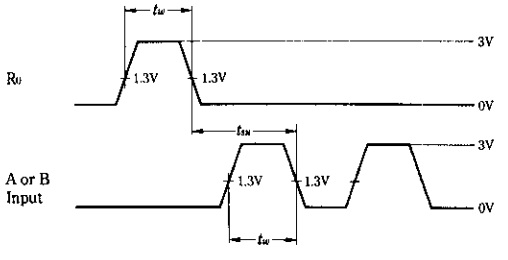

## ■ABSOLUTE MAXIMUM RATINGS

| Item | | Symbol | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 7.0 | V |
| Input voltage | R Input | $V_{IN}$ | 7.0 | V |
| | A, B Input | | 5.5 | V |
| Operating temperature range | | $T_{opr}$ | −20 ~ +75 | ℃ |
| Storage temperature range | | $T_{stg}$ | −65 ~ +150 | ℃ |

## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Count frequency | A input | $f_{count}$ | 0 | – | 32 | MHz |
| | B input | | 0 | – | 16 | |
| Pulse width | A input | $t_W$ | 15 | – | – | ns |
| | B input | | 30 | – | – | |
| | Reset inputs | | 15 | – | – | |
| Setup time | | $t_{su}$ | 25 | – | – | ns |

## ■TIMING DEFINITION




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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | 2.0 | – | | V |
| | | $V_{IL}$ | | – | – | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OH}$ = −400μA | 2.7 | – | | V |
| | | $V_{OL}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $I_{OL}$ = 4mA** | – | – | 0.4 | V |
| | | $V_{OL}$ | $V_{IL}$ = 0.8V, $I_{OL}$ = 8mA** | – | – | 0.5 | V |
| Input current | Any Reset | $I_{IL}$ | $V_{CC}$ = 5.25V, $V_I$ = 0.4V | | – | −0.4 | mA |
| | A input | | | | – | 2.4 | |
| | B input | | | – | – | 3.2 | |
| | Any Reset | $I_{IH}$ | $V_{CC}$ = 5.25V, $V_I$ = 2.7V | – | – | 20 | μA |
| | A input | | | – | – | 40 | |
| | B input | | | – | – | 80 | |
| | Any Reset | $I_I$ | $V_{CC}$ = 5.25V, $V_I$ = 7V | – | – | 0.1 | mA |
| | A input | | $V_I$ = 5.5V | – | – | 0.2 | |
| | B input | | | – | – | 0.4 | |
| Short circuit output current | | $I_{OS}$ | $V_{CC}$ = 5.25V | −20 | – | 100 | mA |
| Supply current *** | | $I_{CC}$ | $V_{CC}$ = 5.25V | – | 9 | 15 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$ = 4.75V, $I_{IK}$ = −18mA | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** $Q_A$ output is tested at specified $I_{OL}$ plus the limit value of $I_{IL}$ for the B input. This permits driving the B input while maintaining full fan-out capability.

*** $I_{CC}$ is measured with all outputs open both $R_0$ inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$ = 5V, $Ta$ = 25°C )

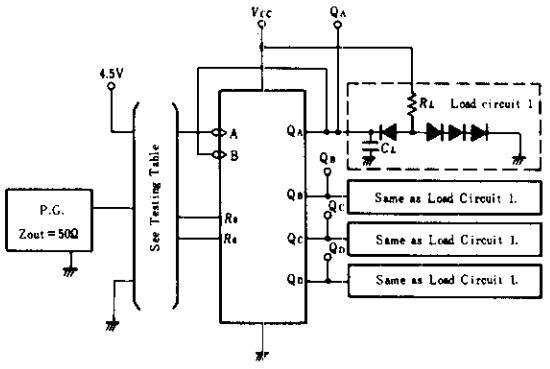
| Item | Symbol | Input | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum count frequency | $f_{max}$ | A | $Q_A$ | $C_L$ = 15pF, $R_L$ = 2kΩ | 32 | 42 | – | MHz |
| | | B | $Q_B$ | | 16 | | – | MHz |
| Propagation delay time | $t_{PLH}$ | A | $Q_A$ | | – | 10 | 16 | ns |
| | $t_{PHL}$ | | | | – | 12 | 18 | ns |
| | $t_{PLH}$ | A | $Q_D$ | | | 32 | 48 | ns |
| | $t_{PHL}$ | | | | – | 34 | 50 | ns |
| | $t_{PLH}$ | B | $Q_B$ | | – | 10 | 16 | ns |
| | $t_{PHL}$ | | | | | 14 | 21 | ns |
| | $t_{PLH}$ | B | $Q_C$ | | – | 10 | 16 | ns |
| | $t_{PHL}$ | | | | – | 14 | 21 | ns |
| | $t_{PLH}$ | B | $Q_D$ | | – | 21 | 32 | ns |
| | $t_{PHL}$ | | | | – | 23 | 35 | ns |
| | $t_{PHL}$ | Set to 0 | $Q_A$ – $Q_D$ | | – | 26 | 40 | ns |



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## ■TESTING METHOD

### 1) Test Circuit



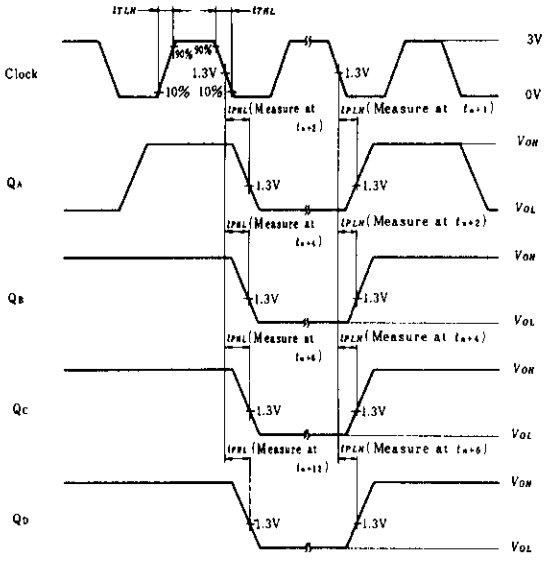

Notes) 1. Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz, duty cycle=50%
2. $C_L$ includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ.

### 2) Testing Table

| Item | From input to output | Inputs A | Inputs B | Inputs $R_0$ | Outputs $Q_A$ | Outputs $Q_B$ | Outputs $Q_C$ | Outputs $Q_D$ |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | A →Q | IN | to $Q_A$ | GND | Out | Out | Out | Out |
| | B →Q | 4.5V | IN | GND | — | Out | Out | Out |
| $t_{PLH}$ $t_{PHL}$ | A →$Q_A$ | IN | to $Q_A$ | GND | Out | — | — | — |
| | A →$Q_D$ | IN | to $Q_A$ | GND | — | — | — | Out |
| | B →$Q_B$ | 4.5V | IN | GND | — | Out | — | — |
| | B →$Q_D$ | 4.5V | IN | GND | — | — | Out | — |
| | B →$Q_D$ | 4.5V | IN | GND | — | — | — | Out |
| | $R_0$ **→Q | IN* | to $Q_A$ | IN | Out | Out | Out | Out |

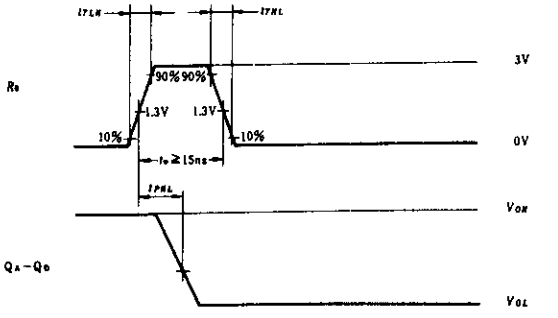
*; For initialized.
**; Measured with each input and unused inputs at 4.5V.

### Waveform-1 $f_{max}$, $t_{PLH}$, $t_{PHL}$(Clock→Q)




Notes) 1. Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 5$ns, $PRR$=1MHz, duty cycle=50% and: for $f_{max}$, $t_{TLH}$=$t_{THL} \leqq 2.5$ns.
2. $t_n$ is reference bit time when all outputs are low.

### Waveform-2 $t_{PHL}$($R_0$→Q)



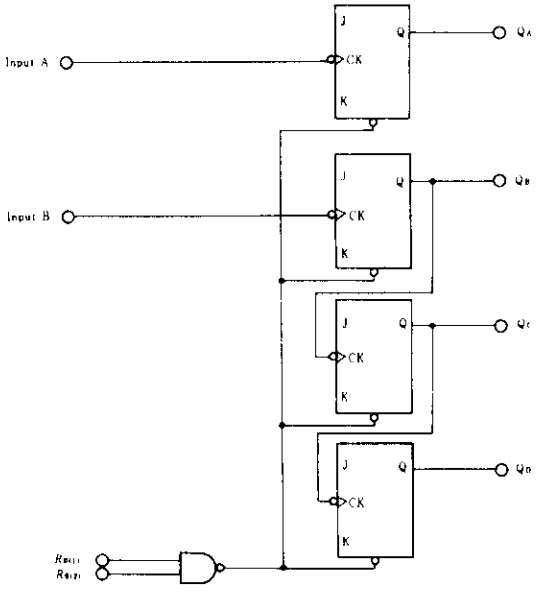

Notes) 1. $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 5$ns.

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# HD74LS93 ●4-bit Binary Counters

The HD74LS93 contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and three-state binary counter for divide-by-eight. To use this maximum count length of this counter, the B input is connected to the $Q_A$ output. The input count pulses are applied to input A and the outputs are described in the appropriate function table.

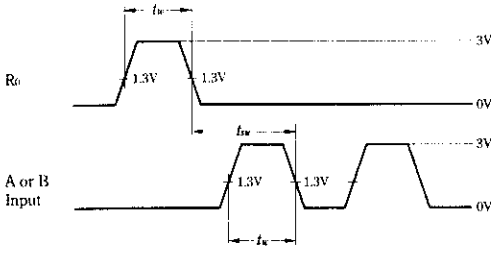
## ■BLOCK DIAGRAM



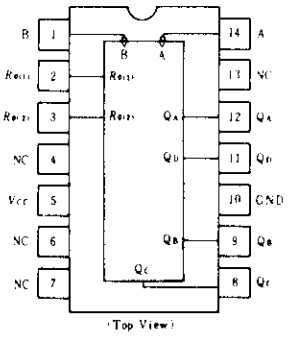

## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Count frequency | A input | $f_{count}$ | 0 | — | 32 | MHz |
| | B input | | 0 | — | 16 | |
| Pulse width | A input | $t_W$ | 15 | — | | ns |
| | B input | | 30 | — | — | |
| | Reset inputs | | 15 | — | — | |
| Setup time | | $t_{su}$ | 25 | — | | ns |

## ■TIMING DEFINITION




## ■PIN ARRANGEMENT




## ■ABSOLUTE MAXIMUM RATINGS

| Item | | Symbol | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 7.0 | V |
| Input voltage | R Inputs | $V_{IN}$ | 7.0 | V |
| | A, B Inputs | | 5.5 | V |
| Operating temperature range | | $T_{opr}$ | −20 ~ +75 | °C |
| Storage temperature range | | $T_{stg}$ | −65 ~ +150 | °C |

## ■FUNCTION TABLE

### ●Reset/Count Function Table

| Reset Inputs | | Outputs | | | |
|---|---|---|---|---|---|
| $R0_{(1)}$ | $R0_{(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | L | L | L |
| L | × | Count | | | |
| × | L | Count | | | |

### ●BCD Count Sequence (Notes 1)

| Count | Outputs | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

Notes) 1. Output $Q_A$ is connected to input B for BCD count.
2. H; high level, L; low level, X; irrelevant



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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$** | — | — | 0.4 | V |
| | | | | $I_{OL}=8mA$** | — | — | 0.5 | |
| Input current | Any Reset | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| | A input | | | | — | — | −2.4 | |
| | B input | | | | — | — | −1.6 | |
| | Any Reset | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | μA |
| | A input | | | | — | — | 40 | |
| | B input | | | | — | — | 40 | |
| | Any Reset | $I_I$ | $V_{CC}=5.25V$ | $V_I=7V$ | — | — | 0.1 | mA |
| | A input | | | $V_I=5.5V$ | — | — | 0.2 | |
| | B input | | | $V_I=5.5V$ | — | — | 0.2 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current | | $I_{CC}$*** | $V_{CC}=5.25V$ | | — | 9 | 15 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

** $Q_A$ output is tested at specified $I_{OL}$ plus the limit value of $I_{IL}$ for the B input. This permits driving the B input while maintaining full fan-out capability.

*** $I_{CC}$ is measured with all outputs open, both $R_0$ inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

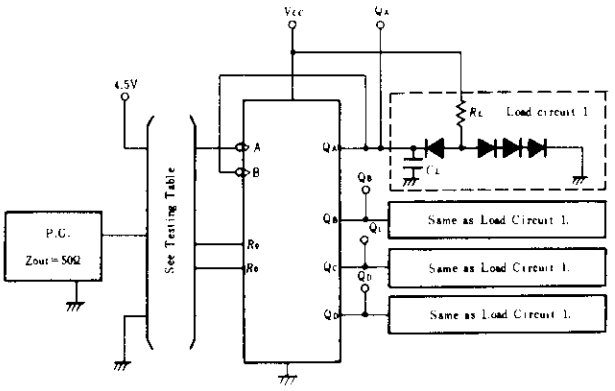
## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum count frequency | $f_{max}$ | A | $Q_A$ | $C_L=15pF$, $R_L=2k\Omega$ | 32 | 42 | — | MHz |
| | | B | $Q_B$ | | 16 | — | — | |
| Propagation delay time | $t_{PLH}$ | A | $Q_A$ | | — | 10 | 16 | ns |
| | $t_{PHL}$ | | | | — | 12 | 18 | |
| | $t_{PLH}$ | A | $Q_D$ | | — | 46 | 70 | ns |
| | $t_{PHL}$ | | | | — | 46 | 70 | |
| | $t_{PLH}$ | B | $Q_B$ | | — | 10 | 16 | ns |
| | $t_{PHL}$ | | | | — | 14 | 21 | |
| | $t_{PLH}$ | B | $Q_C$ | | — | 21 | 32 | ns |
| | $t_{PHL}$ | | | | — | 23 | 35 | |
| | $t_{PLH}$ | B | $Q_D$ | | — | 34 | 51 | ns |
| | $t_{PHL}$ | | | | — | 34 | 51 | |
| | $t_{PHL}$ | Set-to-0 | $Q_A \sim Q_D$ | | — | 26 | 40 | ns |

Home Print

## ■TESTING METHOD

### 1) Test Circuit



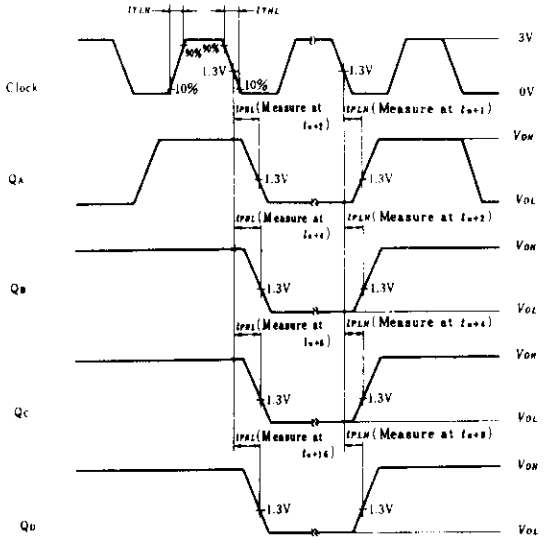

Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

### 2) Testing Table

| Item | From input to output | Inputs A | Inputs B | Inputs $R_0$ | Outputs $Q_A$ | Outputs $Q_B$ | Outputs $Q_C$ | Outputs $Q_D$ |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | A →Q | IN | to $Q_A$ | GND | Out | Out | Out | Out |
| | B →Q | 4.5V | IN | GND | – | Out | Out | Out |
| $t_{PLH}$ $t_{PHL}$ | A →$Q_A$ | IN | to $Q_A$ | GND | Out | – | – | – |
| | A →$Q_D$ | IN | to $Q_A$ | GND | – | – | – | Out |
| | B →$Q_B$ | 4.5V | IN | GND | – | Out | – | – |
| | B →$Q_C$ | 4.5V | IN | GND | – | – | Out | – |
| | B →$Q_D$ | 4.5V | IN | GND | – | – | – | Out |
| | $R_0$*→Q | IN* | to $Q_A$ | IN | Out | Out | Out | Out |

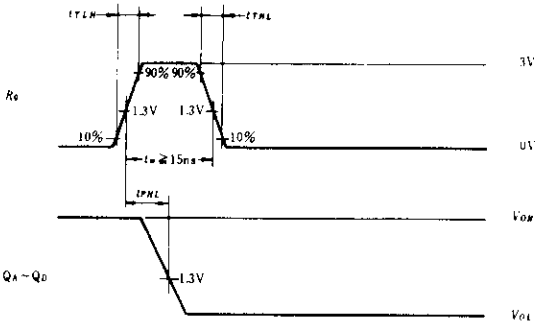
* For initialized.
** Measured with each input and unused inputs at 4.5V.

### Waveform-1 $f_{max}$, $t_{PLH}$, $t_{PHL}$, (Clock→Q)




Notes) 1. Input pulse; $t_{TLH}$≦15ns, $t_{THL}$≦5ns, $PRR$=1MHz, duty cycle=50% and: for $f_{max}$, $t_{TLH}$=$t_{THL}$≦2.5ns.
2. $t_n$ is reference bit time when all outputs are low.

### Waveform-2 $t_{PHL}(R_0 \rightarrow Q)$




Notes) 1. $t_{TLH}$≦15ns, $t_{THL}$≦5ns.



Home Print

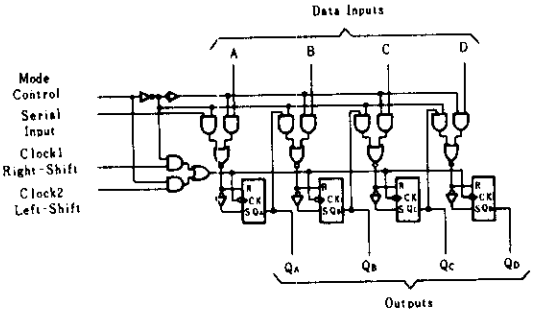
# HD74LS95B ●4-bit Parallel Access Shift Registers

This 4-bit register features parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The register has three mode operation:

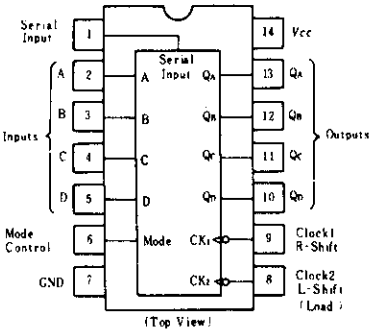
- Parallel (broadside) load
- Shift right (the direction $Q_A$ toward $Q_D$)
- Shift left (the direction $Q_D$ toward $Q_A$)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited. Shift right is accomplished on the high-to-low transition of clock-1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock-2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop ($Q_D$ to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock-1 and clock-2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low: however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




## ■FUNCTION TABLE

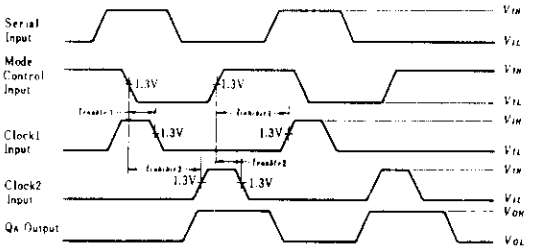
| Inputs | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Mode | Clocks | | Serial | Parallel | | | | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| Control | 2(L) | 1(R) | | A | B | C | D | | | | |
| H | H | × | × | × | × | × | × | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| H | ↓ | × | × | a | b | c | d | a | b | c | d |
| H | ↓ | × | × | $Q_B$† | $Q_C$† | $Q_D$† | d | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | d |
| L | L | H | × | × | × | × | × | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| L | × | ↓ | H | × | × | × | × | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| L | × | ↓ | L | × | × | × | × | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| ↑ | L | L | × | × | × | × | × | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| ↓ | L | L | × | × | × | × | × | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| ↓ | L | H | × | × | × | × | × | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| ↑ | H | L | × | × | × | × | × | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| ↑ | H | H | × | × | × | × | × | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |

Notes) 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. ↓; transition from high to low level
4. a~d; the level of steady-state input at inputs A,B,C, or D, respectively
5. $Q_{A0}$~$Q_{D0}$; the level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the indicated steady-state input conditions were established.
6. $Q_{An}$~$Q_{Dn}$; the level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the most-recent (↑) transition of the clock.
7. †; Shifting left requirs external connection of $Q_B$ to A, $Q_C$ to B, and $Q_D$ to C. Serial data is entered at input D.

Home Print

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Clock frequency | $f_{clock}$ | 0 | — | 25 | MHz |
| Clock pulse width | $t_{w(CK)}$ | 25 | — | — | ns |
| Setup time | $t_{su}$ | 20 | — | — | ns |
| Hold time | $t_h$ | 10 | — | — | ns |
| Enable time 1 | $t_{enable\ 1}$ | 20 | — | — | ns |
| Enable time 2 | $t_{enable\ 2}$ | 20 | — | — | ns |
| Inhibit time 1 | $t_{inhibit\ 1}$ | 20 | — | — | ns |
| Inhibit time 2 | $t_{inhibit\ 2}$ | 20 | — | — | ns |




Clock Enable/Inhibit Times

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, | $I_{OL}=4mA$ | — | — | 0.4 | V |
| | | $V_{IL}=0.8V$ | $I_{OL}=8mA$ | — | — | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}=5.25V$ | | — | 13 | 21 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

**$I_{CC}$ is measured with all outputs and serial input open; A,B,C, and D inputs grounded; mode control at 4.5V; and momentary 3V, then ground, applied both clock inputs.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

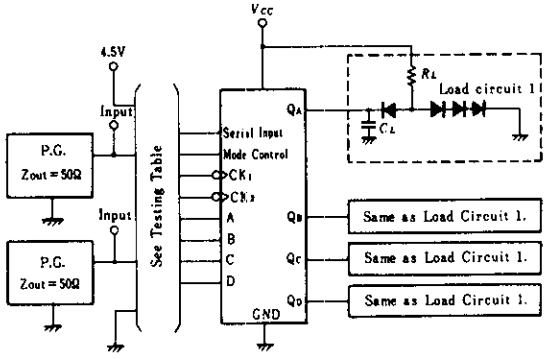
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | $C_L=15pF$, $R_L=2k\Omega$ | 25 | 36 | — | MHz |
| Propagation delay time | $t_{PLH}$ | | — | 18 | 27 | ns |
| | $t_{PHL}$ | | — | 21 | 32 | ns |



Home Print

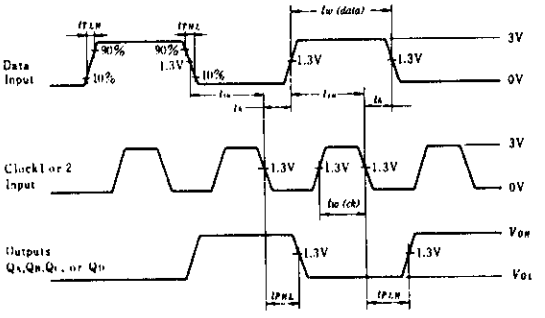
## ■TESTING METHOD

### 1) Test Circuit




Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

### Waveform



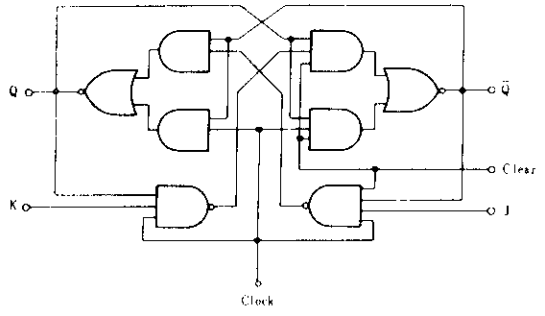

Note) 1. Input pulse: $t_{TLH}$, $t_{THL} \leqq 10$ns,
Data *PRR*=500kHz
Clock *PRR*=1MHz

### 2) Testing Table

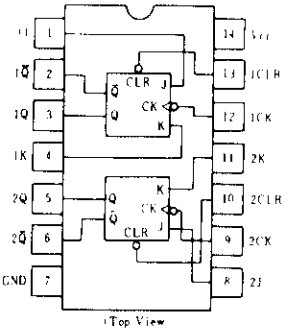
| Item | From input to output | Inputs | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CK-1 | CK-2 | Mode Control | Serial Inputs | A | B | C | D | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| $f_{max}$ | CK-1→Q | IN | 4.5V | 0V | IN | 4.5V | 4.5V | 4.5V | 4.5V | OUT | OUT | OUT | OUT |
| | CK-2→Q | 4.5V | IN | 4.5V | 4.5V | IN | IN | IN | IN | OUT | OUT | OUT | OUT |
| $t_{PLH}$ | CK-1→Q | IN | 4.5V | 0V | IN | 4.5V | 4.5V | 4.5V | 4.5V | OUT | OUT | OUT | OUT |
| $t_{PHL}$ | CK-2→Q | 4.5V | IN | 4.5V | 4.5V | IN | IN | IN | IN | OUT | OUT | OUT | OUT |

# HD74LS107A ● Dual J-K Negative-edge-triggered Flip-Flops (with Clear)

## ■BLOCK DIAGRAM (½)




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | | $f_{clock}$ | 0 | – | 30 | MHz |
| Pulse width | Clock High | $t_w$ | 20 | – | – | ns |
| | Clear Low | | 25 | – | – | ns |
| Setup time | "H" Data | $t_{su}$ | 20↓ | – | – | ns |
| | "L" Data | | 20↓ | – | – | ns |
| Hold time | | $t_h$ | 0↓ | – | – | ns |

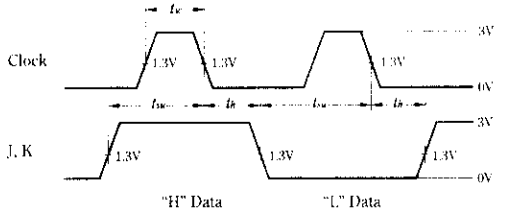
Note) ↓; The arrow indicates the falling edge.

## ■FUNCTION TABLE

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| Clear | Clock | J | K | Q | $\overline{Q}$ |
| L | × | × | × | L | H |
| H | ↓ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | Toggle | |
| H | H | × | × | $Q_0$ | $\overline{Q}_0$ |

Notes) H; high level, L; low level, X; irrelevant
↓; transition from high to low level
$Q_0$; level of Q before the indicated steady-state input conditions were established.
$\overline{Q}_0$; complement of $Q_0$ or level of $\overline{Q}$ before the indicated steady-state input conditions were established.
Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

## ■TIMING DEFINITION






Home Print

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=8mA$ | — | — | 0.5 | V |
| | | | | $I_{OL}=4mA$ | — | — | 0.4 | |
| Input current | J, K | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | μA |
| | Clear | | | | — | — | 60 | |
| | Clock | | | | — | — | 80 | |
| | J, K | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| | Clear | | | | — | — | −0.8 | |
| | Clock | | | | — | — | −0.8 | |
| | J, K | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| | Clear | | | | — | — | 0.3 | |
| | Clock | | | | — | — | 0.4 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current ** | | $I_{CC}$ | $V_{CC}=5.25V$ | | — | 4 | 6 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

** With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

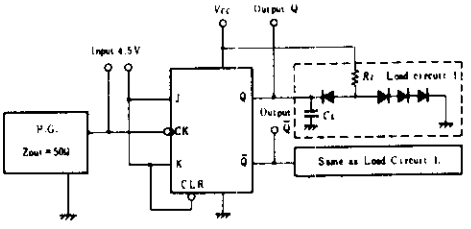
## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | | | $C_L=15pF$, $R_L=2k\Omega$ | 30 | 45 | — | MHz |
| Propagation delay time | $t_{PLH}$ | Clear | Q, $\overline{Q}$ | | — | 15 | 20 | ns |
| | $t_{PHL}$ | Clock | | | — | 15 | 20 | ns |

## ■TESTING METHOD

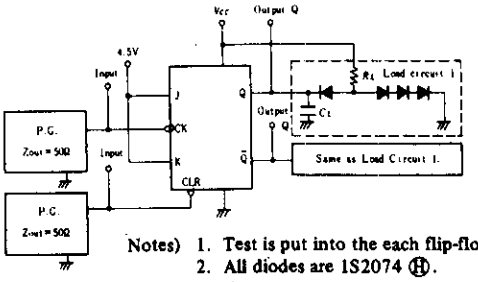
### 1) Test Circuit

#### 1.1) $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Clock→Q, $\overline{Q}$)



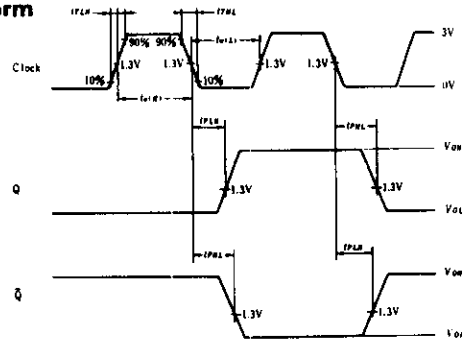

Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

#### 1.2) $t_{PHL}$ (Clear→Q), $t_{PLH}$ (Clear→$\overline{Q}$)

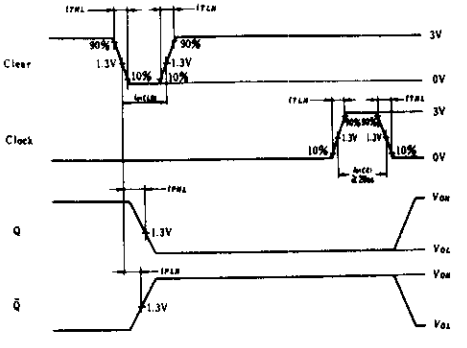



Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

### Waveform




Note) Clock input pulse: $t_{TLH} \leqq 15ns$, $t_{THL} \leqq 6ns$, $PRR=1MHz$, duty cycle=50% and: for $f_{max}$, $t_{TLH}=t_{THL} \leqq 2.5ns$.




Note) Clear and clock input pulse: $t_{TLH} \leqq 15ns$, $t_{THL} \leqq 6ns$, $PRR=1MHz$

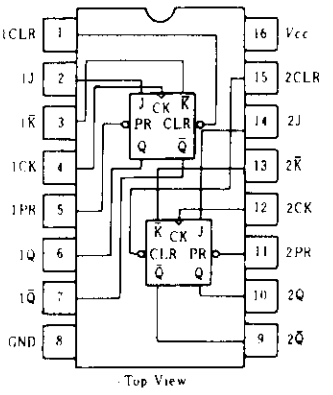
# HD74LS109A ●Dual J-$\bar{K}$ Positive-edge-triggered Flip-Flops (with Preset and Clear)

## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | | $f_{clock}$ | 0 | – | 25 | MHz |
| Pulse width | Clock High | $t_w$ | 25 | – | – | ns |
| | Preset, Clear Low | | 25 | – | – | |
| Setup time | "H" Data | $t_{su}$ | 20↑ | – | – | ns |
| | "L" Data | | 20↑ | – | – | |
| Hold time | | $t_h$ | 5↑ | – | – | ns |

Note) ↑ ; The arrow indicates the rising edge.

## ■PIN ARRANGEMENT



Top View

## ■FUNCTION TABLE

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| Preset | Clear | Clock | J | $\bar{K}$ | Q | $\bar{Q}$ |
| L | H | × | × | × | H | L |
| H | L | × | × | × | L | H |
| L | L | × | × | × | H* | H* |
| H | H | ↑ | L | L | L | H |
| H | H | ↑ | H | L | Toggle | |
| H | H | ↑ | L | H | $Q_0$ | $\bar{Q}_0$ |
| H | H | ↑ | H | H | H | L |
| H | H | L | × | × | $Q_0$ | $\bar{Q}_0$ |

Notes) H; high level, L; low level, X; irrelevant
↑; transition from low to high level
$Q_0$; level of Q before the indicated steady-state conditions were established.
$\bar{Q}_0$; complement of $Q_0$ or level of $\bar{Q}$ before the indicated steady-state input conditions were established.
*; This configuration is nonstable, that is, it will not persist where preset and clear inputs return to their inactive (high) level.

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=8mA$ | – | – | 0.5 | V |
| | | | | $I_{OL}=4mA$ | – | – | 0.4 | |
| Input current | J, $\bar{K}$, CK | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | CLR, PR | | | | – | – | 40 | |
| | J, $\bar{K}$, CK | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | -0.4 | mA |
| | CLR, PR | | | | – | – | -0.8 | |
| | J, $\bar{K}$, CK | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| | CLR, PR | | | | – | – | 0.2 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | -20 | – | -100 | mA |
| Supply current ** | | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 4 | 8 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | -1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C
** With all outputs open, $I_{CC}$ is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.



Home Print

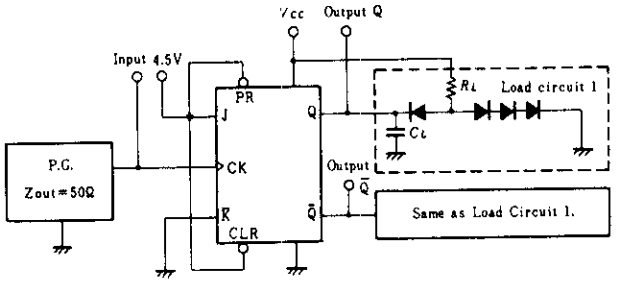
## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | | | $C_L$=15pF, $R_L$=2kΩ | 25 | 33 | – | MHz |
| Propagation delay time | $t_{PLH}$ | Clear Preset Clock | Q, $\overline{Q}$ | | – | 13 | 25 | ns |
| | $t_{PHL}$ | | | | – | 25 | 40 | ns |

## ■TESTING METHOD

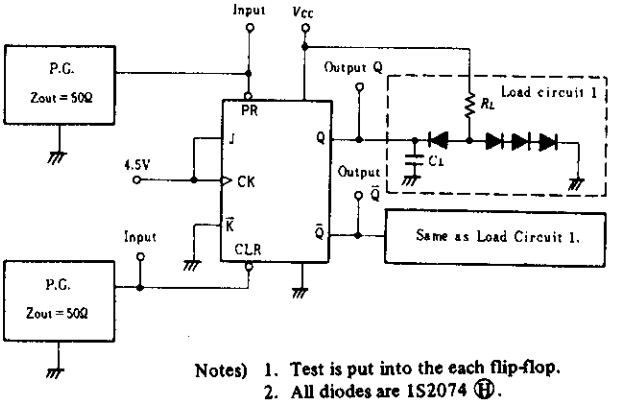
### 1) Test Circuit

**1.1) $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Clock→Q,$\overline{Q}$)**



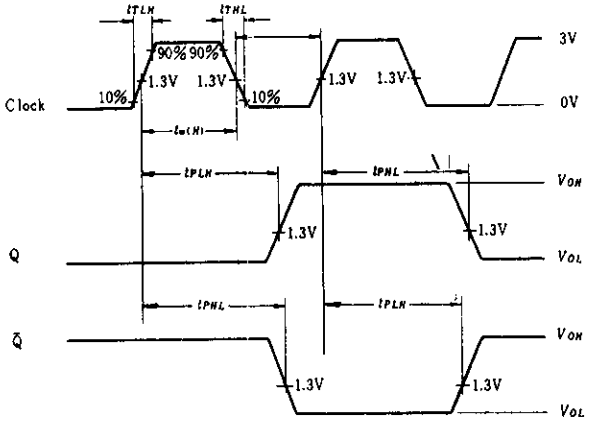

Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

**1.2) $t_{PHL}$, $t_{PLH}$ (Clear, Preset→Q,$\overline{Q}$)**

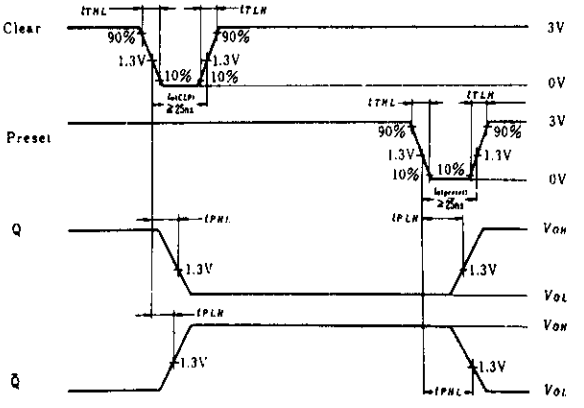



Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

### Waveform




Note) Clock input pulse: $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz, duty cycle=50% and: for $f_{max}$, $t_{TLH}$=$t_{THL}$≦2.5ns.

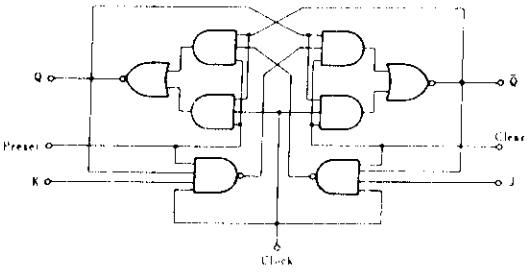



Note) Clear and preset input pulse: $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz.

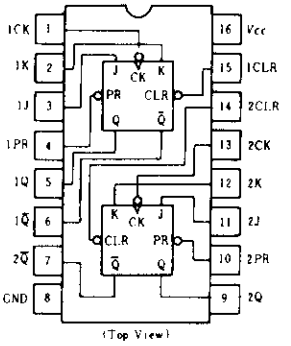
Home Print

# HD74LS112 ● Dual J-K Negative-edge-triggered Flip-Flops (with Preset and Clear)

## ■BLOCK DIAGRAM(½)




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | | $f_{clock}$ | 0 | – | 30 | MHz |
| Pulse width | Clock High | $t_w$ | 20 | – | | ns |
| | Clear, Preset Low | | 25 | – | | |
| Setup time | "H" Data | $t_{su}$ | 20↓ | – | | ns |
| | "L" Data | | 20↓ | – | | |
| Hold time | | $t_h$ | 0↓ | – | | ns |

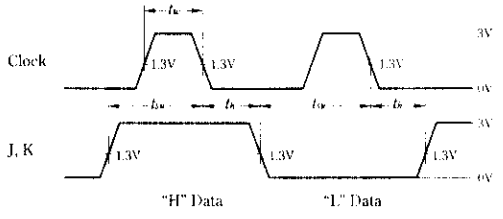
Note) ↓; The arrow indicates the falling edge.

## ■FUNCTION TABLE

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| Preset | Clear | Clock | J | K | Q | Q̄ |
| L | H | × | × | × | H | L |
| H | L | × | × | × | L | H |
| L | L | × | × | × | H* | H* |
| H | H | ↓ | L | L | $Q_0$ | $\bar{Q}_0$ |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | Toggle | |
| H | H | H | × | × | $Q_0$ | $\bar{Q}_0$ |

Notes) H; high level, L; low level, X; irrelevant
↓; transition from high to low level
$Q_0$; level of Q before the indicated steady-state input conditions were established.
$\bar{Q}_0$; complement of $Q_0$ or level of Q̄ before the indicated steady-state input conditions were established.
Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.
*; This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

## ■TIMING DEFINITION






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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=8mA$ | — | — | 0.5 | V |
| | | | | $I_{OL}=4mA$ | — | — | 0.4 | |
| Input current | J, K | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | $\mu A$ |
| | Clear | | | | — | — | 60 | |
| | Preset | | | | — | — | 60 | |
| | Clock | | | | — | — | 80 | |
| | J, K | $I_{IL}$** | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| | Clear | | | | — | — | −0.8 | |
| | Preset | | | | — | — | −0.8 | |
| | Clock | | | | — | — | −0.8 | |
| | J, K | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| | Clear | | | | — | — | 0.3 | |
| | Preset | | | | — | — | 0.3 | |
| | Clock | | | | — | — | 0.4 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current *** | | $I_{CC}$ | $V_{CC}=5.25V$ | | — | 4 | 8 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC} = 5V$, $Ta = 25°C$
** $I_{IL}$ should not be measured when preset and clear inputs are low at same time.
*** With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn.
At the time of measurement, the clock input is grounded.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

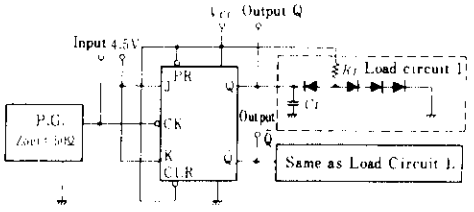
| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | | | $C_L=15pF$, $R_L=2k\Omega$ | 30 | 45 | — | MHz |
| Propagation delay time | $t_{PLH}$ | Clear Preset Clock | Q, $\overline{Q}$ | | — | 11 | 20 | ns |
| | $t_{PHL}$ | | | | — | 15 | 30 | ns |

Home Print

## ■TESTING METHOD

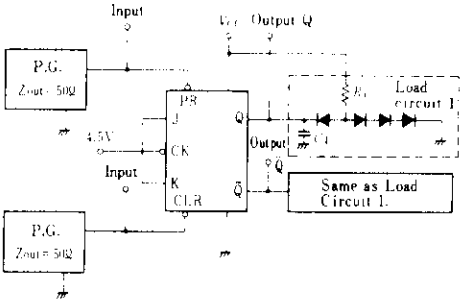
### 1) Test Circuit

#### 1.1) $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Clock→Q,$\overline{Q}$)



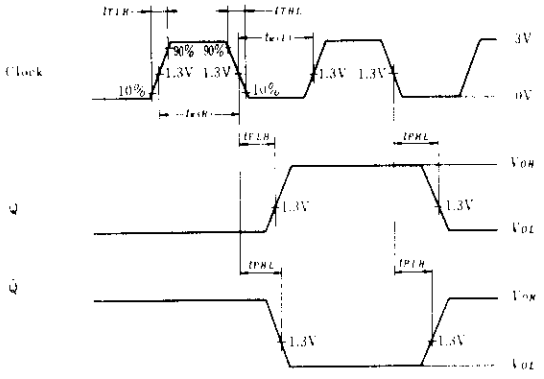

Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

#### 1.2) $t_{PHL}$, $t_{PLH}$ (Clear, Preset→Q,$\overline{Q}$)

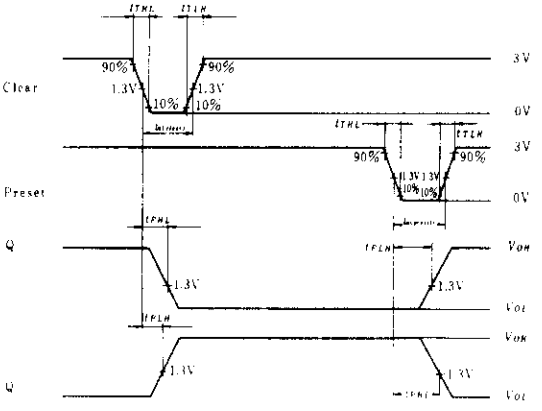



Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

### Waveform




Note) Clock input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz, duty cycle=50% and: for $f_{max}$, $t_{TLH}$=$t_{THL} \leqq 2.5$ns.



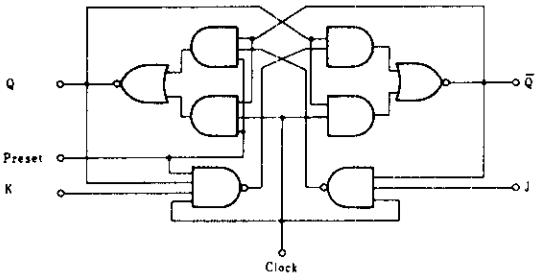

Note) Clear and preset input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz



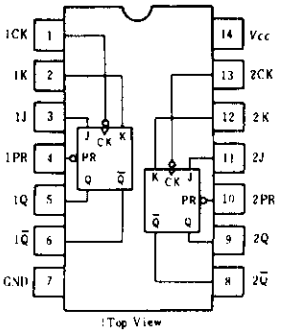
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# HD74LS113 ● Dual J-K Negative-edge-triggered Flip-Flops (with Preset)

## ■BLOCK DIAGRAM(½)




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | | $f_{clock}$ | 0 | – | 30 | MHz |
| Pulse width | CK | $t_w$ | 20 | – | – | ns |
| | PR | | 25 | – | – | |
| Setup time | "H"level | $t_{su}$ | 20↓ | – | – | ns |
| | "L"level | | 20↓ | – | – | |
| Hold time | | $t_h$ | 0↓ | – | – | ns |

Note) ↓; The arrow indicates the falling edge.

## ■FUNCTION TABLE

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| Preset | Clock | J | K | Q | Q̄ |
| L | × | × | × | H | L |
| H | ↓ | L | L | $Q_0$ | $\bar{Q}_0$ |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | Toggle | |
| H | H | × | × | $Q_0$ | $\bar{Q}_0$ |

Notes) H; high level, L; low level, X; irrelevant
↓; transition from high to low level
$Q_0$; level of Q before the indicated steady-state input conditions were established.
$\bar{Q}_0$; complement of $Q_0$ or level of Q̄ before the indicated steady-state input conditions were established.
Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75℃$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$, $V_{IH}=2V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | J, K | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | Preset | | | | – | – | 60 | |
| | Clock | | | | – | – | 80 | |
| | J, K | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | Preset | | | | – | – | −0.8 | |
| | Clock | | | | – | – | −0.8 | |
| | J, K | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| | Preset | | | | – | – | 0.3 | |
| | Clock | | | | – | – | 0.4 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current ** | | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 4 | 8 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$
** With all outputs open, $I_{CC}$ is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

Home Print

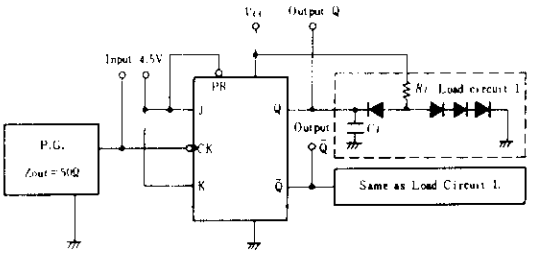
## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | | | $C_L$=15pF, $R_L$=2kΩ | 30 | 45 | -- | MHz |
| Propagation delay time | $t_{PLH}$ | Preset Clock | Q, $\bar{Q}$ | | -- | 11 | 20 | ns |
| | $t_{PHL}$ | | | | -- | 15 | 30 | ns |

## ■TESTING METHOD

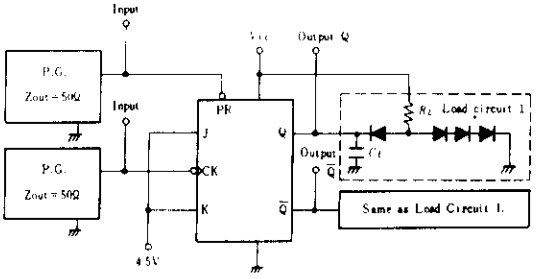
### 1.1) Test Circuit

**1.1) $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Clock→Q,$\bar{Q}$)**



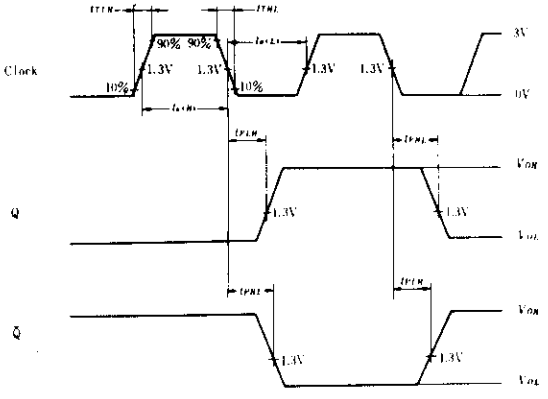

Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

**1.2) $t_{PHL}$ (Preset→$\bar{Q}$), $t_{PLH}$ (Preset→Q)**

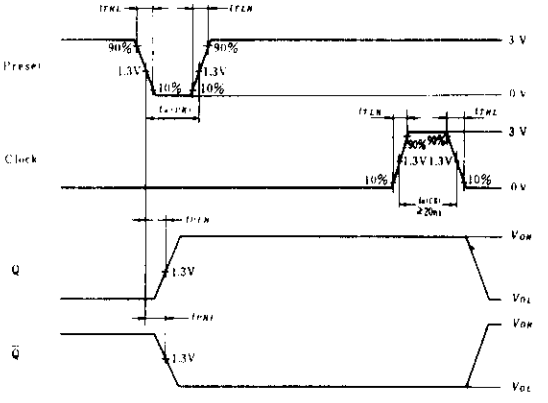



Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

### Waveform




Note) Clock input pulse; $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz, duty cycle=50% and: for $f_{max}$, $t_{TLH}$=$t_{THL}$≦2.5ns.



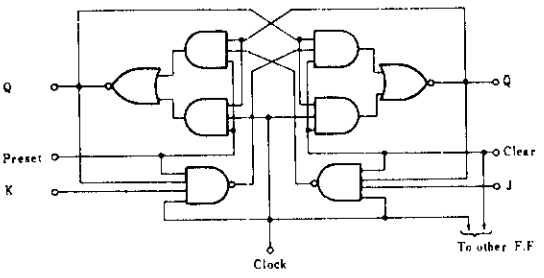

Note) Preset and clock input pulse: $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz



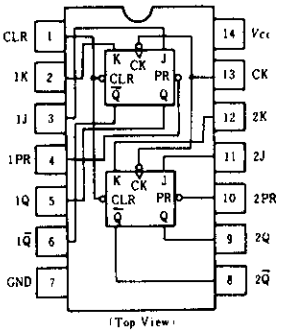
Home Print

# HD74LS114 ●Dual J-K Negative-edge-triggered Flip-Flops (with Preset, Common Clear and Common Clock)

## ■BLOCK DIAGRAM (½)




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | | $f_{clock}$ | 0 | — | 30 | MHz |
| Pulse width | Clock High | $t_w$ | 20 | — | — | ns |
| | Preset, Clear Low | | 25 | — | — | ns |
| Setup time | "H" Data | $t_{su}$ | 20↓ | — | — | ns |
| | "L" Data | | 20↓ | — | — | ns |
| Hold time | | $t_h$ | 0↓ | — | — | ns |

Note) ↓; The arrow indicates the falling edge.

## ■FUNCTION TABLE

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| Preset | Clear | Clock | J | K | Q | $\bar{Q}$ |
| L | H | × | × | × | H | L |
| H | L | × | × | × | L | H |
| L | L | × | × | × | H* | H* |
| H | H | ↓ | L | L | $Q_0$ | $\bar{Q}_0$ |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | Toggle | |
| H | H | H | × | × | $Q_0$ | $\bar{Q}_0$ |

Notes) H; high level, L; low level, X; irrelevant
↓; transition from high to low level
$Q_0$; level of Q before the indicated steady-state input conditions were established.
$\bar{Q}_0$; complement of $Q_0$ or level of $\bar{Q}$ before the indicated steady-state input conditions were established.
Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.
*; This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IL}=0.8V$, $V_{IH}=2V$ | $I_{OL}=8mA$ | — | — | 0.5 | V |
| | | | | $I_{OL}=4mA$ | — | — | 0.4 | |
| Input current | J, K | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | $\mu A$ |
| | Clear | | | | — | — | 120 | |
| | Preset | | | | — | — | 60 | |
| | Clock | | | | — | — | 160 | |
| | J, K | $I_{IL}$** | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| | Clear | | | | — | — | −1.6 | |
| | Preset | | | | — | — | −0.8 | |
| | Clock | | | | — | — | −1.6 | |
| | J, K | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| | Clear | | | | — | — | 0.6 | |
| | Preset | | | | — | — | 0.3 | |
| | Clock | | | | — | — | 0.8 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current *** | | $I_{CC}$ | $V_{CC}=5.25V$ | | — | 4 | 8 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$
** $I_{IL}$ should not be measured when preset and clear inputs are low at same time.
*** With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ output high in turn. At the time of measurement, the clock input is grounded.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | | | $C_L=15pF$, $R_L=2k\Omega$ | 30 | 45 | — | MHz |
| Propagation delay time | $t_{PLH}$ | Clear Preset Clock | Q, $\overline{Q}$ | | — | 11 | 20 | ns |
| | $t_{PHL}$ | | | | — | 15 | 30 | ns |

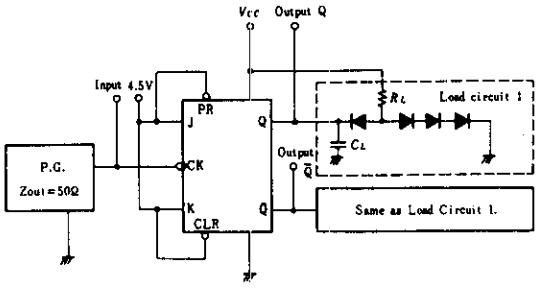


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## ■ TESTING METHOD

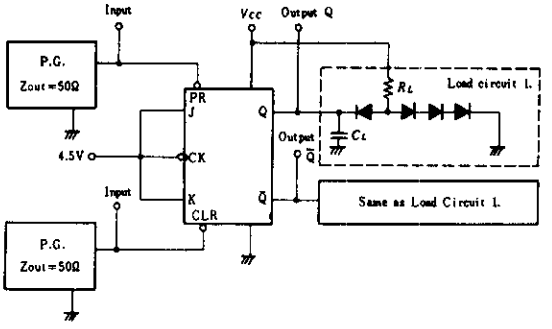
### 1) Test Circuit

#### 1.1) $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Clock→Q,$\bar{Q}$)



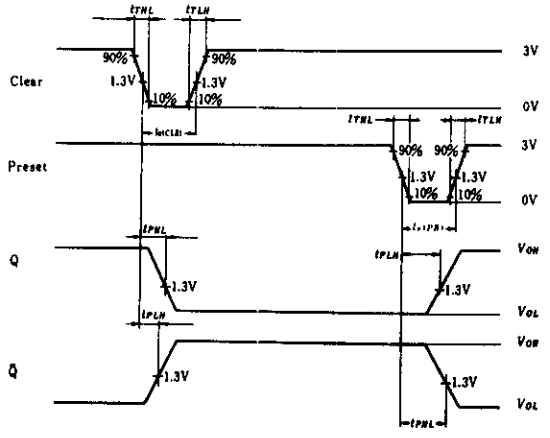

Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

#### 1.2) $t_{PHL}$, $t_{PLH}$ (Clear,Preset→Q,$\bar{Q}$)



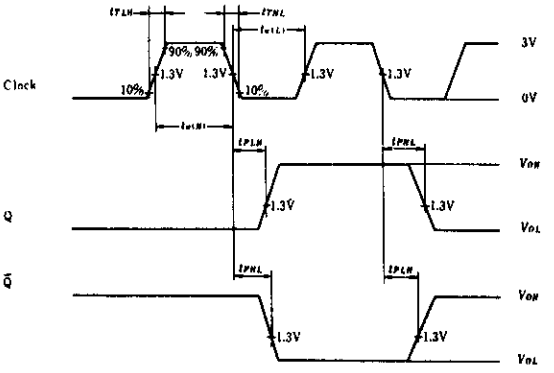

Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

### Waveform




Note) Clock input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz, duty cycle=50% and: for $f_{max}$, $t_{TLH}$=$t_{THL} \leqq 2.5$ns.

### Waveform




Note) Clear and preset input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz

# HD74LS122 ●Retriggerable Monostable Multivibrators (with Clear)

This d-c triggered multivibrator features output pulse width control by three method. The basic pulse time is programmed by selection of external resistance and capacitance values. The HD74LS122 has internal timing resistor that allows the circuit to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs or be reduced by use of the overriding clear. Fig. 1 illustrates pulse control by retriggering and early clear. This device is provided enough Schmitt hysteresis to ensure jitter-free tirggering from the B input with transition rates as slow as 0.1 mV/ns.

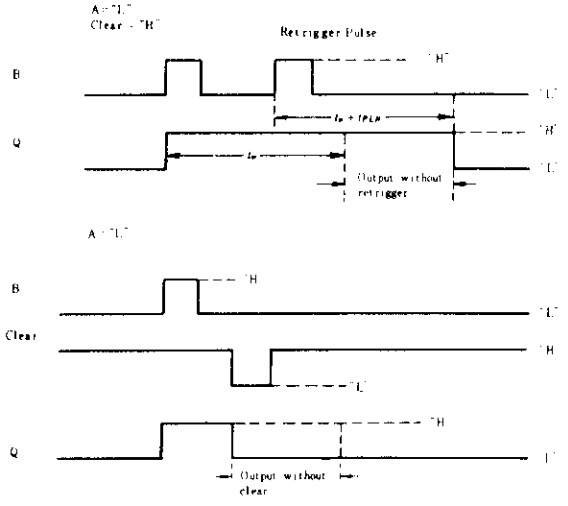
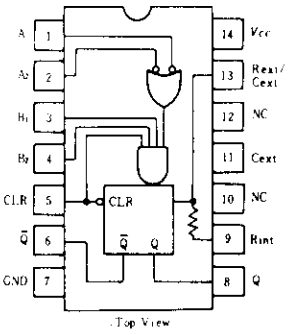
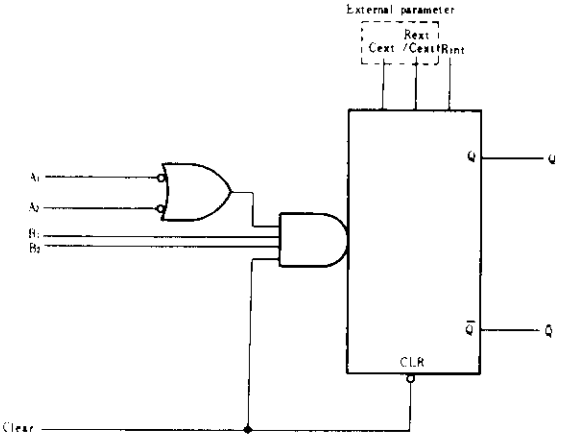



**Fig.1 Typical Input/Output Pulses**

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Input pulse width | $t_w$ | 40 | — | — | ns |
| External timing resistance | $R_{ext}$ | 5 | — | 260 | kΩ |
| External capacitance | $C_{ext}$ | Non restriction | | | |
| Wiring capacitance at Rext/Cext terminal | $R_{ext}$/ $C_{ext}$ | — | — | 50 | pF |

## ■FUNCTION TABLE

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| Clear | $A_1$ | $A_2$ | $B_1$ | $B_2$ | Q | Q̄ |
| L | × | × | × | × | L | H |
| × | H | H | × | × | L | H |
| × | × | × | L | × | L | H |
| × | × | × | × | L | L | H |
| H | L | × | ↑ | H | ⎍ | ⎍ |
| H | L | × | H | ↑ | ⎍ | ⎍ |
| H | × | L | ↑ | H | ⎍ | ⎍ |
| H | × | L | H | ↑ | ⎍ | ⎍ |
| H | H | ↓ | H | H | ⎍ | ⎍ |
| H | ↓ | ↓ | H | H | ⎍ | ⎍ |
| H | ↓ | H | H | H | ⎍ | ⎍ |
| ↑ | L | × | H | H | ⎍ | ⎍ |
| ↑ | × | L | H | H | ⎍ | ⎍ |

H; high level, L; low level, X; irrelevant.
↑; transition from low to high level.
↓; one high-level pulse.
⎍; one low-level pulse.



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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | $V_{IL}=0.8V$ | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current ** | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 6 | 11 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

** With all outputs open and 4.5V applied to all data and clear inputs, $I_{CC}$ is measured after a momentary ground, then 4.5V, is applied to clock.

Note) To measure $V_{OH}$ at Q, $V_{OL}$ at $\bar{Q}$, or $I_{OS}$ at Q, ground $R_{ext}/C_{ext}$, apply 2V to B and clear, and pulse A from 2V to 0V.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A | Q | $C_{ext}=0$ $R_{ext}=5k\Omega$ $C_L=15pF$ $R_L=2k\Omega$ | – | 23 | 33 | ns |
| | $t_{PHL}$ | | $\bar{Q}$ | | – | 32 | 45 | |
| | $t_{PLH}$ | B | Q | | – | 23 | 44 | |
| | $t_{PHL}$ | | $\bar{Q}$ | | – | 34 | 56 | |
| | $t_{PHL}$ | Clear | Q | | – | 20 | 27 | |
| | $t_{PLH}$ | | $\bar{Q}$ | | – | 28 | 45 | |
| Output pulse width | $t_{w(out)min}$ | A or B | Q | | – | 116 | 200 | |
| | $t_{w(out)}$ | A or B | Q | $C_{ext}=1000pF$, $R_{ext}=10k\Omega$ $C_L=15pF$, $R_L=2k\Omega$ | 4 | 4.5 | 5 | $\mu s$ |

## ■TYPICAL APPLICATION DATA FOR HD74LS122

For pulse widths when $Cext \leqq 1000pF$, See Fig. 3.
The output pulse is primarily a function of the external capacitor and resistor. For $Cext > 1000pF$, the output pulse width ($tw$) is defined as : $tw(out) = K \cdot Rext \cdot Cext$ ; See Fig. 4

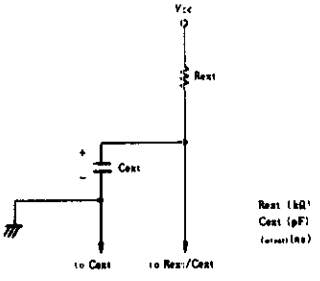



Fig.2 Timing Component Connections

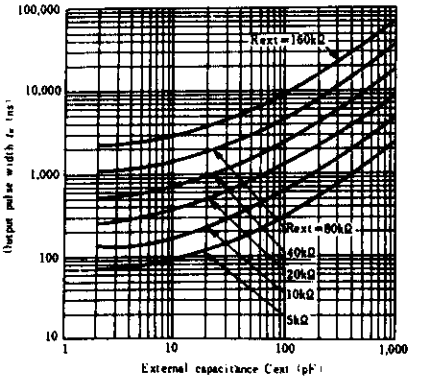
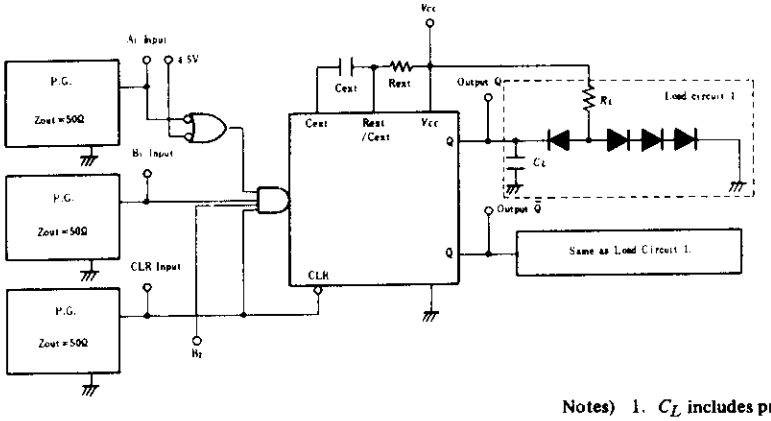



Fig.3 Typical Output Pulse Width ($Cext \leqq 1000pF$)

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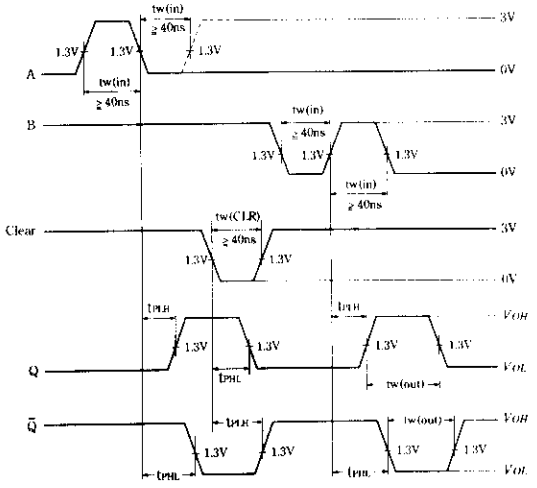
## ■TESTING METHOD

### 1) Test Circuit




Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.
3. Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns.

### Waveform



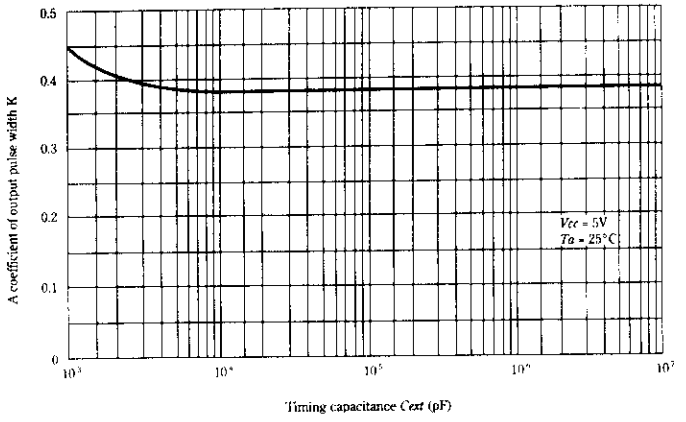




**Fig.4 Cext vs K (Cext > 1000pF)**



Home Print

# HD74LS123 ● Dual Retriggerable Monostable Multivibrators (with Clear)

This d-c triggered multivibrator features output pulse width control by three method. The basic pulse time is programmed by selection of external resistance and capacitance values. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Fig. 1 illustrates pulse control by retriggering and early clear. This device is provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 mV/ns.

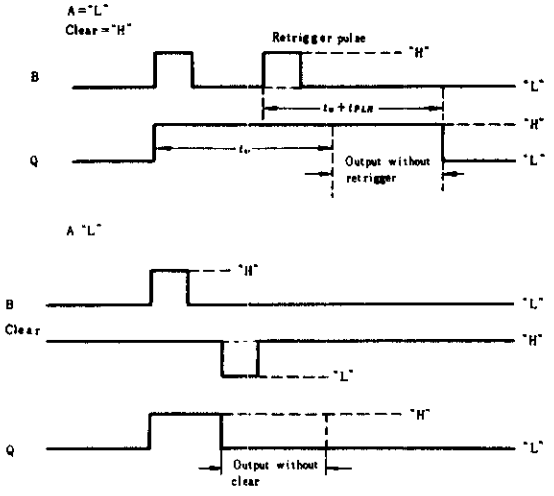
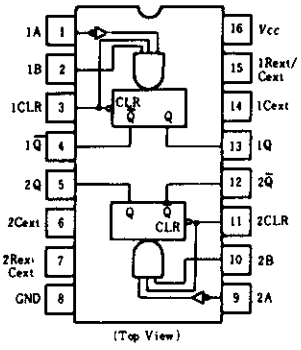
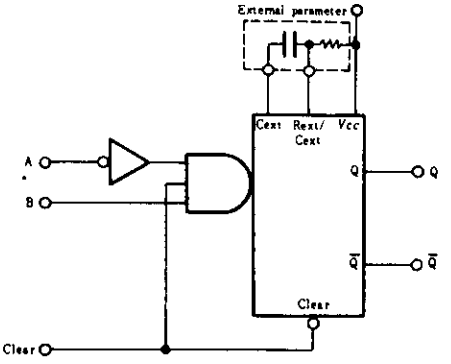



**Fig.1 Typical Input/Output Pulses**

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM(½)




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| Input pulse width | A, B | "H" | $t_{w(in)}$ | 40 | — | — | ns |
| | | "L" | | 40 | — | — | ns |
| | CLR | "L" | | 40 | — | — | ns |
| External timing resistance | | | $R_{ext}$ | 5 | — | 260 | kΩ |
| External capacitance | | | $C_{ext}$ | Non restriction | | | |
| Wiring capacitance at Rext/Cext terminal | | | | — | — | 50 | pF |

## ■FUNCTION TABLE

| Inputs | | | Outputs | |
|---|---|---|---|---|
| CLEAR | A | B | Q | $\bar{Q}$ |
| L | × | × | L | H |
| × | H | × | L | H |
| × | × | L | L | H |
| H | L | ↑ | ⎍ | ⎎ |
| H | ↓ | H | ⎍ | ⎎ |
| ↑ | L | H | ⎍ | ⎎ |

Notes) H; high level, L; low level, X; irrelevant
↓; transition from high to low level
↑; transition from low to high level
⎍; one high-level pulse
⎎; one low-level pulse

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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 12 | 20 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** With all outputs open and 4.5V applied to all data and clear inputs, $I_{CC}$ is measured after a momentary ground, then 4.5V, is applied clock.

Note) To measure $V_{OH}$ at Q, $V_{OL}$ at $\overline{Q}$, or $I_{OS}$ at Q, ground $R_{ext}/C_{ext}$, apply 2V to B and clear, and pulse A from 2V to 0V.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A | Q | $C_{ext}=0pF$, $R_{ext}=5k\Omega$, $C_L=15pF$, $R_L=2k\Omega$ | – | 23 | 33 | ns |
| | $t_{PHL}$ | | $\overline{Q}$ | | – | 32 | 45 | |
| | $t_{PLH}$ | B | Q | | – | 23 | 44 | |
| | $t_{PHL}$ | | $\overline{Q}$ | | – | 34 | 56 | |
| | $t_{PHL}$ | CLR | Q | | – | 20 | 27 | |
| | $t_{PLH}$ | | $\overline{Q}$ | | – | 28 | 45 | |
| Output pulse width | $t_{w(out)min}$ | A, B | Q | $C_{ext}=1,000pF$, $R_{ext}=10k\Omega$, $C_L=15pF$, $R_L=2k\Omega$ | – | 116 | 200 | ns |
| | $t_{w(out)}$ | | | | 4 | 4.5 | 5 | $\mu s$ |

## ■TYPICAL APPLICATION DATA FOR HD74LS123

For pulse widths when $Cext$<1000pF, See Fig. 3.
The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext}$>1000pF, the output pulse width ($tw$) is defined as : $tw(out) = K \cdot Rext \cdot Cext$ ; See Fig. 4

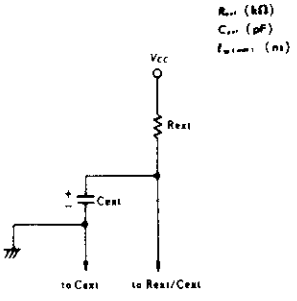



Fig.2 Timing Component Connections

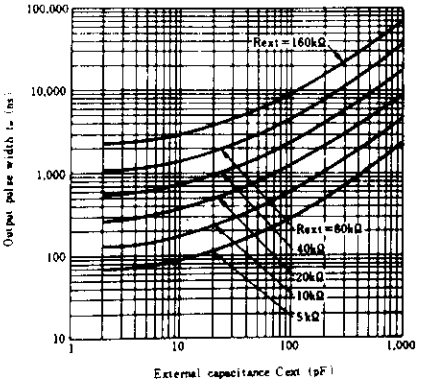



Fig.3 Typical Output Pulse Width (Cext≦1000pF)



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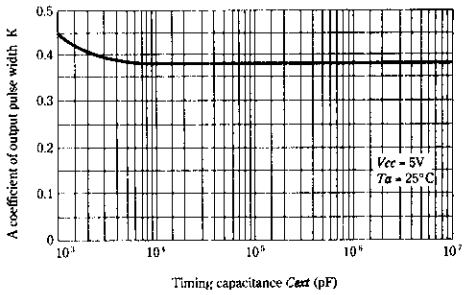
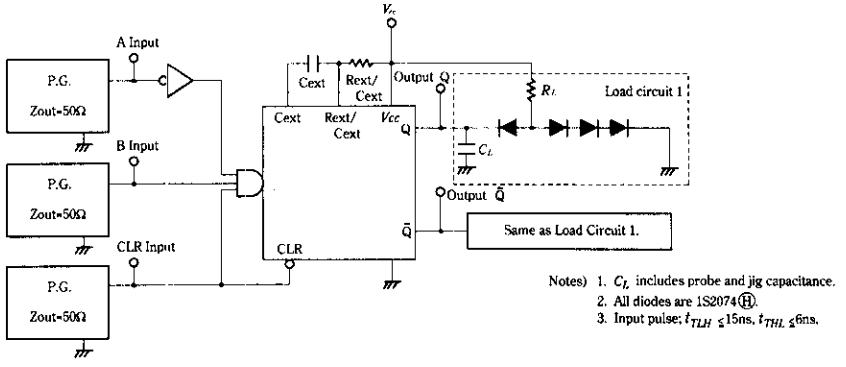



**Fig.4 Cext vs K (Cext > 1000pF)**

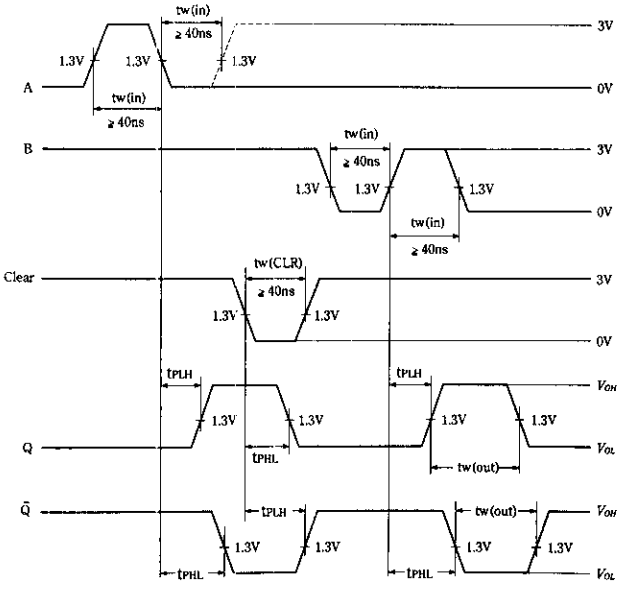
## ■TESTING METHOD

### 1) Test Circuit



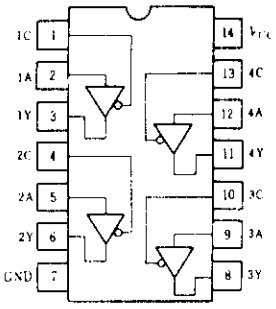

Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074Ⓗ.
3. Input pulse: $t_{TLH} \leq 15$ns, $t_{THL} \leq 6$ns.

### Waveform



# HD74LS125A ●Quadruple Bus Buffer Gates (with three-state outputs)

## ■PIN ARRANGEMENT




(Top View)

## ■FUNCTION TABLE

| Inputs | | Outputs |
|---|---|---|
| C | A | Y |
| H | X | Z |
| L | L | L |
| L | H | H |

Note) H; high level,
L; low level,
X; irrelevant
Z; off (high-impedance) state of a 3-state output

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output current | $I_{OH}$ | – | – | −2.6 | mA |
| Low level output current | $I_{OL}$ | – | – | 24 | mA |

## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20~+75℃)

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−2.6mA | | 2.4 | – | – | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=24mA | – | – | 0.5 | V |
| | | | $I_{OL}$=12mA | – | – | 0.4 | |
| Off-state output current | $I_{OZ}$ | $V_{CC}$=5.25V, $V_{IH}$=2V, $V_{IL}$=0.8V | $V_O$=2.4V | – | – | 20 | μA |
| | | | $V_O$=0.4V | – | – | −20 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −40 | – | −225 | mA |
| Supply current | $I_{CC}$ | $V_{CC}$=5.25V | | – | 11 | 20 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25℃)

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$=45pF, $R_L$=667Ω | – | 9 | 15 | ns |
| | $t_{PHL}$ | | – | 7 | 18 | |
| Output enable time | $t_{ZH}$ | | – | 12 | 20 | |
| | $t_{ZL}$ | | – | 15 | 25 | |
| Output disable time | $t_{HZ}$ | $C_L$=5pF, $R_L$=667Ω | – | – | 20 | |
| | $t_{LZ}$ | | – | – | 20 | |

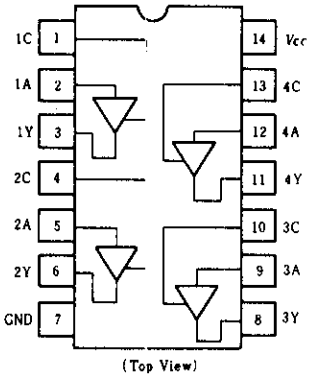
Note) Refer to Test Circuit and Waveform of the Common Item



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# HD74LS126A ●Quadruple Bus Buffer Gates (with three-state outputs)

## ■PIN ARRANGEMENT



(Top View)

## ■FUNCTION TABLE

| Inputs | | Outputs |
|---|---|---|
| C | A | Y |
| L | X | Z |
| H | H | H |
| H | L | L |

Note) H; high level,
L; low level,
X; irrelevant
Z; off (high-impedance) state of a 3-state output

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output current | $I_{OH}$ | – | – | −2.6 | mA |
| Low level output current | $I_{OL}$ | – | – | 24 | mA |

## ■ELECTRICAL CHARACTERISTICS ( $Ta$ = −20 ~ +75°C )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−2.6mA | | 2.4 | – | – | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=24mA | – | – | 0.5 | |
| | | | $I_{OL}$=12mA | – | – | 0.4 | |
| Off-state output current | $I_{OZH}$ | $V_{CC}$=5.25V, $V_{IH}$=2V, $V_{IL}$=0.8V | $V_O$=2.4V | – | – | 20 | μA |
| | $I_{OZL}$ | | $V_O$=0.4V | – | – | −20 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_{IH}$=2.7V | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | A input | – | – | −0.4 | mA |
| | | | C input | – | – | −0.4 | |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −40 | – | −225 | mA |
| Supply current | $I_{CC}$** | $V_{CC}$=5.25V | | – | 12 | 22 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C
** $I_{CC}$ is measured with the A and C input grounded.

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## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25°C )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$=45pF<br>$R_L$=667Ω | – | 9 | 15 | ns |
| | $t_{PHL}$ | | – | 8 | 18 | |
| Output enable time | $t_{ZH}$ | | – | 16 | 25 | ns |
| | $t_{ZL}$ | | – | 21 | 35 | |
| Output disable time | $t_{HZ}$ | $C_L$=5pF<br>$R_L$=667Ω | – | – | 25 | ns |
| | $t_{LZ}$ | | – | – | 25 | |

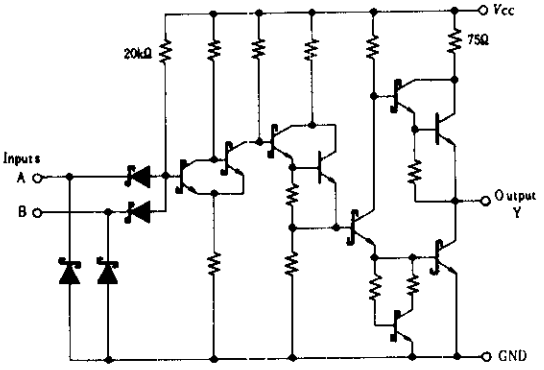
Note) Refer to Test Circuit and Waveform of the Common Item.



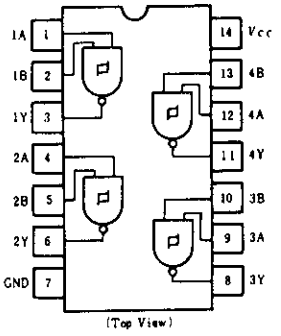
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# HD74LS132 ●Quadruple 2-input Positive NAND Schmitt-triggers

## ■CIRCUIT SCHEMATIC(¼)




## ■PIN ARRANGEMENT




## ■ELECTRICAL CHARACTERISTICS ( $Ta$=−20～+75℃ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input threshold voltage | $V_{T^+}$ | $V_{CC}$=5V | | 1.4 | 1.6 | 1.9 | V |
| | $V_{T^-}$ | $V_{CC}$=5V | | 0.5 | 0.7 | 1.0 | V |
| Hysteresis | $V_{T^+}$-$V_{T^-}$ | $V_{CC}$=5V | | 0.4 | 0.9 | – | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $I_{OH}$=−400μA, $V_I$=0.5V | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_I$=1.9V | $I_{OL}$=8mA | – | – | 0.5 | V |
| | | | $I_{OL}$=4mA | – | – | 0.4 | |
| Input threshold current | $I_{T^+}$ | $V_{CC}$=5V, $V_I$=$V_{T^+}$ | | – | −0.14 | – | mA |
| | $I_{T^-}$ | $V_{CC}$=5V, $V_I$=$V_{T^-}$ | | – | −0.18 | – | mA |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | – | −100 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}$=5.25V | | – | 5.9 | 11 | mA |
| | $I_{CCL}$ | $V_{CC}$=5.25V | | – | 8.2 | 14 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | V |

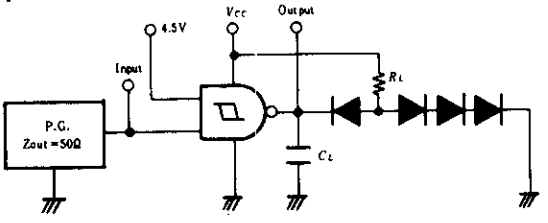
* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

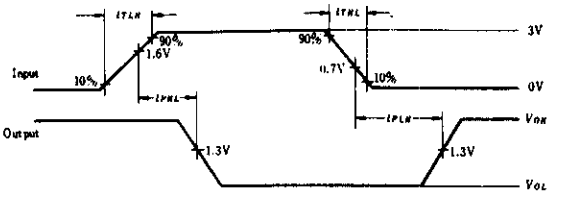
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$=15pF, $R_L$=2kΩ | – | 15 | 22 | ns |
| | $t_{PHL}$ | | – | 15 | 22 | ns |

## ■TESTING METHOD

### 1) Test Circuit




### Waveform




Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.
3. Input pulse: $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz, duty cycle 50%.

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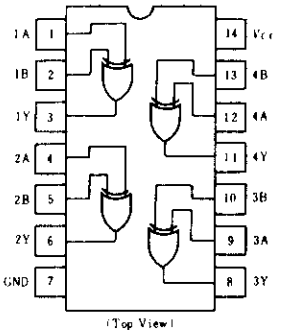
# HD74LS136 ●Quadruple 2-input Exclusive-OR Gates (with open collector outputs)

## ■FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

H; high level, L; low level, X; irrelevant.

## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output voltage | $V_{OH}$ | — | — | 5.5 | V |
| Low level output current | $I_{OL}$ | — | — | 8 | mA |

## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output current | $I_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$ | | — | — | 100 | μA |
| Output voltage | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | — | — | 0.4 | V |
| | | | $I_{OL}=8mA$ | — | — | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 40 | μA |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.8 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.2 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}=5.25V$ | | — | 6.1 | 10 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

** $I_{CC}$ is measured with one input of each gate at 4.5V, the other inputs grounded, and the outputs open.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Test Conditions | | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A or B | Other inputs "L" | $C_L=15pF$, $R_L=2k\Omega$ | — | 18 | 30 | ns |
| | $t_{PHL}$ | | | | — | 18 | 30 | |
| | $t_{PLH}$ | A or B | Other inputs "H" | | — | 18 | 30 | ns |
| | $t_{PHL}$ | | | | — | 18 | 30 | |

Note) Refer to Test Circuit and Waveform of the Common Item

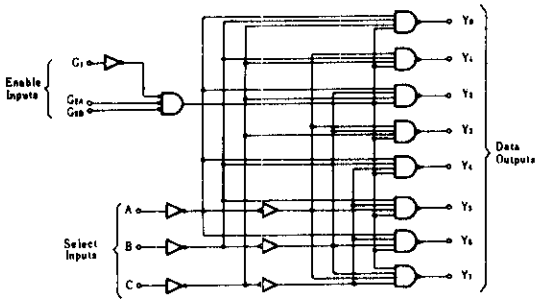


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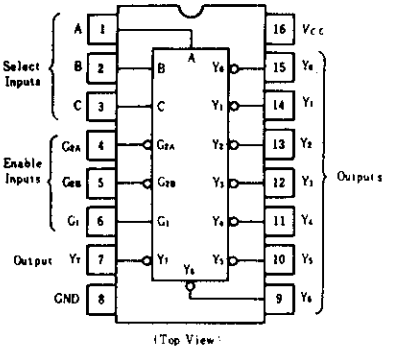
# HD74LS138 ●3-Line-to-8-Line Decoders/Demultiplexers

The HD74LS138 decodes one-of-eight line dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




## ■FUNCTION TABLE

| Inputs | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Enable | | Select | | | | | | | | | | |
| G1 | G2* | C | B | A | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ |
| × | H | × | × | × | H | H | H | H | H | H | H | H |
| L | × | × | × | × | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

H; high level, L; low level, X; irrelevant
*; $G_2 = G_{2A} + G_{2B}$

## ■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

| Item | Symbol | Test Conditions | min | typ* | max | Unit |
|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | 2.0 | – | – | V |
| | $V_{IL}$ | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OL}$=4mA | – | – | 0.4 | V |
| | | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OL}$=8mA | – | – | 0.5 | V |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | −20 | – | −100 | mA |
| Supply current | $I_{CC}$ | $V_{CC}$=5.25V, Outputs enabled and open | – | 6.3 | 10 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

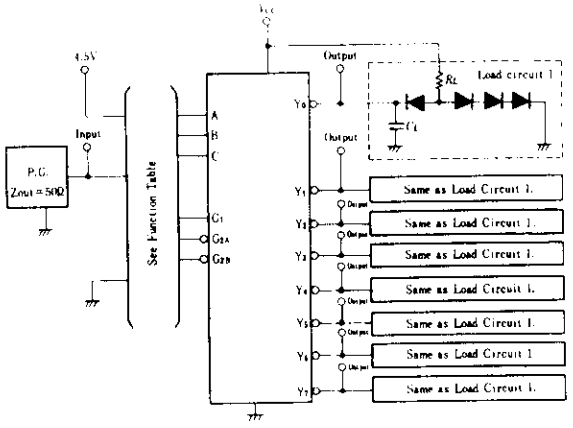
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## ■SWITCHING CHARACTERISTICS ( $Vcc=5V$, $Ta=25℃$ )

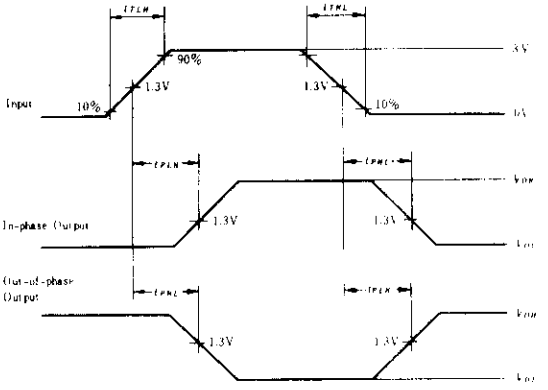
| Item | Symbol | Inputs | Output | Levels of delay | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | Binary Select A, B, C | Y | 2 | $C_L=15pF$ $R_L=2k\Omega$ | – | 13 | 20 | ns |
| | $t_{PHL}$ | | | | | – | 27 | 41 | ns |
| | $t_{PLH}$ | | | 3 | | – | 18 | 27 | ns |
| | $t_{PHL}$ | | | | | – | 26 | 39 | ns |
| | $t_{PLH}$ | Enable $G_{2A}$, $G_{2B}$ | Y | 2 | | – | 12 | 18 | ns |
| | $t_{PHL}$ | | | | | – | 21 | 32 | ns |
| | $t_{PLH}$ | Enable $G_1$ | | 3 | | – | 17 | 26 | ns |
| | $t_{PHL}$ | | | | | – | 25 | 38 | ns |

## ■TESTING METHOD

### 1) Test Circuit




### Waveform




Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.
3. Input pulse: $t_{TLH}\leqq 15ns$, $t_{THL}\leqq 6ns$, $PRR=1MHz$, duty cycle 50%.

## ■RELATION BETWEEN INPUT AND OUTPUT TO LEVELS OF DELAY

| Inputs | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 2 levels of delay | | | | 3 levels of delay | | | |
| A | $Y_0$ | $Y_2$ | $Y_4$ | $Y_6$ | $Y_1$ | $Y_3$ | $Y_5$ | $Y_7$ |
| B | $Y_0$ | $Y_1$ | $Y_4$ | $Y_5$ | $Y_2$ | $Y_3$ | $Y_6$ | $Y_7$ |
| C | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ |
| $G_1$ | | | | | $Y_0\sim Y_7$ | | | |
| $G_{2A}$, $G_{2B}$ | $Y_0\sim Y_7$ | | | | | | | |

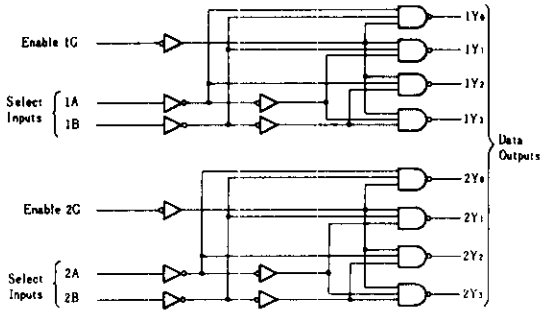


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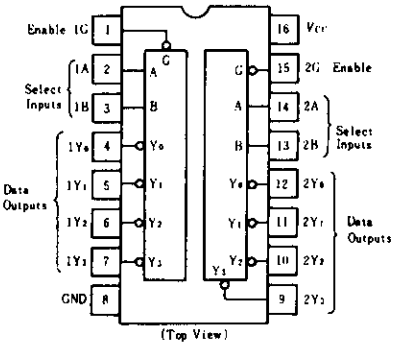
# HD74LS139 ●Dual 2-line-to-4-line Decoders/Demultiplexers

The HD74LS139 comprises two individual two-line-to-four-line decoder in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




## ■FUNCTION TABLE

| Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|
| Enable | Select | | | | | |
| G | B | A | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ |
| H | × | × | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

H; high level, L; low level, X; irrelevant

## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75°C$ )

| Item | Symbol | Test Conditions | min | typ* | max | Unit |
|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | 2.0 | – | – | V |
| | $V_{IL}$ | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | – | – | 0.1 | mA |
| | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | – | – | −0.4 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | −5 | – | −42 | mA |
| Supply current | $I_{CC}$ | $V_{CC}=5.25V$, Outputs enabled and open | – | 6.8 | 11 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

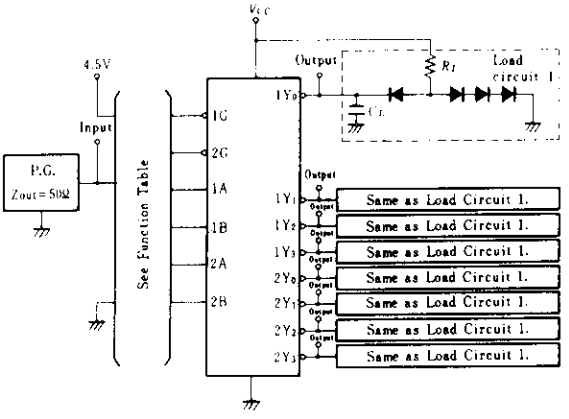
## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Outputs | Levels of delay | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | Binary Select 1A, 1B | $1Y_0\sim1Y_3$ $2Y_0\sim2Y_3$ | 2 | $C_L=15pF$ $R_L=2k\Omega$ | – | 13 | 20 | ns |
| | $t_{PHL}$ | | | | | – | 22 | 33 | ns |
| | $t_{PLH}$ | | | 3 | | – | 18 | 29 | ns |
| | $t_{PHL}$ | 2A, 2B | | | | – | 25 | 38 | ns |
| | $t_{PLH}$ | Enable 1G, 2G | $1Y_0\sim1Y_3$ $2Y_0\sim2Y_3$ | 2 | | – | 16 | 24 | ns |
| | $t_{PHL}$ | | | | | – | 21 | 32 | ns |

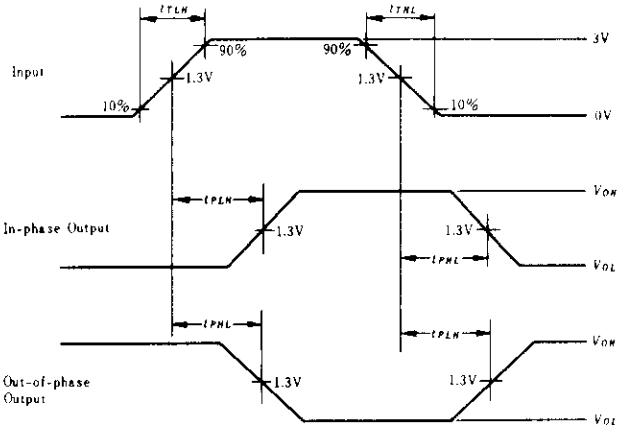
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## ■TESTING METHOD

### 1) Test Circuit




### Waveform




Notes) 1. Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz, duty cycle=50%
2. $C_L$ includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ.

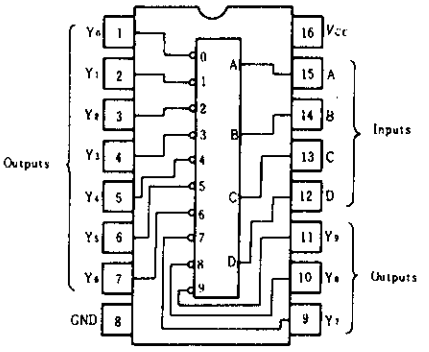


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# HD74LS145 ●BCD-to-Decimal Decoders/Drivers (with 15V outputs)

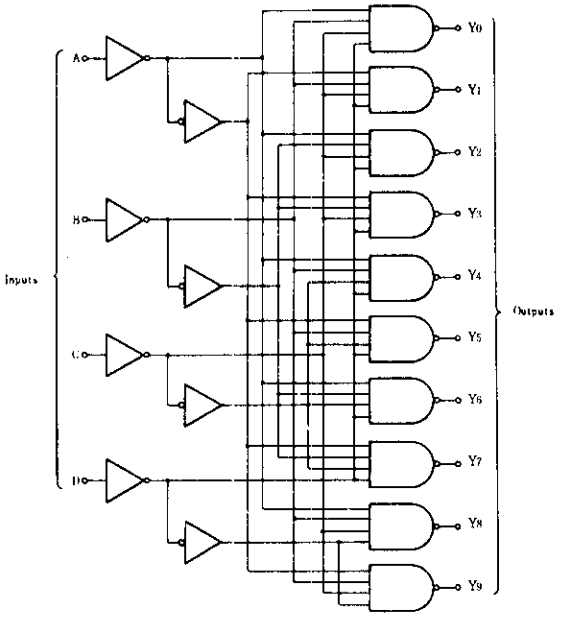
This BCD-to-decimal decoder/driver consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. This decoder features high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers.

## ■PIN ARRANGEMENT




(Top View)

## ■BLOCK DIAGRAM




## ■FUNCTION TABLE

| No. | Inputs | | | | Outputs | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | L | L | L | L | L | H | H | H | H | H | H | H | H | H |
| 1 | L | L | L | H | H | L | H | H | H | H | H | H | H | H |
| 2 | L | L | H | L | H | H | L | H | H | H | H | H | H | H |
| 3 | L | L | H | H | H | H | H | L | H | H | H | H | H | H |
| 4 | L | H | L | L | H | H | H | H | L | H | H | H | H | H |
| 5 | L | H | L | H | H | H | H | H | H | L | H | H | H | H |
| 6 | L | H | H | L | H | H | H | H | H | H | L | H | H | H |
| 7 | L | H | H | H | H | H | H | H | H | H | H | L | H | H |
| 8 | H | L | L | L | H | H | H | H | H | H | H | H | L | H |
| 9 | H | L | L | H | H | H | H | H | H | H | H | H | H | L |
| INVALID | H | L | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

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## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Off-state output voltage | $V_{O(off)}$ | – | – | 15 | V |
| Low level output current | $I_{OL}$ | – | – | 80 | mA |

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Off-state output current | $I_{O(off)}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $V_{O(off)}=15V$ | | – | – | 250 | μA |
| On-state output voltage | $V_{O(on)}$ | $V_{CC}=4.75V$, $V_{IL}=2V$, $V_{IL}=0.8V$ | $I_{OL}=12mA$ | – | – | 0.4 | V |
| | | | $I_{OL}=24mA$ | – | – | 0.5 | |
| | | | $I_{OL}=80mA$ | – | – | 3.0 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | | 20 | μA |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Supply current ** | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 7 | 13 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

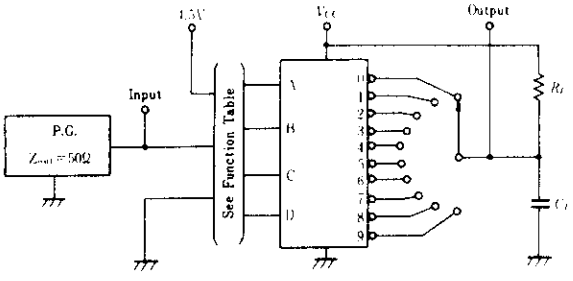
** $I_{CC}$ is measured with all outputs open and all inputs grounded.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

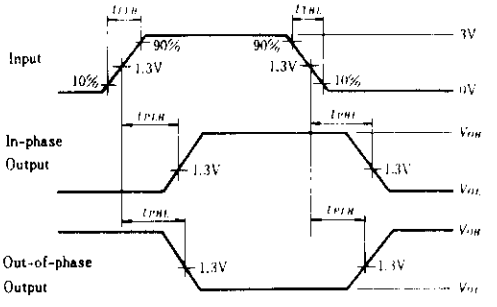
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=45pF$, $R_L=665\Omega$ | – | – | 50 | ns |
| | $t_{PHL}$ | | | – | 50 | |

## ■TESTING METHOD

### 1) Test Circuit




### Waveform




Notes) 1. Input pulse; $t_{TLH} \leqq 15ns$, $t_{THL} \leqq 6ns$, $PRR=1MHz$, duty cycle=50%

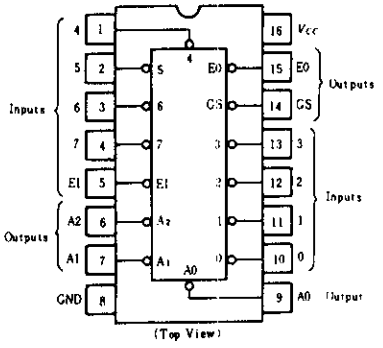


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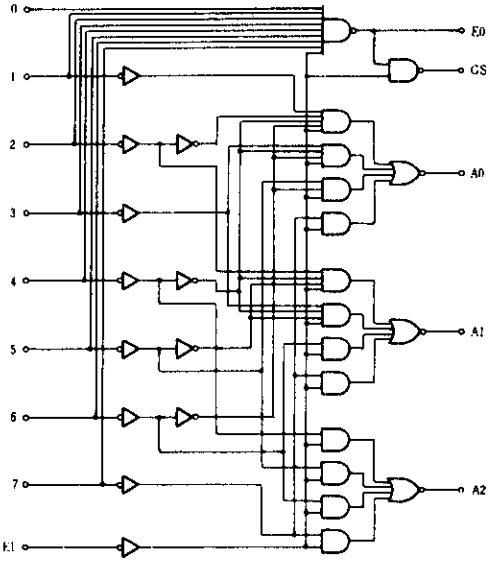
# HD74LS148 ●8-line-to-3-line Octal Priority Encoders

The HD74LS148 encodes eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. The data inputs and outputs are active at the low logic level.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■FUNCTION TABLE

| Inputs | | | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EI | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | A2 | A1 | A0 | GS | EO |
| H | × | × | × | × | × | × | × | × | H | H | H | H | H |
| L | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | × | × | × | × | × | × | × | L | L | L | L | L | H |
| L | × | × | × | × | × | × | L | H | L | L | H | L | H |
| L | × | × | × | × | × | L | H | H | L | H | L | L | H |
| L | × | × | × | × | L | H | H | H | L | H | H | L | H |
| L | × | × | × | L | H | H | H | H | H | L | L | L | H |
| L | × | × | L | H | H | H | H | H | H | L | H | L | H |
| L | × | L | H | H | H | H | H | H | H | H | L | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | L | H |

H; high level, L; low level, X; irrelevant

## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | | 2.7 | – | – | V |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | – | – | 0.4 | V |
| | | | | $I_{OL}$=8mA | – | – | 0.5 | |
| Input current | 1～7 Inputs | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | – | – | 40 | μA |
| | Other inputs | | | | – | – | 20 | |
| | 1～7 Inputs | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | – | – | −0.8 | mA |
| | Other inputs | | | | – | – | −0.4 | |
| | 1～7 Inputs | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.2 | mA |
| | Other inputs | | | | – | – | 0.1 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | – | −100 | mA |
| Supply current ** | | $I_{CC}$ | $V_{CC}$=5.25V | Condition 1 | – | 12 | 20 | mA |
| | | | | Condition 2 | – | 10 | 17 | |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** The condition 1 is measured with inputs 7 and EI grounded, other inputs and outputs open, the condition 2 is measured with all inputs and outputs open.

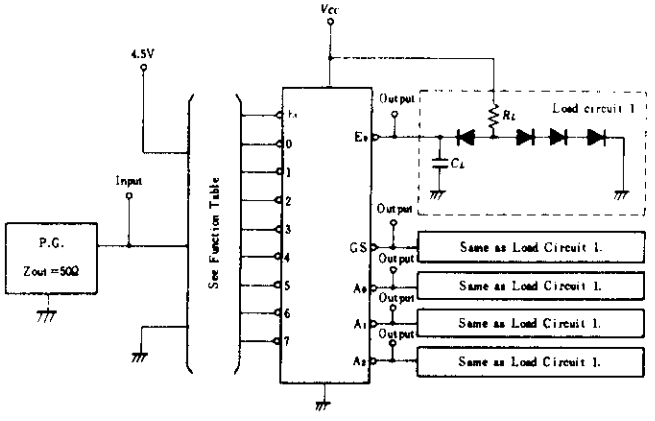
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## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

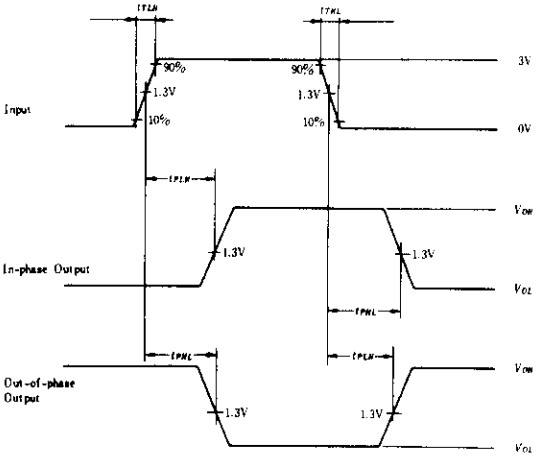
| Item | Symbol | Inputs | Outputs | Output Waveforms | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | 0~7 | $A_0$, $A_1$ or $A_2$ | In-phase Output | $C_L$=15pF, $R_L$=2kΩ | – | 14 | 18 | ns |
| | $t_{PHL}$ | | | | | – | 15 | 25 | |
| | $t_{PLH}$ | 0~7 | $A_0$, $A_1$ or $A_2$ | Out-of-phase Output | | – | 20 | 36 | ns |
| | $t_{PHL}$ | | | | | – | 16 | 29 | |
| | $t_{PLH}$ | 0~7 | EO | Out-of-phase Output | | – | 7 | 18 | ns |
| | $t_{PHL}$ | | | | | – | 25 | 40 | |
| | $t_{PLH}$ | 0~7 | GS | In-phase Output | | – | 35 | 55 | ns |
| | $t_{PHL}$ | | | | | – | 9 | 21 | |
| | $t_{PLH}$ | EI | $A_0$, $A_1$ or $A_2$ | In-phase Output | | – | 16 | 25 | ns |
| | $t_{PHL}$ | | | | | – | 12 | 25 | |
| | $t_{PLH}$ | EI | GS | In-phase Output | | – | 12 | 17 | ns |
| | $t_{PHL}$ | | | | | – | 14 | 36 | |
| | $t_{PLH}$ | EI | EO | In-phase Output | | – | 12 | 21 | ns |
| | $t_{PHL}$ | | | | | – | 23 | 35 | |

## ■TESTING METHOD

### 1) Test Circuit




### Waveform




Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

Input pulse; $t_{TLH}$≦15ns, $t_{THL}$≦6ns,
$PRR$=1MHz, duty cycle 50%.

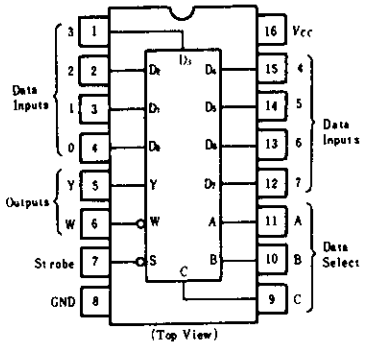


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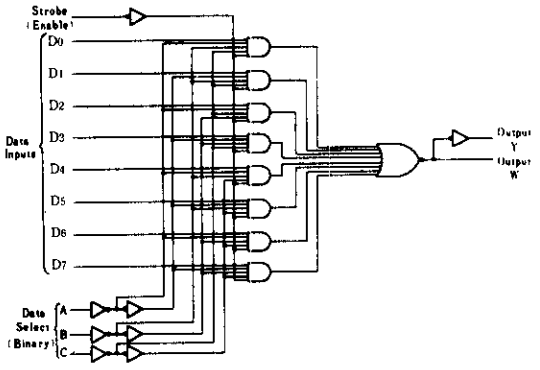
# HD74LS151 ●1-of-8 Data Selectors/Multiplexers (with strobe)

This data selector/multiplexer contains full-on chip binary decoding to select the desired data source. The HD74LS151 selects one-of-eight data sources and has a strobe input which must be at a low logic level to enable this device. A high level at the strobe forces the W output high, and the Y output low.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■FUNCTION TABLE

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| SELECT | | | STROBE | Y | W |
| C | B | A | S | | |
| × | × | × | H | L | H |
| L | L | L | L | $D_0$ | $\overline{D_0}$ |
| L | L | H | L | $D_1$ | $\overline{D_1}$ |
| L | H | L | L | $D_2$ | $\overline{D_2}$ |
| L | H | H | L | $D_3$ | $\overline{D_3}$ |
| H | L | L | L | $D_4$ | $\overline{D_4}$ |
| H | L | H | L | $D_5$ | $\overline{D_5}$ |
| H | H | L | L | $D_6$ | $\overline{D_6}$ |
| H | H | H | L | $D_7$ | $\overline{D_7}$ |

H; high level, L; low level, X; irrelevant

## ■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | – | – | 0.4 | V |
| | | | $I_{OL}$=8mA | – | – | 0.5 | |
| Input current | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.1 | mA |
| | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | – | – | −0.4 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | – | −100 | mA |
| Supply current ** | $I_{CC}$ | $V_{CC}$=5.25V | | – | 6.0 | 10.0 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** $I_{CC}$ is measured with all outputs open and all inputs at 4.5V.

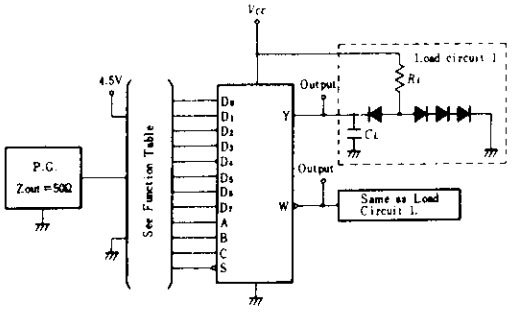
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## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

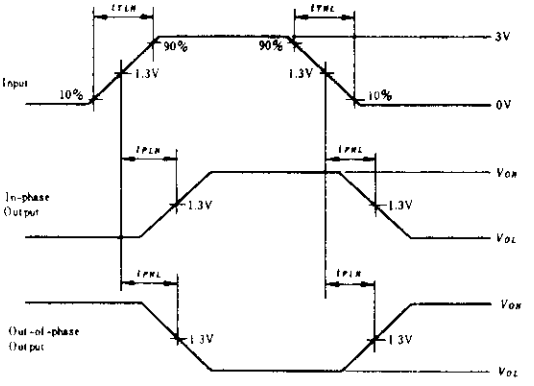
| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A, B, C (4 Level) | Y | $C_L$=15pF, $R_L$=2kΩ | – | 27 | 43 | ns |
| | $t_{PHL}$ | | | | – | 18 | 30 | |
| | $t_{PLH}$ | A, B, C (3 Level) | W | | – | 14 | 23 | |
| | $t_{PHL}$ | | | | – | 20 | 32 | |
| | $t_{PLH}$ | Strobe | Y | | – | 26 | 42 | |
| | $t_{PHL}$ | | | | – | 20 | 32 | |
| | $t_{PLH}$ | Strobe | W | | – | 15 | 24 | |
| | $t_{PHL}$ | | | | – | 18 | 30 | |
| | $t_{PLH}$ | D | Y | | – | 20 | 32 | |
| | $t_{PHL}$ | | | | – | 16 | 26 | |
| | $t_{PLH}$ | D | W | | – | 13 | 21 | |
| | $t_{PHL}$ | | | | – | 12 | 20 | |

## ■TESTING METHOD

### 1) Test Circuit




### Waveform




Notes) 1. Input pulse; $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz, duty cycle=50%
2. $C_L$ includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ.

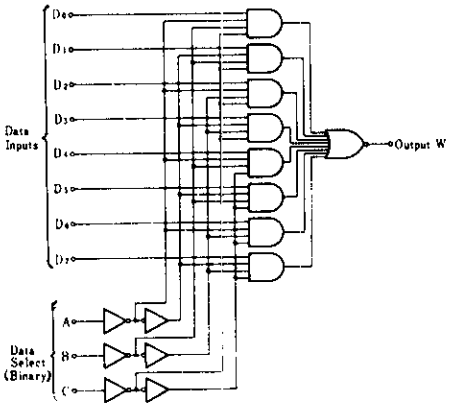


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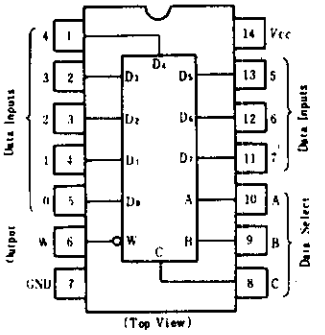
# HD74LS152 ● 1-of-8 Data Selectors/Multiplexers

This data selector/multiplexer contains full-on-chip binary decoding to select the desired data source. The HD74LS152 selects one-of-eight data sources.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




## ■FUNCTION TABLE

| Select inputs | | | Output | Select inputs | | | Output |
|---|---|---|---|---|---|---|---|
| C | B | A | W | C | B | A | W |
| L | L | L | $\overline{D_0}$ | H | L | L | $\overline{D_4}$ |
| L | L | H | $\overline{D_1}$ | H | L | H | $\overline{D_5}$ |
| L | H | L | $\overline{D_2}$ | H | H | L | $\overline{D_6}$ |
| L | H | H | $\overline{D_3}$ | H | H | H | $\overline{D_7}$ |

Notes) $D_0 \sim D_7$ ; the level of the D respecitve input
H; high level
L; low level

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $I_{OH}=-400\mu A$, $V_{IH}=2V$, $V_{IL}=0.8V$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 6.0 | 10 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$
** $I_{CC}$ is measured with all outputs open and all inputs at 4.5V.

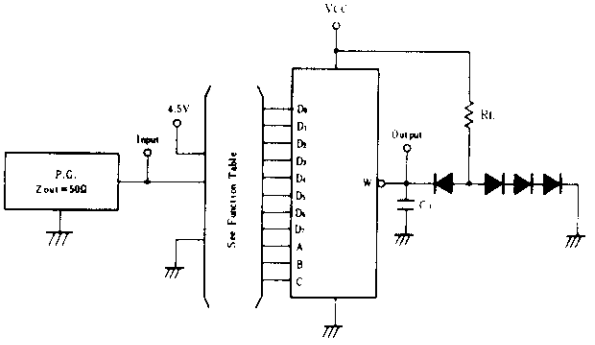
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## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

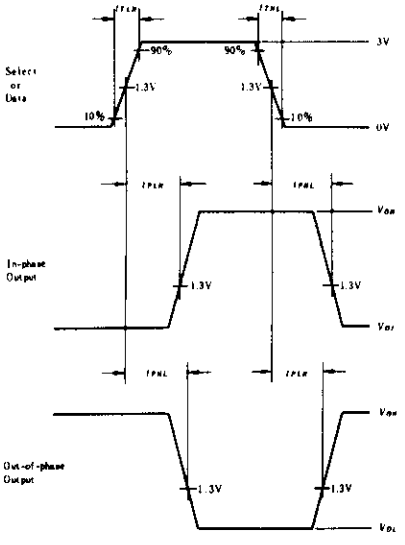
| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A, B, C | W | $C_L$=15pF, $R_L$=2kΩ | — | 14 | 23 | ns |
| | $t_{PHL}$ | | | | — | 20 | 32 | |
| | $t_{PLH}$ | Data | W | | — | 13 | 21 | |
| | $t_{PHL}$ | | | | — | 12 | 20 | |

## ■TESTING METHOD

### 1) Test Circuit




### Waveform




Notes) 1. Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz, duty cycle=50%
2. $C_L$ includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ.

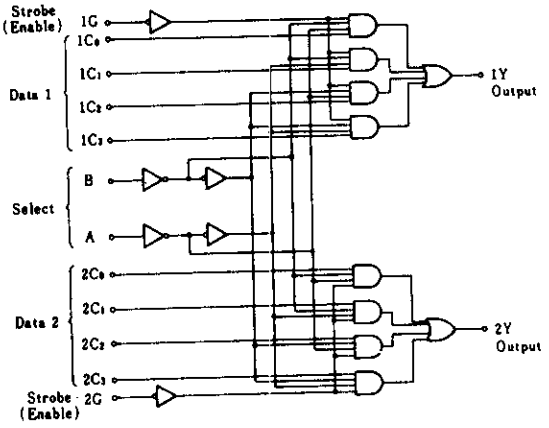


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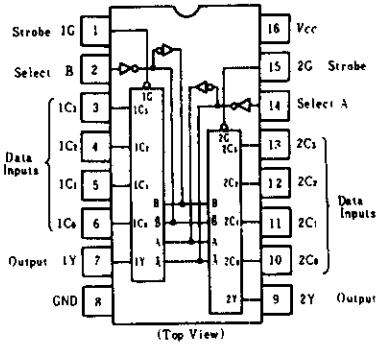
# HD74LS153 ●Dual 4-Line to 1-Line Data Selectors/Multiplexers

This data selector/multiplexer contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-INVERT gates. Separate strobe inputs are provided for each of the two four-line sections.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




## ■FUNCTION TABLE

| Inputs | | | | | | | Outputs |
|---|---|---|---|---|---|---|---|
| Select | | Data | | | | Strobe | |
| B | A | $C_0$ | $C_1$ | $C_2$ | $C_3$ | G | Y |
| × | × | × | × | × | × | H | L |
| L | L | L | × | × | × | L | L |
| L | L | H | × | × | × | L | H |
| L | H | × | L | × | × | L | L |
| L | H | × | H | × | × | L | H |
| H | L | × | × | L | × | L | L |
| H | L | × | × | H | × | L | H |
| H | H | × | × | × | L | L | L |
| H | H | × | × | × | H | L | H |

H; high level, L; low level, X; irrelevant

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current** | $I_{CCL}$ | $V_{CC}=5.25V$ | | – | 6.2 | 10 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** $I_{CC}$ is measured with all outputs open and all inputs grounded.

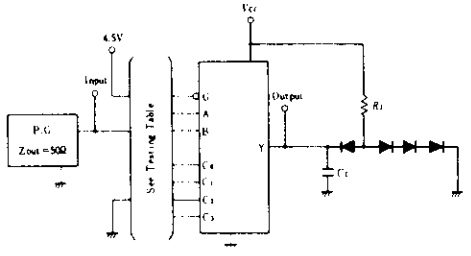
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## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | Data | Y | $C_L$=15pF, $R_L$=2kΩ | – | 10 | 15 | ns |
| | $t_{PHL}$ | Data | Y | | – | 17 | 26 | ns |
| | $t_{PLH}$ | Select | Y | | – | 19 | 29 | ns |
| | $t_{PHL}$ | Select | Y | | – | 25 | 38 | ns |
| | $t_{PLH}$ | Strobe | Y | | – | 16 | 24 | ns |
| | $t_{PHL}$ | Strobe | Y | | – | 21 | 32 | ns |

## ■TESTING METHOD

### 1) Test Circuit



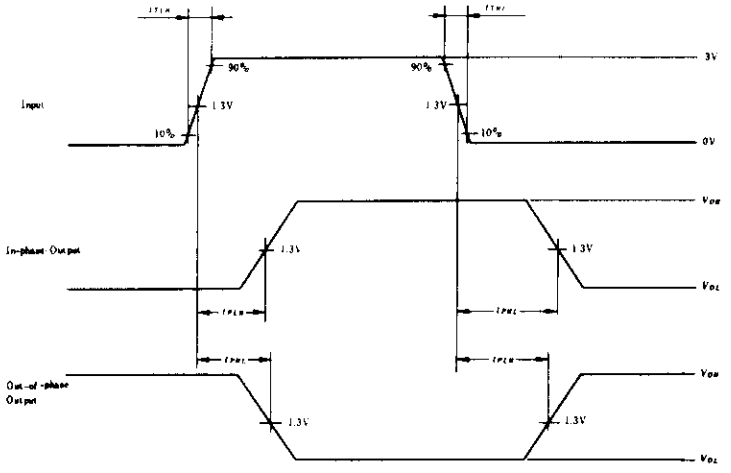

Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

### 2) Testing Table

| Item | Inputs | | | | | | | Output |
|---|---|---|---|---|---|---|---|---|
| | B | A | $C_0$ | $C_1$ | $C_2$ | $C_3$ | G | Y |
| | GND | GND | IN | × | × | × | GND | OUT |
| | GND | 4.5V | × | IN | × | × | GND | OUT |
| | 4.5V | GND | × | × | IN | × | GND | OUT |
| | 4.5V | 4.5V | × | × | × | IN | GND | OUT |
| $t_{PLH}$ / $t_{PHL}$ | GND | IN | GND | 4.5V | × | × | GND | OUT |
| | | | 4.5V | GND | | | | |
| | IN | GND | GND | × | 4.5V | × | GND | OUT |
| | | | 4.5V | | GND | | | |
| | GND | GND | 4.5V | × | × | × | IN | OUT |

X: "4.5V" or "GND"

### Waveform




Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns,
$PRR \geqq 1$MHz, duty cycle 50%.

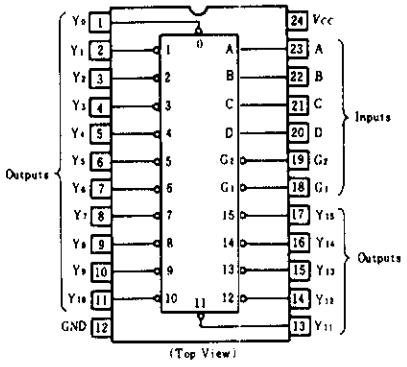


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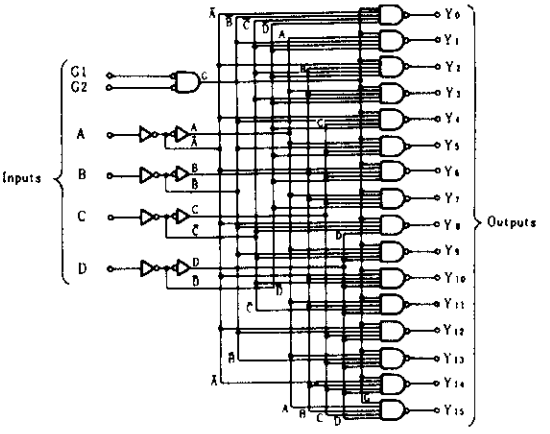
# HD74LS154 ●4-line-to-16-line Decoders/Demultiplexers

This decoder utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from the one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■FUNCTION TABLE

| Inputs | | | | | | Outputs | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $G_1$ | $G_2$ | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | L | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H |
| L | L | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H |
| L | L | H | H | L | L | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H |
| L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H |
| L | L | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | H | × | × | × | × | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | L | × | × | × | × | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | × | × | × | × | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

* H; high level, L; low level, X; irrelevant

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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | min | typ* | max | Unit |
|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | 2.0 | | | V |
| | $V_{IL}$ | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OH}$ = −400μA | 2.7 | – | | V |
| | $V_{OL}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $I_{OL}$ = 4mA | – | – | 0.4 | V |
| | | $V_{IL}$ = 0.8V, $I_{OL}$ = 8mA | – | | 0.5 | V |
| Input current | $I_{IH}$ | $V_{CC}$ = 5.25V, $V_I$ = 2.7V | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}$ = 5.25V, $V_I$ = 0.4V | – | – | 0.4 | mA |
| | $I_I$ | $V_{CC}$ = 5.25V, $V_I$ = 7V | – | – | 0.1 | mA |
| Short circuit output current | $I_{OS}$ | $V_{CC}$ = 5.25V | −20 | – | −100 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}$ = 5.25V | | 9 | 14 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$ = 4.75V, $I_{IN}$ = −18mA | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

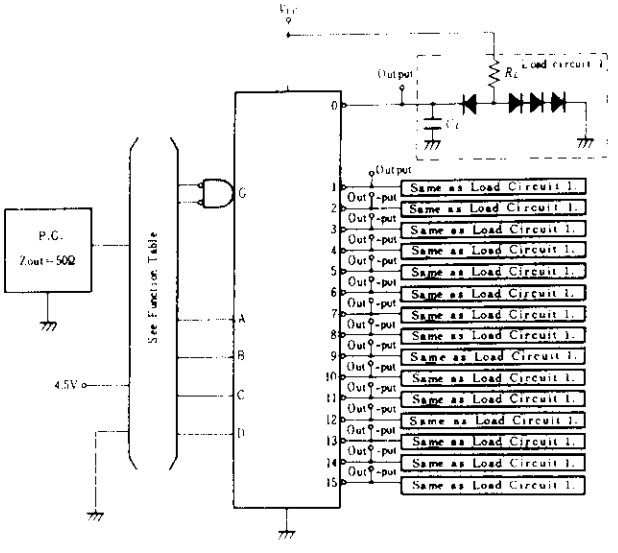
** $I_{CC}$ is measured with all outputs open and all inputs grounded.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$ = 5V, $Ta$ = 25°C )

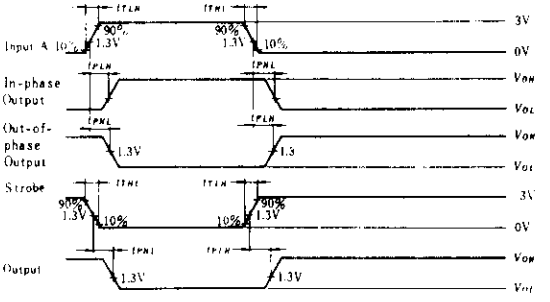
| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A, B, C, D | $Y_0 \sim Y_{15}$ | $C_L$ = 15pF, $R_L$ = 2kΩ | – | 24 | 36 | ns |
| | $t_{PHL}$ | A, B, C, D | $Y_0 \sim Y_{15}$ | | – | 22 | 33 | ns |
| | $t_{PLH}$ | G1, G2 | $Y_0 \sim Y_{15}$ | | – | 20 | 30 | ns |
| | $t_{PHL}$ | G1, G2 | $Y_0 \sim Y_{15}$ | | – | 18 | 27 | ns |

## ■TESTING METHOD

### 1) Test Circuit




### Waveform




Notes) 1. Input pulse; $t_{TLH} \leq 15$ns, $t_{THL} \leq 6$ns, $PRR$=1MHz, duty cycle=50%

2. $C_L$ includes probe and jig capacitance.

3. All diodes are 1S2074 Ⓗ.

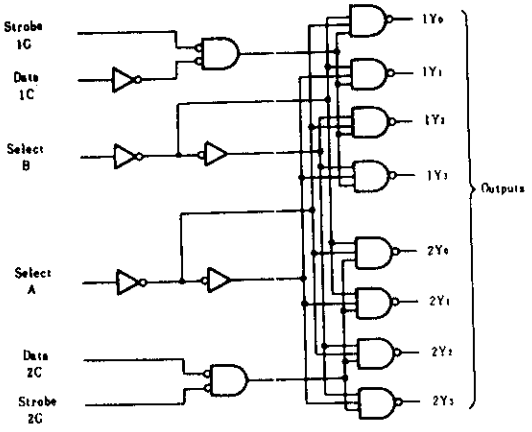


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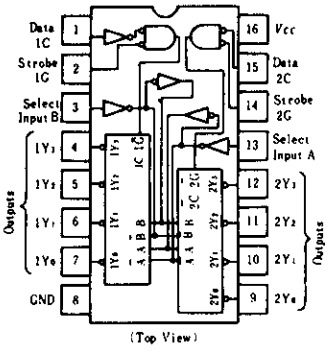
# HD74LS155 ●Dual 2-line-to-4-line Decoders/Demultiplexers

This circuit features dual 1-line-to-4-line demultiplexer with individual strobes and common binary-address input. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




## ■FUNCTION TABLE

### ●2-line-to-4-line Decoder/1-line-to-4-line Demultiplexer

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| Select | | Strobe | Data | | | | |
| B | A | 1G | 1C | 1Y0 | 1Y1 | 1Y2 | 1Y3 |
| × | × | H | × | H | H | H | H |
| L | L | L | H | L | H | H | H |
| L | H | L | H | H | L | H | H |
| H | L | L | H | H | H | L | H |
| H | H | L | H | H | H | H | L |
| × | × | × | L | H | H | H | H |

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| Select | | Strobe | Data | | | | |
| B | A | 2G | 2C | 2Y0 | 2Y1 | 2Y2 | 2Y3 |
| × | × | H | × | H | H | H | H |
| L | L | L | L | L | H | H | H |
| L | H | L | L | H | L | H | H |
| H | L | L | L | H | H | L | H |
| H | H | L | L | H | H | H | L |
| × | × | × | H | H | H | H | H |

### ●3-line-to-8-line Decoder/1-line-to-8-line Demultiplexer

| Inputs | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Select | | | Strobe Data | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| C | B | A | G | 2Y0 | 2Y1 | 2Y2 | 2Y3 | 1Y0 | 1Y1 | 1Y2 | 1Y3 |
| × | × | × | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H |
| L | H | L | L | H | H | L | H | H | H | H | H |
| L | H | H | L | H | H | H | L | H | H | H | H |
| H | L | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | L | H | H |
| H | H | L | L | H | H | H | H | H | H | L | H |
| H | H | H | L | H | H | H | H | H | H | H | L |

Notes) 1. C; input 1C and 2C connected together
2. G; inputs 1G and 2G connected together
3. H; high level, L; low level, X; irrelevant

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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | — | — | 0.4 | V |
| | | | $I_{OL}=8mA$ | — | — | 0.5 | |
| Input current | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −5 | — | −42 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}=5.25V$ | | — | 6.1 | 10 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

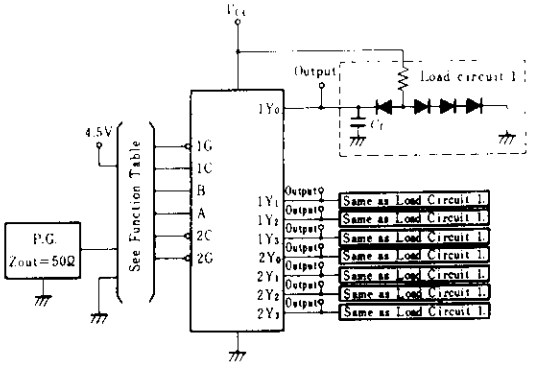
** $I_{CC}$ is measured with outputs open, A, B, and 1C inputs at 4.5V, and 2C, 1G, and 2G inputs grounded.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

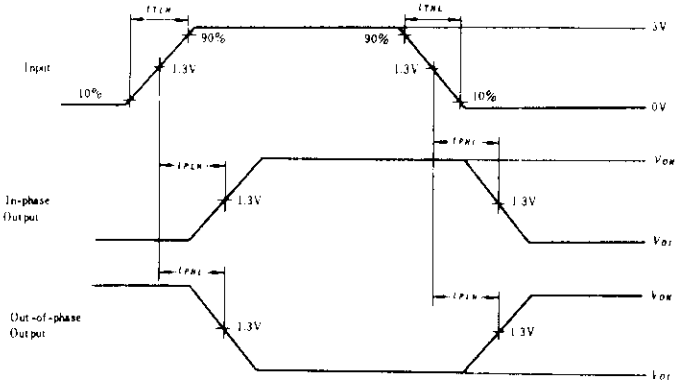
| Item | Inputs | Output | Levels of logic | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | A, B, 2C | Y | 2 | $C_L=15pF$, $R_l=2k\Omega$ | — | 10 | 15 | ns |
| $t_{PHL}$ | 1G or 2G | | | | — | 19 | 30 | ns |
| $t_{PLH}$ | A or B | Y | 3 | | — | 17 | 26 | ns |
| $t_{PHL}$ | | | | | — | 19 | 30 | ns |
| $t_{PLH}$ | 1C | Y | 3 | | — | 18 | 27 | ns |
| $t_{PHL}$ | | | | | | 18 | 27 | ns |

## ■TESTING METHOD

### 1) Test Circuit




### Waveform




Notes) 1. Input pulse; $t_{TLH} \leqq 15ns$, $t_{THL} \leqq 6ns$, $PRR=1MHz$, duty cycle=50%
2. $C_L$ includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ.

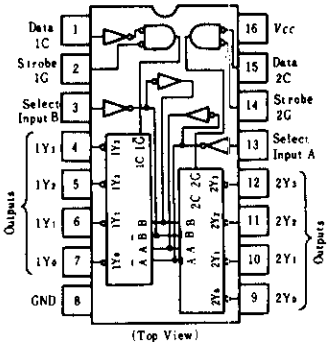


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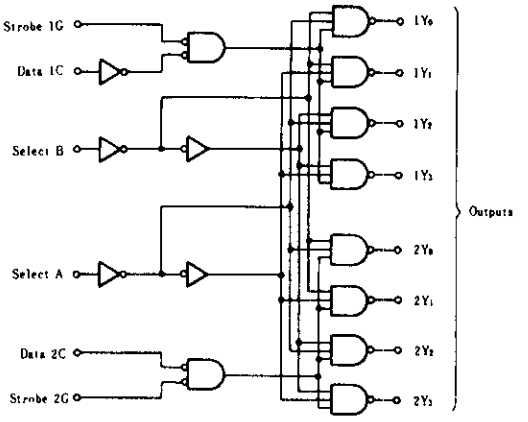
# HD74LS156 ●Dual 2-line-to-4-line Decoders/Demultiplexers (with open collector outputs)

This circuit features dual 1-line-to-4-line demultiplexer with individual strobes and common binary-address inputs. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output voltage | $V_{OH}$ | — | — | 5.5 | V |
| Low level output current | $I_{OL}$ | — | — | 8 | mA |

## ■FUNCTION TABLE

### ●2-to-4-line Decoder/1-to-4-line Demultiplexer

| Inputs | | | | Outputs | | | | Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SELECT | | STROBE | DATA | | | | | SELECT | | STROBE | DATA | | | | |
| B | A | 1G | 1C | 1Y0 | 1Y1 | 1Y2 | 1Y3 | B | A | 2G | 2C | 2Y0 | 2Y1 | 2Y2 | 2Y3 |
| × | × | H | × | H | H | H | H | × | × | H | × | H | H | H | H |
| L | L | L | H | L | H | H | H | L | L | L | L | L | H | H | H |
| L | H | L | H | H | L | H | H | L | H | L | L | H | L | H | H |
| H | L | L | H | H | H | L | H | H | L | L | L | H | H | L | H |
| H | H | L | H | H | H | H | L | H | H | L | L | H | H | H | L |
| × | × | × | L | H | H | H | H | × | × | × | H | H | H | H | H |

### ●3-to-8-line Decoder/1-to-8-line Demultiplexer

| Inputs | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SELECT | | | STROBE OR DATA | (0) | (1) | (2) | (3) | (4) | (5) | (6) | (7) |
| C[1] | B | A | G[2] | 2Y0 | 2Y1 | 2Y2 | 2Y3 | 1Y0 | 1Y1 | 1Y2 | 1Y3 |
| × | × | × | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H |
| L | H | L | L | H | H | L | H | H | H | H | H |
| L | H | H | L | H | H | H | L | H | H | H | H |
| H | L | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | L | H | H |
| H | H | L | L | H | H | H | H | H | H | L | H |
| H | H | H | L | H | H | H | H | H | H | H | L |

Notes) 1. C; input 1C and 2C connected together
2. G; inputs 1G and 2G connected together
3. H; high level, L; low level, X; irrelevant

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## ■ELECTRICAL CHARACTERISTICS ( $Ta$ = −20 ~ +75°C )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output current | $I_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $V_{OH}$=5.5V | | — | — | 100 | μA |
| Output voltage | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | — | — | 0.4 | V |
| | | | $I_{OL}$=8mA | — | — | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.1 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}$=5.25V | | — | 6.1 | 10 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

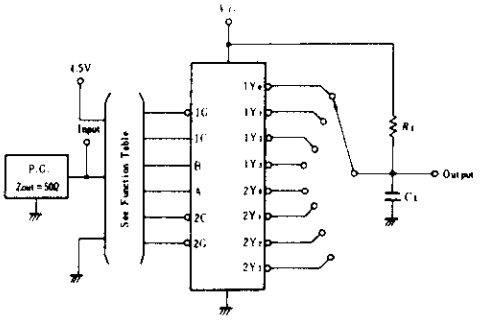
** $I_{CC}$ is measured with outputs open, A, B, and 1C inputs at 4.5V, and 2C, 1G, and 2G inputs grounded.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25°C )

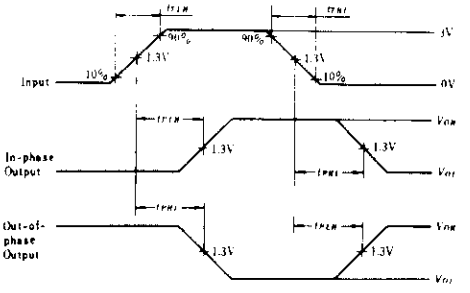
| Item | Symbol | Inputs | Output | Level of logic | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A, B, 2C, 1G or 2G | Y | 2 | $C_L$=15pF, $R_L$=2kΩ | — | 25 | 40 | ns |
| | $t_{PHL}$ | A, B, 2C, 1G or 2G | Y | 2 | | — | 34 | 51 | |
| | $t_{PLH}$ | A or B | Y | 3 | | — | 31 | 46 | |
| | $t_{PHL}$ | A or B | Y | 3 | | — | 34 | 51 | |
| | $t_{PLH}$ | 1C | Y | 3 | | — | 32 | 48 | |
| | $t_{PHL}$ | 1C | Y | 3 | | — | 32 | 48 | |

## ■TESTING METHOD

### 1) Test Circuit




### Waveform




Notes) 1. Input pulse; $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz, duty cycle=50%.

2. $C_L$ includes probe and jig capacitance.

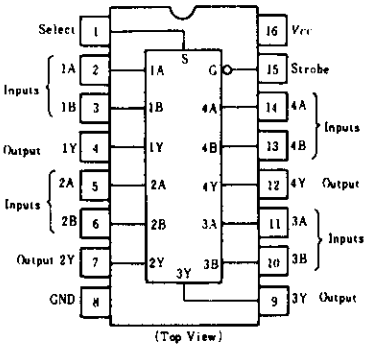


Home Print

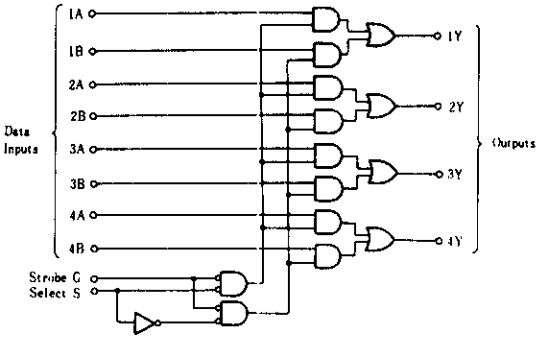
# HD74LS157 ●Quadruple 2-line-to-1-line Data Selectors/Multiplexers (noninverted outputs)

This data selector/multiplexer contains inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. Then, outputs present true data to minimize propagation delay time.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■FUNCTION TABLE

| Inputs | | | | Output |
|---|---|---|---|---|
| Strobe | Select | A | B | Y |
| H | × | × | × | L |
| L | L | L | × | L |
| L | L | H | × | H |
| L | H | × | L | L |
| L | H | × | H | H |

H; high level, L; low level, X; irrelevant

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | S, G | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 40 | $\mu A$ |
| | A, B | | | | – | – | 20 | |
| | S, G | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.8 | mA |
| | A, B | | | | – | – | −0.4 | |
| | S, G | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.2 | mA |
| | A, B | | | | – | – | 0.1 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current** | | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 9.7 | 16 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

** $I_{CC}$ is measured with all outputs open and all inputs at 4.5V.

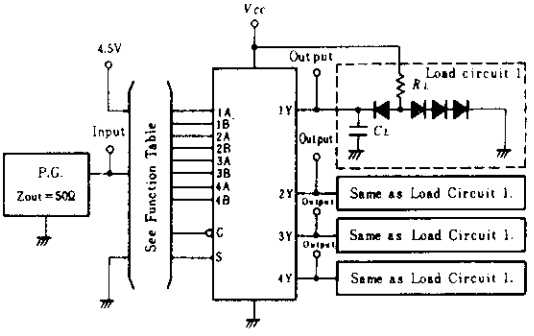
## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Output | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | Data | Y | $C_L=15pF$, $R_L=2k\Omega$ | – | 9 | 14 | ns |
| | $t_{PHL}$ | | | | – | 9 | 14 | ns |
| | $t_{PLH}$ | Strobe | Y | | – | 13 | 20 | ns |
| | $t_{PHL}$ | | | | – | 14 | 21 | ns |
| | $t_{PLH}$ | Select | Y | | – | 15 | 23 | ns |
| | $t_{PHL}$ | | | | – | 18 | 27 | ns |

Home Print

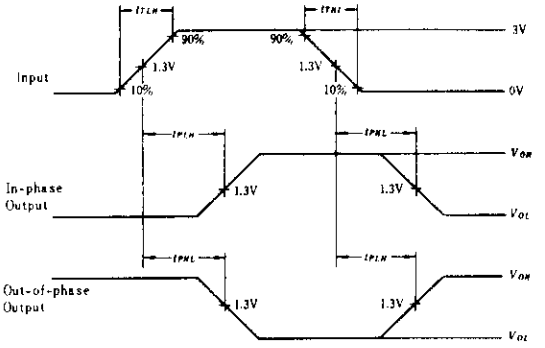
## ■TESTING METHOD

### 1) Test Circuit




Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

### Waveform




Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns,
$PRR = 1$MHz, duty cycle 50%.

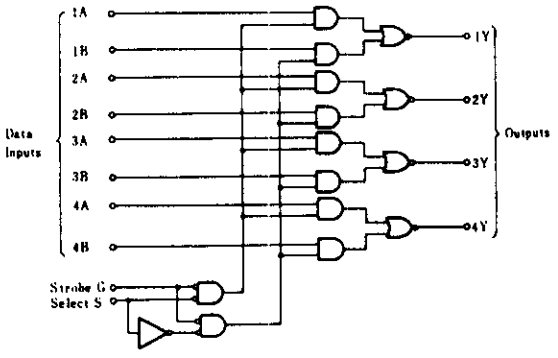


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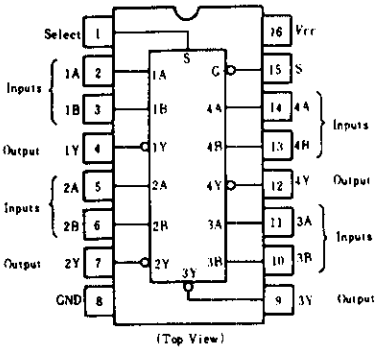
# HD74LS158 ● Quadruple 2-line-to-1-line Data Selectors/Multiplexers (inverted outputs)

This data selector/multiplexer contains inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. Then, outputs present inverted data to minimize propagation delay time.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




## ■FUNCTION TABLE

| Inputs | | | | Output |
|---|---|---|---|---|
| Strobe | Select | A | B | Y |
| H | × | × | × | H |
| L | L | L | × | H |
| L | L | H | × | L |
| L | H | × | L | H |
| L | H | × | H | L |

H; high level L; low level, X; irrelevant

## ■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | G, S | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 40 | $\mu A$ |
| | A, B | | | | – | – | 20 | |
| | G, S | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.8 | mA |
| | A, B | | | | – | – | −0.4 | |
| | G, S | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.2 | mA |
| | A, B | | | | – | – | 0.1 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current ** | | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 4.8 | 8 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

** $I_{CC}$ is measured with all outputs open and all inputs at 4.5V.

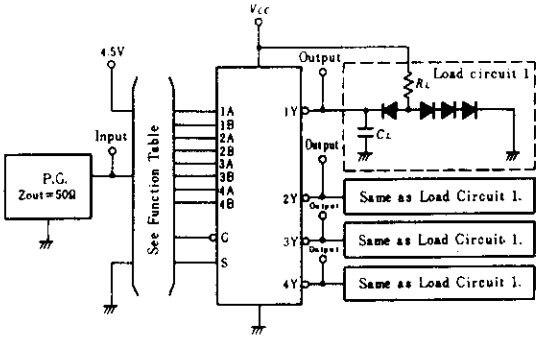
Home Print

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

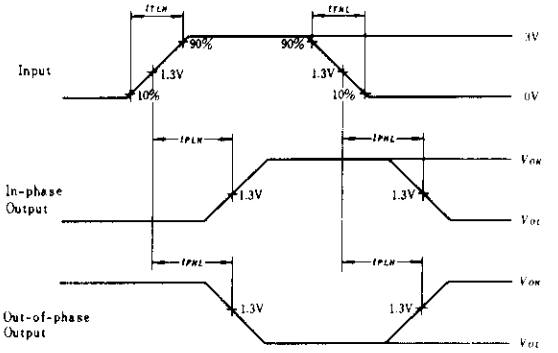
| Item | Symbol | Inputs | Output | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | Data | Y | $C_L$=15pF, $R_L$=2kΩ | – | 7 | 12 | ns |
| | $t_{PHL}$ | | | | – | 7 | 12 | |
| | $t_{PLH}$ | Strobe | Y | | – | 11 | 17 | ns |
| | $t_{PHL}$ | | | | – | 12 | 18 | |
| | $t_{PLH}$ | Select | Y | | – | 13 | 20 | ns |
| | $t_{PHL}$ | | | | – | 16 | 24 | |

## ■TESTING METHOD

### 1) Test Circuit




### Waveform




Notes) 1. $C_L$ includes probe and jig capacitance.
2 All diodes are 1S2074 (H).

Input pulse; $t_{TLH}$≦15ns, $t_{THL}$≦6ns,
$PRR$=1MHz, duty cycle 50%.

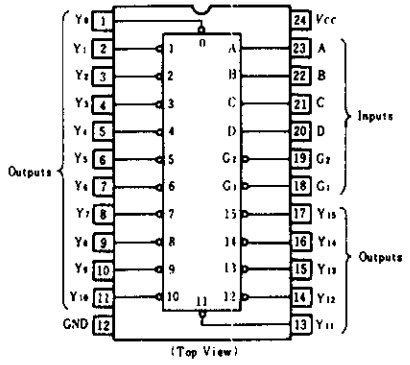


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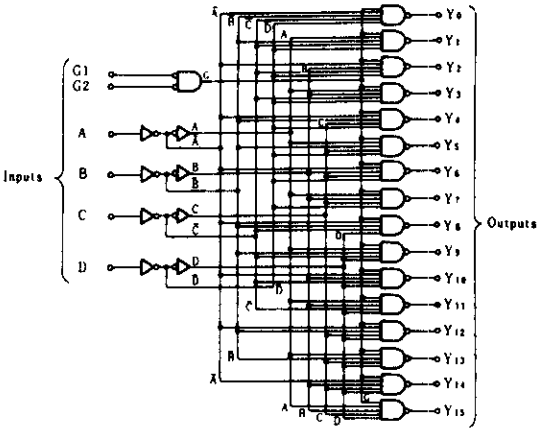
# HD74LS159 ● 4-line-to-16-line Decoders/Demultiplexers (with Open Collector Outputs)

This decoder utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from the one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■FUNCTION TABLE

| Inputs | | | | | | Outputs | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $G_1$ | $G_2$ | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | L | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H |
| L | L | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H |
| L | L | H | H | L | L | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H |
| L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H |
| L | L | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | H | × | × | × | × | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | L | × | × | × | × | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | × | × | × | × | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

* H; high level, L; low level, X; irrelevant

Home Print

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | min | typ* | max | Unit |
|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | 2.0 | - | — | V |
| | $V_{IL}$ | | — | — | 0.8 | V |
| Output current | $I_{OH}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $V_{OH}$ = 5.5V | — | — | 100 | μA |
| Output voltage | $V_{OL}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $I_{OL}$ = 4mA | — | — | 0.4 | V |
| | | $V_{IL}$ = 0.8V, $I_{OL}$ = 8mA | — | — | 0.5 | V |
| Input current | $I_{IH}$ | $V_{CC}$ = 5.25V, $V_I$ = 2.7V | — | — | 20 | μA |
| | $I_{IL}$ | $V_{CC}$ = 5.25V, $V_I$ = 0.4V | — | — | 0.4 | mA |
| | $I_I$ | $V_{CC}$ = 5.25V, $V_I$ = 7V | — | — | 0.1 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}$ = 5.25V | — | 9 | 14 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$ = 4.75V, $I_{IN}$ = −18mA | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

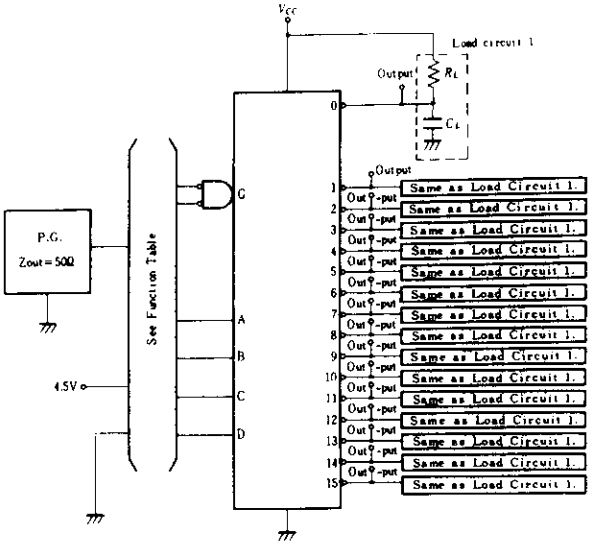
** $I_{CC}$ is measured with all outputs open and all inputs grounded.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$ = 5V, $Ta$ = 25°C )

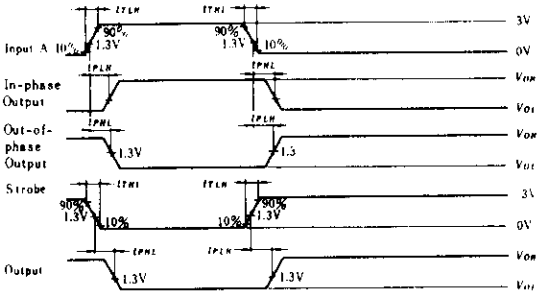
| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A, B, C, D | $Y_0 \sim Y_{15}$ | $C_L$ = 15pF, $R_L$ = 2kΩ | — | 23 | 36 | ns |
| | $t_{PHL}$ | A, B, C, D | $Y_0 \sim Y_{15}$ | | — | 24 | 36 | ns |
| | $t_{PLH}$ | G1, G2 | $Y_0 \sim Y_{15}$ | | | 15 | 25 | ns |
| | $t_{PHL}$ | G1, G2 | $Y_0 \sim Y_{15}$ | | | 22 | 36 | ns |

## ■TESTING METHOD

### 1) Test Circuit




### Waveform




Notes) 1. Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz, duty cycle=50%

2. $C_L$ includes probe and jig capacitance.

3. All diodes are 1S2074 Ⓗ.

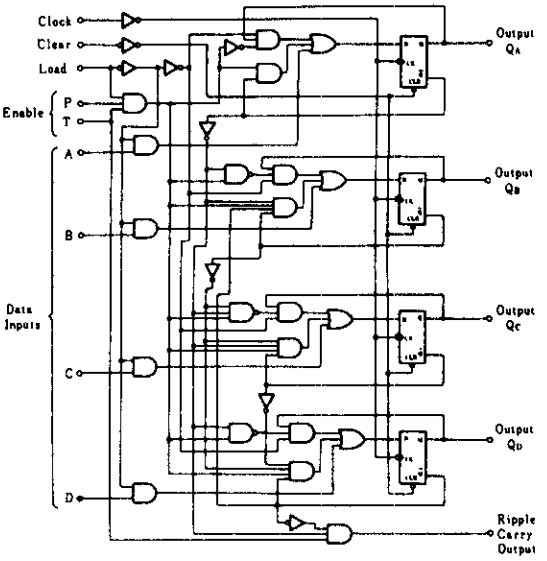


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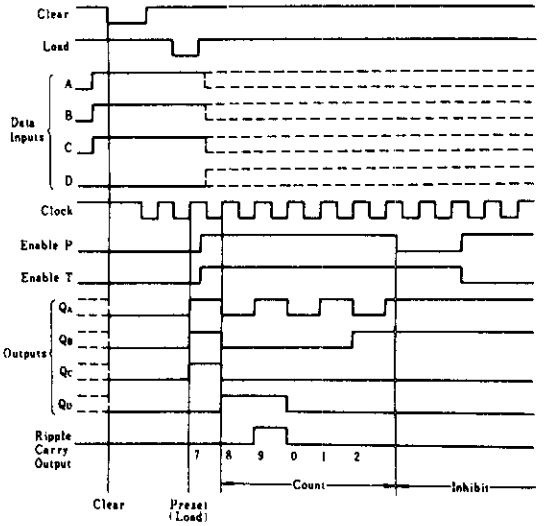
# HD74LS160A ● Synchronous Decade Counters (direct clear)

This synchronous decade counter features an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode is operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform. This counter is fully programmable; that is, the output may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of this device should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function is two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the $Q_A$ output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs should occur only when the clock input is high.

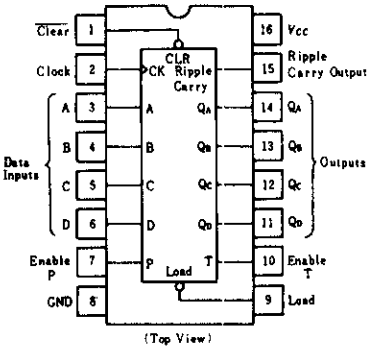
## ■BLOCK DIAGRAM




## ■TYPICAL CLEAR, PRESET, AND INHIBIT SEQUENCE




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATIING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | | $f_{clock}$ | 0 | — | 25 | MHz |
| Clock pulse width | | $t_{w(clock)}$ | 25 | — | — | ns |
| Clear pulse width | | $t_{w(clear)}$ | 20 | — | — | ns |
| Setup time | A, B, C, D | $t_{su}$ | 20 | — | — | ns |
| | Enable P, T | | 20 | — | — | |
| | Load | | 20 | — | — | |
| Hold time | | $t_h$ | 3 | — | — | ns |

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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | $V_{IL}=0.8V$ | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | Data, Enable P | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | Load, Clock, Enable T | | | | – | – | 40 | |
| | Clear | | | | – | – | 20 | |
| | Data, Enable P | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | Load, Clock, Enable T | | | | – | – | −0.8 | |
| | Clear | | | | – | – | −0.4 | |
| | Data, Enable P | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| | Load, Clock, Enable T | | | | – | – | 0.2 | |
| | Clear | | | | – | – | 0.1 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current ** | | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 18 | 31 | mA |
| | | $I_{CCL}$ | $V_{CC}=5.25V$ | | – | 19 | 32 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

** $I_{CCH}$ is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
$I_{CCL}$ is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

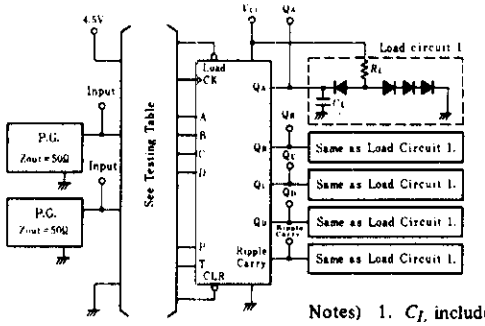
| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | Clock | $Q_A \sim Q_D$ | $C_L=15pF$, $R_L=2k\Omega$ | 25 | 32 | – | MHz |
| Propagation delay time | $t_{PLH}$ | Clock | Ripple Carry | | – | 20 | 35 | ns |
| | $t_{PHL}$ | | | | – | 18 | 35 | ns |
| | $t_{PLH}$ | Clock (Load="H") | $Q_A \sim Q_D$ | | – | 13 | 24 | ns |
| | $t_{PHL}$ | | | | – | 18 | 27 | ns |
| | $t_{PLH}$ | Clock (Load="L") | $Q_A \sim Q_D$ | | – | 13 | 24 | ns |
| | $t_{PHL}$ | | | | – | 18 | 27 | ns |
| | $t_{PLH}$ | Enable T | Ripple Carry | | – | 9 | 14 | ns |
| | $t_{PHL}$ | | | | – | 9 | 14 | ns |
| | $t_{PHL}$ | Clear | $Q_A \sim Q_D$ | | – | 20 | 28 | ns |



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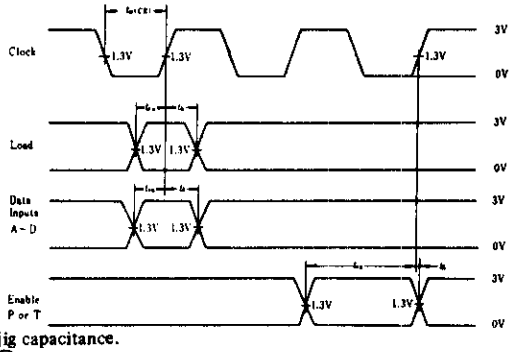
## ■TESTING METHOD

### 1) Test Circuit




Notes) 1. $C_L$ includes probe and jig capacitance.
2 All diodes are 1S2074 Ⓗ.

## ■TIMING METHOD

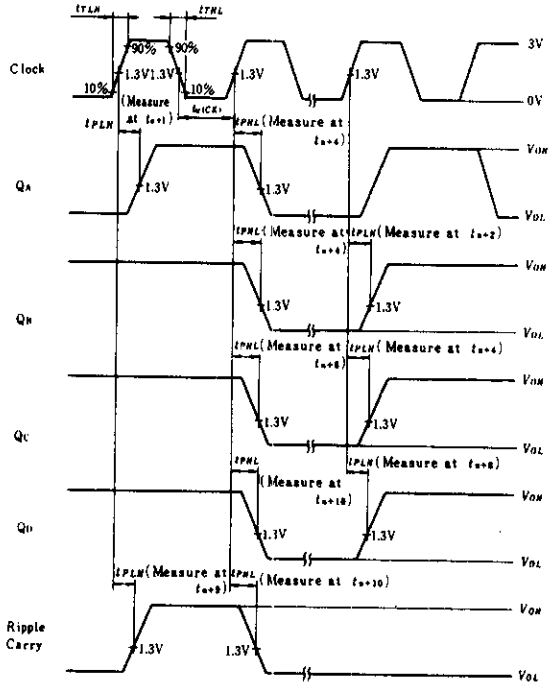



### 2) Testing Table

| Item | From input to output | Inputs | | | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Clear | Load | Enable P | Enable T | Clock | Data A | Data B | Data C | Data D | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | Ripple Carry |
| $f_{max}$ | | 4.5V | 4.5V | 4.5V | 4.5V | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | OUT |
| $t_{PLH}$ $t_{PHL}$ | CK→Ripply Carry | 4.5V | 4.5V | 4.5V | 4.5V | IN | GND | GND | GND | GND | – | – | – | – | OUT |
| | CK→Q | 4.5V | 4.5V | 4.5V | 4.5V | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | – |
| | CK→Q | 4.5V | GND | GND | GND | IN | IN* | IN* | IN* | IN* | OUT | OUT | OUT | OUT | – |
| | Enable T→Ripple Carry | 4.5V | GND | 4.5V | IN | IN** | 4.5V | GND | GND | 4.5V | – | – | – | – | OUT |
| | CLR→Q | IN | GND | GND | GND | IN** | 4.5V | 4.5V | 4.5V | 4.5V | OUT | OUT | OUT | OUT | – |

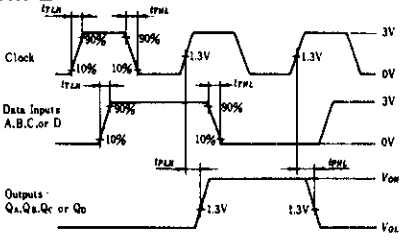
* Measuring outputs correspond to this condition, each outputs ($Q_A$, $Q_B$, $Q_C$, and $Q_D$) must not be over the following rate, "H", "L", "L", and "H '.
** For initialized

### Waveform-1 $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Clock→Q, Ripple Carry)



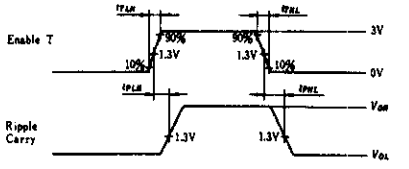

Notes) Clock input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz, duty cycle=50% and: for $f_{max}$, $t_{TLH}$=$t_{THL} \leqq 2.5$ns.
$t_n$ is reference bit time when all outputs are low.

### Waveform-2 $t_{PLH}$, $t_{PHL}$ (Clock→Q)



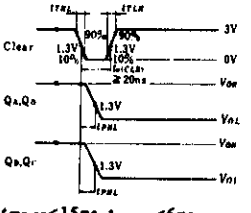

Notes) Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, Clock input: $PRR$= 1MHz, duty cycle 50%, Data input: $PRR$=500kHz, duty cycle 50%

### Waveform-3 $t_{PLH}$, $t_{PHL}$ (Enable T→Ripple Carry)




Note) Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz

### Waveform-4 $t_{PHL}$ (Clear→Q)



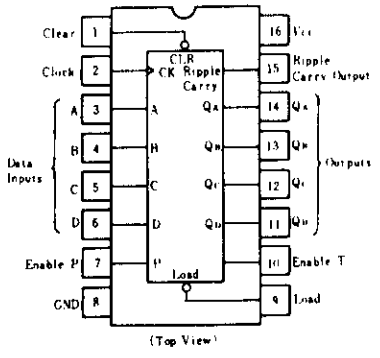

Note) Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns

# HD74LS161A ● Synchronous 4-bit Binary Counters (direct clear)

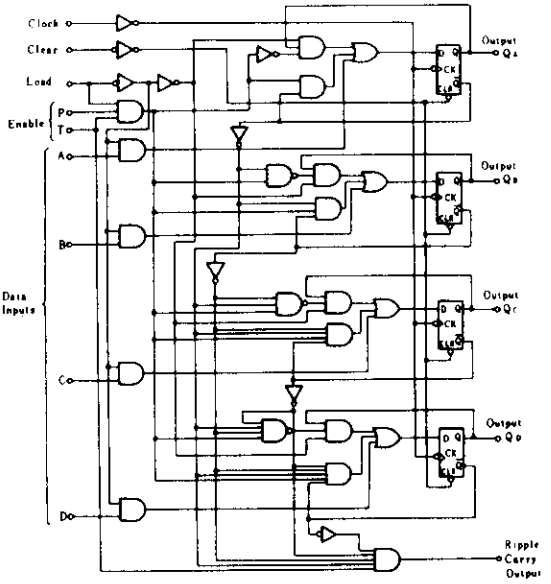
This synchronous 4-bit binary counter features an internal carry look-ahead for application in high speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs changes coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The carry look-ahead circuity provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the $Q_A$ output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs should occur only when the clock input is high.

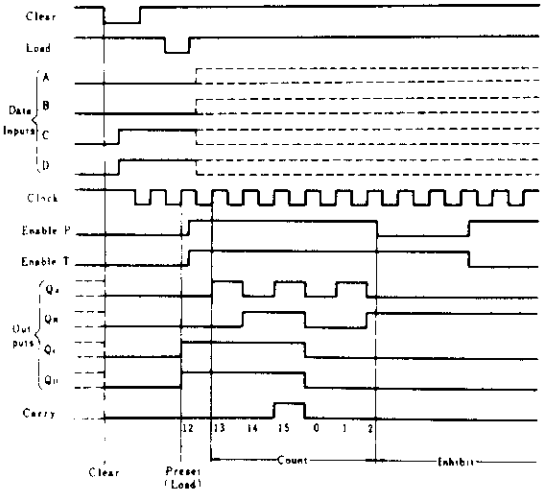
## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■TYPICAL CLEAR, PRESET, AND INHIBIT SEQUENSE




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | | $f_{clock}$ | 0 | – | 25 | MHz |
| Clock pulse width | | $t_{w(CK)}$ | 25 | – | – | ns |
| Clear pulse width | | $t_{w(CLR)}$ | 20 | – | – | ns |
| Setup time | A, B, C, D | $t_{su}$ | 20 | – | – | ns |
| | Enable P, T | | 20 | – | – | |
| | Load | | 20 | – | – | |
| Hold time | | $t_h$ | 3 | – | – | ns |



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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | Data, Enable P | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | Load, Clock, Enable T | | | | – | – | 40 | |
| | Clear | | | | – | – | 20 | |
| | Data, Enable P | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | Load, Clock, Enable T | | | | – | – | −0.8 | |
| | Clear | | | | – | – | −0.4 | |
| | Data, Enable P | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| | Load, Clock, Enable T | | | | – | – | 0.2 | |
| | Clear | | | | – | – | 0.1 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current** | | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 18 | 31 | mA |
| | | $I_{CCL}$ | $V_{CC}=5.25V$ | | – | 19 | 32 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

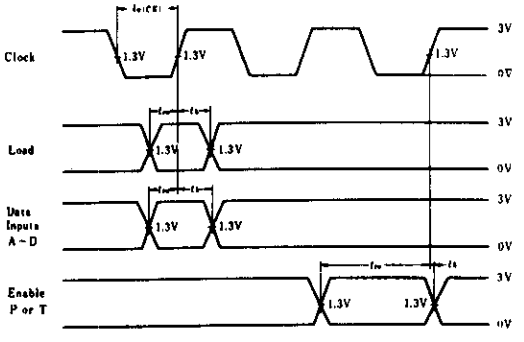
* $V_{CC}=5V$, $Ta=25°C$

** $I_{CCH}$ is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open. $I_{CCL}$ is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

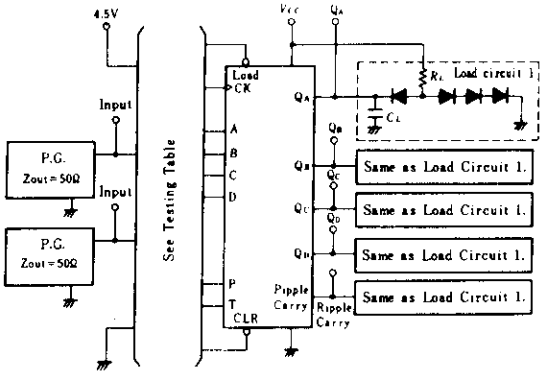
| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | Clock | $Q_A \sim Q_D$ | $C_L=15pF$, $R_L=2k\Omega$ | 25 | 32 | – | MHz |
| Propagation delay time | $t_{PLH}$ | Clock | Ripple Carry | | – | 20 | 35 | ns |
| | $t_{PHL}$ | | | | – | 18 | 35 | ns |
| | $t_{PLH}$ | Clock (Load="H") | $Q_A \sim Q_D$ | | – | 13 | 24 | ns |
| | $t_{PHL}$ | | | | – | 18 | 27 | ns |
| | $t_{PLH}$ | Clock (Load="L") | $Q_A \sim Q_D$ | | – | 13 | 24 | ns |
| | $t_{PHL}$ | | | | – | 18 | 27 | ns |
| | $t_{PLH}$ | Enable T | Ripple Carry | | – | 9 | 14 | ns |
| | $t_{PHL}$ | | | | – | 9 | 14 | ns |
| | $t_{PHL}$ | Clear | $Q_A \sim Q_D$ | | – | 20 | 28 | ns |

## ■TIMING DEFINITION



## ■TESTING METHOD

1) Test Circuit



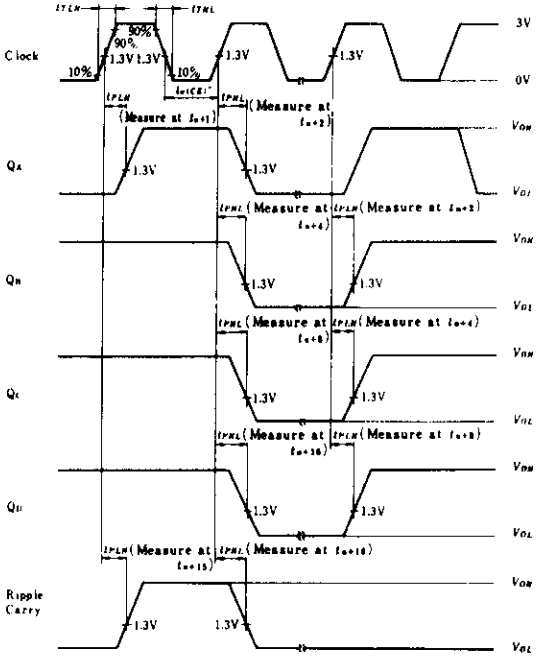

Notes) 1 $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ

2) Testing Table

| Item | From input to output | Inputs | | | | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Clear | Load | Enable P | Enable T | Clock | Data A | Data B | Data C | Data D | | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | Ripple Carry |
| $f_{max}$ | | 4.5V | 4.5V | 4.5V | 4.5V | IN | GND | GND | GND | GND | | OUT | OUT | OUT | OUT | OUT |
| $t_{PLH}$ $t_{PHL}$ | CK→Ripple Carry | 4.5V | 4.5V | 4.5V | 4.5V | IN | GND | GND | GND | GND | | – | – | – | – | OUT |
| | CK→Q | 4.5V | 4.5V | 4.5V | 4.5V | IN | GND | GND | GND | GND | | OUT | OUT | OUT | OUT | – |
| | CK→Q | 4.5V | GND | GND | GND | IN | IN* | IN* | IN* | IN* | | OUT | OUT | OUT | OUT | – |
| | Enable T→Ripple Carry | 4.5V | GND | 4.5V | IN | IN* | 4.5V | 4.5V | 4.5V | 4.5V | | – | – | – | – | OUT |
| | CLR→Q | IN | GND | GND | GND | IN* | 4.5V | 4.5V | 4.5V | 4.5V | | OUT | OUT | OUT | OUT | – |

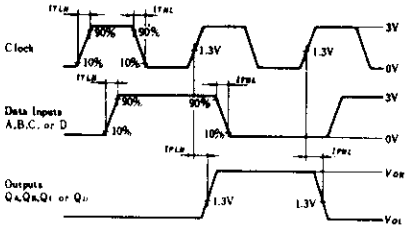
* For initialized

Waveform−1 $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Clock→Q, Ripple Carry)



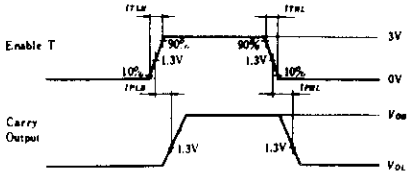

Notes) 1. Clock input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz, duty cycle=50% and: for $f_{max}$, $t_{TLH}$=$t_{THL} \leqq 2.5$ns.
2. $t_n$ is reference bit time when all outputs are low.

Waveform−2 $t_{PLH}$, $t_{PHL}$ (Clock→Q)

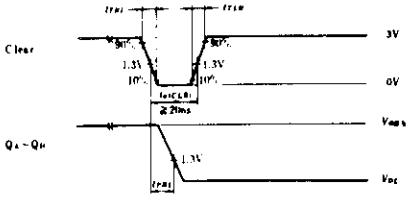



Notes) Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, Clock input: $PRR$= 1MHz, duty cycle 50%, Data input: $PRR$=500kHz, duty cycle 50%

Waveform−3 $t_{PLH}$, $t_{PHL}$ (Enable T→Ripple Carry)




Note) Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz




Note) Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns

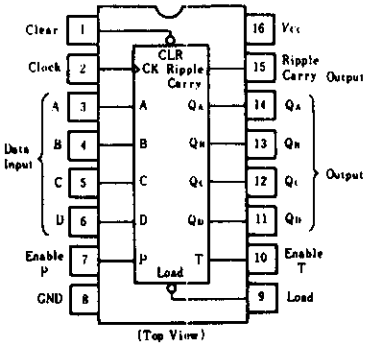


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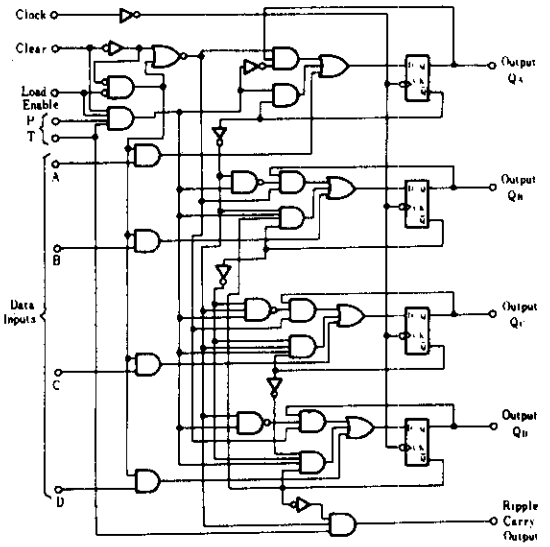
# HD74LS162A ● Synchronous Decade Counters (synchronous clear)

This synchronous decade counter features an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform. This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to LLLL. Low-to-high transitions at the clear input should be avoided when the clock is low if the enable and load inputs are high at or before the transition. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the $Q_A$ output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs should occur only when the clock input is high.

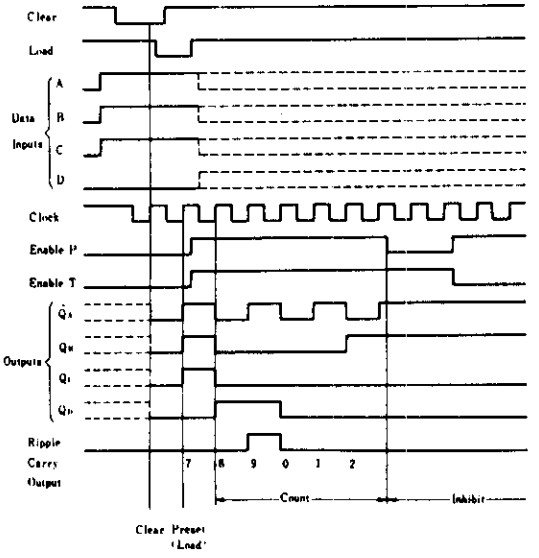
## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■TYPICAL CLEAR, PRESET, AND INHIBIT SEQUENCE

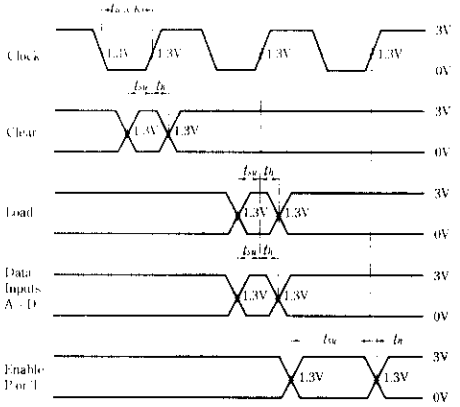



## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | | $f_{clock}$ | 0 | — | 25 | MHz |
| Clock pulse width | | $t_{w(CK)}$ | 25 | — | — | ns |
| Clear pulse width | | $t_{w(CLR)}$ | 20 | — | — | ns |
| Setup time | A, B, C, D | $t_{su}$ | 20 | — | — | ns |
| | Enable P, T | | 20 | — | — | ns |
| | Load | | 20 | — | — | ns |
| | Clear | | 20 | — | — | ns |
| Hold time | | $t_h$ | 3 | — | — | ns |

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## ■TIMING DEFINITION




## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | 2.0 | – | – | V |
| | | $V_{IL}$ | | – | – | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OH}$ = −400μA | 2.7 | – | – | V |
| | | $V_{OL}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OL}$ = 4mA | – | – | 0.4 | V |
| | | | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OL}$ = 8mA | – | – | 0.5 | V |
| Input current | Data, Enable P | $I_{IH}$ | $V_{CC}$ = 5.25V, $V_I$ = 2.7V | – | – | 20 | μA |
| | Load, Clock, Enable T | | | – | – | 40 | μA |
| | Clear | | | – | – | 40 | μA |
| | Data, Enable P | $I_{IL}$ | $V_{CC}$ = 5.25V, $V_I$ = 0.4V | – | – | −0.4 | mA |
| | Load, Clock, Enable T | | | – | – | −0.8 | mA |
| | Clear | | | – | – | −0.8 | mA |
| | Data, Enable P | $I_I$ | $V_{CC}$ = 5.25V, $V_I$ = 7V | – | – | 0.1 | mA |
| | Load, Clock, Enable T | | | – | – | 0.2 | mA |
| | Clear | | | – | – | 0.2 | mA |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$ = 5.25V | −20 | – | −100 | mA |
| Supply current** | | $I_{CCH}$ | $V_{CC}$ = 5.25V | – | 18 | 31 | mA |
| | | $I_{CCL}$ | $V_{CC}$ = 5.25V | – | 19 | 32 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$ = 4.75V, $I_{IN}$ = −18mA | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** $I_{CCH}$ is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open. $I_{CCL}$ is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$ = 5V, $Ta$ = 25°C )

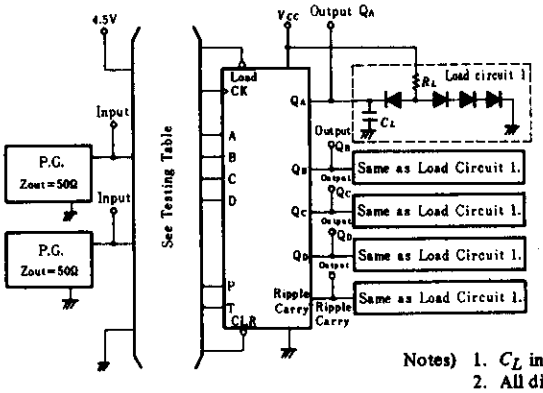
| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | Clock | $Q_A \sim Q_D$ | $C_L$ = 15pF, $R_L$ = 2kΩ | 25 | 32 | | MHz |
| Propagation delay time | $t_{PLH}$ | Clock | Ripple Carry | | – | 20 | 35 | ns |
| | $t_{PHL}$ | | | | – | 18 | 35 | ns |
| | $t_{PLH}$ | Clock (Load="H") | $Q_A \sim Q_D$ | | – | 13 | 24 | ns |
| | $t_{PHL}$ | | | | – | 18 | 27 | ns |
| | $t_{PLH}$ | Clock (Load="L") | $Q_A \sim Q_D$ | | – | 13 | 24 | ns |
| | $t_{PHL}$ | | | | – | 18 | 27 | ns |
| | $t_{PLH}$ | Enable T | Ripple Carry | | – | 9 | 14 | ns |
| | $t_{PHL}$ | | | | – | 9 | 14 | ns |
| | $t_{PHL}$ | Clear | $Q_A \sim Q_D$ | | – | 20 | 28 | ns |



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## ■TESTING METHOD

1) Test Circuit



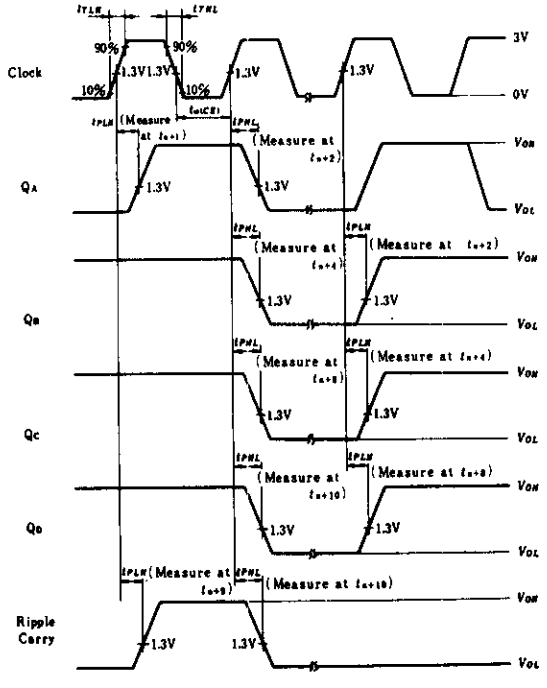

Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ

2) Testing Table

| Item | From input to output | Inputs | | | | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Clear | Load | Enable P | Enable T | Clock | Data A | Data B | Data C | Data D | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | Ripple Carry |
| $f_{max}$ | | 4.5V | 4.5V | 4.5V | 4.5V | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | OUT |
| $t_{PLH}$ $t_{PHL}$ | CK→Ripple Carry | 4.5V | 4.5V | 4.5V | 4.5V | IN | GND | GND | GND | GND | – | – | – | – | OUT |
| | CK→Q | 4.5V | 4.5V | 4.5V | 4.5V | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | – |
| | CK→Q | 4.5V | GND | GND | GND | IN | IN* | IN* | IN* | IN* | OUT | OUT | OUT | OUT | – |
| | Enable T→Ripple Carry | 4.5V | GND | 4.5V | IN | IN** | 4.5V | GND | GND | 4.5V | – | – | – | – | OUT |
| | Clear→Q | IN | GND | GND | GND | IN** | 4.5V | 4.5V | 4.5V | 4.5V | OUT | OUT | OUT | OUT | – |

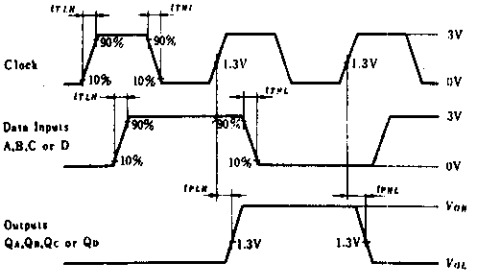
* Measuring outputs correspond to this condition, each outputs ($Q_A$, $Q_B$, $Q_C$, and $Q_D$) must not be over the following rate, "H", "L", "L", and " H".
** For initialized

3) Waveform−1 $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Clock→Q, Ripple Carry)



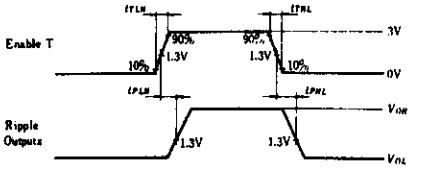

Notes) 1. Clock input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz, duty cycle=50% and: for $f_{max}$, $t_{TLH}$=$t_{THL} \leqq 2.5$ns.
2. $t_n$ is reference bit time when all outputs are low.

Waveform−2 $t_{PLH}$, $t_{PHL}$ (Clock→Q)



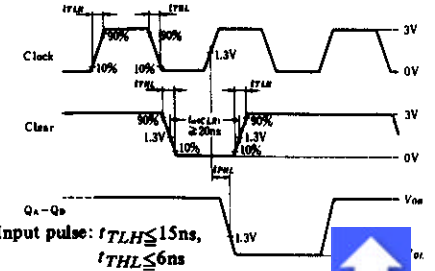

Notes) Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, Clock input: $PRR$= 1MHz, duty cycle 50%, Data input: $PRR$=500kHz, duty cycle 50%

Waveform−3 $t_{PLH}$, $t_{PHL}$ (Enable T→Ripple Carry)




Note) Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz

Waveform−4 $t_{PHL}$ (Clear→Q)




Note) Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns

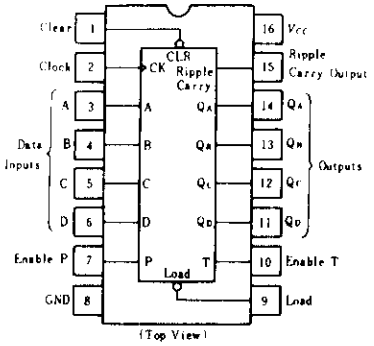
This synchronous 4-bit binary counter features an internal carry look-ahead to application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clock simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform. This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input would be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate.

The gate output is connected to the clear input to synchronously clear the counter to LLLL. Low-to-high transitions at the clear input should be avoided when the clock is low if the enable and load inputs are high at or before the transition. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating.

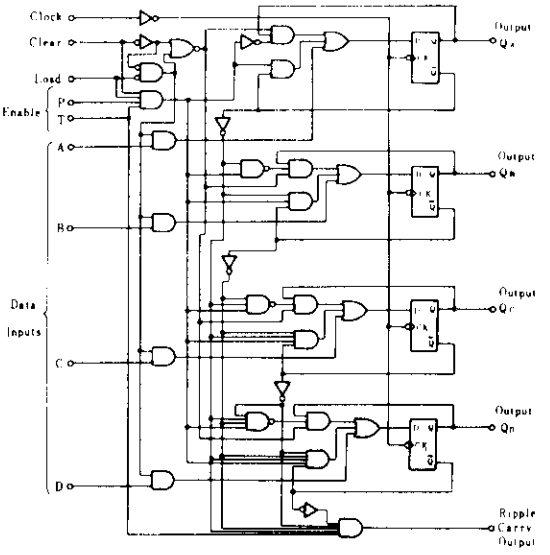
Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the $Q_A$ output.

This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs should occur only when the clock input is high.

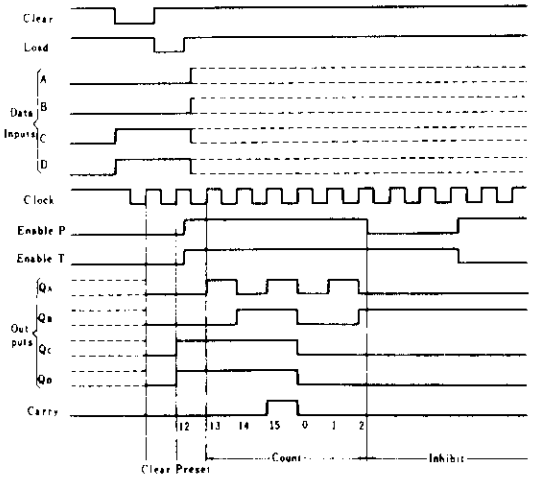
## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■TYPICAL CLEAR, PRESET, AND INHIBIT SEQUENCE



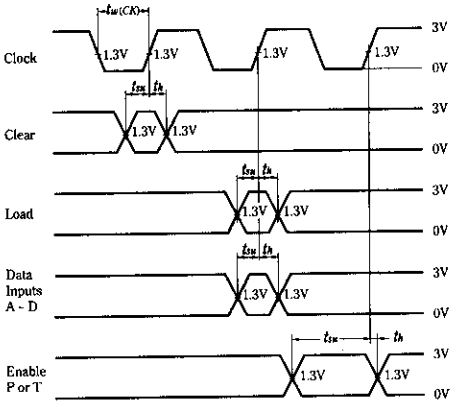

## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | | *fclock* | 0 | – | 25 | MHz |
| Clock pulse width | | *tw (CK)* | 25 | – | – | ns |
| Clear pulse width | | *tw (CLR)* | 20 | – | – | ns |
| Setup time | A, B, C, D | *tsu* | 20 | – | – | ns |
| | Enable P, T | | 20 | – | – | ns |
| | Load | | 20 | – | – | ns |
| | Clear | | 20 | – | – | ns |
| Hold time | | *th* | 3 | – | – | ns |



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## ■TIMING DEFINITION




## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | — | — | 0.4 | V |
| | | | | $I_{OL}=8mA$ | — | — | 0.5 | |
| Input current | Data, Enable P | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | $\mu A$ |
| | Load, Clock, Enable T | | | | — | — | 40 | |
| | Clear | | | | — | — | 40 | |
| | Data, Enable P | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| | Load, Clock, Enable T | | | | — | — | −0.8 | |
| | Clear | | | | — | — | −0.8 | |
| | Data, Enable P | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| | Load, Clock, Enable T | | | | — | — | 0.2 | |
| | Clear | | | | — | — | 0.2 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current** | | $I_{CCH}$ | $V_{CC}=5.25V$ | | — | 18 | 31 | mA |
| | | $I_{CCL}$ | $V_{CC}=5.25V$ | | — | 19 | 32 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** $I_{CCH}$ is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open. $I_{CCL}$ is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

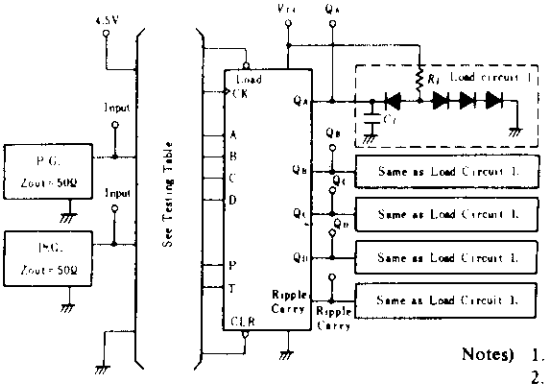
## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | Clock | $Q_A \sim Q_D$ | $C_L=15pF$, $R_L=2k\Omega$ | 25 | 32 | — | MHz |
| Propagation delay time | $t_{PLH}$ | Clock | Ripple Carry | | — | 20 | 35 | ns |
| | $t_{PHL}$ | | | | — | 18 | 35 | ns |
| | $t_{PLH}$ | Clock (Load="H") | $Q_A \sim Q_D$ | | — | 13 | 24 | ns |
| | $t_{PHL}$ | | | | — | 18 | 27 | ns |
| | $t_{PLH}$ | Clock (Load="L") | $Q_A \sim Q_D$ | | — | 13 | 24 | ns |
| | $t_{PHL}$ | | | | — | 18 | 27 | ns |
| | $t_{PLH}$ | Enable T | Ripple Carry | | — | 9 | 14 | ns |
| | $t_{PHL}$ | | | | — | 9 | 14 | ns |
| | $t_{PHL}$ | Clear | $Q_A \sim Q_D$ | | — | 20 | 28 | ns |

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## ■TESTING METHOD

1) Test Circuit



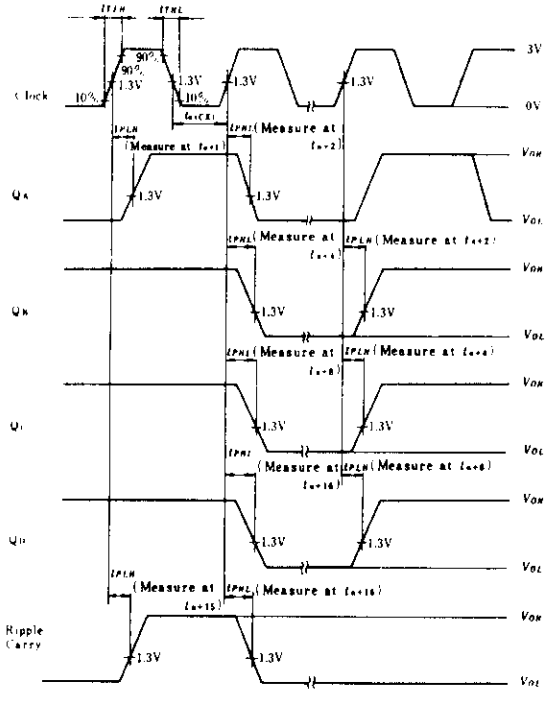

Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

2) Testing Table

| Item | From input to output | Inputs | | | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Clear | Load | Enable P | Enable T | Clock | Data A | Data B | Data C | Data D | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | Ripple Carry |
| $f_{max}$ | | 4.5V | 4.5V | 4.5V | 4.5V | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | OUT |
| $t_{PLH}$ $t_{PHL}$ | CK→Ripple Carry | 4.5V | 4.5V | 4.5V | 4.5V | IN | GND | GND | GND | GND | -- | -- | -- | -- | OUT |
| | CK→Q | 4.5V | 4.5V | 4.5V | 4.5V | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | -- |
| | CK→Q | 4.5V | GND | GND | GND | IN | IN* | IN* | IN* | IN* | OUT | OUT | OUT | OUT | -- |
| | Enable T→Ripple Carry | 4.5V | GND | 4.5V | IN | IN* | 4.5V | 4.5V | 4.5V | 4.5V | -- | -- | -- | -- | OUT |
| | CLR→Q | IN | GND | GND | GND | IN* | 4.5V | 4.5V | 4.5V | 4.5V | OUT | OUT | OUT | OUT | -- |

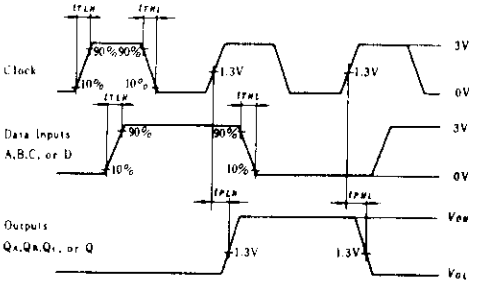
* For initialized

Waveform−1 $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Clock→Q, Ripple Carry)



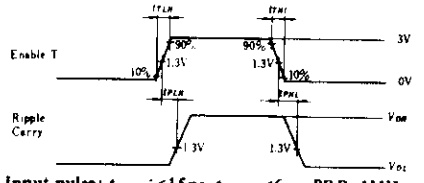

Notes) 1. Clock input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz, duty cycle=50% and: for $f_{max}$, $t_{TLH}$=$t_{THL} \leqq 2.5$ns.
2. $t_n$ is reference bit time when all outputs are low.

Waveform−2 $t_{PLH}$, $t_{PHL}$ (Clock→Q)



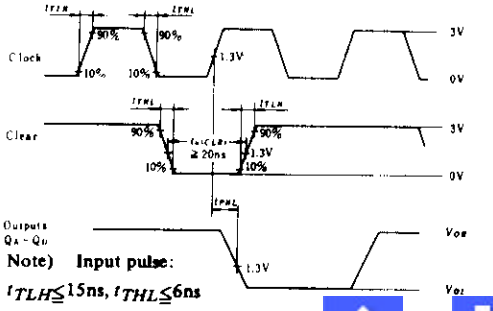

Notes) Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, Clock input: $PRR$= 1MHz, duty cycle 50%, Data input: $PRR$=500kHz, duty cycle 50%

Waveform−3 $t_{PLH}$, $t_{PHL}$ (Enable T→Ripple Carry)




Note) Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz

Waveform−4 $t_{PHL}$ (Clear→Q)




Note) Input pulse:
$t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns

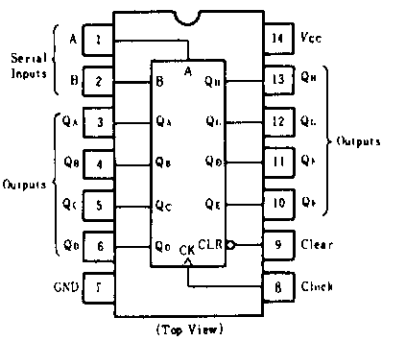


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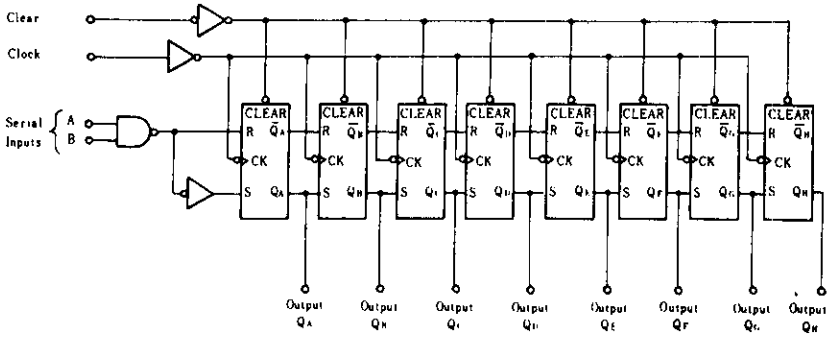
# HD74LS164 ●8-Bit Parallel-Out Serial-In Shift Registers

This 8-bit shift register features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will them determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■FUNCTION TABLE

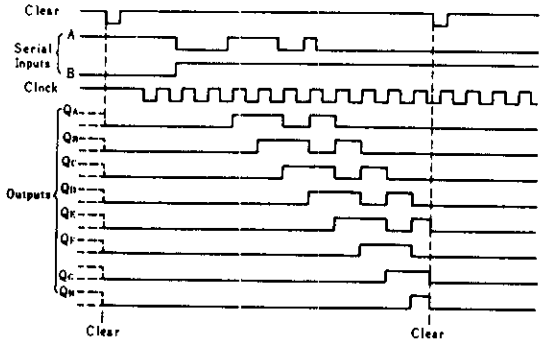
| Inputs | | | | Outputs | | |
|---|---|---|---|---|---|---|
| Clear | Clock | A | B | $Q_A$ | $Q_B$ ····· | $Q_H$ |
| L | × | × | × | L | L | L |
| H | L | × | × | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |
| H | ↑ | H | H | H | $Q_{An}$ | $Q_{Gn}$ |
| H | ↑ | L | × | L | $Q_{An}$ | $Q_{Gn}$ |
| H | ↑ | × | L | L | $Q_{An}$ | $Q_{Gn}$ |

Notes) 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. $Q_{A0}$, $Q_{B0}$, $Q_{H0}$; the level of $Q_A$, $Q_B$, or $Q_H$, respectively, before the indicated steady-state input conditions were established.
4. $Q_{An}$, $Q_{Gn}$; the level of $Q_A$ or $Q_G$ before the most-recent ↑ transition of the clock; indicates a one-bit shift.

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Clock frequency | $f_{clock}$ | 0 | — | 25 | MHz |
| Clock pulse width | $t_{w(CK)}$ | 20 | — | — | ns |
| Clear pulse width | $t_{w(CLR)}$ | 20 | — | — | ns |
| Data setup time | $t_{su}$ | 15 | — | — | ns |
| Data hold time | $t_h$ | 5 | — | — | ns |

## ■TYPICAL CLEAR, SHIFT, AND CLEAR SEQUENCES




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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | | | V |
| | $V_{IL}$ | | | | | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | | | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | | | 0.4 | V |
| | | | $I_{OL}=8mA$ | | | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | | | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | | | -0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | | | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | -20 | | 100 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}=5.25V$ | | | 16 | 27 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | | | -1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

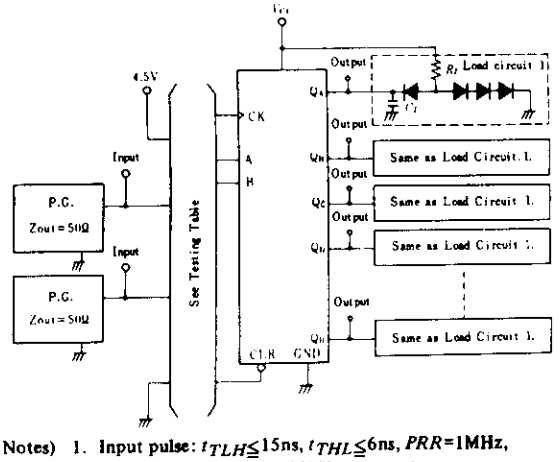
** $I_{CC}$ is measured with outputs open, serial inputs grounded, the clock input at 2.4V, and a momentary grounded, then 4.5V applied to clear.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | | | $C_L=15pF$, $R_L=2k\Omega$ | 25 | 36 | | MHz |
| Propagation delay time | $t_{PHL}$ | Clear | Q | | | 24 | 36 | ns |
| | $t_{PLH}$ | Clock | Q | | | 17 | 27 | ns |
| | $t_{PHL}$ | Clock | Q | | | 21 | 32 | ns |

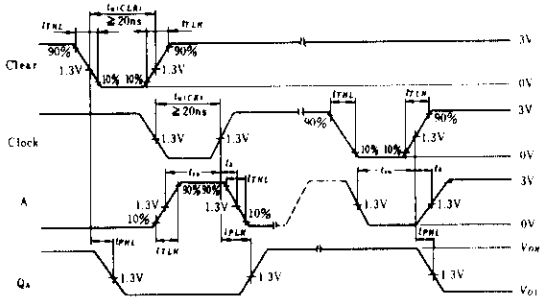
## ■TESTING METHOD

### 1) Test Circuit




Notes) 1. Input pulse: $t_{TLH} \leqq 15ns$, $t_{THL} \leqq 6ns$, $PRR=1MHz$, (Clock, Clear), $PRR=500kHz$ (A or B)
2. $C_L$ includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ

### Waveform




Notes) $Q_A$ output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the timing chart.

### 2) Testing Table

| Item | From input to output | Inputs | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CLR | CK | A | B | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $Q_E$ | $Q_F$ | $Q_G$ | $Q_H$ |
| $f_{max}$ | | 4.5V | IN | IN | 4.5V | OUT | OUT | OUT | OUT | OUT | OUT | OUT | OUT |
| $t_{PLH}$ | Clear→Q | IN | IN | IN | 4.5V | OUT | OUT | OUT | OUT | OUT | OUT | OUT | OUT |
| $t_{PHL}$ | CK → Q | 4.5V | IN | IN | 4.5V | OUT | OUT | OUT | OUT | OUT | OUT | OUT | OUT |



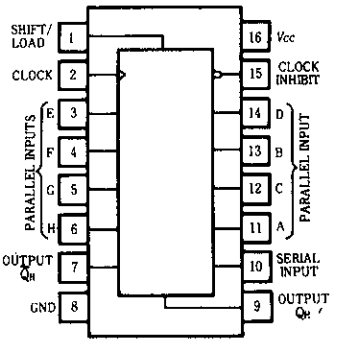
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# HD74LS165A ●Parallel-Load 8-bit Shift Register

The LS165A are 8-bit serial shift registers that shift the data in the direction of $Q_A$ toward $Q_H$ when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

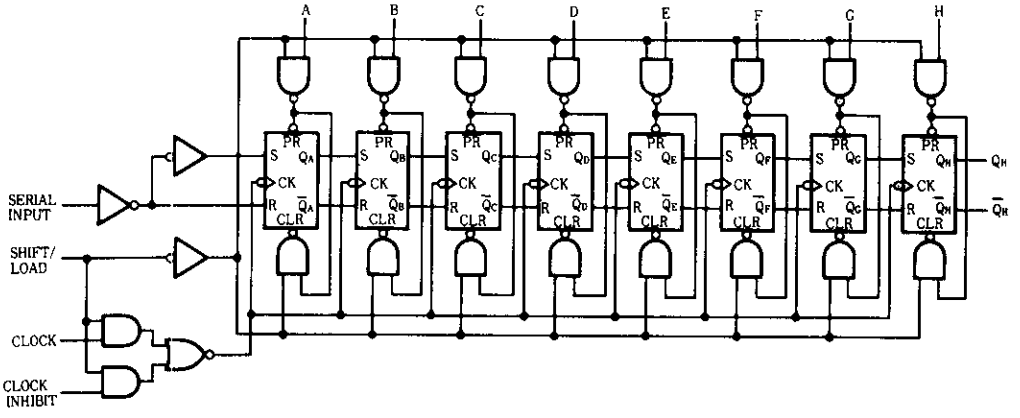
Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift/load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input independently of the levels of the clock, clock inhibit, or serial inputs.

## ■PIN ARRANGEMENT




(Top View)

## ■BLOCK DIAGRAM




## ■FUNCTION TABLE

| INPUTS | | | | | INTERNAL OUTPUTS | | OUTPUT |
|---|---|---|---|---|---|---|---|
| SHIFT/ LOAD | CLOCK INHIBIT | CLOCK | SERIAL | PARALLEL A. . .H | $Q_A$ | $Q_B$ | $Q_H$ |
| L | X | X | X | a. . .h | a | b | h |
| H | L | L | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |
| H | L | ↑ | H | X | H | $Q_{An}$ | $Q_{Gn}$ |
| H | L | ↑ | L | X | L | $Q_{An}$ | $Q_{Gn}$ |
| H | H | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |

Notes) 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. a ~ h; the level of steady-state input at inputs A to H respectively
4. $Q_{A0}$ ~ $Q_{H0}$; the level of $Q_A$ to $Q_H$, respectively, before the indicated steady-state input conditions were established.
5. $Q_{An}$ ~ $Q_{Gn}$; the level of $Q_A$ to $Q_G$, respectively, before the most recent ↓ transition of the clock.

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## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output current | $I_{OH}$ | – | – | −400 | μA |
| Low level output current | $I_{OL}$ | – | – | 8 | mA |
| Clock frequency | $f_{clock}$ | 0 | | 25 | MHz |
| Clock pulse width | $t_w$ (clock) | 25 | – | – | ns |
| Load pulse width | $t_w$ (load) | 15 | – | – | ns |
| Clock-enable Setup time | $t_{su}$ | 30 | – | – | ns |
| Parallel-input Setup time | $t_{su}$ | 10 | – | – | ns |
| Serial input setup time | $t_{su}$ | 20 | – | – | ns |
| Shift setup time | $t_{su}$ | 45 | – | – | ns |
| Hold time at only input | $t_h$ | 0 | – | – | ns |

## ■ELECTRICAL CHARACTERISTICS ($Ta$= −20~ +75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | | V |
| | | $V_{IL}$ | | | | – | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OH}$ = −400μA | | 2.7 | – | – | V |
| | | $V_{OL}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V | $I_{OL}$ = 4mA | | – | 0.4 | V |
| | | | | $I_{OL}$ = 8mA | | | 0.5 | V |
| Input current | Shift/Load | $I_I$ | $V_{CC}$ = 5.25V, $V_I$ = 7V | | – | – | 0.3 | mA |
| | Other inputs | | | | | | 0.1 | mA |
| High level input current | Shift/Load | $I_{IH}$ | $V_{CC}$ = 5.25V, $V_I$ = 2.7V | | – | | 60 | μA |
| | Other inputs | | | | | | 20 | μA |
| Low level input current | Shift/Load | $I_{IL}$ | $V_{CC}$ = 5.25V, $V_I$ = 0.4V | | – | – | −1.2 | mA |
| | Other inputs | | | | – | – | −0.4 | mA |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$ = 5.25V | | −20 | | −100 | mA |
| Supply current** | | $I_{CC}$ | $V_{CC}$ = 5.25V | | – | – | 36 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$ = 4.75V, $I_{IN}$ = −18mA | | – | | −1.5 | V |

* $V_{CC}$ = 5V, $Ta$ = 25°C

** With the outputs open, clock inhibit and clock at 4.5V, and a clock pulse applied to the shift/load, $I_{CC}$ is measured with the parallel inputs at 4.5V, than with the parallel inputs grounded.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

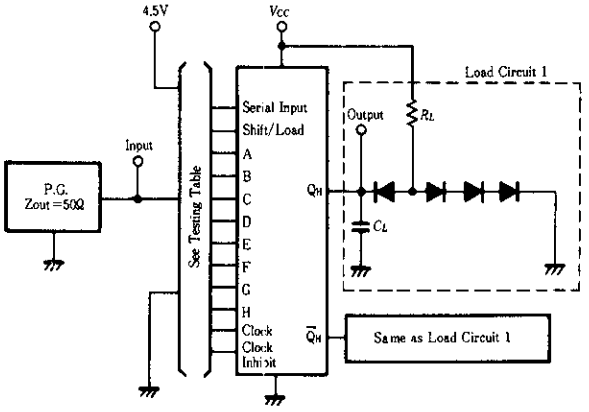
| Item | Symbol | Input | Output | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum Clock frequency | $f_{max}$ | | | $C_L$ = 15pF, $R_L$ = 2kΩ | 25 | 35 | – | MHz |
| Propagation Delay time | $t_{PHL}$ | Load | Any | | – | 21 | 35 | ns |
| | $t_{PLH}$ | | | | – | 26 | 35 | ns |
| | $t_{PHL}$ | Clock | Any | | – | 14 | 25 | ns |
| | $t_{PLH}$ | | | | – | 16 | 25 | ns |
| | $t_{PHL}$ | H | $Q_H$ | | | 13 | 25 | ns |
| | $t_{PLH}$ | | | | – | 24 | 30 | ns |
| | $t_{PLH}$ | H | $Q_H$ | | – | 19 | 30 | ns |
| | $t_{PHL}$ | | | | – | 17 | 25 | ns |



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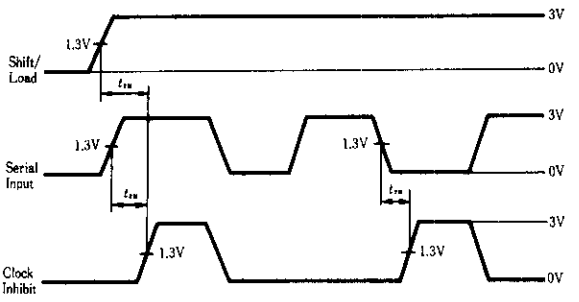
## ■TESTING METHOD

### Test Circuit



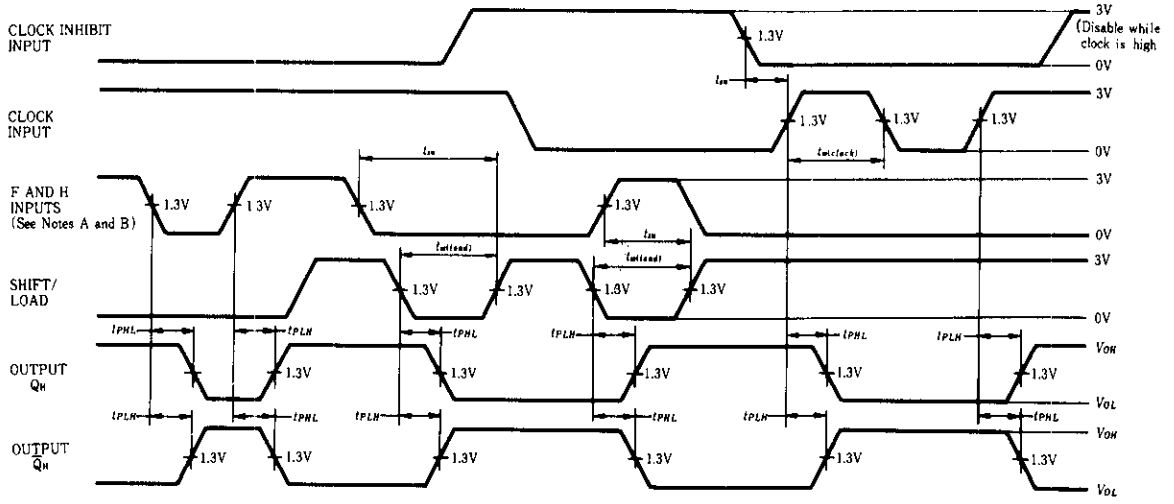

Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

### Waveform




Notes) A. The eight data inputs and the clock-inhibit input are low. Results are monitored at output $Q_H$ at $t_{n+7}$.
B. The input pulse generators have the following characteristics: $PRR < 1$ MHz, duty cycle < 50%, $Z_{out} \approx 50\Omega$, $t_r \leqq 15$ ns, $t_f \leqq 6$ ns.

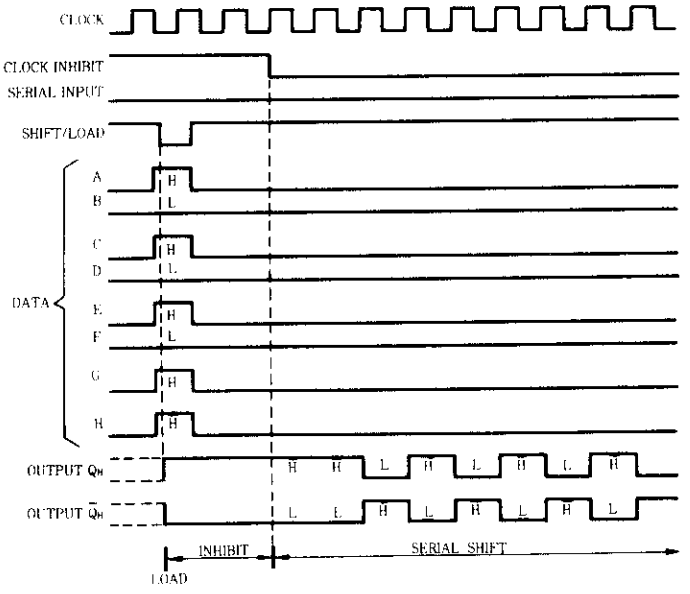
### Waveform




Notes) A. The remaining six data inputs and the serial input are low.
B. Prior to test, high-level data is loaded into H input.
C. The input pulse generators have the following characteristics: $PRR \leqq 1$ MHz, duty cycle $\leqq 50\%$ $Z_{out} \approx 50\Omega$, $t_r \leqq 15$ ns, $t_f \leqq 6$ ns.

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## ■TYPICAL SHIFT, LOAD AND INHIBIT SEQUENCES






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# HD74LS166A ●8-bit Shift Registers

The inputs are buffered to lower the drive requirements to one series 74 or 74LS standard load, respectively. Input clamping diodes minimize switching transients and simplify system design. This parallel-in or serial-in, serial-out shift register has a complexity of 77 equivalent gates on a monolithic chip. This device features gated clock inputs and an overriding clear input.

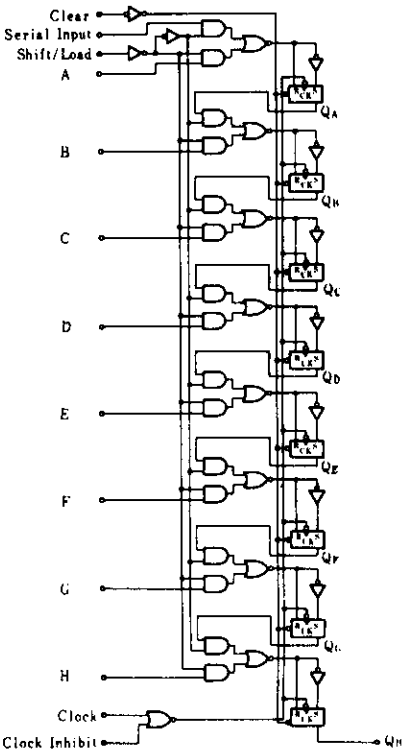
The parallel-in or serial-in modes are established by the shift/load input.

When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited.

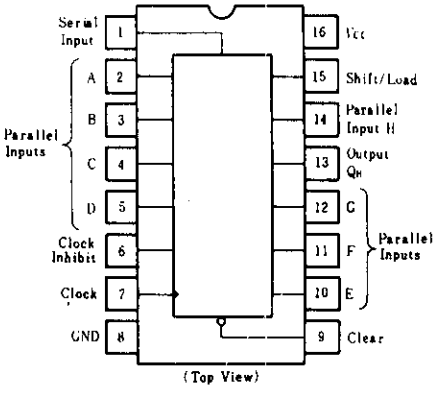
Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input.

This, of course, allows the system clock to be free-running and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overides all other inputs, including the clock, and sets all flip-flops to zero.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT



(Top View)

## ■FUNCTION TABLE

| Inputs | | | | | | Internal Outputs | | Outputs |
|---|---|---|---|---|---|---|---|---|
| Clear | Shift Load | Clock Inhibit | Clock | Serial | Parallel A……H | $Q_A$ | $Q_B$ | $Q_H$ |
| L | X | X | X | X | X | L | L | L |
| H | X | L | L | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |
| H | L | L | ↑ | X | a……h | a | b | h |
| H | H | L | ↑ | H | X | H | $Q_{An}$ | $Q_{Gn}$ |
| H | H | L | ↑ | L | X | L | $Q_{An}$ | $Q_{Gn}$ |
| H | X | H | ↑ | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |

Notes)
1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. ↓; transition from high to low level
4. a~h; the level of steady-state input at inputs A to H respectively
5. $Q_{A0}$~$Q_{H0}$; the level of $Q_A$ to $Q_H$, respectively, before the indicated steady-state input conditions were established.
6. $Q_{An}$~$Q_{Hn}$; the level of $Q_A$ to $Q_H$, respectively, before the most recent ↓ transition of the clock.

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | nom | max | Unit |
|---|---|---|---|---|---|
| High level output current | $I_{OH}$ | – | – | −400 | μA |
| Low level output current | $I_{OL}$ | – | – | 8 | mA |
| Clock frequency | $f_{clock}$ | 0 | – | 25 | MHz |
| Clock and clear pulse width | $t_w$ | 20 | – | – | ns |
| Mode control seup time | $t_{ms}$ | 30 | – | – | ns |
| Data setup time | $t_{ds}$ | 20 | – | – | ns |
| Hold time | $t_h$ | 0 | – | – | ns |

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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | min | typ* | max | Unit |
|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | 2.0 | — | — | V |
| | $V_{IL}$ | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $V_{IH}$ = 0.8V, $I_{OH}$ = −400μA | 2.7 | — | — | V |
| | $V_{OL}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $I_{OL}$ = 4mA | — | — | 0.4 | V |
| | | $V_{IL}$ = 0.8V, $I_{OL}$ = 8mA | — | — | 0.5 | V |
| Input current | $I_{IH}$ | $V_{CC}$ = 5.25V, $V_I$ = 2.7V | — | — | 20 | μA |
| | $I_{IL}$ | $V_{CC}$ = 5.25V, $V_I$ = 0.4V | — | — | −0.4 | mA |
| | $I_I$ | $V_{CC}$ = 5.25V, $V_I$ = 7V | — | — | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$ = 5.25V | −20 | — | −100 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}$ = 5.25V | — | 20 | 32 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$ = 4.75V, $I_{IN}$ = −18mA | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

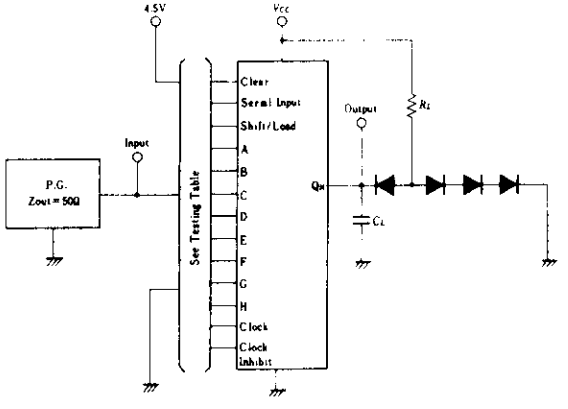
** With all outputs open, 4.5V applied to the serial input and all other inputs except the clock grounded, $I_{CC}$ is measured after a momentary ground, then 4.5V, is applied to clock.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$ = 5V, $Ta$ = 25°C )

| Item | Symbol | Inputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | | $C_L$ = 15pF, $R_L$ = 2kΩ | 25 | 35 | — | MHz |
| Propagation delay time | $t_{PHL}$ | Clear | | — | 19 | 30 | ns |
| | $t_{PHL}$ | Clock | | 7 | 14 | 25 | ns |
| | $t_{PLH}$ | | | 5 | 11 | 20 | ns |

## ■TESTING METHOD

1) Test Circuit

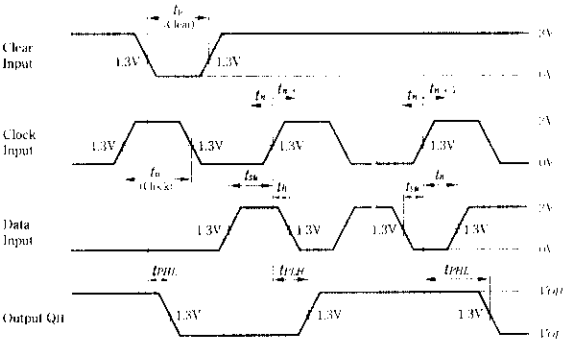



Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

2) Testing Table

| Data inputs | Shift/Load | Output | Bit time |
|---|---|---|---|
| Data H | 0V | $Q_H$ | $t_{n+1}$ |
| Serial-in | 4.5V | $Q_H$ | $t_{n+8}$ |

Waveform

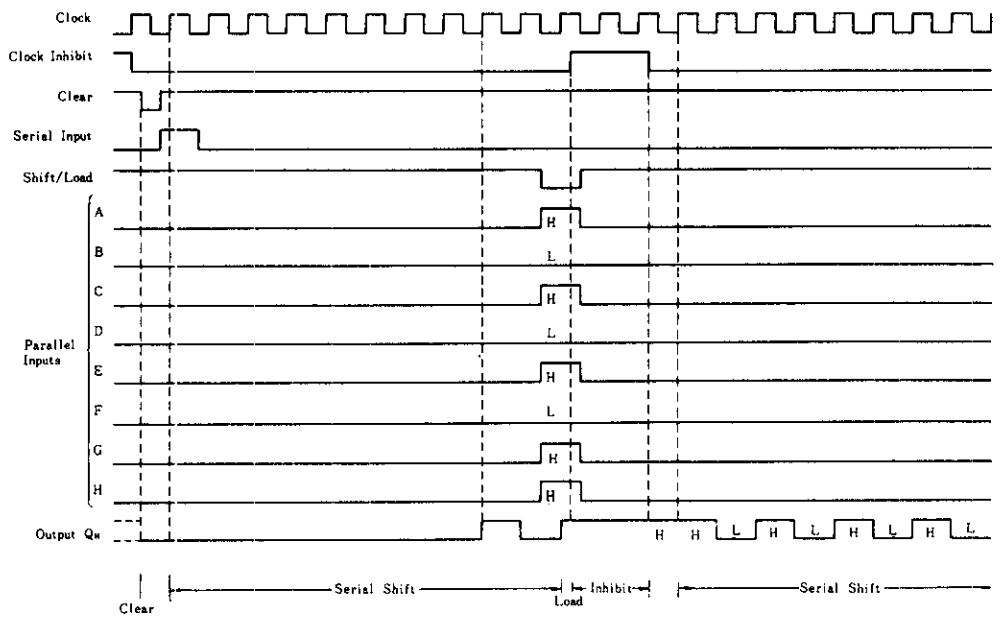



Notes) 1. Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz
duty cycle 50%
Clock input: $t_w \geqq 20$ns
Clear input: $t_w \geqq 20$ns, $t_h$=10ns, when testing $f_{max}$, vary the clock $PRR$.
2. Propagation delay time ($t_{PLH}$ and $t_{PHL}$) are measured at $t_{n+1}$. Proper shifting of data is verified at $t_{n+8}$ with a functional test.
3. $t_n$; bit time before clocking transition.
$t_{n+1}$; bit time after one clocking transition.
$t_{n+8}$; bit time after eight clocking transition.



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## ■TYPICAL CLEAR, SHIFT, LOAD, INHIBIT, AND SHIFT SEQUENCES



# HD74LS170 ●4-by-4 Register File (with open collector outputs)

The HD74LS170 is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

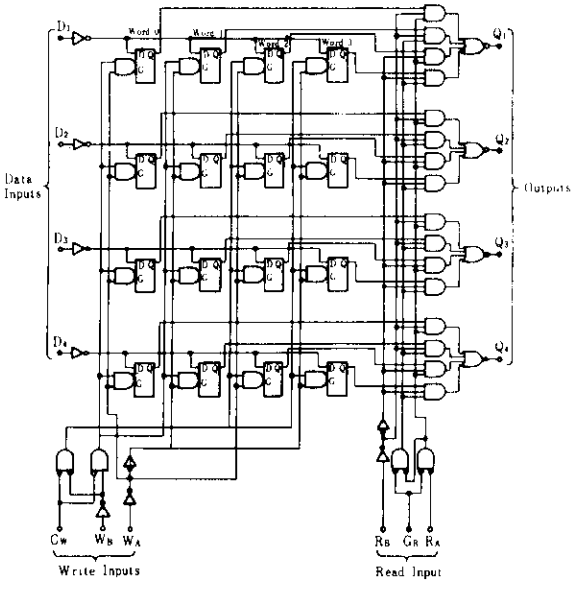
Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal.

Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, $G_W$, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches.

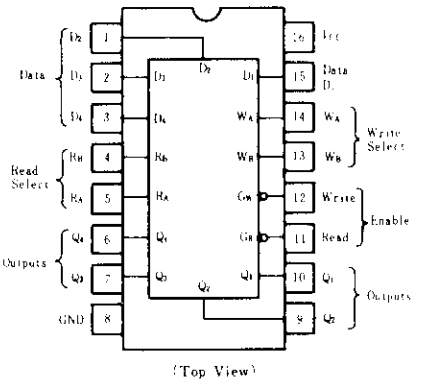
When the read-enable input, $G_R$, is high, the data outputs are inhibited and remain high, the individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word.

When the read address is made in conjunction with the read-enable signal the word appears at the four outputs.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




## ■FUNCTION TABLE

| Write Inputs | | | Word | | | |
|---|---|---|---|---|---|---|
| $W_B$ | $W_A$ | $G_W$ | 0 | 1 | 2 | 3 |
| L | L | L | Q=D | $Q_0$ | $Q_0$ | $Q_0$ |
| L | H | L | $Q_0$ | Q=D | $Q_0$ | $Q_0$ |
| H | L | L | $Q_0$ | $Q_0$ | Q=D | $Q_0$ |
| H | H | L | $Q_0$ | $Q_0$ | $Q_0$ | Q=D |
| × | × | H | $Q_0$ | $Q_0$ | $Q_0$ | $Q_0$ |

| Read Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|
| $W_B$ | $W_A$ | $G_W$ | 0 | 1 | 2 | 3 |
| L | L | L | $W_0B_1$ | $W_0B_2$ | $W_0B_3$ | $W_0B_4$ |
| L | H | L | $W_1B_1$ | $W_1B_2$ | $W_1B_3$ | $W_1B_4$ |
| H | L | L | $W_2B_1$ | $W_2B_2$ | $W_2B_3$ | $W_2B_4$ |
| H | H | L | $W_3B_1$ | $W_3B_2$ | $W_3B_3$ | $W_3B_4$ |
| × | × | H | H | H | H | H |

Notes: H = high level, L = low level, X = irrelevant.
(Q=D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
$Q_0$ = The level of Q before the indicated input conditions were established.
$W_0B_1$ = The first bit of word 0, etc.



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## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | | $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| Output Voltage | | $V_{OH}$ | — | — | 5.5 | V |
| Output Current | | $I_{OL}$ | — | — | 8 | mA |
| Pulse width | Read enable | $t_w$ | 25 | — | — | ns |
| | Write enable | | 60 | — | — | |
| Setup Time | Data input | $t_{su}$ | 10 | — | — | ns |
| | Write select | | 15 | — | — | |
| Hold Time | Data input | $t_h$ | 15 | — | — | ns |
| | Write select | | 5 | — | — | |
| Latch time | | $t_{latch}$ | 60 | — | — | ns |

## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | | Symbol | Test Condition | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input Voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output Current | | $I_{OH}$ | $V_{CC}$=4.75V, $V_{OH}$=5.5V, $V_{IL}$=0.8V, $V_{IH}$=2V | | — | — | 100 | μA |
| Output Voltage | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | — | — | 0.4 | V |
| | | | | $I_{OL}$=8mA | — | — | 0.5 | |
| Input Current | Any D, R or W | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | $G_R$ or Gw | | | | — | — | 40 | |
| | Any D, R or W | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| | $G_R$ or Gw | | | | — | — | −0.8 | |
| | Any D, R or W | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.1 | mA |
| | $G_R$ or Gw | | | | — | — | 0.2 | |
| Supply Current | | $I_{CC}$** | $V_{CC}$=5.25V | | — | 25 | 40 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

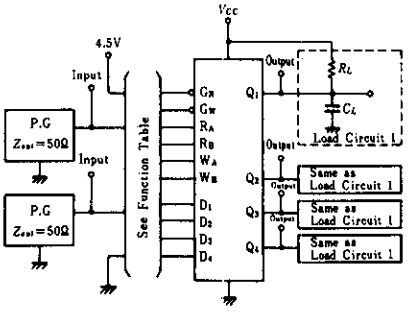
* $V_{CC}$=5V, $Ta$=25°C

** : Typical $I_{CC}$ shown is an average for 50% duty cycle. Maximum $I_{CC}$ is guaranteed for the following worst case conditions: 4.5V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time | $t_{PLH}$ | Read enable | $Q_1$～$Q_4$ | $C_L$=15pF, $R_L$=2kΩ | — | 20 | 30 | ns |
| | $t_{PHL}$ | | | | — | 20 | 30 | |
| | $t_{PLH}$ | Read select | $Q_1$～$Q_4$ | | — | 25 | 40 | |
| | $t_{PHL}$ | | | | — | 24 | 40 | |
| | $t_{PLH}$ | Write enable | $Q_1$～$Q_4$ | | — | 30 | 45 | |
| | $t_{PHL}$ | | | | — | 26 | 40 | |
| | $t_{PLH}$ | Data | $Q_1$～$Q_4$ | | — | 30 | 45 | |
| | $t_{PHL}$ | | | | — | 22 | 30 | |

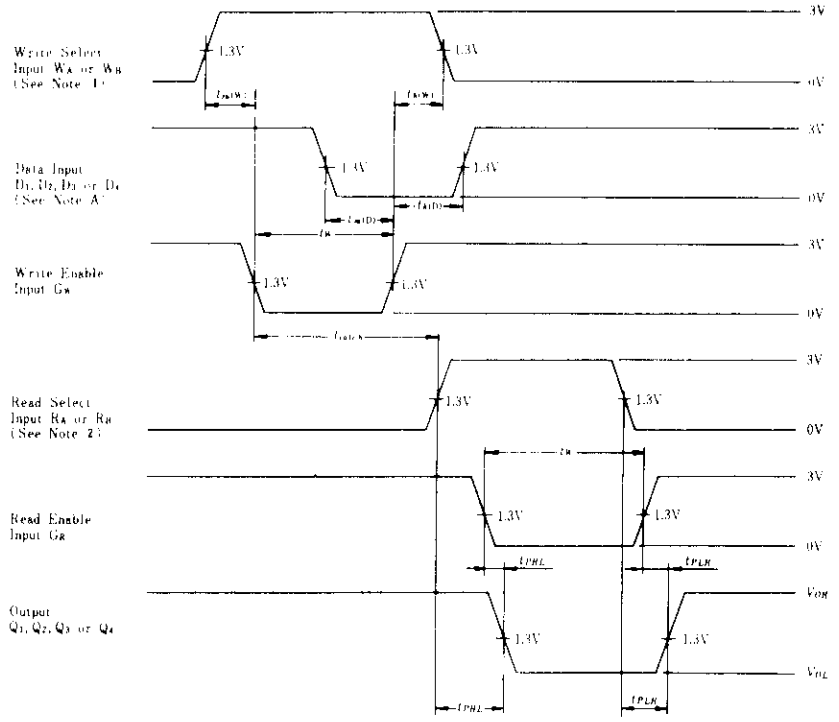
## ■TESTING METHOD




Notes: 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

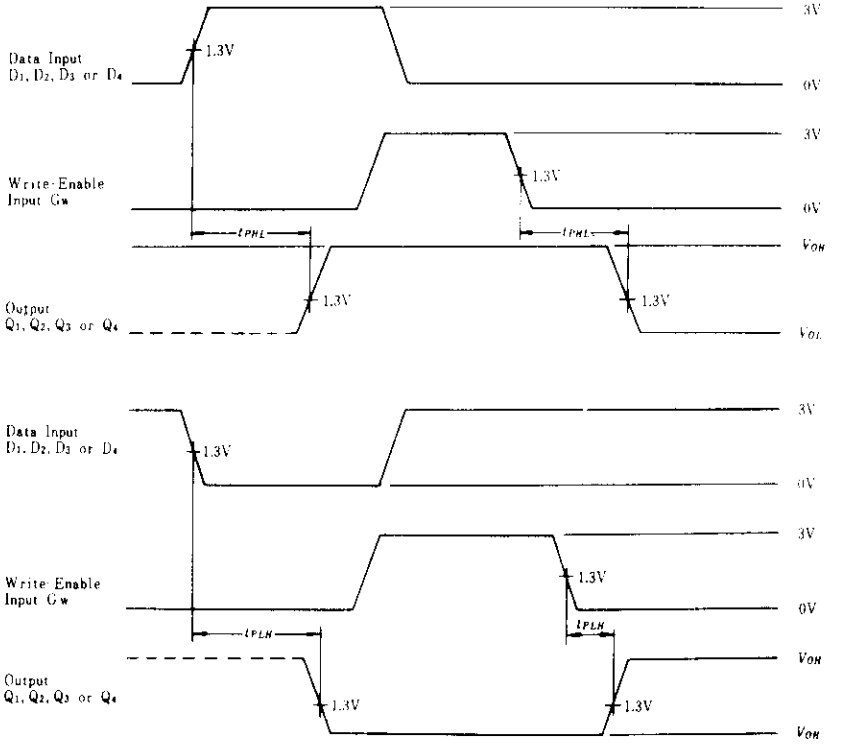
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Waveform-1




Notes:
1. High-level input pulses at the select and data inputs are illustrated in Waveform-1; however, times associated with low-level pulses are measured from the same reference points.
2. When measuring delay times from a read-select input, the read-enable input is low. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.
3. Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR \leqq 1$MHz, duty cycle 50%.

Waveform-2




Note: In Waveform-2, each select address is tested. Prior to the start of each of the above tests, both write and read address inputs are stabilized with $W_A$=$R_A$ and $W_B$=$R_B$. During the test $G_R$ is low.



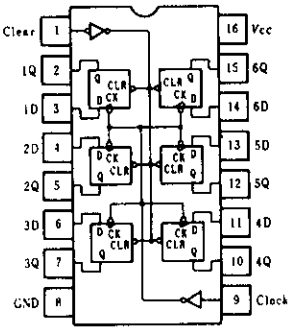
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# HD74LS174/HD74LS175 ●Hex/Quadruple D-type Flip-Flops (with clear)

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the HD74LS175 features complementary outputs from each flip-flops. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the outputs.

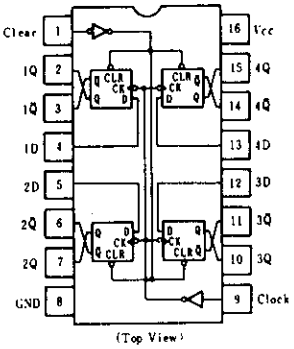
## ■PIN ARRANGEMENT

HD74LS174




(Top View)

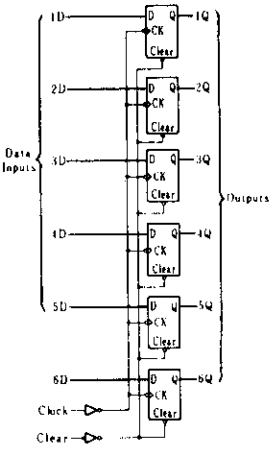
HD74LS175



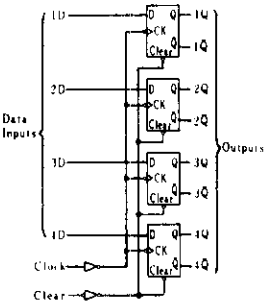

(Top View)

## ■BLOCK DIAGRAM

HD74LS174




HD74LS175




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | max | Unit |
|---|---|---|---|---|---|
| Clock frequency | | $f_{clock}$ | 0 | 30 | MHz |
| Clock pulse width | | $t_{w(CK)}$ | 20 | – | ns |
| Clear pulse width | | $t_{w(CLR)}$ | 20 | – | ns |
| Setup time | Data input | $t_{su(data)}$ | 20 | – | ns |
| | Clear inactive-state | $t_{su(CLR)}$ | 25 | – | ns |
| Data hold time | | $t_{h(data)}$ | 5 | – | ns |

## ■FUNCTION TABLE

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Clear | Clock | D | Q | Q̄ |
| L | × | × | L | H |
| H | ↑ | H | H | L |
| H | ↑ | L | L | H |
| H | L | × | $Q_0$ | $\bar{Q}_0$ |

Notes) 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. $Q_0$; the level of Q before the indicated steady-state input conditions were established.
4. Q̄ is applied to HD74LS175 only.

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=8mA$ | – | – | 0.5 | V |
| | | | $I_{OL}=4mA$ | – | – | 0.4 | |
| Input current | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}=5.25V$ | HD74LS174 | – | 16 | 26 | mA |
| | | | HD74LS175 | – | 11 | 18 | |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** With all outputs open and 4.5V applied to all data and clear inputs, $I_{CC}$ is measured after a momentary grounded, then 4.5V, is applied to clock.

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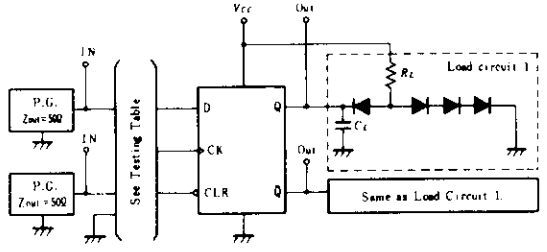
## ■SWITCHING CHARACTERISTICS ( $V_{CC}$ = 5V, $Ta$ = 25°C )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | Clock | Q, $\bar{Q}$* | $C_L$ = 15pF, $R_L$ = 2kΩ | 30 | 40 | – | MHz |
| Propagation delay time | $t_{PLH}$ | Clear | $\bar{Q}$* | | – | 16 | 25 | ns |
| | $t_{PHL}$ | | Q | | – | 23 | 35 | |
| | $t_{PLH}$ | Clock | Q, $\bar{Q}$* | | – | 20 | 30 | |
| | $t_{PHL}$ | Clock | Q, $\bar{Q}$* | | – | 21 | 30 | |

* HD74LS175 only

## ■TESTING METHOD

1) Test Circuit



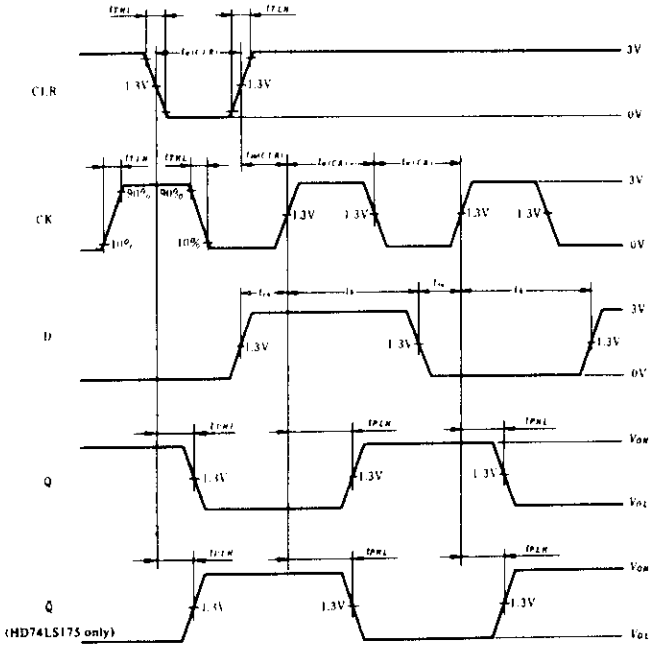

2) Testing Table

| Item | From input to output | Inputs | | | Outputs | |
|---|---|---|---|---|---|---|
| | | CLR | CK | D | Q | $\bar{Q}$* |
| $f_{max}$ | CK→Q, $\bar{Q}$* | 4.5V | IN | IN | OUT | OUT |
| $t_{PLH}$ | CK→Q, $\bar{Q}$* | 4.5V | IN | IN | | |
| $t_{PHL}$ | CLR→Q, $\bar{Q}$* | IN | IN | 4.5V | | |

* HD74LS175 only

Notes) 1. Test is put into the each flip-flop
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

Waveform




Notes) 1. Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz
and: for $f_{max}$, $t_{TLH} = t_{THL} \leqq 2.5$ns.



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# HD74LS181 ●Arithmetic Logic Units/Function Generators

The HD74LS181 is arithmetic logic unit (ALU)/function generator that have a complexity of 75 equivalent gates. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in Function Table (Table 1 and 2).

These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer.

When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M).

A full carry look-ahead scheme is made available in this device for fast, simultaneous carry generation by means of two cascade-outputs (pin 15 and 17) for the four bits in the package. When used in conjunction with the HD74182 or HD74S182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown above illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. If high speed is not of importance, a ripple-carry input ($C_n$) and a ripple-carry output ($C_{n+4}$) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The HD74LS181 will accommodate active-high or active-low data if the pin designations are interpreted as follows.

| Pin No. | 2 | 1 | 23 | 22 | 21 | 20 | 19 | 18 |
|---|---|---|---|---|---|---|---|---|
| Active-high data (Table 1) | $A_0$ | $B_0$ | $A_1$ | $B_1$ | $A_2$ | $B_2$ | $A_3$ | $B_3$ |
| Active-low data (Table 2) | $\bar{A}_0$ | $B_0$ | $\bar{A}_1$ | $B_1$ | $\bar{A}_2$ | $B_2$ | $\bar{A}_3$ | $B_3$ |
| Pin No. | 9 | 10 | 11 | 13 | 7 | 16 | 15 | 17 |
| Active-high data (Table 1) | $F_0$ | $F_1$ | $F_2$ | $F_3$ | $\bar{C}_n$ | $\bar{C}_{n+4}$ | X | Y |
| Active-low data (Table 2) | $F_0$ | $F_1$ | $F_2$ | $F_3$ | $C_n$ | $C_{n+4}$ | P | G |

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-arround or forced carry to provide A-B.

The HD74LS181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, 'F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with Cn=H when performing this comparison. The A=B output is open-collector so that is can be wire-AND connected to give a comparison for more than four bits. The carry output (Cn+4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

| Input Cn | Output $C_{n+4}$ | Active-high data (Table 1) | Active-low data (Table 2) |
|---|---|---|---|
| H | H | A ≦ B | A ≧ B |
| H | L | A > B | A < B |
| L | H | A < B | A > B |
| L | L | A ≧ B | A ≦ B |

This circuit have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Table 1 and 2 and include exclusive-OR, NAND, AND NOR, and OR functions.

● Signal Designations

The HD74LS181 together with the HD74182 and HD74S182 can be used with the signal designations of either Figure 1 or Figure 2. The inversion indicators and the bars over the terminal letter symbols (e.g. $\bar{C}$) each indicate that the associated input or output is active with respect to the selected function of the device when that input or output is low. That is, a low at $\bar{C}$ means "do carry" while a high means "to not carry". The logic functions and arithmetic operations of Figure 2 are given in Table 2.

Figure 1

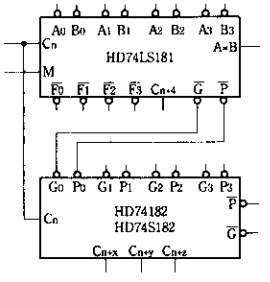
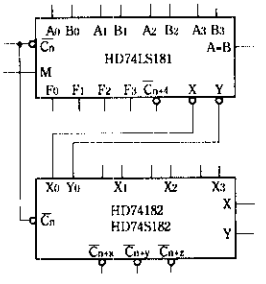



Figure 2




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## ■FUNCTION TABLE

● Table 1

| S Inputs | | | | Active-high data | | |
|---|---|---|---|---|---|---|
| | | | | M = "H" | M = "L" : Arithmetic Operations | |
| $S_3$ | $S_2$ | $S_1$ | $S_0$ | Logic Functions | $\overline{C}_n$ = "H" (no carry) | $\overline{C}_n$ = "L" (with carry) |
| L | L | L | L | $F = \overline{A}$ | F = A | F = A plus 1 |
| L | L | L | H | $F = \overline{A+B}$ | F = A + B | F = (A + B) plus 1 |
| L | L | H | L | $F = \overline{A}B$ | F = A + $\overline{B}$ | F = (A + $\overline{B}$) plus 1 |
| L | L | H | H | F = 0 | F = minus 1 (2's compl) | F = Zero |
| L | H | L | L | $F = \overline{AB}$ | F = A plus A$\overline{B}$ | F = A plus A$\overline{B}$ plus 1 |
| L | H | L | H | $F = \overline{B}$ | F = (A + B) plus A$\overline{B}$ | F = (A + B) plus A$\overline{B}$ plus 1 |
| L | H | H | L | $F = A \oplus B$ | F = A minus B minus 1 | F = A minus B |
| L | H | H | H | F = A$\overline{B}$ | F = A$\overline{B}$ minus 1 | F = A$\overline{B}$ |
| H | L | L | L | $F = \overline{A}+B$ | F = A plus AB | F = A plus AB plus 1 |
| H | L | L | H | $F = \overline{A \oplus B}$ | F = A plus B | F = A plus B plus 1 |
| H | L | H | L | F = B | F = (A + $\overline{B}$) plus AB | F = (A + $\overline{B}$) plus AB plus 1 |
| H | L | H | H | F = AB | F = AB minus 1 | F = AB |
| H | H | L | L | F = 1 | F = A plus A* | F = A plus A plus 1 |
| H | H | L | H | F = A + $\overline{B}$ | F = (A + B) plus A | F = (A + B) plus A plus 1 |
| H | H | H | L | F = A + B | F = (A + $\overline{B}$) plus A | F = (A + $\overline{B}$) plus A plus 1 |
| H | H | H | H | F = A | F = A minus 1 | F = A |

Notes) H; high level, L; low level

* Each bit is shifted to the next more significant position.

● Table 2

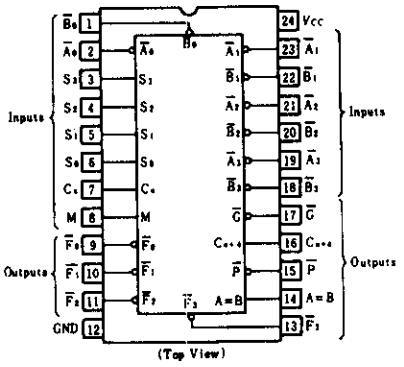
| S Inputs | | | | Active-low data | | |
|---|---|---|---|---|---|---|
| | | | | M = "H" | M = "L" : Arithmetic Operations | |
| $S_3$ | $S_2$ | $S_1$ | $S_0$ | Logic Functions | $C_n$ = "L" (no carry) | $C_n$ = "H" (with carry) |
| L | L | L | L | $F = \overline{A}$ | F = A minus 1 | F = A |
| L | L | L | H | $F = \overline{AB}$ | F = AB minus 1 | F = AB |
| L | L | H | L | $F = \overline{A}+B$ | F = A$\overline{B}$ minus 1 | F = A$\overline{B}$ |
| L | L | H | H | F = 1 | F = minus 1 (2's compl) | F = 0 |
| L | H | L | L | $F = \overline{A+B}$ | F = A plus (A + $\overline{B}$) | F = A plus (A + $\overline{B}$) plus 1 |
| L | H | L | H | $F = \overline{B}$ | F = AB plus (A + $\overline{B}$) | F = AB plus (A + $\overline{B}$) plus 1 |
| L | H | H | L | $F = \overline{A \oplus B}$ | F = A minus B minus 1 | F = A minus B |
| L | H | H | H | F = A + $\overline{B}$ | F = A + $\overline{B}$ | F = (A + $\overline{B}$) plus 1 |
| H | L | L | L | F = $\overline{A}$B | F = A plus (A + B) | F = A plus (A + B) plus 1 |
| H | L | L | H | $F = A \oplus B$ | F = A plus B | F = A plus B plus 1 |
| H | L | H | L | F = B | F = A$\overline{B}$ plus (A + B) | F = A$\overline{B}$ plus (A + B) plus 1 |
| H | L | H | H | F = A + B | F = A + B | F = (A + B) plus 1 |
| H | H | L | L | F = 0 | F = A plus A* | F = A plus A plus 1 |
| H | H | L | H | F = A$\overline{B}$ | F = AB plus A | F = AB plus A plus 1 |
| H | H | H | L | F = AB | F = A$\overline{B}$ plus A | F = A$\overline{B}$ plus A plus 1 |
| H | H | H | H | F = A | F = A | F = A plus 1 |

* Each bit is shifted to the next more significant position.

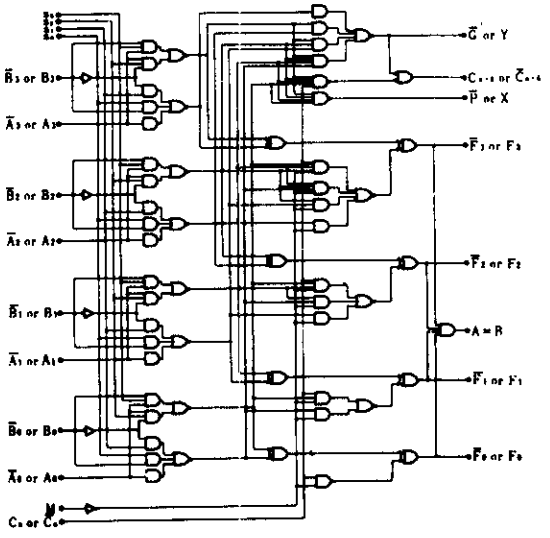


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## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM



## ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7.0 | V |
| Input voltage | $V_{IN}$ | 5.5 | V |
| Operating temperature range | $T_{opr}$ | −20～+75 | ℃ |
| Storage temperature range | $T_{stg}$ | −65～+150 | ℃ |

## ■PIN DESIGNATIONS

| Item | Functions |
|---|---|
| $\overline{A}_3, \overline{A}_2, \overline{A}_1, \overline{A}_0$ | Word A Inputs |
| $\overline{B}_3, \overline{B}_2, \overline{B}_1, \overline{B}_0$ | Word B Inputs |
| $S_3, S_2, S_1, S_0$ | Function-Select Inputs |
| $C_n$ | Ripple-Carry Input |
| M | Mode Control Input |
| $F_3, F_2, F_1, F_0$ | Function Outputs |
| A=B | Comparator Output |
| P | Carry Propagate Output |
| $\overline{C_{n+4}}$ | Ripple-Carry Output |
| G | Carry Generate Output |

## ■ELECTRICAL CHARACTERISTICS ( $Ta$ = −20 ~ +75°C )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output current △ | | $I_{OH}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $V_{OH}$ = 5.5V | | – | – | 100 | μA |
| Output voltage △△ | | $V_{OH}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OH}$ = −400μA | | 2.7 | – | – | V |
| Output voltage | All outputs | $V_{OL}$ | $V_{CC}$ = 4.75V, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V | $I_{OL}$ = 4mA | – | – | 0.4 | V |
| | | | | $I_{OL}$ = 8mA | – | – | 0.5 | |
| | output $\overline{G}$ | | | $I_{OL}$ = 16mA | – | – | 0.7 | |
| Input current | Mode | $I_{IH}$ | $V_{CC}$ = 5.25V, $V_I$ = 2.7V | | – | – | 20 | μA |
| | $\overline{A}$, $\overline{B}$ | | | | – | – | 60 | |
| | S | | | | – | – | 80 | |
| | Carry | | | | – | – | 100 | |
| | Mode | $I_{IL}$ | $V_{CC}$ = 5.25V, $V_I$ = 0.4V | | – | – | −0.4 | mA |
| | $\overline{A}$, $\overline{B}$ | | | | – | – | −1.2 | |
| | S | | | | – | – | −1.6 | |
| | Carry | | | | – | – | −2 | |
| | Mode | $I_I$ | $V_{CC}$ = 5.25V, $V_I$ = 5.5V | | – | – | 0.1 | mA |
| | $\overline{A}$, $\overline{B}$ | | | | – | – | 0.3 | |
| | S | | | | – | – | 0.4 | |
| | Carry | | | | – | – | 0.5 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$ = 5.25V | | −20 | – | −100 | mA |
| Supply current | | $I_{CC}$** | $V_{CC}$ = 5.25V | Condition A | – | 20 | 34 | mA |
| | | | | Condition B | – | 21 | 37 | |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$ = 4.75V, $I_{IN}$ = −18mA | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

△ A=B output only.

△△ any output except A=B.

** With outputs open, $I_{CC}$ is measured for the following conditions:

A. $S_0$ through $S_3$, M, and $\overline{A}$ inputs are at 4.5V, all other inputs are grounded.

B. $S_0$ through $S_3$ and M are at 4.5V, all other inputs are grounded.

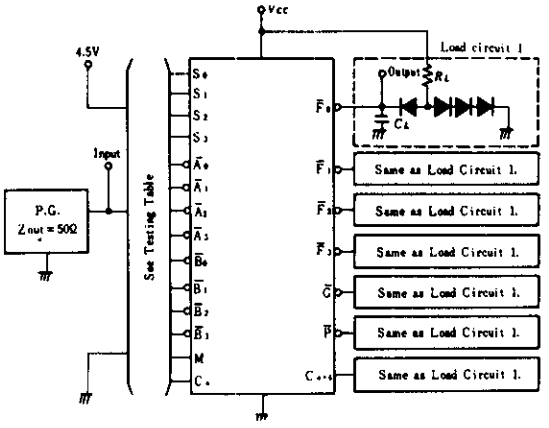
## ■SWITCHING CHARACTERISTICS ( $V_{CC}$ = 5V, $Ta$ = 25°C , $C_L$ = 15pF, $R_L$ = 2kΩ)

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_n$ | $C_{n+4}$ | | – | 18 | 27 | ns |
| | $t_{PHL}$ | | | | – | 13 | 20 | |
| | $t_{PLH}$ | $\overline{A}i$ or $\overline{B}i$ | $C_{n+4}$ | M = 0V, $S_0$ = $S_3$ = 4.5V, $S_1$ = $S_2$ = 0V (SUM mode) | – | 25 | 38 | ns |
| | $t_{PHL}$ | | | | – | 25 | 38 | |
| | $t_{PLH}$ | $\overline{A}i$ or $\overline{B}i$ | $C_{n+4}$ | M = 0V, $S_0$ = $S_3$ = 0V, $S_1$ = $S_2$ = 4.5V (DIFF mode) | – | 27 | 41 | ns |
| | $t_{PHL}$ | | | | – | 27 | 41 | |
| | $t_{PLH}$ | $C_n$ | $A_n$, F | M = 0V (SUM or DIFF mode) | – | 17 | 26 | ns |
| | $t_{PHL}$ | | | | – | 13 | 20 | |
| | $t_{PLH}$ | $\overline{A}i$ or $\overline{B}i$ | $\overline{G}$ | M = 0V, $S_0$ = $S_3$ = 4.5V, $S_1$ = $S_2$ = 0V (SUM mode) | – | 19 | 29 | ns |
| | $t_{PHL}$ | | | | – | 15 | 23 | |
| | $t_{PLH}$ | $\overline{A}i$ or $\overline{B}i$ | $\overline{G}$ | M = 0V, $S_0$ = $S_3$ = 0V, $S_1$ = $S_2$ = 4.5V (DIFF mode) | – | 21 | 32 | ns |
| | $t_{PHL}$ | | | | – | 21 | 32 | |
| | $t_{PLH}$ | $\overline{A}i$ or $\overline{B}i$ | P | M = 0V, $S_0$ = $S_3$ = 4.5V, $S_1$ = $S_2$ = 0V (SUM mode) | – | 20 | 30 | ns |
| | $t_{PHL}$ | | | | – | 20 | 30 | |
| | $t_{PLH}$ | $\overline{A}i$ or $\overline{B}i$ | P | M = 0V, $S_0$ = $S_3$ = 0V, $S_1$ = $S_2$ = 4.5V (DIFF mode) | – | 20 | 30 | ns |
| | $t_{PHL}$ | | | | – | 22 | 33 | |
| | $t_{PLH}$ | $\overline{A}i$ or $\overline{B}i$ | Fi | M = 0V, $S_0$ = $S_3$ = 4.5V, $S_1$ = $S_2$ = 0V (SUM mode) | – | 21 | 32 | ns |
| | $t_{PHL}$ | | | | – | 13 | 20 | |
| | $t_{PLH}$ | $\overline{A}i$ or $\overline{B}i$ | Fi | M = 0V, $S_0$ = $S_3$ = 0V, $S_1$ = $S_2$ = 4.5V (DIFF mode) | – | 21 | 32 | ns |
| | $t_{PHL}$ | | | | – | 21 | 32 | |
| | $t_{PLH}$ | $\overline{A}i$ or $\overline{B}i$ | Fi | M = 4.5V (logic mode) | – | 22 | 33 | ns |
| | $t_{PHL}$ | | | | – | 26 | 38 | |
| | $t_{PLH}$ | $\overline{A}i$ or $\overline{B}i$ | A = B | M = 0V, $S_0$ = $S_3$ = 0V, $S_1$ = $S_2$ = 4.5V (DIFF mode) | – | 33 | 50 | ns |
| | $t_{PHL}$ | | | | – | 41 | 62 | |

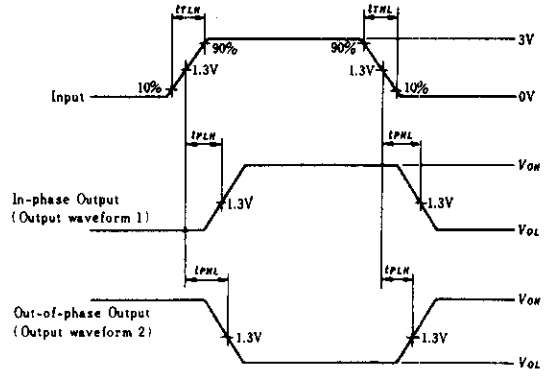


Home Print

## ■TESTING METHOD




Waveform




Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

## SUM Mode Test Table ($S_0=S_3=4.5V, S_1=S_2=M=0V$)

| Item | Test inputs | Other inputs | | Other data inputs | | Test outputs | Output waveform |
|---|---|---|---|---|---|---|---|
| | | 4.5V | GND | 4.5V | GND | | |
| $t_{PLH}$ / $t_{PHL}$ | $\bar{A}_i$ | $B_i$ | – | Remaining $\bar{A}$, B | $C_n$ | $F_i$ | 1 |
| $t_{PLH}$ / $t_{PHL}$ | $B_i$ | $\bar{A}_i$ | – | Remaining $\bar{A}$, B | $C_n$ | $F_i$ | 1 |
| $t_{PLH}$ / $t_{PHL}$ | $\bar{A}_i$ | $B_i$ | – | – | Remaining $\bar{A}$, B, $C_n$ | $\bar{P}$ | 1 |
| $t_{PLH}$ / $t_{PHL}$ | $B_i$ | $\bar{A}_i$ | – | – | Remaining $\bar{A}$, B, $C_n$ | $\bar{P}$ | 1 |
| $t_{PLH}$ / $t_{PHL}$ | $\bar{A}_i$ | – | $B_i$ | Remaining B | Remaining $\bar{A}$, $C_n$ | $\bar{G}$ | 1 |
| $t_{PLH}$ / $t_{PHL}$ | $B_i$ | – | $\bar{A}_i$ | Remaining B | Remaining $\bar{A}$, $C_n$ | $\bar{G}$ | 1 |
| $t_{PLH}$ / $t_{PHL}$ | $C_n$ | – | – | All $\bar{A}$ | All B | F, $C_{n+4}$ | 1 |
| $t_{PLH}$ / $t_{PHL}$ | $\bar{A}_i$ | – | $B_i$ | Remaining B | Remaining $\bar{A}$, $C_n$ | $C_{n+4}$ | 2 |
| $t_{PLH}$ / $t_{PHL}$ | $B_i$ | – | $\bar{A}_i$ | Remaining B | Remaining $\bar{A}$, $C_n$ | $C_{n+4}$ | 2 |

## $\overline{\text{DIFF}}$ Mode Test Table ($S_1=S_2=4.5V$, $S_0=S_3=M=0V$)

| Item | Test inputs | Other inputs | | Other data inputs | | Test outputs | Output waveform |
|---|---|---|---|---|---|---|---|
| | | 4.5V | GND | 4.5V | GND | | |
| $t_{PLH}$ / $t_{PHL}$ | $\bar{A}_i$ | — | $B_i$ | Remaining $\bar{A}$ | Remaining B, $C_n$ | $F_i$ | 1 |
| $t_{PLH}$ / $t_{PHL}$ | $B_i$ | $\bar{A}_i$ | — | Remaining $\bar{A}$ | Remaining B, $C_n$ | $F_i$ | 2 |
| $t_{PLH}$ / $t_{PHL}$ | $\bar{A}_i$ | — | $B_i$ | — | Remaining $\bar{A}$, B, $C_n$ | P | 1 |
| $t_{PLH}$ / $t_{PHL}$ | $B_i$ | $\bar{A}_i$ | — | — | Remaining $\bar{A}$, B, $C_n$ | P | 2 |
| $t_{PLH}$ / $t_{PHL}$ | $\bar{A}_i$ | $B_i$ | — | — | Remaining $\bar{A}$, B, $C_n$ | G | 1 |
| $t_{PLH}$ / $t_{PHL}$ | $B_i$ | — | $\bar{A}_i$ | — | Remaining $\bar{A}$, B, $C_n$ | G | 2 |
| $t_{PLH}$ / $t_{PHL}$ | $\bar{A}_i$ | — | $B_i$ | Remaining $\bar{A}$ | Remaining B, $C_n$ | A=B | 1 |
| $t_{PLH}$ / $t_{PHL}$ | $B_i$ | $\bar{A}_i$ | — | Remaining $\bar{A}$ | Remaining B, $C_n$ | A=B | 2 |
| $t_{PLH}$ / $t_{PHL}$ | $C_n$ | — | — | All $\bar{A}$, B | — | $C_{n+1}$, F | 1 |
| $t_{PLH}$ / $t_{PHL}$ | $\bar{A}_i$ | $B_i$ | — | — | Remaining $\bar{A}$, B, $C_n$ | $C_{n+4}$ | 2 |
| $t_{PLH}$ / $t_{PHL}$ | $B_i$ | — | $\bar{A}_i$ | — | Remaining $\bar{A}$, B, $C_n$ | $C_{n+4}$ | 1 |

## Logic Mode Test Table ($S_1=S_2=M=4.5V$, $S_0=S_3=0V$)

| Item | Test inputs | Other inputs | | Other data inputs | | Test outputs | Output waveform |
|---|---|---|---|---|---|---|---|
| | | 4.5V | GND | 4.5V | GND | | |
| $t_{PLH}$ / $t_{PHL}$ | $\bar{A}_i$ | $B_i$ | — | — | Remaining $\bar{A}$, B, $C_n$ | $F_i$ | 2 |
| $t_{PLH}$ / $t_{PHL}$ | $B_i$ | $\bar{A}_i$ | — | — | Remaining $\bar{A}$, B, $C_n$ | $F_i$ | 2 |



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# HD74LS190 ●Synchronous Up/Down Decade Counters (single clock line)

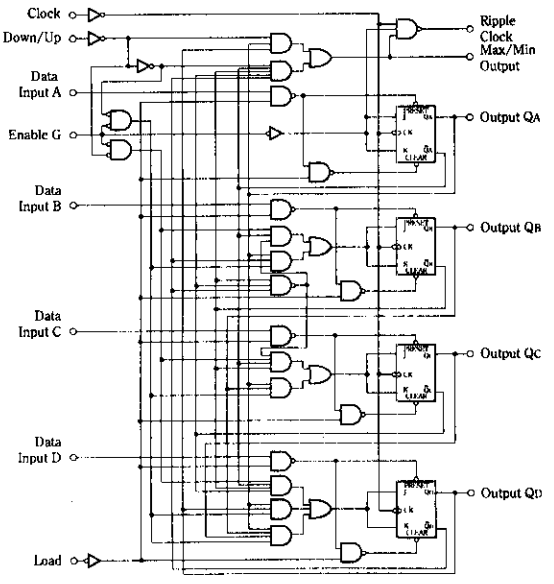
Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down. Level changes at the down/up input should be made only when the clock input is high. This counter is fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs. The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

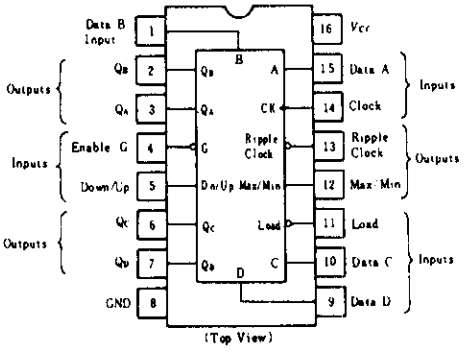
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycles to the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow conditions exists.

The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Clock frequency | $f_{clock}$ | 0 | – | 20 | MHz |
| Clock pulse width | $t_w$ (CK) | 25 | – | – | ns |
| Load input pulse width | $t_w$ (load) | 35 | – | – | ns |
| Setup time | $t_{su}$ | 20 | – | – | ns |
| Hold time | $t_h$ | 3 | – | – | ns |
| Enable time | $t_{enable}$ | 40 | – | – | ns |

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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | — | — | 0.4 | V |
| | | | | $I_{OL}=8mA$ | — | — | 0.5 | |
| Input current | Enable | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 60 | $\mu A$ |
| | Others | | | | — | — | 20 | |
| | Enable | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −1.2 | mA |
| | Others | | | | — | — | −0.4 | |
| | Enable | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.3 | mA |
| | Others | | | | — | — | 0.1 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current** | | $I_{CC}$ | $V_{CC}=5.25V$ | | — | 20 | 35 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

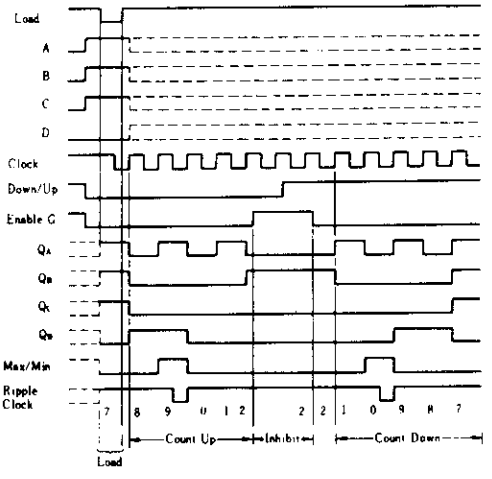
* $V_{CC}$=5V, $Ta$=25°C

** $I_{CC}$ is measured with all outputs open and all inputs grounded.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | Clock | $Q_A$,$Q_B$,$Q_C$,$Q_D$ | $C_L=15pF$ $R_L=2k\Omega$ | 20 | 25 | — | MHz |
| Propagation delay time | $t_{PLH}$ | Load | $Q_A$,$Q_B$,$Q_C$,$Q_D$ | | — | 22 | 33 | ns |
| | $t_{PHL}$ | | | | — | 33 | 50 | |
| | $t_{PLH}$ | A, B, C, D | $Q_A$,$Q_B$,$Q_C$,$Q_D$ | | — | 20 | 32 | ns |
| | $t_{PHL}$ | | | | — | 27 | 40 | |
| | $t_{PLH}$ | Clock | Ripple Clock | | — | 13 | 20 | ns |
| | $t_{PHL}$ | | | | — | 16 | 24 | |
| | $t_{PLH}$ | Clock | $Q_A$,$Q_B$,$Q_C$,$Q_D$ | | — | 16 | 24 | ns |
| | $t_{PHL}$ | | | | — | 24 | 36 | |
| | $t_{PLH}$ | Clock | Max/Min | | — | 28 | 42 | ns |
| | $t_{PHL}$ | | | | — | 37 | 52 | |
| | $t_{PLH}$ | Down/Up | Ripple Clock | | — | 30 | 45 | ns |
| | $t_{PHL}$ | | | | — | 30 | 45 | |
| | $t_{PLH}$ | Down/Up | Max/Min | | — | 21 | 33 | ns |
| | $t_{PHL}$ | | | | — | 22 | 33 | |
| | $t_{PLH}$ | Enable | Ripple Clock | | — | 21 | 33 | ns |
| | $t_{PHL}$ | | | | — | 22 | 33 | |

## ■COUNT SEQUENCES




Illustrated below is the following sequence:

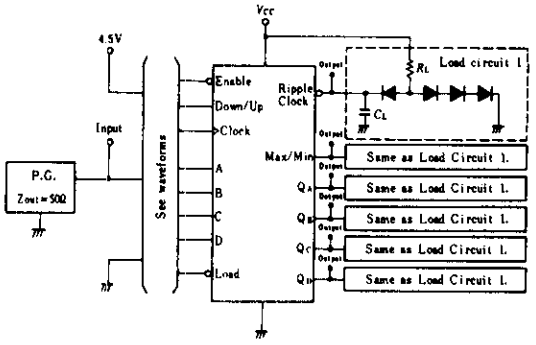
1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one and two.
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven.



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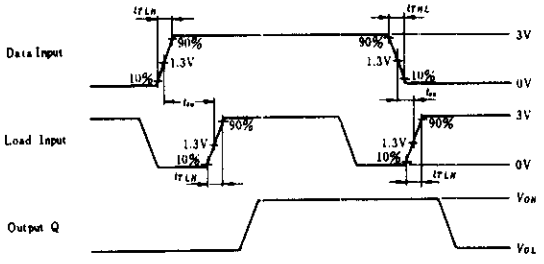
## ■TESTING METHOD

1) Test Circuit



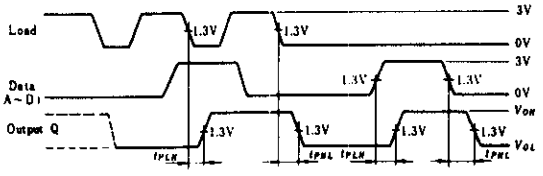

Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 (H).

Waveform



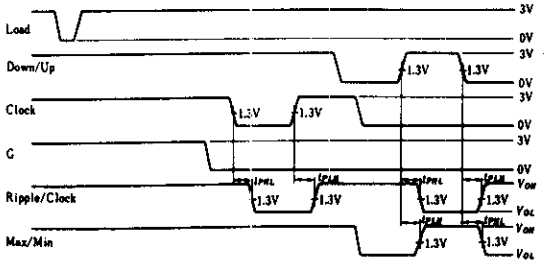

Input pulse: $t_{TLH}$, $t_{THL} \leqq 10$ns, $PRR = 1$MHz, Duty cycle $\leqq 50\%$

Waveform 1. Load→Q, Data→Q



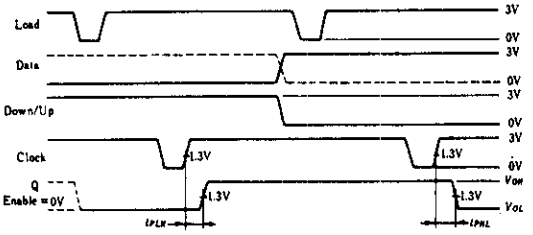

Note) Conditions on other inputs are irrelevant

Waveform 2. G→Ripple CK, CK→Ripple CK, Down/UP→Ripple CK, Down/Up→Max/Min



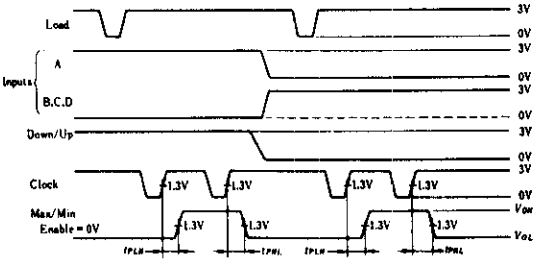

Note) All data inputs are low

Waveform 3. Clock→Q




Notes) 1. When test the $Q_A$, $Q_B$, and $Q_C$ outputs, data inputs A, B and C are shown by the solid line, and data input D is shown by the dashed line.
2. When test the $Q_D$ output, data inputs A and D are shown by the solid line, and data inputs B and C are held at the low logic level.

Waveform 4. Clock→Max/Min




Note) Data inputs B and C are shown by the dashed line. Data input D is shown by the solid line.

Home Print

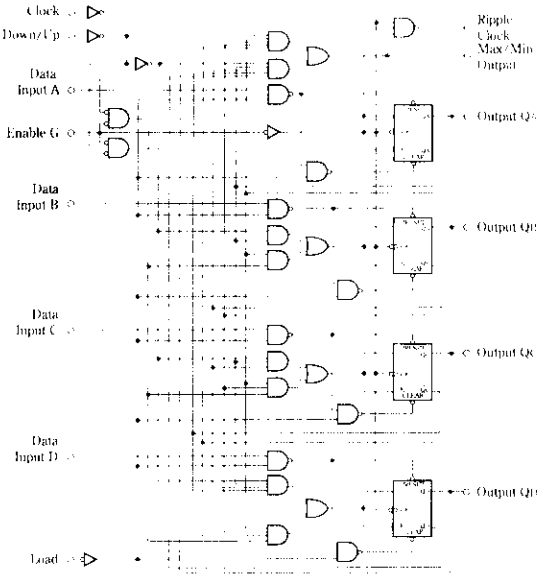
Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down. Level changes at the down/up input should be made only when the clock input is high. This counter is fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs. The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

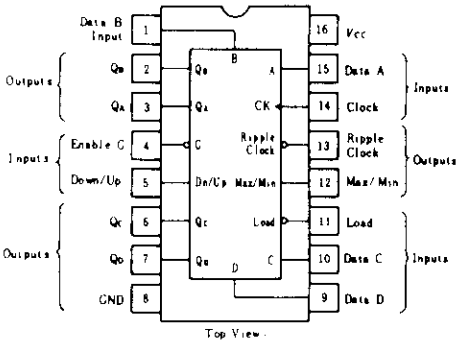
Two outputs have been made available to perform the cascading function; ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycles to the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists.

The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Clock frequency | $f_{clock}$ | 0 | – | 20 | MHz |
| Clock pulse width | $t_w$ (CK) | 25 | – | – | ns |
| Load input pulse width | $t_w$ (load) | 35 | – | | ns |
| Setup time | $t_{su}$ | 20 | | – | ns |
| Hold time | $t_h$ | 3 | – | | ns |
| Enable time | $t_{enable}$ | 40 | – | | ns |



Home Print

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V, I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | | $V_{OL}$ | $V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | Enable | $I_{IH}$ | $V_{CC}=5.25V, V_I=2.7V$ | | – | – | 60 | $\mu A$ |
| | Others | | | | – | – | 20 | |
| | Enable | $I_{IL}$ | $V_{CC}=5.25V, V_I=0.4V$ | | – | – | −1.2 | mA |
| | Others | | | | – | – | −0.4 | |
| | Enable | $I_I$ | $V_{CC}=5.25V, V_I=7V$ | | – | – | 0.3 | mA |
| | Others | | | | – | – | 0.1 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current** | | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 20 | 35 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V, I_{IN}=-18mA$ | | – | – | −1.5 | V |

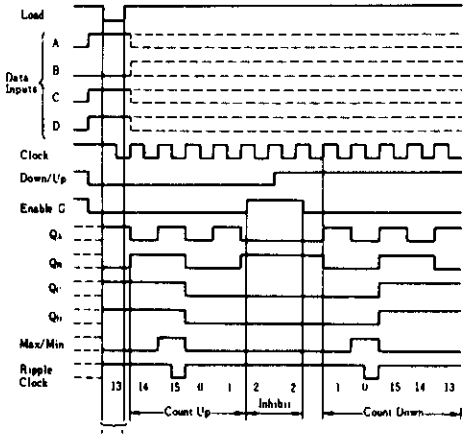
* $V_{CC}$=5V, $Ta$=25°C

** $I_{CC}$ is measured with all outputs open and all inputs grounded.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | | | $C_L=15pF$ $R_L=2k\Omega$ | 20 | 25 | – | MHz |
| Propagation delay time | $t_{PLH}$ | Load | $Q_A, Q_B, Q_C, Q_D$ | | – | 22 | 33 | ns |
| | $t_{PHL}$ | | | | – | 33 | 50 | |
| | $t_{PLH}$ | Data A ,B,C,D | $Q_A, Q_B, Q_C, Q_D$ | | – | 20 | 32 | ns |
| | $t_{PHL}$ | | | | – | 27 | 40 | |
| | $t_{PLH}$ | Clock | Ripple Clock | | – | 13 | 20 | ns |
| | $t_{PHL}$ | | | | – | 16 | 24 | |
| | $t_{PLH}$ | Clock | $Q_A, Q_B, Q_C, Q_D$ | | – | 16 | 24 | ns |
| | $t_{PHL}$ | | | | – | 24 | 36 | |
| | $t_{PLH}$ | Clock | Max/Min | | – | 28 | 42 | ns |
| | $t_{PHL}$ | | | | – | 37 | 52 | |
| | $t_{PLH}$ | Down/Up | Ripple Clock | | – | 30 | 45 | ns |
| | $t_{PHL}$ | | | | – | 30 | 45 | |
| | $t_{PLH}$ | Down/Up | Max/Min | | – | 21 | 33 | ns |
| | $t_{PHL}$ | | | | – | 22 | 33 | |
| | $t_{PLH}$ | Enable | Ripple Clock | | – | 21 | 33 | ns |
| | $t_{PHL}$ | | | | – | 22 | 33 | |

## ■COUNT SEQUENCES

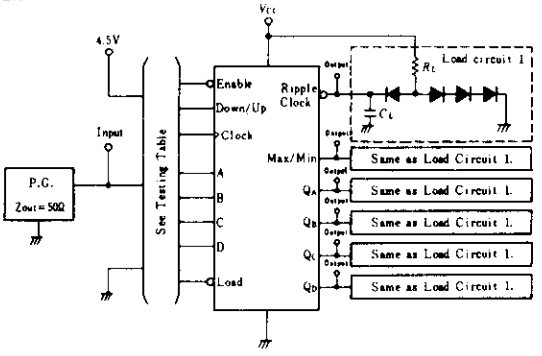



Illustrated below is the following sequence;

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.

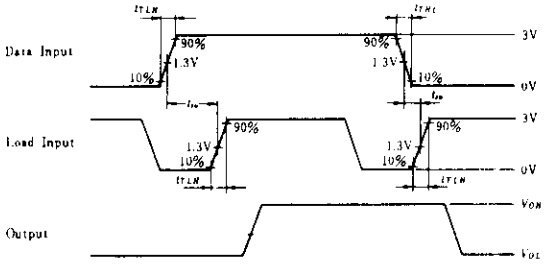
## ■TESTING METHOD

1) Test Circuit



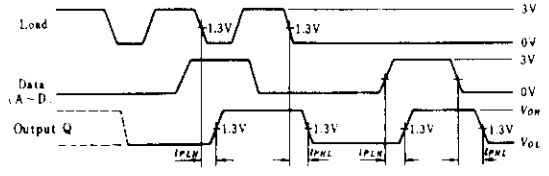

Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

Waveform



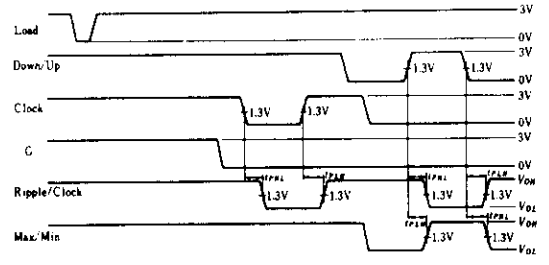

Input pulse: $t_{TLH}$, $t_{THL} \leqq 10$ns, $PRR = 1$MHz, Duty cycle $\leqq 50\%$

Waveform 1. Load→Q, Data→Q

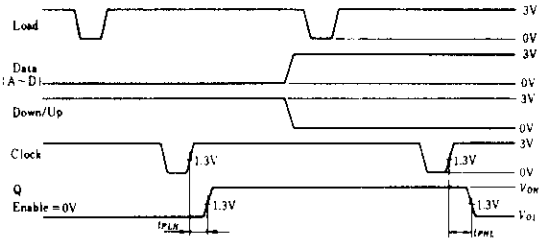



Note) Conditions on other inputs are irrelevant.

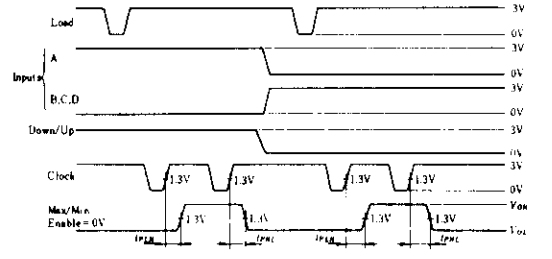
Waveform 2. G→Ripple CK, CK→Ripple CK, Down/Up→Ripple CK, Down/Up→Max/Min




Waveform 3. Clock→Q




Waveform 4. Clock→Max/Min






Home Print

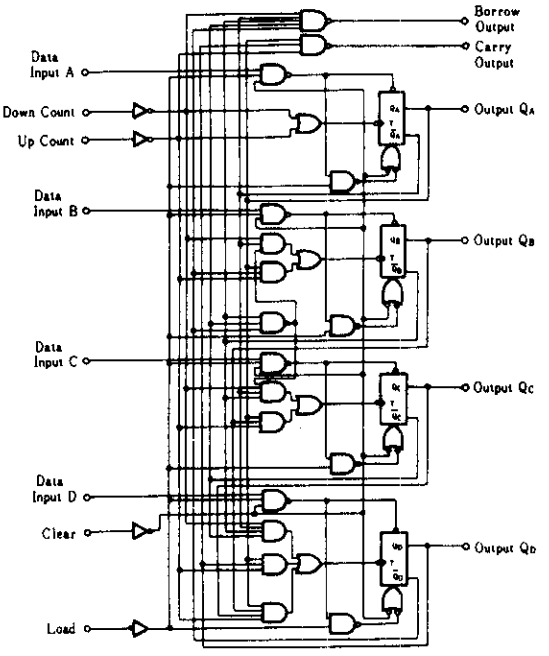
# HD74LS192 ●Synchronous Up/Down Decade Counters (dual clock lines)

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters. The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high. This counter is fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs. A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words. This counter was designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up-and down-counting functions.

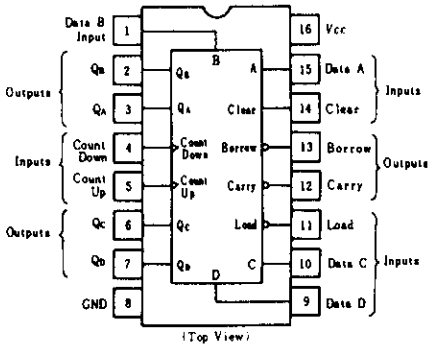
The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists.

The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Clock frequency | $f_{clock}$ | 0 | – | 25 | MHz |
| Pulse width | $t_w$ | 20 | – | – | ns |
| Setup time (Clear) | $t_{su(CLR)}$ | 40 | – | – | ns |
| Setup time | $t_{su}$ | 20 | – | – | ns |
| Hold time | $t_h$ | 3 | – | – | ns |

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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | — | — | 0.4 | V |
| | | | $I_{OL}=8mA$ | — | — | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}=5.25V$ | | — | 19 | 34 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

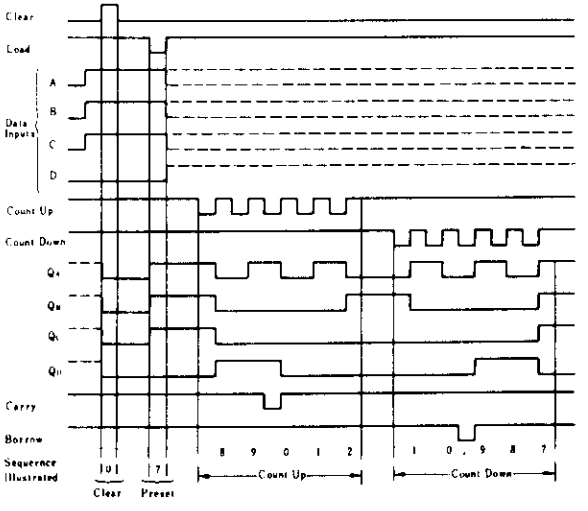
* $V_{CC}$=5V, $Ta$=25°C

** $I_{CC}$ is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5V.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | | | $C_L=15pF$ $R_L=2k\Omega$ | 25 | 32 | — | MHz |
| Propagation delay time | $t_{PLH}$ | Count-up | Carry | | — | 17 | 26 | ns |
| | $t_{PHL}$ | | | | — | 18 | 24 | |
| | $t_{PLH}$ | Count-down | Borrow | | — | 16 | 24 | ns |
| | $t_{PHL}$ | | | | — | 15 | 24 | |
| | $t_{PLH}$ | Either Count | Q | | — | 27 | 38 | ns |
| | $t_{PHL}$ | | | | — | 30 | 47 | |
| | $t_{PLH}$ | Load | Q | | — | 24 | 40 | ns |
| | $t_{PHL}$ | | | | — | 25 | 40 | |
| | $t_{PHL}$ | Clear | Q | | — | 23 | 35 | ns |

## ■COUNT SEQUENCE

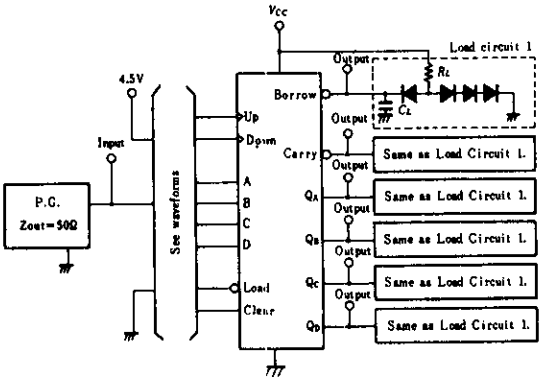





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## ■TESTING METHOD

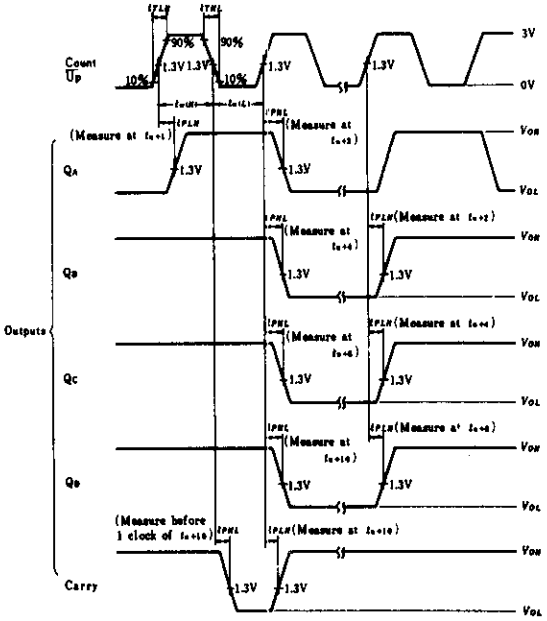
### 1) Test Circuit




Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

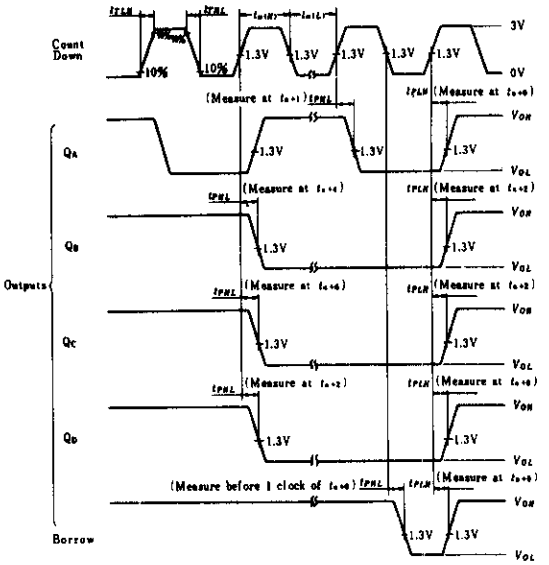
Input pulse: $t_{TLH}, t_{THL} \leqq 7$ns, $PRR$=500kHz (Data input).
$PRR$=1MHz (except data input)
Duty Cycle=50%

### Waveform−1 $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Count Up)



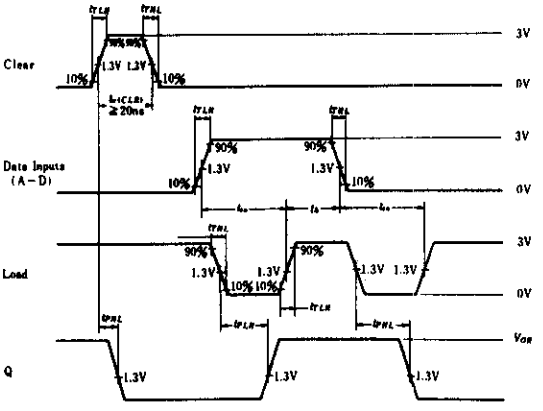

Notes) 1. Input pulse: $t_{TLH} \leqq 7$ns, $t_{THL} \leqq 7$ns, $PRR$=1MHz, duty cycle 50%
2. for $f_{max}$, $t_{TLH}$, $t_{THL} \leqq 2.5$ns
3. $t_n$ is reference bit time when all outputs are low.

### Waveform−2 $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Count Down)




Notes) 1. for $f_{max}$, $t_{TLH}$=$t_{THL} \leqq 2.5$ns.
2. $t_n$ is reference bit time when all outputs are high.

### Waveform−3 $t_{PLH}$, $t_{PHL}$ (Load, Clear→Q)




Note) Input pulse: $t_{TLH} \leqq 7$ns, $t_{THL} \leqq 7$ns

### 2) Testing Table

| Item | From input to output | Inputs | | | | | | | | Outputs | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CLR | Load | Up | Down | A | B | C | D | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | Carry | Borrow |
| $f_{max}$ | | GND | 4.5V | IN | 4.5V | GND | GND | GND | GND | OUT | OUT | OUT | OUT | OUT | — |
| | | GND | 4.5V | 4.5V | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | — | OUT |
| $t_{PLH}$ $t_{PHL}$ | Up Count | GND | 4.5V | IN | 4.5V | GND | GND | GND | GND | OUT | OUT | OUT | OUT | OUT | — |
| | Down Count | GND | 4.5V | 4.5V | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | — | OUT |
| | Load→Q | GND | IN | GND | GND | IN | IN | IN | IN | OUT | OUT | OUT | OUT | — | — |
| | Clear→Q | IN | IN* | GND | GND | 4.5V | 4.5V | 4.5V | 4.5V | OUT | OUT | OUT | OUT | — | — |

* for initialized

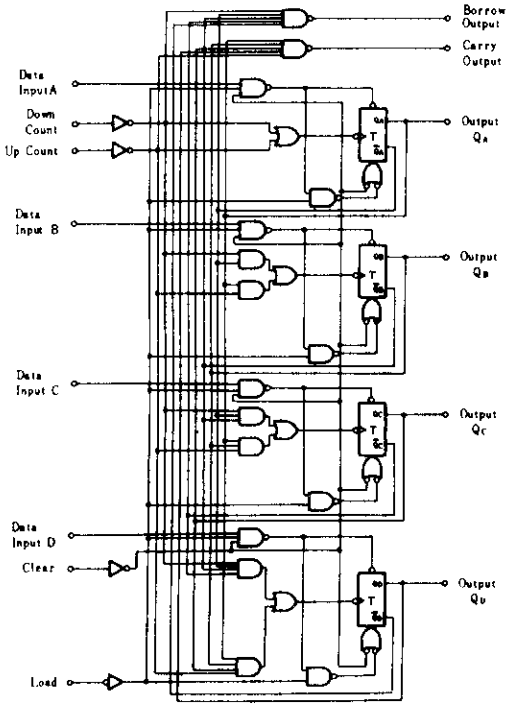
Home Print

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters. The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high. This counter is fully programmable; That is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs. A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words. This counter was designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up-and down-counting functions.

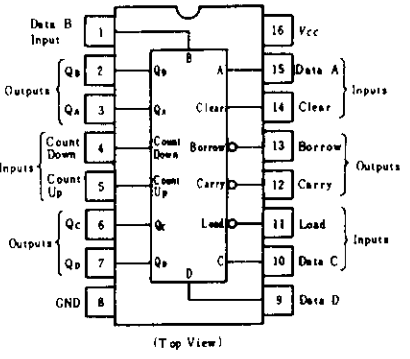
The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists.

The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT



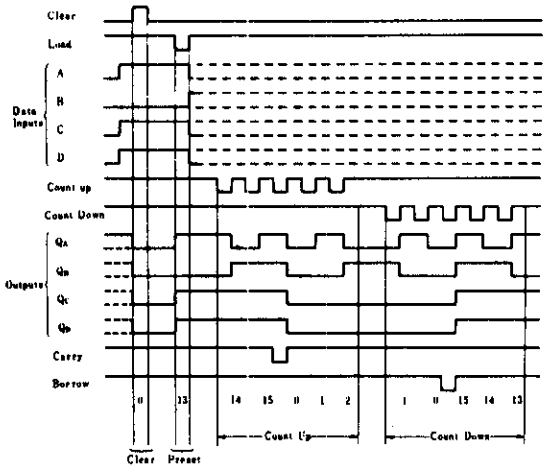

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Clock frequency | $f_{clock}$ | 0 | — | 25 | MHz |
| Pulse width | $t_w$ | 20 | — | — | ns |
| Setup time (Clear) | $t_{su(clear)}$ | 40 | — | — | ns |
| Setup time | $t_{su}$ | 20 | — | — | ns |
| Hold time | $t_h$ | 3 | — | — | ns |



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## ■COUNT SEQUENCES




Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

## ■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 19 | 34 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C
** $I_{CC}$ is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5V.

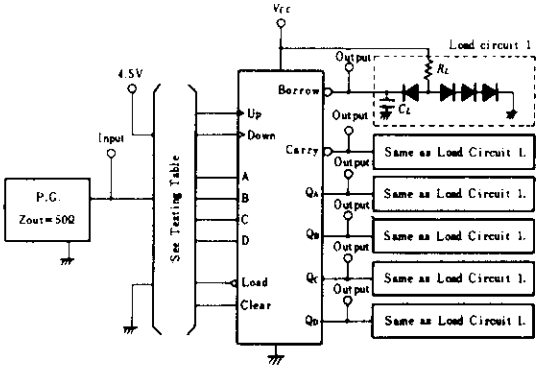
## ■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | | | $C_L=15pF$, $R_L=2k\Omega$ | 25 | 32 | – | MHz |
| Propagation delay time | $t_{PLH}$ | Count-up | Carry | | – | 17 | 26 | ns |
| | $t_{PHL}$ | | | | – | 18 | 24 | ns |
| | $t_{PLH}$ | Count-down | Borrow | | – | 16 | 24 | ns |
| | $t_{PHL}$ | | | | – | 15 | 24 | ns |
| | $t_{PLH}$ | Either Count | Q | | – | 27 | 38 | ns |
| | $t_{PHL}$ | | | | – | 30 | 47 | ns |
| | $t_{PLH}$ | Load | Q | | – | 24 | 40 | ns |
| | $t_{PHL}$ | | | | – | 25 | 40 | ns |
| | $t_{PHL}$ | Clear | Q | | – | 23 | 35 | ns |

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## ■TESTING METHOD

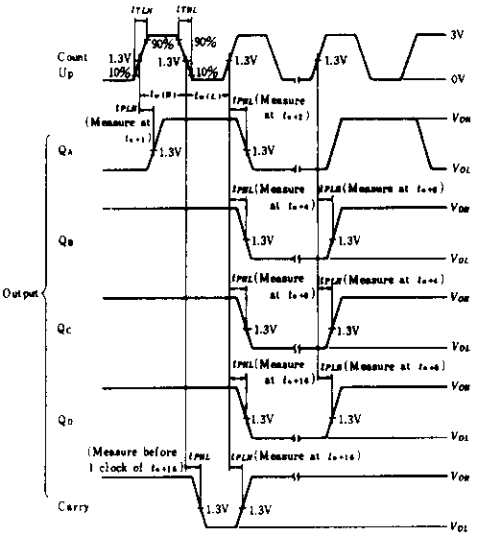
1) Test Circuit




Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ

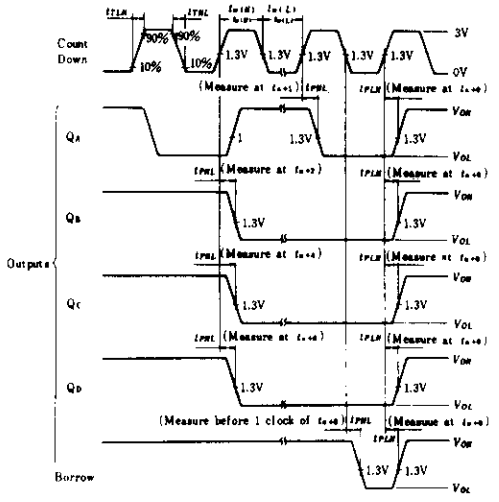
Input pulse: $t_{TLH}, t_{THL} \leqq 7$ns
Duty Cycle $\leqq$ 50%, $PRR$=500kHz (Data input)
$PRR$=1MHz (except data input)

Waveform−1 $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Count Up)



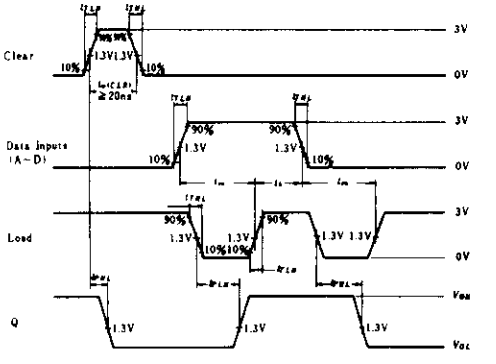

Notes) 1. for $f_{max}$, $t_{TLH}=t_{THL} \leqq 2.5$ns.
2. $t_n$ is reference bit time when all outputs are low.

Waveform−2 $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Count Down)




Notes) 1. Input pulse: $t_{TLH} \leqq 7$ns, $t_{THL} \leqq 7$ns, $PRR$=1MHz, duty cycle 50%
2. for $f_{max}$, $t_{TLH}, t_{THL} \leqq 2.5$ns
3. $t_n$ is reference bit time when all outputs are high.

Waveform−3 $t_{PLH}$, $t_{PHL}$ (Load, Clear→Q)




Note) Input pulse: $t_{TLH} \leqq 7$ns, $t_{THL} \leqq 7$ns

2) Testing Table

| Item | From input to output | Inputs | | | | | | | | Outputs | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CLR | Load | Up | Down | A | B | C | D | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | Carry | Borrow |
| $f_{max}$ | Up Count | GND | 4.5V | IN | 4.5V | GND | GND | GND | GND | OUT | OUT | OUT | OUT | OUT | – |
| | Down Count | GND | 4.5V | 4.5V | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | – | OUT |
| $t_{PLH}$ | Up Count | GND | 4.5V | IN | 4.5V | GND | GND | GND | GND | OUT | OUT | OUT | OUT | OUT | – |
| | Down Count | GND | 4.5V | 4.5V | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | – | OUT |
| $t_{PHL}$ | Load→Q | GND | IN | GND | GND | IN | IN | IN | IN | OUT | OUT | OUT | OUT | – | – |
| | Clear→Q | IN | IN* | GND | GND | 4.5V | 4.5V | 4.5V | 4.5V | OUT | OUT | OUT | OUT | – | – |

* for initialized



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# HD74LS194A ●4-bit Bidirectional Universal Shift Registers

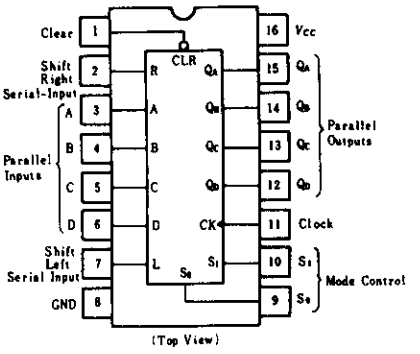
This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs. Operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction $Q_A$ toward $Q_D$)
Shift left (in direction $Q_D$ toward $Q_A$)
Inhibit clock (do nothing)

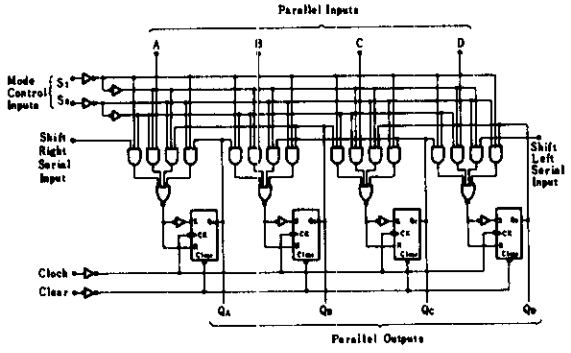
Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low.

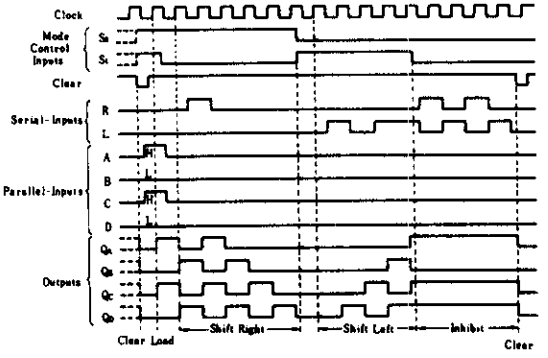
## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■COUNT SEQUENCE




## ■FUNCTION TABLE

| Inputs | | | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CLEAR | MODE | | CLOCK | SERIAL | | PARALLEL | | | | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| | $S_1$ | $S_0$ | | LEFT | RIGHT | A | B | C | D | | | | |
| L | × | × | × | × | × | × | × | × | × | L | L | L | L |
| H | × | × | L | × | × | × | × | × | × | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| H | H | H | ↑ | × | × | a | b | c | d | a | b | c | d |
| H | L | H | ↑ | × | H | × | × | × | × | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| H | L | H | ↑ | × | L | × | × | × | × | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| H | H | L | ↑ | H | × | × | × | × | × | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | H |
| H | H | L | ↑ | L | × | × | × | × | × | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | L |
| H | L | L | × | × | × | × | × | × | × | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |

Notes) 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. ↓; transition from high to low level
4. a~d; the level of steady-state input at inputs A,B,C, or D, respectively
5. $Q_{A0}$~$Q_{D0}$; the level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the indicated steady-state input conditions were established.
6. $Q_{An}$~$Q_{Dn}$; the level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the most-recent ↑ transition of the clock.

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## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | | $f_{clock}$ | 0 | – | 25 | MHz |
| Clock pulse width | | $t_{w(CK)}$ | 20 | – | – | ns |
| Clear pulse width | | $t_{w(CLR)}$ | 20 | – | – | ns |
| Setup time | Mode Control | $t_{su}$ | 30 | – | – | ns |
| | A, B, C, D, R, L | | 20 | – | – | ns |
| | CLR (inactive state) | | 25 | – | – | ns |
| Hold time | | $t_h$ | 0 | – | – | ns |

## ■ELECTRICAL CHARACTERISTICS ( $Ta=-20\sim+75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | $V_{IL}=0.8V$ | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 15 | 23 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

** With all outputs open, inputs A through D grounded, and 4.5V applied to $S_0$, $S_1$, clear, and the serial inputs, $I_{CC}$ is tested with a momentary GND, then 4.5V, applied to clock.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

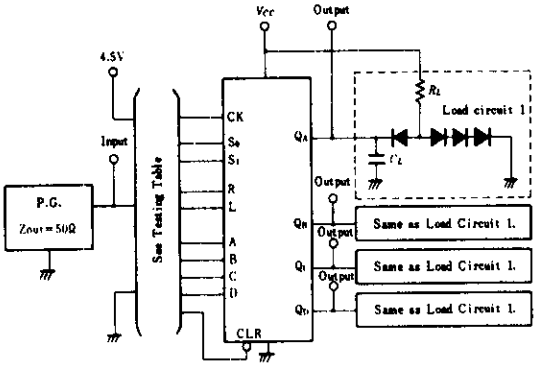
| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | | | | 25 | 36 | – | MHz |
| Propagation delay time | $t_{PHL}$ | Clear | Q | $C_L=15pF$ | – | 19 | 30 | ns |
| | $t_{PLH}$ | Clock | | $R_L=2k\Omega$ | – | 14 | 22 | ns |
| | $t_{PHL}$ | Clock | | | – | 17 | 26 | ns |



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## ■TESTING METHOD

1) Test Circuit

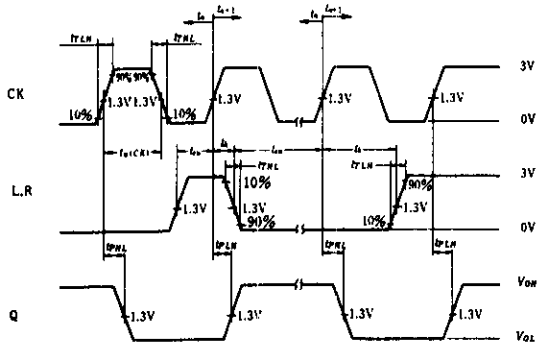



Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

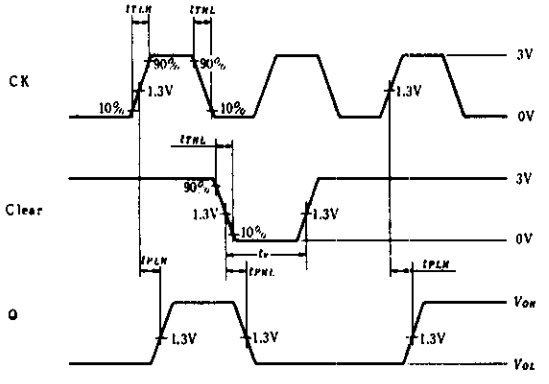
2) Testing Table

| Item | From input to output | Inputs | | | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CLR | $S_1$ | $S_0$ | CK | L | R | A | B | C | D | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| $f_{max}$ | right-shift | 4.5V | 4.5V | GND | IN | 4.5V | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT |
| | left-shift | 4.5V | GND | 4.5V | IN | IN | 4.5V | GND | GND | GND | GND | OUT | OUT | OUT | OUT |
| $t_{PHL}$ | Clear→Q | IN | 4.5V | 4.5V | IN | GND | GND | 4.5V | 4.5V | 4.5V | 4.5V | OUT | OUT | OUT | OUT |
| $t_{PHL}$ $t_{PLH}$ | Clock→Q | 4.5V | 4.5V | GND | IN | 4.5V | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT |
| | | 4.5V | 4.5V | GND | IN | IN | 4.5V | GND | GND | GND | GND | OUT | OUT | OUT | OUT |

Waveform−1 ($f_{max}$, CK→Q)




Waveform−2 (Clear→Q)




Notes) 1. Right-shift is measured with $Q_A$ at $t_{n+1}$, $Q_B$ at $t_{n+2}$, $Q_C$ at $t_{n+3}$, and $Q_D$ at $t_{n+4}$. Left-shift is measured with $Q_A$ at $t_{n+4}$, $Q_B$ at $t_{n+3}$, $Q_C$ at $t_{n+2}$, and $Q_D$ at $t_{n+1}$.

Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns

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# HD74LS195A● 4-bit Parallel-Access Shift Registers

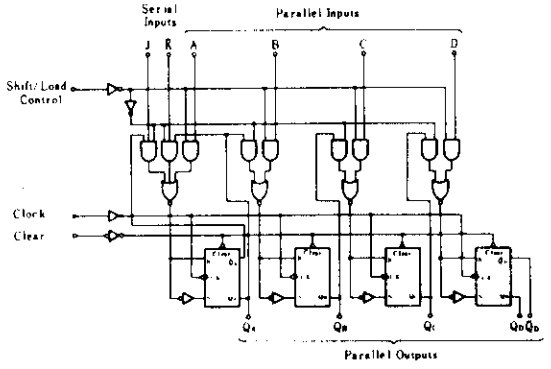
This 4-bit register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load

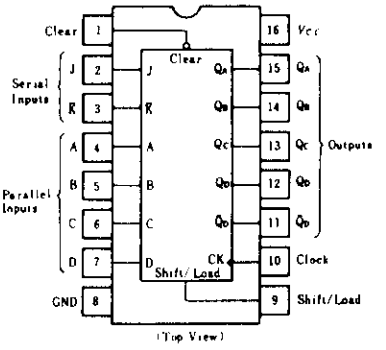
Shift (in the direction $Q_A$ toward $Q_D$)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | | $f_{clock}$ | 0 | – | 30 | MHz |
| Clock pulse width | | $t_{w(CK)}$ | 16 | – | – | ns |
| Clear pulse width | | $t_{w(CLR)}$ | 12 | – | – | ns |
| Setup time | Shift/load | $t_{su}$ | 25 | – | – | ns |
| | Seiral and parallel data | | 15 | – | – | |
| | Clear inactive-state | | 25 | – | – | |
| Release time | | $t_{release}$ | – | – | 5 | ns |
| Hold time | | $t_h$ | 0 | – | – | ns |

## ■FUNCTION TABLE

| Inputs | | | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear | Shift/Load | Clock | Serial | | Parallel | | | | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $\overline{Q}_D$ |
| | | | J | $\overline{K}$ | A | B | C | D | | | | | |
| L | × | × | × | × | × | × | × | × | L | L | L | L | H |
| H | L | ↑ | × | × | a | b | c | d | a | b | c | d | $\overline{d}$ |
| H | H | L | × | × | × | × | × | × | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $\overline{Q}_{D0}$ |
| H | H | ↑ | L | H | × | × | × | × | $Q_{A0}$ | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |
| H | H | ↑ | L | L | × | × | × | × | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |
| H | H | ↑ | H | H | × | × | × | × | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |
| H | H | ↑ | H | L | × | × | × | × | $\overline{Q}_{An}$ | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |

Notes) 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. ↓; transition from high to low level
4. a~d; the level of steady-state input at inputs A,B,C, or D, respectively
5. $Q_{A0}$~$Q_{D0}$; the level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the indicated steady-state input conditions were established.
6. $Q_{An}$~$Q_{Dn}$; the level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the most-recent ↑ transition of the clock.



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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 14 | 21 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

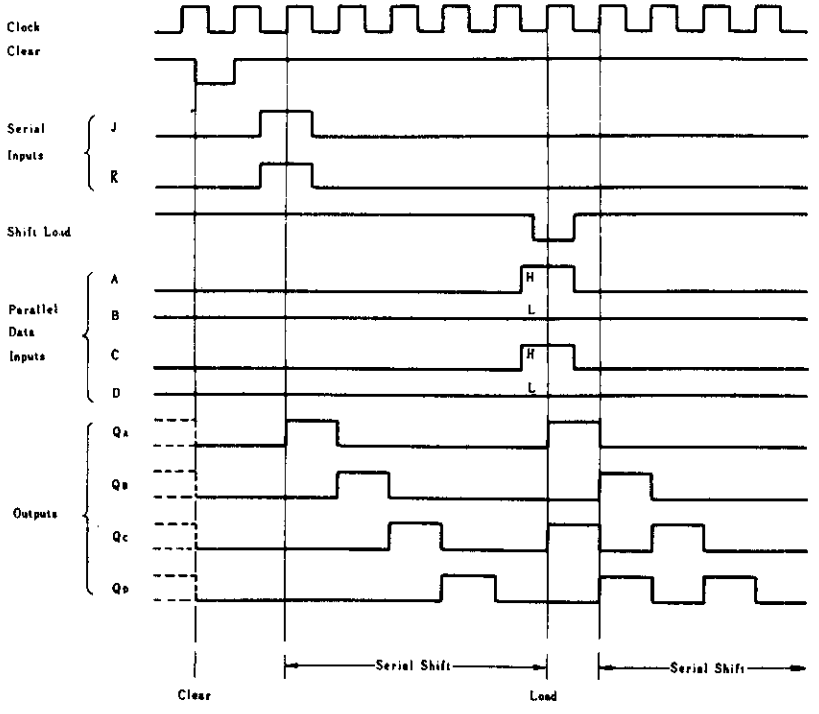
* $V_{CC}=5V$, $Ta=25°C$

** With all outputs open, shift/load grounded, and 4.5V applied to the J, $\overline{K}$, and data inputs, $I_{CC}$ is measured by applying a momentary ground, followed by 4.5V, to clear and then applying a momentary ground, followed by 4.5V, to clock.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | Clock | $Q_A \sim Q_D$ | $C_L=15pF$, $R_L=2k\Omega$ | 30 | 39 | – | MHz |
| Propagation delay time | $t_{PHL}$ | Clear | $Q_A \sim Q_D$ | | – | 19 | 30 | ns |
| | $t_{PLH}$ | Clock | $Q_A \sim Q_D$, $\overline{Q}_D$ | | – | 14 | 22 | ns |
| | $t_{PHL}$ | | | | – | 17 | 26 | ns |

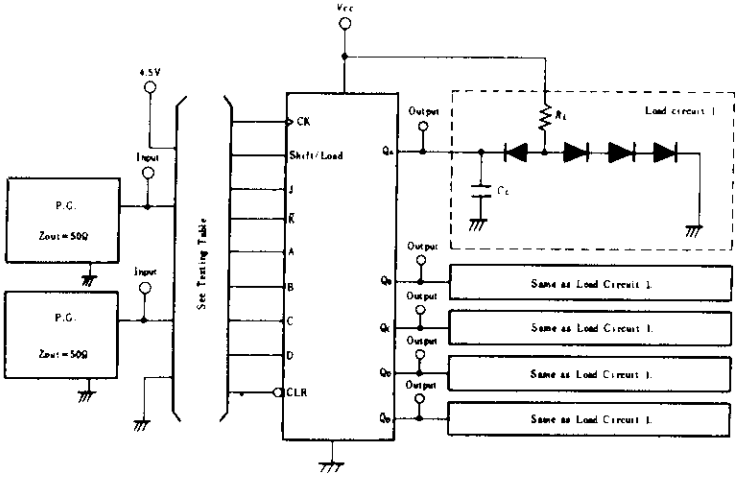
## ■COUNT SEQUENCE




Print

## ■TESTING METHOD

1) Test Circuit

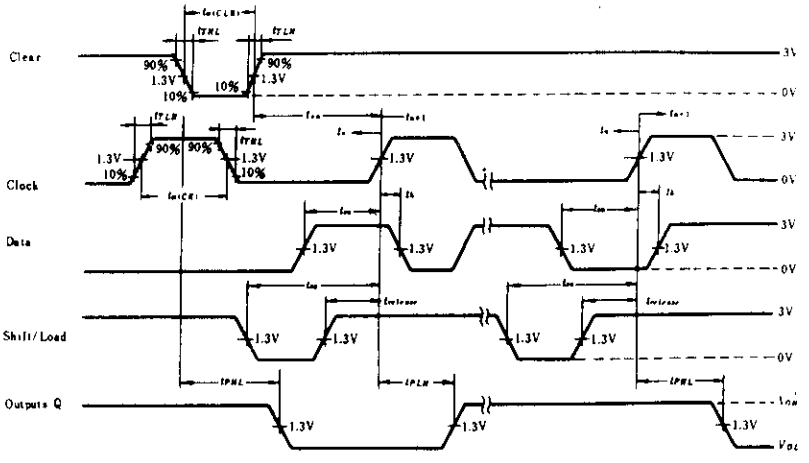



Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 (H).

2) Testing Table

| Item | From input to output | Inputs | | | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CLR | Shift/Load | J | $\overline{K}$ | CK | A | B | C | D | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $\overline{Q}_D$ |
| $f_{max}$ | | 4.5V | 4.5V | 4.5V | GND | IN | 4.5V | 4.5V | 4.5V | 4.5V | OUT | OUT | OUT | OUT | OUT |
| $t_{PHL}$ | Clear→ $Q_A \sim Q_D$ | IN | GND | 4.5V | 4.5V | IN | 4.5V | 4.5V | 4.5V | 4.5V | OUT | OUT | OUT | OUT | — |
| $t_{PLH}$ | Clock→ $Q_A \sim Q_D$, $\overline{Q}_D$ | 4.5V | 4.5V | 4.5V | GND | IN | 4.5V | 4.5V | 4.5V | 4.5V | OUT | OUT | OUT | OUT | OUT |
| $t_{PHL}$ | | 4.5V | GND | 4.5V | 4.5V | IN | IN | IN | IN | IN | OUT | OUT | OUT | OUT | OUT |

Waveform




Notes) 1. Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz, duty cycle 50%
2. A clear pulse is applied prior to each test.
3. Propagation delay times ($t_{PLH}$ and $t_{PHL}$) are measured at $t_{n+1}$. Proper shifting of data is verified at $t_{n+4}$ with a functional test.
4. J and $\overline{K}$ inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.
5. $t_n$; bit time before clocking transition.
6. $t_{n+1}$; bit time after one clocking transition.
7. $t_{n+4}$; bit time after four clocking transition.



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# HD74LS221 ●Dual Monostable Multivibrators

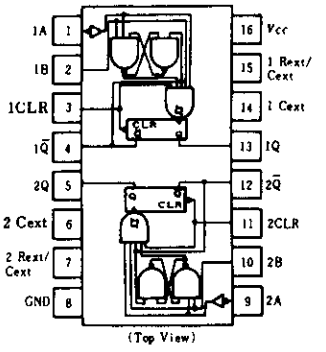
This multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input. Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1V/s, providing the circuit with excellent noise immunity of typically 1.2V. A high immunity to $V_{CC}$ noise of typically 1.5V is also provided by internal latching circuitry. Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output rise and fall times are TTL compatible and independent of pulse length.

Typical triggering and clearing sequence are illustrated as a part of the switching characteristics waveforms. Pulse width stability is achieved through internal compensation and is virtually independent of $V_{CC}$ and temperature.

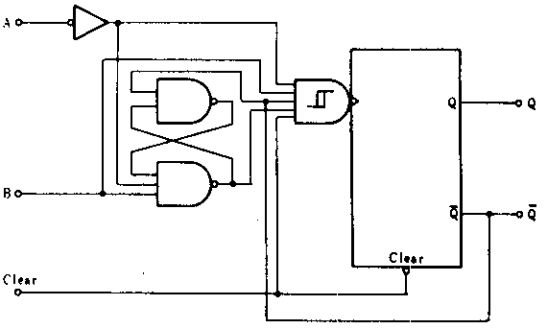
In most applications, pulse stability will only be limited by the accuracy of external timing components. Jitter-free operation is maintained over the full temperature and $V_{CC}$ range for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 100kΩ).

Throughout these ranges, pulse width is defined by the relationship: $t_{w(out)}$=Cext·Rext·1n2.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM (½)




## ■FUNCTION TABLE

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Clear | A | B | Q | $\bar{Q}$ |
| L | × | × | L | H |
| × | H | × | L | H |
| × | × | L | L | H |
| H | L | ↑ | ⎍ | ⎍ |
| H | ↓ | H | ⎍ | ⎍ |
| ↑ | L | H | ⎍ | ⎍ |

H; high level, L; low level, X; irrelevant.
↓; Transition from high to low level.
↑; Transition from low to high level.
⎍; one high-level pulse.
⎍; one low-level pulse.

## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Rate of rise or fall of input pulse | Schmitt input, B | $dV/dt$ | 1 | – | – | V/s |
| | logic input, A | | 1 | – | – | V/μs |
| Input pulse width | A or B | $t_{w(in)}$ | 40 | – | – | ns |
| | Clear | $t_{w(clear)}$ | 40 | – | – | |
| Setup time | | $t_{su}$ | 15 | – | – | ns |
| External timing resistance | | $R_{ext}$ | 1.4 | – | 100 | kΩ |
| External timing capacitance | | $C_{ext}$ | 0 | – | 1,000 | μF |
| Duty cycle | $R_T$=2kΩ | | – | – | 50 | % |
| | $R_T$=100kΩ | | – | – | 90 | |

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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Threshold voltage | A | $V_{T+}$ | $V_{CC}=4.75V$ | | – | 1.0 | 2.0 | V |
| | | $V_{T-}$ | $V_{CC}=4.75V$ | | 0.8 | 1.0 | – | V |
| | B | $V_{T+}$ | $V_{CC}=4.75V$ | | – | 1.0 | 2.0 | V |
| | | $V_{T-}$ | $V_{CC}=4.75V$ | | 0.8 | 0.9 | – | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $I_{OH}=-400\mu A$ | | 2.7 | – | – | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | A | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | A | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | B, Clear | | | | – | – | −0.8 | |
| | | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | – | −100 | mA |
| Supply current | | $I_{CC}$ | $V_{CC}=5.25V$ | Quiescent | – | 4.7 | 11 | mA |
| | | | | Triggered | – | 19 | 27 | |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

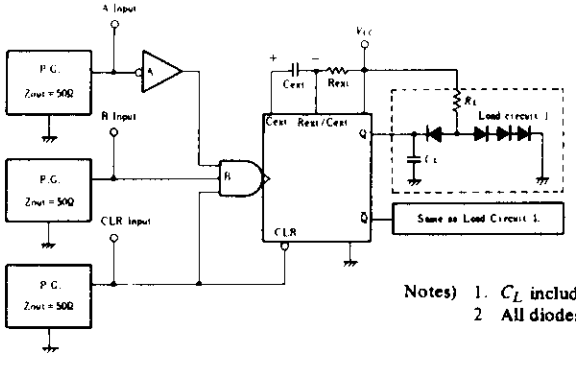
* $V_{CC}=5V$, $Ta=25°C$

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A | Q | $C_{ext}=80pF$, $R_{ext}=2k\Omega$, $C_L=15pF$, $R_L=2k\Omega$ | – | 45 | 70 | ns |
| | | B | Q | | – | 35 | 55 | |
| | $t_{PHL}$ | A | $\overline{Q}$ | | – | 50 | 80 | ns |
| | | B | $\overline{Q}$ | | – | 40 | 65 | |
| | $t_{PHL}$ | Clear | Q | | – | 35 | 55 | ns |
| | $t_{PLH}$ | Clear | $\overline{Q}$ | | – | 44 | 65 | ns |
| Output pulse width | $t_{w(out)}$ | A or B | Q or $\overline{Q}$ | $C_{ext}=80pF$, $R_{ext}=2k\Omega$ | 70 | 120 | 150 | ns |
| | | | | $C_{ext}=0$, $R_{ext}=2k\Omega$ | 20 | 47 | 70 | |
| | | | | $C_{ext}=100pF$, $R_{ext}=10k\Omega$ | 600 | 670 | 750 | |
| | | | | $C_{ext}=1\mu F$, $R_{ext}=10k\Omega$ | 6 | 6.7 | 7.5 | ms |

## ■TESTING METHOD

1) Test Circuit

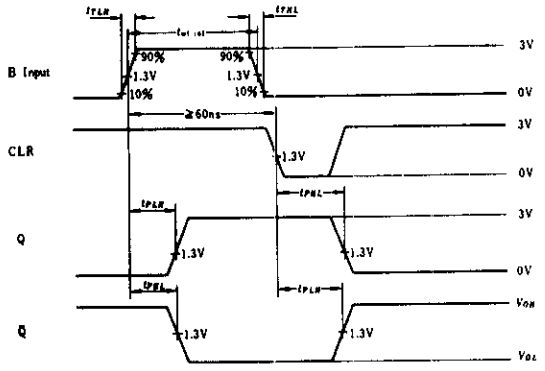



Notes) 1. $C_L$ includes probe and jig capacitance.
2 All diodes are 1S2074 Ⓗ.

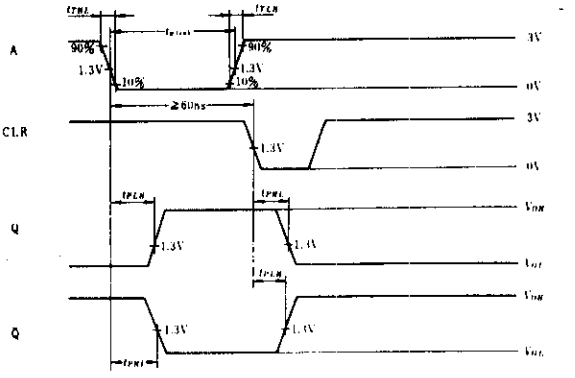


Home Print

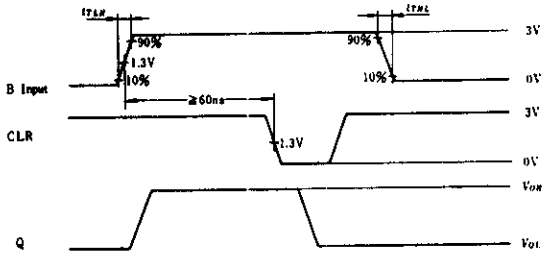
## Waveform



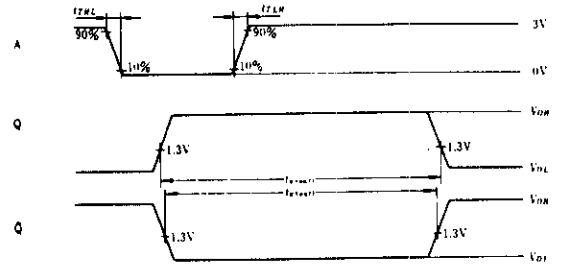

Trigger from B, then clear (A input is low).



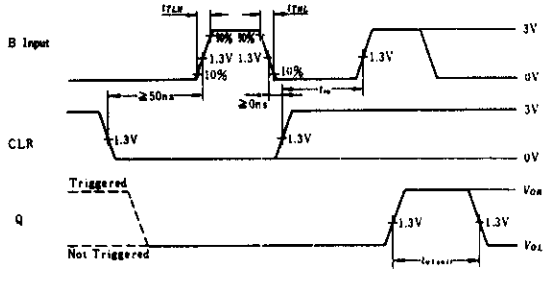

Trigger from A, then clear (B input is high).




Trigger from B, then clear (A input is low).

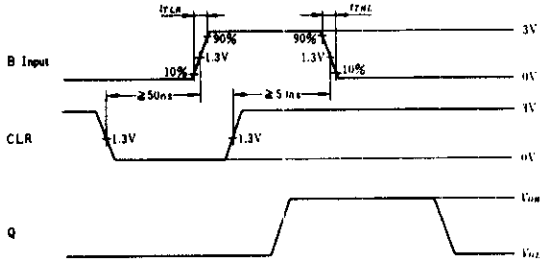



Trigger from A (B and clear inputs are high).




Clear overriding B, then trigger from B.

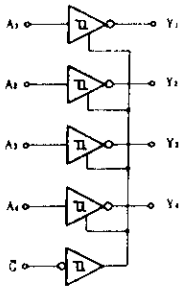
**Note)** **Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz**




Triggering from positive transition of Clear.

# HD74LS240 ●Octal Buffers/Line Drivers/Line Receivers (inverted three-state outputs)

## ■BLOCK DIAGRAM (1/2)

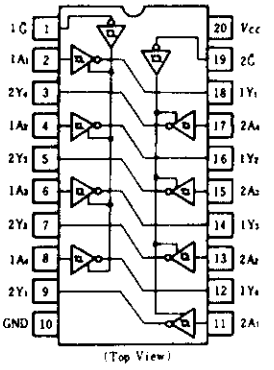


## ■FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| $\overline{G}$ | A | Y |
| H | × | Z |
| L | H | L |
| L | L | H |

Note) H; high level,
L; low level,
X; irrelevant
Z; off (high-impedance) state of a 3-state output

## ■PIN ARRANGEMENT



(Top View)

## ■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Hysteresis | | $V_{T^+} - V_{T^-}$ | $V_{CC} = 4.75V$ | | 0.2 | 0.4 | – | V |
| Output voltage | | $V_{OH}$ | $V_{CC} = 4.75V$, | $V_{IL} = 0.8V$, $I_{OH} = -3mA$ | 2.4 | – | – | V |
| | | | $V_{IH} = 2V$ | $V_{IL} = 0.5V$, $I_{OH} = -15mA$ | 2.0 | – | – | |
| | | $V_{OL}$ | $V_{CC} = 4.75V$, $V_{IH} = 2V$, | $I_{OL} = 12mA$ | – | – | 0.4 | V |
| | | | $V_{IL} = 0.8V$ | $I_{OL} = 24mA$ | – | – | 0.5 | |
| Output current | | $I_{OZH}$ | $V_{CC} = 5.25V$, $V_{IH} = 2V$, | $V_O = 2.7V$ | – | – | 20 | μA |
| | | $I_{OZL}$ | $V_{IL} = 0.8V$ | $V_O = 0.4V$ | – | – | −20 | μA |
| Input current | | $I_{IH}$ | $V_{CC} = 5.25V$, $V_I = 2.7V$ | | – | – | 20 | μA |
| | | $I_{IL}$ | $V_{CC} = 5.25V$, $V_I = 0.4V$ | | – | – | −0.2 | mA |
| | | $I_I$ | $V_{CC} = 5.25V$, $V_I = 7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | | $I_{OS}$ | $V_{CC} = 5.25V$ | | −40 | – | −225 | mA |
| Supply current** | Outputs high | $I_{CC}$ | $V_{CC} = 5.25V$ | | – | 13 | 23 | mA |
| | Outputs low | | | | – | 26 | 44 | |
| | All outputs disabled | | | | – | 29 | 50 | |
| Input clamp voltage | | $V_{IK}$ | $V_{CC} = 4.75V$, $I_{IN} = -18mA$ | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C
** $I_{CC}$ is measured with all outputs open.

## ■SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $Ta = 25°C$)

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L = 45pF$, $R_L = 667\Omega$ | – | 9 | 14 | ns |
| | $t_{PHL}$ | | – | 12 | 18 | |
| Output enable time | $t_{ZL}$ | | – | 20 | 30 | ns |
| | $t_{ZH}$ | | – | 15 | 23 | ns |
| Output disable time | $t_{LZ}$ | $C_L = 5pF$, $R_L = 667\Omega$ | – | 15 | 25 | ns |
| | $t_{HZ}$ | | – | 10 | 18 | ns |

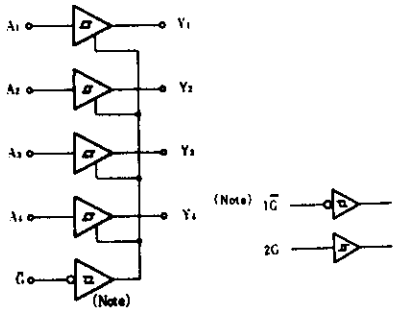
Note) Refer to Test Circuit and Waveform of the Common Item



Home Print

# HD74LS241 ●Octal Buffers/Line Drivers/Line Receivers (non inverted three-state outputs)

## ■BLOCK DIAGRAM (½)

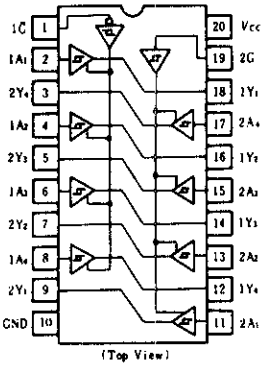



## ■FUNCTION TABLE

| Inputs | | | Output |
|---|---|---|---|
| $1\overline{G}$ | 2G | A | Y |
| H | L | × | Z |
| L | H | H | H |
| L | H | L | L |

Note) H; high level,
L; low level,
X; irrelevant
Z; off (high-impedance) state of a 3-state output

## ■PIN ARRANGEMENT




## ■ELECTRICAL CHARACTERISTICS ($Ta=-20\sim+75°C$)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Hysteresis | | $V_T^+ - V_T^-$ | $V_{CC}=4.75V$ | | 0.2 | 0.4 | – | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-3mA$ | | 2.4 | – | – | V |
| | | | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.5V$, $I_{OH}=-15mA$ | | 2.0 | – | – | |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=12mA$ | – | – | 0.4 | V |
| | | | | $I_{OL}=24mA$ | – | – | 0.5 | |
| Output current | | $I_{OZH}$ | $V_{CC}=5.25V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $V_O=2.7V$ | – | – | 20 | μA |
| | | $I_{OZL}$ | | $V_O=0.4V$ | – | – | −20 | |
| Input current | | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.2 | mA |
| | | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −40 | – | −225 | mA |
| Supply current** | Outputs high | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 13 | 23 | mA |
| | Outputs low | | | | – | 27 | 46 | |
| | All outputs disabled | | | | – | 32 | 54 | |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$
** $I_{CC}$ is measured with all outputs open.

## ■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

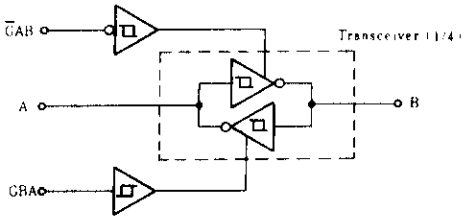
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=45pF$, $R_L=667\Omega$ | – | 12 | 18 | ns |
| | $t_{PHL}$ | | – | 12 | 18 | |
| Output enable time | $t_{ZL}$ | | – | 20 | 30 | ns |
| | $t_{ZH}$ | | – | 15 | 23 | ns |
| Output disable time | $t_{LZ}$ | $C_L=5pF$, $R_L=667\Omega$ | – | 15 | 25 | ns |
| | $t_{HZ}$ | | – | 10 | 18 | ns |

Note) Refer to Test Circuit and Waveform of the Common Item

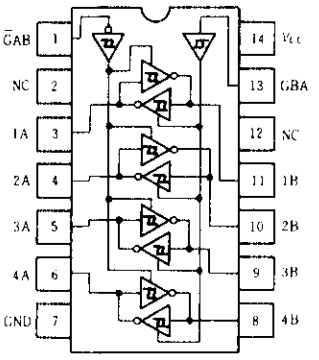
Home Print

# HD74LS242 ●Quadruple Bus Transceivers (with three-state outputs)

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




(Top View)

## ■FUNCTION TABLE

| Control input | | Data port status | |
|---|---|---|---|
| $\overline{G}AB$ | GBA | A | B |
| H | H | Inverting output | Input |
| L | H | * | |
| H | L | Isolated | Isolated |
| L | L | Input | Inverting output |

Notes) 1. H; high level, L; low level
2. *; Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Output current | $I_{OH}$ | – | – | –15 | mA |
| | $I_{OL}$ | – | – | 24 | mA |

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | |
| Hysteresis | | $V_{T^+} - V_{T^-}$ | $V_{CC}=4.75V$ | | 0.2 | 0.4 | – | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-3mA$ | | 2.4 | – | – | V |
| | | | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.5V$, $I_{OH}=-15mA$ | | 2 | – | – | |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=12mA$ | – | – | 0.4 | V |
| | | | | $I_{OL}=24mA$ | – | – | 0.5 | |
| Output current | | $I_{OZH}$ | $V_{CC}=5.25V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $V_O=2.7V$ | – | – | 40 | μA |
| | | $I_{OZL}$ | | $V_O=0.4V$ | – | – | –200 | |
| Input current | | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | A Input | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$, $\overline{G}AB$ and GBA at GND | | – | – | –0.2 | mA |
| | B Input | | $V_{CC}=5.25V$, $V_I=0.4V$, $\overline{G}AB$ and GBA at 4.5V | | – | – | –0.2 | |
| | $\overline{G}AB$ or GBA | | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | –0.2 | |
| | A or B | $I_I$ | $V_{CC}=5.25V$, $V_I=5.5V$ | | – | – | 0.1 | mA |
| | $\overline{G}AB$ or GBA | | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | –40 | – | –225 | mA |
| Supply current** | | $I_{CCH}$ | $V_{CC}=5.25V$ | | – | 22 | 38 | mA |
| | | $I_{CCL}$ | | | – | 29 | 50 | |
| | | $I_{CCZ}$ | | | – | 29 | 50 | |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IK}=-18mA$ | | – | – | –1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C
** With all outputs open, $I_{CC}$ is measured with transceivers enabled in one direction only, or with all transceivers disabled.



Home Print

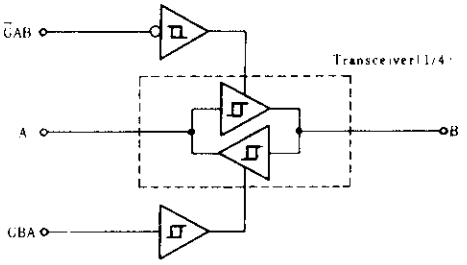
## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$=45pF<br>$R_L$=667Ω | – | 9 | 14 | ns |
| | $t_{PHL}$ | | – | 12 | 18 | |
| Output enable time | $t_{ZL}$ | | – | 20 | 30 | |
| | $t_{ZH}$ | | – | 15 | 23 | |
| Output disable time | $t_{LZ}$ | $C_L$=5pF<br>$R_L$=667Ω | – | 15 | 25 | |
| | $t_{HZ}$ | | – | 10 | 18 | |

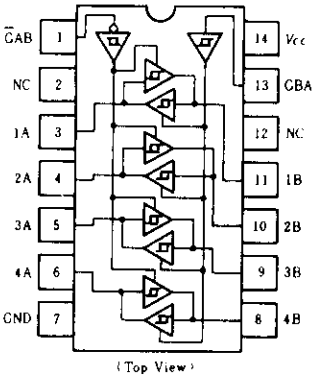
Note) Refer to Test Circuit and Waveform of the Common Item

# HD74LS243 ●Quadruple Bus Transceivers (with three-state outputs)

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




(Top View)

## ■FUNCTION TABLE

| Control input | | Data port status | |
|---|---|---|---|
| $\overline{G}AB$ | GBA | A | B |
| H | H | Output | Input |
| L | H | * | |
| H | L | Isolated | Isolated |
| L | L | Input | Output |

Notes) 1. H; high level, L; low level
2. *; Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Output current | $I_{OH}$ | – | – | −15 | mA |
| | $I_{OL}$ | – | – | 24 | mA |

## ■ELECTRICAL CHARACTERISTICS ($Ta$ = −20 ~ +75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Hysteresis | | $V_{T^+} - V_{T^-}$ | $V_{CC}$=4.75V | | 0.2 | 0.4 | – | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−3mA | | 2.4 | – | – | V |
| | | | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.5V, $I_{OH}$=−15mA | | 2 | – | – | |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=12mA | – | – | 0.4 | V |
| | | | | $I_{OL}$=24mA | – | – | 0.5 | |
| Output current | | $I_{OZH}$ | $V_{CC}$=5.25V, $V_{IH}$=2V, $V_{IL}$=0.8V | $V_O$=2.7V | – | – | 40 | μA |
| | | $I_{OZL}$ | | $V_O$=0.4V | – | – | −200 | |
| Input current | | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | – | – | 20 | μA |
| | A input | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V, $\overline{G}AB$ and GBA at GND | | – | – | −0.2 | mA |
| | B input | | $V_{CC}$=5.25V, $V_I$=0.4V, $\overline{G}AB$ and GBA at 4.5V | | – | – | −0.2 | |
| | $\overline{G}AB$ or GBA | | $V_{CC}$=5.25V, $V_I$=0.4V | | – | – | −0.2 | |
| | A or B | $I_I$ | $V_{CC}$=5.25V, $V_I$=5.5V | | – | – | 0.1 | mA |
| | $\overline{G}AB$ or GBA | | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.1 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$=5.25V | | −40 | – | −225 | mA |
| Supply current** | | $I_{CCH}$ | $V_{CC}$=5.25V | | – | 22 | 38 | mA |
| | | $I_{CCL}$ | | | – | 29 | 50 | |
| | | $I_{CCZ}$ | | | – | 32 | 54 | |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C
** With all outputs open, $I_{CC}$ is measured with transceivers enabled in one direction only, or with all transceivers disabled.



Home Print

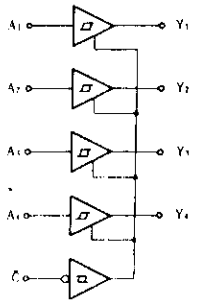
## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$=45pF<br>$R_L$=667Ω | – | 12 | 18 | ns |
| | $t_{PHL}$ | | – | 12 | 18 | |
| Output enable time | $t_{ZL}$ | | – | 20 | 30 | |
| | $t_{ZH}$ | | – | 15 | 23 | |
| Output disable time | $t_{LZ}$ | $C_L$=5pF<br>$R_L$=667Ω | – | 15 | 25 | |
| | $t_{HZ}$ | | – | 10 | 18 | |

Note) Refer to Test Circuit and Waveform of the Common Item

# HD74LS244 ●Octal Buffers/Line Drivers/Line Receivers (non inverted three-state outputs)

## ■BLOCK DIAGRAM(½)

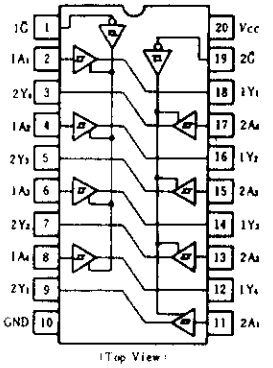


## ■FUNCTION TABLE

| Input | | Output |
|---|---|---|
| $\overline{G}$ | A | Y |
| H | × | Z |
| L | H | H |
| L | L | L |

Note) H; high level,
L; low level,
X; irrelevant
Z; off (high-impedance) state of a 3-state output

## ■PIN ARRANGEMENT



(Top View)

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Hysteresis | | $V_T^+ - V_T^-$ | $V_{CC}=4.75V$ | | 0.2 | 0.4 | — | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$ | $V_{IL}=0.8V$, $I_{OH}=-3mA$ | 2.4 | — | — | V |
| | | | | $V_{IL}=0.5V$, $I_{OH}=-15mA$ | 2.0 | — | — | |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=12mA$ | — | — | 0.4 | V |
| | | | | $I_{OL}=24mA$ | — | — | 0.5 | |
| Output current | | $I_{OZH}$ | $V_{CC}=5.25V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $V_O=2.7V$ | — | — | 20 | μA |
| | | $I_{OZL}$ | | $V_O=0.4V$ | — | — | −20 | |
| Input current | | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | μA |
| | | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.2 | mA |
| | | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}=5.25V$ | | −40 | — | −225 | mA |
| Supply current | Output "H" | $I_{CC}$ | $V_{CC}=5.25V$ | | — | 13 | 23 | mA |
| | Output "L" | | | | — | 27 | 46 | |
| | All outputs disabled | | | | — | 32 | 54 | |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$
** $I_{CC}$ is measured with all outputs open.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L=45pF$, $R_L=667\Omega$ | — | 12 | 18 | ns |
| | $t_{PHL}$ | | — | 12 | 18 | |
| Output enable time | $t_{ZL}$ | | — | 20 | 30 | ns |
| | $t_{ZH}$ | | — | 15 | 23 | ns |
| Output disable time | $t_{LZ}$ | $C_L=5pF$, $R_L=667\Omega$ | — | 15 | 25 | ns |
| | $t_{HZ}$ | | — | 10 | 18 | ns |

Note) Refer to Test Circuit and Waveform of the Common Item

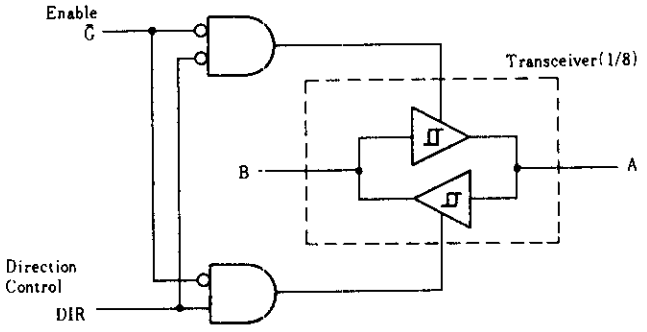


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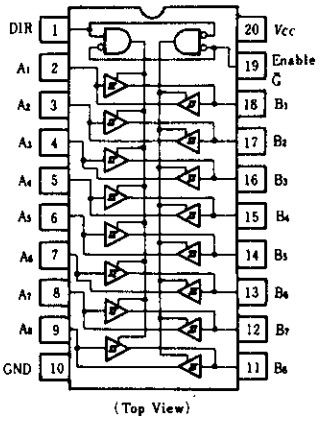
# HD74LS245 ●Octal Bus Transceivers (with three-state outputs)

This octal bus transceiver is designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements. The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT



(Top View)

## ■FUNCTION TABLE

| ENABLE $\overline{G}$ | DIRECTION CONTROL DIR | OPERATION |
|---|---|---|
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

H; high level,
L; low level,
X; irrelevant

## ■ABSOLUTE MAXIMUM RATINGS

| Item | | Symbol | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 7.0 | V |
| Input voltage | DIR, $\overline{G}$ | $V_{IN}$ | 7.0 | V |
| | A, B | | 5.5 | |
| Operating temperature range | | $T_{opr}$ | −20~+75 | ℃ |
| Storage temperature range | | $T_{stg}$ | −65~+150 | ℃ |

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Output current | $I_{OH}$ | − | − | −15 | mA |
| | $I_{OL}$ | − | − | 24 | mA |

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## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | |
| Hysteresis | | $V_{T^+} - V_{T^-}$ | $V_{CC} = 4.75V$ | | 0.2 | 0.4 | — | V |
| Output voltage | | $V_{OH}$ | $V_{CC} = 4.75V$, $V_{IH} = 2V$, | $I_{OH} = -3mA$ | 2.4 | — | — | V |
| | | | $V_{IL} = 0.8V$ | $I_{OH} = -15mA$ | 2 | — | — | |
| | | $V_{OL}$ | $V_{CC} = 4.75V$, $V_{IH} = 2V$, | $I_{OL} = 12mA$ | — | — | 0.4 | V |
| | | | $V_{IL} = 0.8V$ | $I_{OL} = 24mA$ | — | — | 0.5 | |
| Output current | | $I_{OZH}$ | $V_{CC} = 5.25V$ | $V_O = 2.7V$ | — | — | 10 | μA |
| | | $I_{OZL}$ | $\overline{G} = 2V$ | $V_O = 0.4V$ | — | — | −200 | |
| Input current | | $I_{IH}$ | $V_{CC} = 5.25V$, $V_I = 2.7V$ | | — | — | 20 | μA |
| | | $I_{IL}$ | $V_{CC} = 5.25V$, $V_I = 0.4V$ | | — | — | −0.2 | mA |
| | A or B | $I_I$ | $V_{CC} = 5.25V$ | $V_I = 5.5V$ | — | — | 0.1 | mA |
| | DIR or $\overline{G}$ | | | $V_I = 7V$ | — | — | 0.1 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC} = 5.25V$ | | −40 | — | −225 | mA |
| Supply current** | | $I_{CCH}$ | $V_{CC} = 5.25V$ | | — | 48 | 70 | mA |
| | | $I_{CCL}$ | | | — | 62 | 90 | |
| | | $I_{CCZ}$ | | | — | 64 | 95 | |
| Input clamp voltage | | $V_{IK}$ | $V_{CC} = 4.75V$, $I_{IN} = -18mA$ | | — | — | −1.5 | V |

* $V_{CC} = 5V$, $Ta = 25°C$
** $I_{CC}$ is measured with all outputs open.

## ■SWITCHING CHARACTERISTICS ( $V_{CC} = 5V$, $Ta = 25°C$ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L = 45pF$ $R_L = 667\Omega$ | — | 8 | 15 | ns |
| | $t_{PHL}$ | | — | 8 | 15 | |
| Output enable time | $t_{ZL}$ | | — | 27 | 40 | |
| | $t_{ZH}$ | | — | 25 | 40 | |
| Output disable time | $t_{LZ}$ | $C_L = 5pF$ $R_L = 667\Omega$ | — | 15 | 25 | |
| | $t_{HZ}$ | | — | 15 | 25 | |

Note) Refer to Test Circuit and Waveform of the Common Item

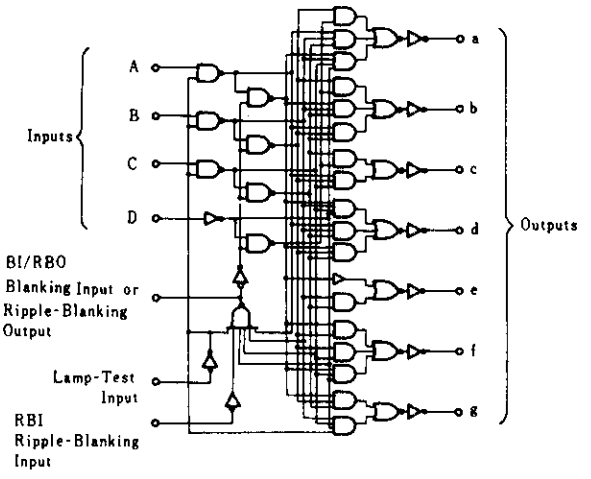


Home Print

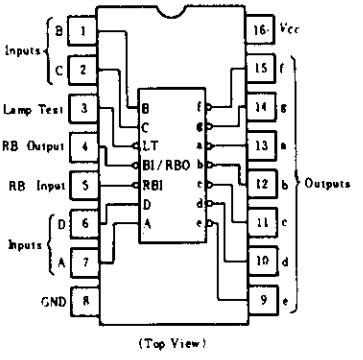
# HD74LS247 ●BCD-to-Seven-Segment Decoders/Drivers (with 15V outputs)

The HD74LS247 is electrically and functionally identical to the HD74LS47, respectively, and has the same pin assignments as its equivalents.
It can be used interchangeably in present or future designs to offer designers a choice between two indicator fonts. The HD74LS47 composes the 6 and the 9 without tails and the HD74LS247 composes the 6 and the 9 with tails. Composition of all other characters, including display patterns for BCD inputs above nine, is identical. The HD74LS247 features active-low outputs designed for driving indicators directly. All of the circuits have full ripple-blanking input/output controls and a lamp test input.
Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions. This circuit incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of this type may be performed at any time when the BI/RBO node is at a high level.
This type contains an overriding blanking input (BI) which can be used to control the lamp intensity be pulsing or to inhibit the outputs.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT

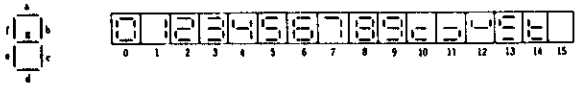



## ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7.0 | V |
| Input voltage | $V_{IN}$ | 7.0 | V |
| Output current ($t_W \leq 1$ms, duty cycle $\leq 10\%$) | $I_{O(peak)}$ | 200 | mA |
| Output current (off-state) | $I_{O(off)}$ | 1 | mA |
| Operating temperature range | $T_{opr}$ | −20～+75 | ℃ |
| Storage temperature range | $T_{stg}$ | −65～+150 | ℃ |

## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Output voltage | a～g | $V_{O(off)}$ | – | – | 15 | V |
| Output current | a～g | $I_{O(on)}$ | – | – | 24 | mA |
| | BI/RBO | $I_{OH}$ | – | – | −50 | μA |
| | BI/RBO | $I_{OL}$ | – | – | 3.2 | mA |




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## ■FUNCTION TABLE

| Decimal or Function | Inputs | | | | | | BI/RBO | Outputs | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LT | RBI | D | C | B | A | | a | b | c | d | e | f | g | |
| 0 | H | H | L | L | L | L | H | ON | ON | ON | ON | ON | ON | OFF | |
| 1 | H | × | L | L | L | H | H | OFF | ON | ON | OFF | OFF | OFF | OFF | |
| 2 | H | × | L | L | H | L | H | ON | ON | OFF | ON | ON | OFF | ON | |
| 3 | H | × | L | L | H | H | H | ON | ON | ON | ON | OFF | OFF | ON | |
| 4 | H | × | L | H | L | L | H | OFF | ON | ON | OFF | OFF | ON | ON | |
| 5 | H | × | L | H | L | H | H | ON | OFF | ON | ON | OFF | ON | ON | |
| 6 | H | × | L | H | H | L | H | ON | OFF | ON | ON | ON | ON | ON | |
| 7 | H | × | L | H | H | H | H | ON | ON | ON | OFF | OFF | OFF | OFF | |
| 8 | H | × | H | L | L | L | H | ON | ON | ON | ON | ON | ON | ON | 1 |
| 9 | H | × | H | L | L | H | H | ON | ON | ON | ON | OFF | ON | ON | |
| 10 | H | × | H | L | H | L | H | OFF | OFF | OFF | ON | ON | OFF | ON | |
| 11 | H | × | H | L | H | H | H | OFF | OFF | ON | ON | OFF | OFF | ON | |
| 12 | H | × | H | H | L | L | H | OFF | ON | OFF | OFF | OFF | ON | ON | |
| 13 | H | × | H | H | L | H | H | ON | OFF | OFF | ON | OFF | ON | ON | |
| 14 | H | × | H | H | H | L | H | OFF | OFF | OFF | ON | ON | ON | ON | |
| 15 | H | × | H | H | H | H | H | OFF | OFF | OFF | OFF | OFF | OFF | OFF | |
| BI | × | × | × | × | × | × | L | OFF | OFF | OFF | OFF | OFF | OFF | OFF | 2 |
| RBI | H | L | L | L | L | L | L | OFF | OFF | OFF | OFF | OFF | OFF | OFF | 3 |
| LT | L | × | × | × | × | × | H | ON | ON | ON | ON | ON | ON | ON | 4 |

H; high level, L; low level, X; irrelevant

Notes) 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.

3. When ripple-blanking input (RBI) and inputs A, B C, and D are a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).

4. When a blanking input ripple blanking input (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | BI/RBO | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-50\mu A$ | | 2.4 | – | – | V |
| | BI/RBO | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$ | $I_{OL}=1.6mA$ | – | – | 0.4 | V |
| | | | $V_{IL}=0.8V$ | $I_{OL}=3.2mA$ | – | – | 0.5 | |
| Output current | a~g | $I_{O(off)}$ | $V_{CC}=5.25V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $V_{O(off)}=15V$ | | – | – | 250 | $\mu A$ |
| Output voltage | a~g | $V_{O(on)}$ | $V_{CC}=5.25V$, $V_{IH}=2V$ | $I_{O(on)}=12mA$ | – | – | 0.4 | V |
| | | | $V_{IL}=0.8V$ | $I_{O(on)}=24mA$ | – | – | 0.5 | |
| Input current | | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | $\mu A$ |
| | except BI/RBO | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | -0.4 | mA |
| | BI/RBO | | | | – | – | -1.2 | |
| | | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Short-circuit output current | BI/RBO | $I_{OS}$ | $V_{CC}=5.25V$ | | -0.3 | – | -2 | mA |
| Supply current** | | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 7 | 13 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | -1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

** $I_{CC}$ is measured with all outputs open and all inputs at 4.5V.



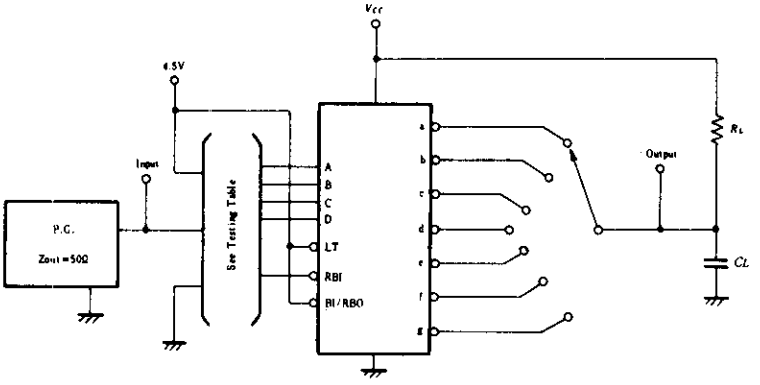
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## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

| Item | Symbol | Input | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| Turn-on time | $t_{on}$ | A | $C_L$=15pF, $R_L$=665Ω | – | – | 100 | ns |
| | | RBI | | – | – | 100 | |
| Turn-off time | $t_{off}$ | A | | – | – | 100 | ns |
| | | RBI | | – | – | 100 | |

## ■TESTING METHOD

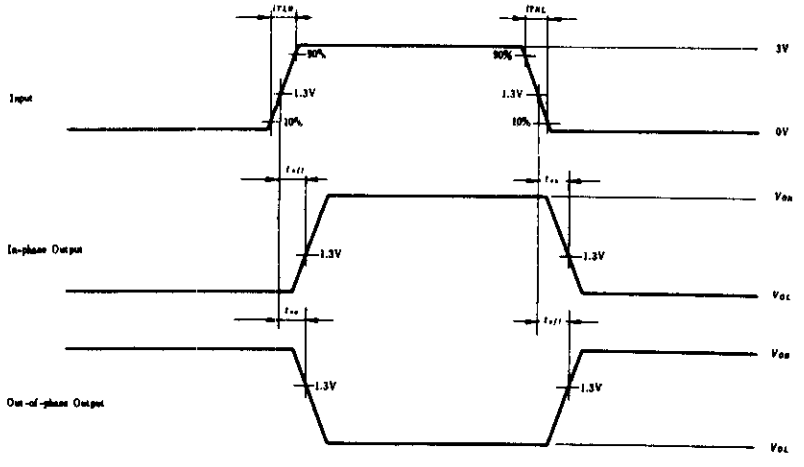
1) Test Circuit




2) Testing Table

| Item | Inputs | | | | | Outputs | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RBI | D | C | B | A | a | b | c | d | e | f | g |
| $t_{on}$ $t_{off}$ | 4.5V | GND | GND | GND | IN | OUT | – | – | OUT | OUT | OUT | – |
| | 4.5V | GND | GND | 4.5V | IN | – | – | OUT | – | OUT | – | – |
| | 4.5V | GND | 4.5V | 4.5V | IN | – | OUT | – | OUT | OUT | OUT | OUT |
| | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | OUT | OUT | – |

Waveform



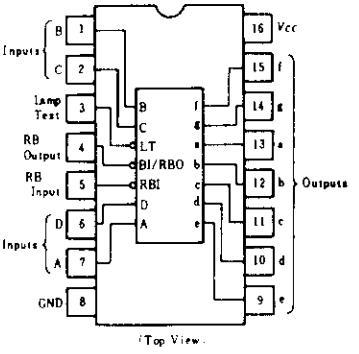

Notes) 1. Input pulse: $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz, duty cycle=50%.
2. $C_L$ includes probe and jig capacitance.

# HD74LS248 ●BCD-to-Seven-Segment Decoders/Drivers (internal pull-up outputs)

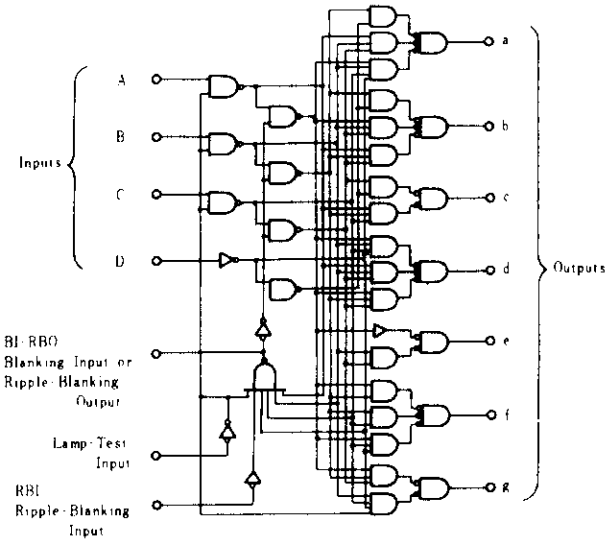
The HD74LS248 is electrically and functionally identical to the HD74LS48, respectively, and has the same pin assignments as its equivalents. It can be used interchangeably in present or future designs to offer designers a choice between two indicator fonts. The HD74LS48 composes the 6 and the 9 without tails and the HD74LS248 composes the 6 and the 9 with tails. Composition of all other characters, including display patterns for BCD inputs above nine, is identical. The HD74LS248 features active-low outputs designed for driving indicators directly. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions. This circuit incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO).

Lamp test (LT) of this type may be performed at any time when the BI/RBO node is at a high level. This type contains an overriding blanking input (BI) which can be used to control the lamp intensity be pulsing or to inhibit the outputs.

## ■PIN ARRANGEMENT

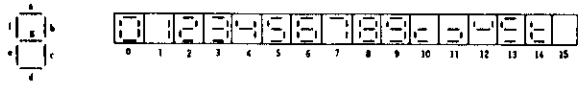



## ■BLOCK DIAGRAM




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Output current | a~g | $I_{OH}$ | – | – | −100 | μA |
| | BI/RBO | | – | – | −50 | |
| | a~g | $I_{OL}$ | – | – | 6 | mA |
| | BI/RBO | | – | – | 3.2 | |





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## ■FUNTION TABLE

| Decimal or Function | Inputs | | | | | | BI/RBO | Outputs | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LT | RBI | D | C | B | A | | a | b | c | d | e | f | g | |
| 0 | H | H | L | L | L | L | H | H | H | H | H | H | H | L | 1 |
| 1 | H | × | L | L | L | H | H | L | H | H | L | L | L | L | |
| 2 | H | × | L | L | H | L | H | H | H | L | H | H | L | H | |
| 3 | H | × | L | L | H | H | H | H | H | H | H | L | L | H | |
| 4 | H | × | L | H | L | L | H | L | H | H | L | L | H | H | |
| 5 | H | × | L | H | L | H | H | H | L | H | H | L | H | H | |
| 6 | H | × | L | H | H | L | H | H | L | H | H | H | H | H | |
| 7 | H | × | L | H | H | H | H | H | H | H | L | L | L | L | |
| 8 | H | × | H | L | L | L | H | H | H | H | H | H | H | H | |
| 9 | H | × | H | L | L | H | H | H | H | H | H | L | H | H | |
| 10 | H | × | H | L | H | L | H | L | L | L | H | H | L | H | |
| 11 | H | × | H | L | H | H | H | L | L | H | H | L | L | H | |
| 12 | H | × | H | H | L | L | H | L | H | L | L | L | H | H | |
| 13 | H | × | H | H | L | H | H | H | L | L | H | L | H | H | |
| 14 | H | × | H | H | H | L | H | L | L | L | H | H | H | H | |
| 15 | H | × | H | H | H | H | H | L | L | L | L | L | L | L | |
| BI | × | × | × | × | × | × | L | L | L | L | L | L | L | L | 2 |
| RBI | H | L | L | L | L | L | L | L | L | L | L | L | L | L | 3 |
| LT | L | × | × | × | × | × | H | H | H | H | H | H | H | H | 4 |

H; high level, L; low level, X; irrelevant

Notes: 1. The blanking input (BI) must be open or held at a high-logic level when output functions 0 through 15 are desired.

2. When a low logic level is applied directly to the blanking input.

3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).

4. When a blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

## ■ELECTRICAL CHARACTERISTICS ($Ta$= −20~ +75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | a~g | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OH}$=−100μA | 2.4 | – | – | V |
| | BI/RBO | | | $I_{OH}$=−50μA | | | | |
| Output current** | a~g | $I_O$ | $V_{CC}$=4.75V, $V_O$=0.85V | | −1.3 | – | – | mA |
| Output voltage | a~g | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=2mA | – | – | 0.4 | V |
| | | | | $I_{OL}$=6mA | – | – | 0.5 | |
| | BI/RBO | | | $I_{OL}$=1.6mA | – | – | 0.4 | |
| | | | | $I_{OL}$=3.2mA | – | – | 0.5 | |
| Input current | except BI/RBO | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | – | – | 20 | μA |
| | except BI/RBO | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | – | – | −0.4 | mA |
| | BI/RBO | | | | – | – | −1.2 | |
| | except BI/RBO | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.1 | mA |
| Short-circuit output current | BI/RBO | $I_{OS}$ | $V_{CC}$=5.25V | | −0.3 | – | −2 | mA |
| Supply current*** | | $I_{CC}$ | $V_{CC}$=5.25V | | – | 25 | 38 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** Input condition as for $V_{OH}$

*** $I_{CC}$ is measured with all outputs open and all inputs at 4.5V.

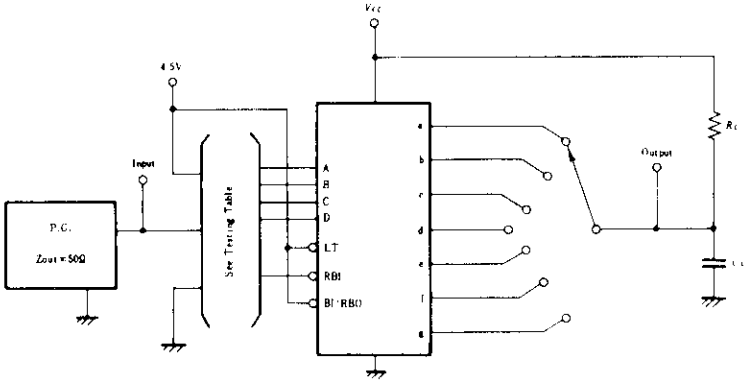
Home Print

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

| Item | Symbol | Input | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A | $C_L$=15pF, $R_L$=4kΩ | – | – | 100 | ns |
| | $t_{PHL}$ | | | – | – | 100 | |
| | $t_{PLH}$ | RBI | $C_L$=15pF, $R_L$=6kΩ | – | – | 100 | ns |
| | $t_{PHL}$ | | | – | – | 100 | |

## ■TESTING METHOD

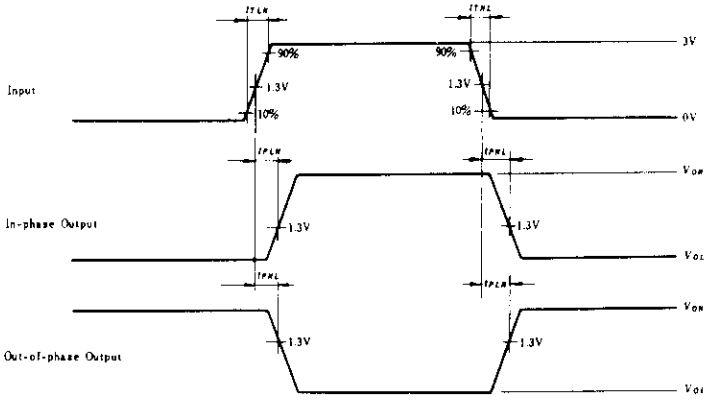
1) Test Circuit




2) Testing Table

| Item | Inputs | | | | | Outputs | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RBI | D | C | B | A | a | b | c | d | e | f | g |
| | 4.5V | GND | GND | GND | IN | OUT | – | – | OUT | OUT | OUT | – |
| $t_{PLH}$ | 4.5V | GND | GND | 4.5V | IN | – | – | OUT | – | OUT | – | – |
| $t_{PHL}$ | 4.5V | GND | 4.5V | 4.5V | IN | – | OUT | – | OUT | OUT | OUT | OUT |
| | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | OUT | OUT | – |

Waveform




Notes) 1. Input pulse: $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz, duty cycle=50%
2. $C_L$ includes probe and jig capacitance.



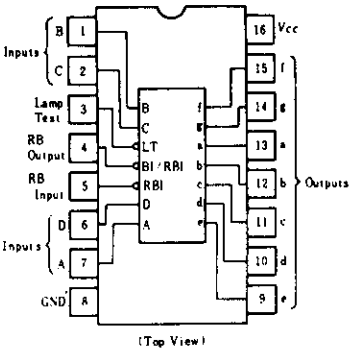
Home Print

# HD74LS249 ●BCD-to-Seven-Segment Decoders/Drivers (with open collector outputs)

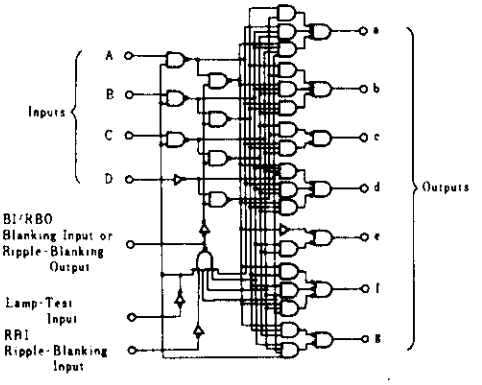
The HD74LS249 is 16-pin versions of the HD74LS49, respectively. Included in the HD74LS249 circuits is the full functional capability for lamp test and ripple blanking, which is not available in the HD74LS circuits. The HD74LS49 composes the 6 and 9 without tails and the HD74LS249 composes the 6 and 9 with tails. Composition of all other characters, including display patterns for BCD inputs above nine, is identical. The HD74LS249 features active-low outputs designed for driving indicators directly. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions. This circuit incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO).

Lamp test (LT) of this type may be performed at any time when the BI/RBO node is at a high level. This type contains an overriding blanking input (BI) which can be used to control the lamp intensity be pulsing or to inhibit the outputs.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM

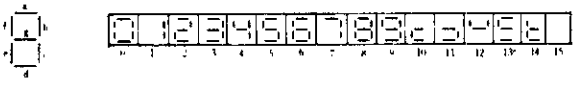



## ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7.0 | V |
| Input voltage | $V_{IN}$ | 7.0 | V |
| Output current (off-state) | $I_{O(off)}$ | 1 | mA |
| Operating temperature range | $T_{opr}$ | −20~+75 | ℃ |
| Storage temperature range | $T_{stg}$ | −65~+150 | ℃ |

## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Output voltage | a~g | $V_{OH}$ | – | – | 5.5 | V |
| Output current | BI/RBO | $I_{OH}$ | – | – | −50 | μA |
| | a~g | $I_{OL}$ | – | – | 8 | mA |
| | BI/RBO | | – | – | 3.2 | |



Home Print

## ■FUNCTION TABLE

| Decimal or Function | Inputs | | | | | | BI/RBO | Outputs | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LT | RBI | D | C | B | A | | a | b | c | d | e | f | g | |
| 0 | H | H | L | L | L | L | H | H | H | H | H | H | H | L | 1 |
| 1 | H | × | L | L | L | H | H | L | H | H | L | L | L | L | |
| 2 | H | × | L | L | H | L | H | H | H | L | H | H | L | H | |
| 3 | H | × | L | L | H | H | H | H | H | H | H | L | L | H | |
| 4 | H | × | L | H | L | L | H | L | H | H | L | L | H | H | |
| 5 | H | × | L | H | L | H | H | H | L | H | H | L | H | H | |
| 6 | H | × | L | H | H | L | H | H | L | H | H | H | H | H | |
| 7 | H | × | L | H | H | H | H | H | H | H | L | L | L | L | |
| 8 | H | × | H | L | L | L | H | H | H | H | H | H | H | H | |
| 9 | H | × | H | L | L | H | H | H | H | H | H | L | H | H | |
| 10 | H | × | H | L | H | L | H | L | L | L | H | H | L | H | |
| 11 | H | × | H | L | H | H | H | L | L | H | H | L | L | H | |
| 12 | H | × | H | H | L | L | H | L | H | L | L | L | H | H | |
| 13 | H | × | H | H | L | H | H | H | L | L | H | L | H | H | |
| 14 | H | × | H | H | H | L | H | L | L | L | H | H | H | H | |
| 15 | H | × | H | H | H | H | H | L | L | L | L | L | L | L | |
| BI | × | × | × | × | × | × | L | L | L | L | L | L | L | L | 2 |
| RBI | H | L | L | L | L | L | L | L | L | L | L | L | L | L | 3 |
| LT | L | × | × | × | × | × | H | H | H | H | H | H | H | H | 4 |

H; high level, L; low level, X; irrelevant

Notes: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired.
2. When a low logic level is applied directly to blanking input (BI), all segment outputs are low regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When a blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

## ■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | BI/RBO | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-50\mu A$ | | 2.4 | — | — | V |
| Output current | a ~ g | $I_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$ | | — | — | 250 | $\mu A$ |
| Output voltage | BI/RBO | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=1.6mA$ | — | — | 0.4 | V |
| | | | | $I_{OL}=3.2mA$ | — | — | 0.5 | |
| | a ~ g | | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | — | — | 0.4 | |
| | | | | $I_{OL}=8mA$ | — | — | 0.5 | |
| Input current | except BI/RBO | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | $\mu A$ |
| | except BI/RBO | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| | BI/RBO | | | | | — | −1.2 | |
| | except BI/RBO | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| Short-circuit output current | BI/RBO | $I_{OS}$ | $V_{CC}=5.25V$ | | −0.3 | — | −2 | mA |
| Supply current** | | $I_{CC}$ | $V_{CC}=5.25V$ | | — | 8 | 15 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

** $I_{CC}$ is measured with all outputs open and all inputs at 4.5V.



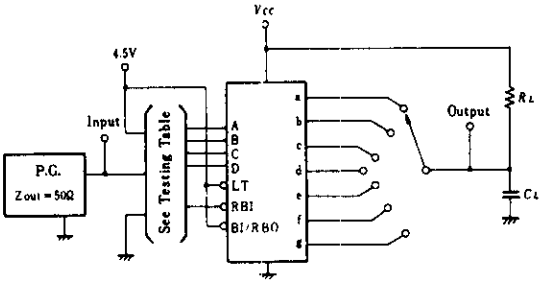
Home Print

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

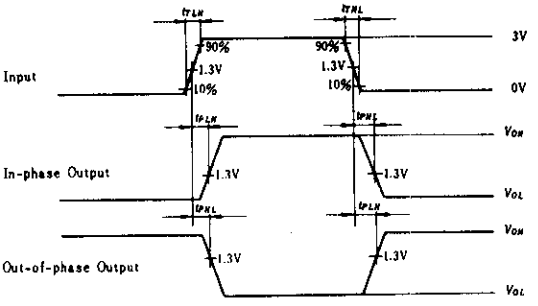
| Item | Symbol | Input | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A | $C_L$=15pF | – | – | 100 | ns |
| | $t_{PHL}$ | | $R_L$=2kΩ | – | – | 100 | |
| | $t_{PLH}$ | RBI | $C_L$=15pF | – | – | 100 | ns |
| | $t_{PHL}$ | | $R_L$=6kΩ | – | – | 100 | |

## ■TESTING METHOD

1) Test Circuit




Waveform




2) Testing Table

| Item | Inputs | | | | | Outputs | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RBI | D | C | B | A | a | b | c | d | e | f | g |
| | 4.5V | GND | GND | GND | IN | OUT | – | | OUT | OUT | OUT | |
| $t_{PLH}$ | 4.5V | GND | GND | 4.5V | IN | – | – | OUT | – | OUT | – | – |
| $t_{PHL}$ | 4.5V | GND | 4.5V | 4.5V | IN | – | OUT | – | OUT | OUT | OUT | OUT |
| | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | OUT | OUT | – |

Notes) 1. Input pulse: $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz, duty cycle=50%.
2. $C_L$ includes probe and jig capacitance.

# HD74LS251 ● 1 of 8 Data Selectors/Multiplexers (with strobe and three-state outputs)

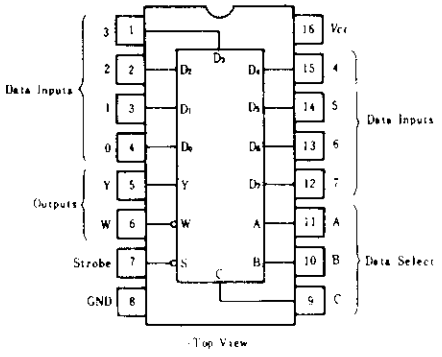
This data selector/multiplexer contains full on-chip binary decoding to select one-of-eight data sources and features a strobe-controlled 3-state output.

The strobe must be at a low logic level to enable this device. The 3-state outputs permit a number of outputs to be connected to a common bus.

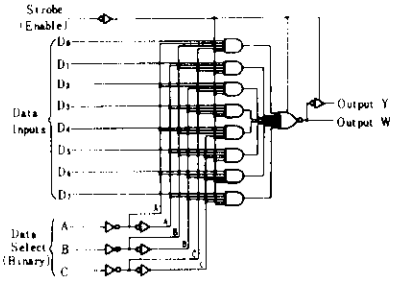
When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7.0 | V |
| Input voltage | $V_{IN}$ | 7.0 | V |
| Output voltage (off-state) | $V_{O(off)}$ | 5.5 | V |
| Operating temperature range | $T_{opr}$ | −20 ~ +75 | ℃ |
| Storage temperature range | $T_{stg}$ | −65 ~ +150 | ℃ |

## ■FUNCTION TABLE

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| SELECT | | | STROBE | | |
| C | B | A | S | Y | W |
| × | × | × | H | Z | Z |
| L | L | L | L | $D_0$ | $\overline{D_0}$ |
| L | L | H | L | $D_1$ | $\overline{D_1}$ |
| L | H | L | L | $D_2$ | $\overline{D_2}$ |
| L | H | H | L | $D_3$ | $\overline{D_3}$ |
| H | L | L | L | $D_4$ | $\overline{D_4}$ |
| H | L | H | L | $D_5$ | $\overline{D_5}$ |
| H | H | L | L | $D_6$ | $\overline{D_6}$ |
| H | H | H | L | $D_7$ | $\overline{D_7}$ |

Notes) 1. H; high level, L; low level, X; irrelevant
2. Z; high impedance (off-state)
3. $D_0$ through $D_7$; the level of the respective D input.

## ■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75℃$)

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−2.6mA | | 2.4 | – | – | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | – | – | 0.4 | V |
| | | | $I_{OL}$=8mA | – | – | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.1 | mA |
| Output current | $I_{OZ}$ | $V_{CC}$=5.25V, $V_{IH}$=2V | $V_O$=2.7V | – | – | 20 | μA |
| | | | $V_O$=0.4V | – | – | −20 | |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −30 | – | −130 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}$=5.25V | ConditionA | – | 6.1 | 10 | mA |
| | | | ConditionB | – | 7.1 | 12 | |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** $I_{CC}$ is measured with the outputs open and all data and select inputs at 4.5V under the following conditions:
A. Strobe grounded, B. Strobe at 4.5V



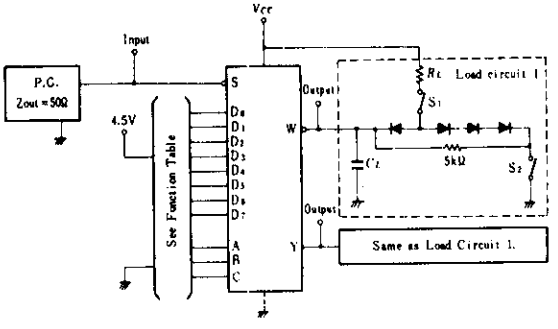
Home Print

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

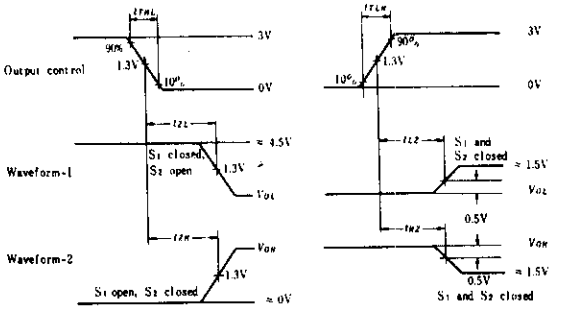
| Item | Inputs | Outputs | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | A, B, C (4 level) | Y | $t_{PLH}$ | $C_L$=15pF $R_L$=2kΩ | – | 29 | 45 | ns |
| | | | $t_{PHL}$ | | – | 28 | 45 | |
| | A, B, C (3 level) | W | $t_{PLH}$ | | – | 20 | 33 | |
| | | | $t_{PHL}$ | | – | 21 | 33 | |
| | Data | Y | $t_{PLH}$ | | – | 17 | 28 | |
| | | | $t_{PHL}$ | | – | 18 | 28 | |
| | Data | W | $t_{PLH}$ | | – | 10 | 15 | |
| | | | $t_{PHL}$ | | – | 9 | 15 | |
| Output enable time | Strobe | Y | $t_{ZH}$ | | – | 30 | 45 | ns |
| | | | $t_{ZL}$ | | – | 26 | 40 | |
| | Strobe | W | $t_{ZH}$ | | – | 17 | 27 | |
| | | | $t_{ZL}$ | | – | 24 | 40 | |
| Output disable time | Strobe | Y | $t_{HZ}$ | $C_L$=5pF $R_L$=2kΩ | – | 30 | 45 | ns |
| | | | $t_{LZ}$ | | – | 15 | 25 | |
| | Strobe | W | $t_{HZ}$ | | – | 37 | 55 | |
| | | | $t_{LZ}$ | | – | 15 | 25 | |

## ■TESTING METHOD

1) Test Circuit




Waveform



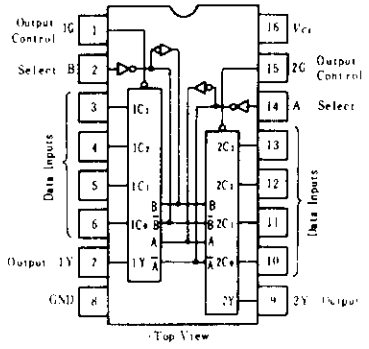

Notes) 1. Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz, duty cycle = 50%.
2. $C_L$ includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ.
4. Waveform-1 is for an output with internal conditions such that the output is low except when disabled by the output control.
5. Waveform-2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Home Print

# HD74LS253 ●Dual 4-line-to-1-line Data Selectors/Multiplexers (with three-state outputs)

This data selector/multiplexer contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to AND-OR gates.
Separate output control inputs are provided for each of the two four-line sections. The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at high-impedance state) the low-impedance of the single enabled output will dirve the bus line to a high or low logic level.

## ■PIN ARRANGEMENT

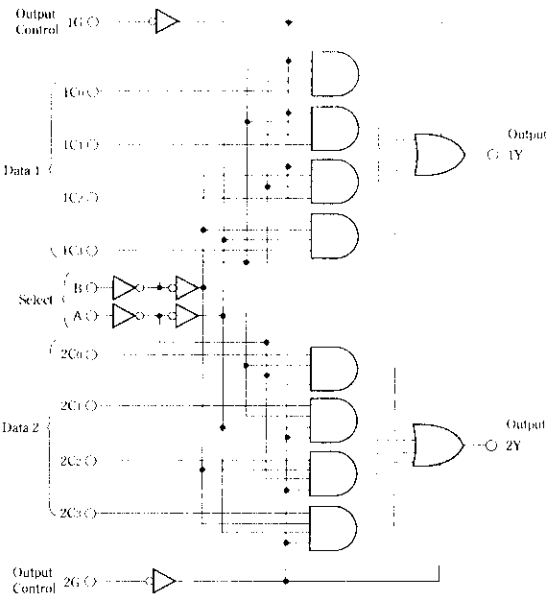



## ■FUNCTION TABLE

| Select inputs | | Data inputs | | | | Output control | Output |
|---|---|---|---|---|---|---|---|
| B | A | $C_0$ | $C_1$ | $C_2$ | $C_3$ | G | Y |
| × | × | × | × | × | × | H | Z |
| L | L | L | × | × | × | L | L |
| L | L | H | × | × | × | L | H |
| L | H | × | L | × | × | L | L |
| L | H | × | H | × | × | L | H |
| H | L | × | × | L | × | L | L |
| H | L | × | × | H | × | L | H |
| H | H | × | × | × | L | L | L |
| H | H | × | × | × | H | L | H |

Notes) 1. H; high level, L; low level, X; irrelevant
2. Address inputs A and B are common to both sections.

## ■BLOCK DIAGRAM




## ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7.0 | V |
| Input voltage | $V_{IN}$ | 7.0 | V |
| Output voltage (off-state) | $V_{O(off)}$ | 5.5 | V |
| Operating temperature range | $T_{opr}$ | −20～+75 | ℃ |
| Storage temperature range | $T_{stg}$ | −65～+150 | ℃ |



Home Print

## ■ELECTRICAL CHARACTERISTICS ( $Ta$=−20～+75℃ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unjt |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−2.6mA | | 2.4 | — | — | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | — | — | 0.4 | V |
| | | | $I_{OL}$=8mA | — | — | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.1 | mA |
| Output current | $I_{OZ}$ | $V_{CC}$=5.25V, $V_{IH}$=2V | $V_O$=2.7V | — | — | 20 | μA |
| | | | $V_O$=0.4V | — | — | −20 | |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −30 | — | −130 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}$=5.25V | ConditionA | — | 7 | 12 | mA |
| | | | ConditionB | — | 8.5 | 14 | |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

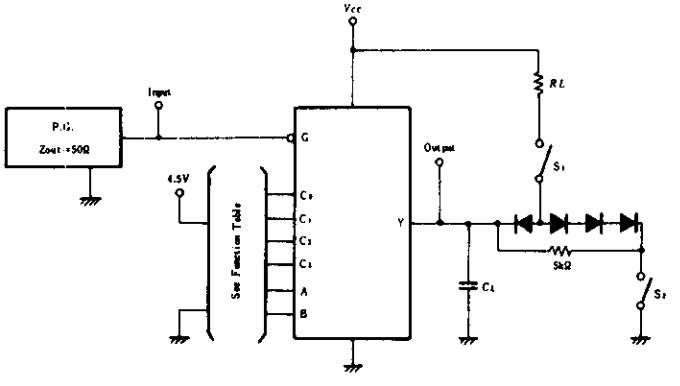
* $V_{CC}$=5V, $Ta$=25°C
** $I_{CC}$ is measured with the outputs open under the following conditions: A. All inputs grounded, B. Output control at 4.5V, all inputs grounded.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

| Item | Inputs | Output | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | Data | Y | $t_{PLH}$ | $C_L$=15pF, $R_L$=2kΩ | — | 17 | 25 | ns |
| | | | $t_{PHL}$ | | — | 13 | 20 | |
| | Select | Y | $t_{PLH}$ | | — | 30 | 45 | |
| | | | $t_{PHL}$ | | — | 21 | 32 | |
| Output enable time | Output Control | Y | $t_{ZH}$ | | — | 15 | 28 | ns |
| | | | $t_{ZL}$ | | — | 15 | 23 | |
| Output disable time | Output Control | Y | $t_{HZ}$ | $C_L$=5pF, $R_L$=2kΩ | — | 27 | 41 | ns |
| | | | $t_{LZ}$ | | — | 18 | 27 | |

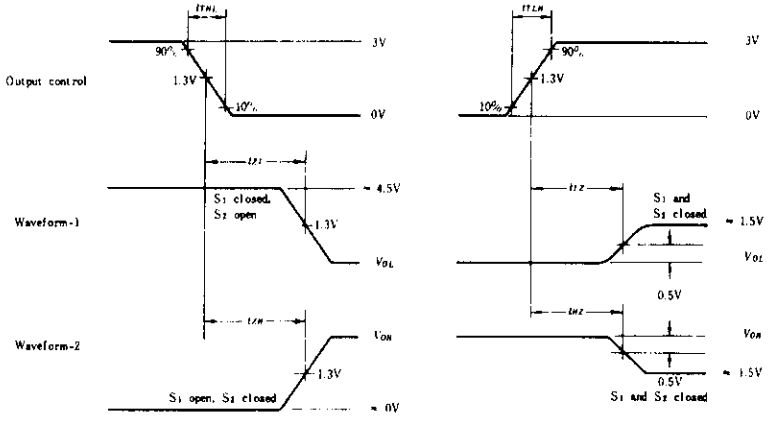
## ■TESTING METHOD

1) Test Circuit




Home Print

Waveform




Notes) 1. Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz, duty cycle = 50%.
2. $C_L$ includes probe and jig capacitance.
3. All diodes are 1S2074 (H).
4. Waveform-1 is for an output with internal conditions such that the output is low except when disabled by the output control.
5. Waveform-2 is for an output with internal conditions such that the output is high except when disabled by the output control.

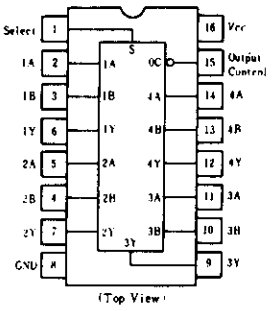


Home Print

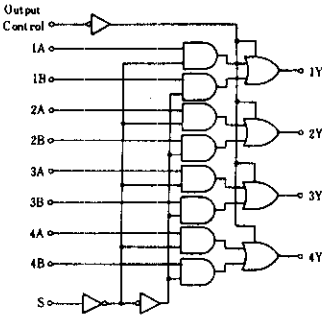
# HD74LS257 ●Quadruple 2-line-to-1-line Data Selectors/Multiplexers (with non inverted 3-state outputs)

This multiplexer features three-state outputs that can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level.
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7.0 | V |
| Input voltage | $V_{IN}$ | 7.0 | V |
| Output voltage (off-state) | $V_{O(off)}$ | 5.5 | V |
| Operating temperature range | $T_{opr}$ | −20~+75 | ℃ |
| Storage temperature range | $T_{stg}$ | −65~+150 | ℃ |

## ■FUNCTION TABLE

| Inputs | | | | Outputs |
|---|---|---|---|---|
| OC | S | A | B | |
| H | × | × | × | Z |
| L | L | L | × | L |
| L | L | H | × | H |
| L | H | × | L | L |
| L | H | × | H | H |

Note) H; high level, L; low level, X; irrelevant
Z; off (high-impedance) state of a 3-state output

## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20~+75℃)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | – | – | V |
| | | $V_{IL}$ | | | – | – | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−2.6mA | | 2.4 | – | – | V |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=8mA | – | – | 0.5 | V |
| | | | | $I_{OL}$=4mA | – | – | 0.4 | |
| Input current | S | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | – | – | 40 | μA |
| | S except | | | | – | – | 20 | |
| | S | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | – | – | −0.8 | mA |
| | S except | | | | – | – | −0.4 | |
| | S | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | – | – | 0.2 | mA |
| | S except | | | | – | – | 0.1 | |
| Output current | | $I_{OZ}$ | $V_{CC}$=5.25V, $V_{IH}$=2V | $V_O$=2.4V | – | – | 20 | μA |
| | | | | $V_O$=0.4V | – | – | −20 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$=5.25V | | −30 | – | −130 | mA |
| Supply current** | All outputs high | $I_{CC}$ | $V_{CC}$=5.25V | | – | 5.9 | 10 | mA |
| | All outputs low | | | | – | 9.2 | 16 | |
| | All outputs off | | | | – | 10 | 19 | |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | – | – | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C
** $I_{CC}$ is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

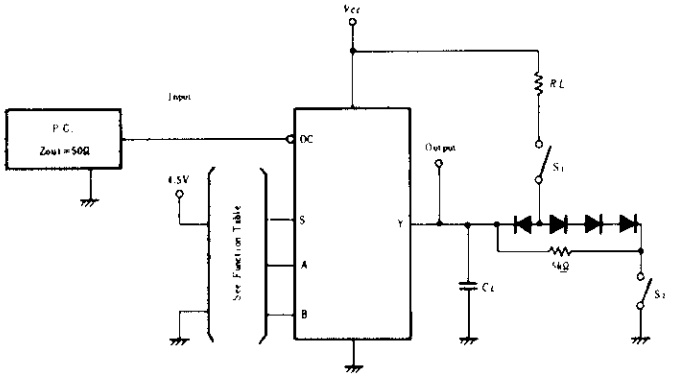
Home Print

## ■SWITCHING CHARACTERISTICS ( $V_{CC}$=5V, $Ta$=25℃ )

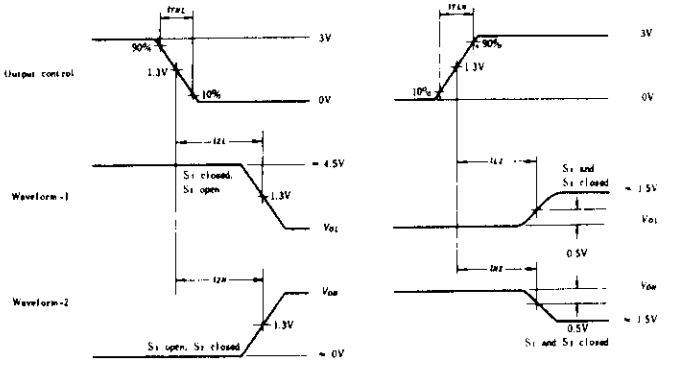
| Item | Inputs | Output | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | A, B | Y | $t_{PLH}$ | $R_L$=2kΩ<br>$C_L$=15pF | – | 12 | 18 | ns |
| | | | $t_{PHL}$ | | – | 12 | 18 | |
| | S | Y | $t_{PLH}$ | | – | 14 | 21 | ns |
| | | | $t_{PHL}$ | | – | 14 | 21 | |
| Output enable time | OC | Y | $t_{ZH}$ | | – | 20 | 30 | ns |
| | | | $t_{ZL}$ | | – | 20 | 30 | |
| Output disable time | OC | Y | $t_{HZ}$ | $R_L$=2kΩ<br>$C_L$=5pF | – | 18 | 30 | ns |
| | | | $t_{LZ}$ | | – | 16 | 25 | |

## ■TESTING METHOD

1) Test Circuit




Waveform




Notes) 1. Input pulse: $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz, duty cycle = 50%.
2. $C_L$ includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ.
4. Waveform-1 is for an output with internal conditions such that the output is low except when disabled by the output control.
5. Waveform-2 is for an output with internal conditions such that the output is high except when disabled by the output control.

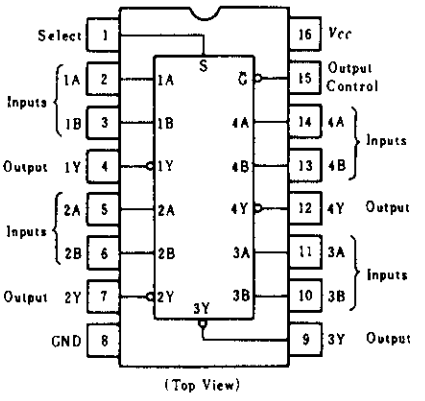


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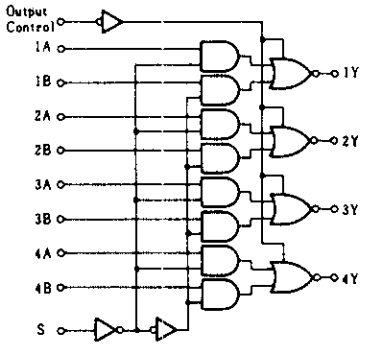
# HD74LS258 ●Quadruple 2-line-to-1-line Data Selectors/Multiplexers (with three-state outputs)

This multiplexer features three-state outputs that can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level.
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■FUNCTION TABLE

| Input | | | | Output |
|---|---|---|---|---|
| OC | S | A | B | Y |
| H | X | X | X | Z |
| L | L | L | X | H |
| L | L | H | X | L |
| L | H | X | L | H |
| L | H | X | H | L |

Note) H; high level, L; low level, X; irrelevant
Z; off (high-impedance) state of a 3-state output

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Output current | $I_{OH}$ | — | — | −2.6 | mA |
| | $I_{OL}$ | — | — | 8 | mA |

## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75℃)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−2.6mA | | 2.4 | — | — | V |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | — | — | 0.4 | V |
| | | | | $I_{OL}$=8mA | — | — | 0.5 | V |
| Output current | | $I_{OZH}$ | $V_{CC}$=5.25V, $V_{IH}$=2V, $V_O$=2.4V | | — | — | 20 | μA |
| | | $I_{OZL}$ | $V_{CC}$=5.25V, $V_{IH}$=2V, $V_O$=0.4V | | — | — | −20 | μA |
| Input current | S | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 40 | μA |
| | except S | | | | — | — | 20 | μA |
| | S | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.8 | mA |
| | except S | | | | — | — | −0.4 | mA |
| | S | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.2 | mA |
| | except S | | | | — | — | 0.1 | mA |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$=5.25V | | −30 | — | −130 | mA |
| ** Supply current | All outputs high | $I_{CC}$ | $V_{CC}$=5.25V | | — | — | 7 | mA |
| | All outputs low | | | | — | — | 11 | mA |
| | All outputs off | | | | — | — | 12 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C
** $I_{CC}$ is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

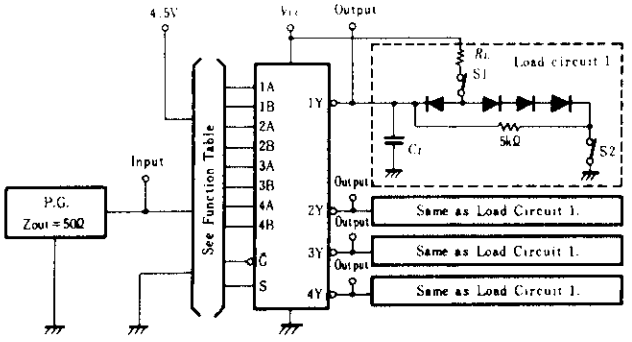
Home Print

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25℃)

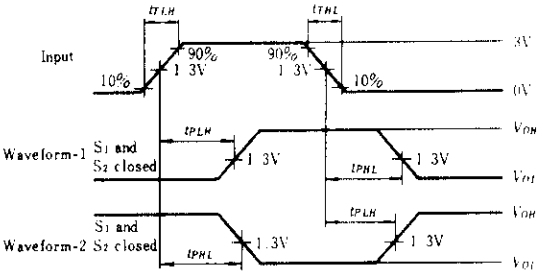
| Item | Symbol | Input | Output | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A, B | Y | $R_l$=2kΩ, $C_l$=15pF | — | 12 | 18 | ns |
| | $t_{PHL}$ | | | | — | 12 | 18 | ns |
| | $t_{PLH}$ | S | Y | | — | 14 | 21 | ns |
| | $t_{PHL}$ | | | | — | 14 | 21 | ns |
| Output enable time | $t_{ZH}$ | OUTPUT CONTROL | Y | | — | 20 | 30 | ns |
| | $t_{ZL}$ | | | | — | 20 | 30 | ns |
| Output disable time | $t_{HZ}$ | OUTPUT CONTROL | Y | $R_l$=2kΩ, $C_l$=5pF | — | 18 | 30 | ns |
| | $t_{LZ}$ | | | | — | 16 | 25 | ns |

## ■TESTING METHOD

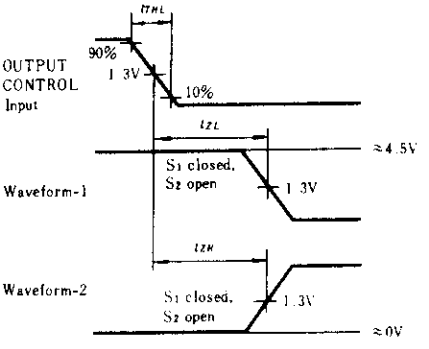
### 1) Test Circuit

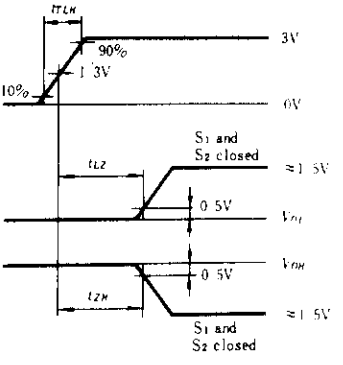



### Waveform




Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.




Notes) 1. Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR$=1MHz, duty cycle=50%
2. Waveform-1 is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform-2 is for an output with internal conditions such that the output is high except when disabled by the output control.



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# HD74LS259 ●8-bit Addressable Latches

This 8-bit addressable latch is designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. This is multifunctional device capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

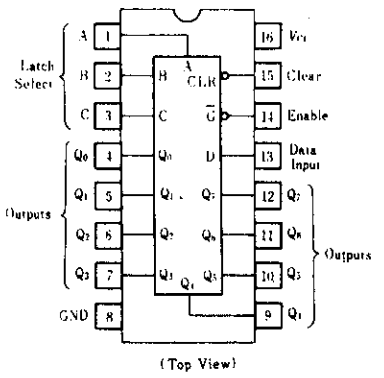
Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch.

The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, latch remains in their previous states and is unaffected by the data or address inputs.

To eliminate the possibility of entering erroneous data in the latch, the enable should be held high (inactive) while the address lines are changing.

In the clear mode, all outputs are low and unaffected by the address and data inputs.

## ■PIN ARRANGEMENT



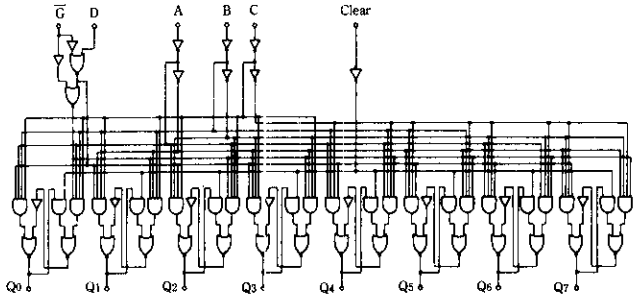

## ■FUNCTION TABLE

| Input | | Output of addressed latch | Each other output | Function |
|---|---|---|---|---|
| CLR | $\overline{G}$ | | | |
| H | L | D | Qio | Addressable latch |
| H | H | Qio | Qio | Memory |
| L | L | D | L | 8-line demultiplexer |
| L | H | L | L | Clear |

| Select inputs | | | Latch addressed |
|---|---|---|---|
| C | B | A | |
| L | L | L | 0 |
| L | L | H | 1 |
| L | H | L | 2 |
| L | H | H | 3 |
| H | L | L | 4 |
| H | L | H | 5 |
| H | H | L | 6 |
| H | H | H | 7 |

Notes) 1. H; high level, L; low level
2. D; the level at the data input
3. $O_{fo}$; the level of $Q_i$ (i=0, 1, ..... 7, as apropriate) before the indicated steady-state input conditions were established.

## ■BLOCK DIAGRAM




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Pulse width | | $t_w$ | 15 | — | — | ns |
| Setup time | Data | $t_{su}$ | 20 ↑ | — | — | ns |
| | Address | | 20 ↑ | — | — | |
| Hold time | Data | $t_h$ | 0 ↑ | — | — | ns |
| | Address | | 0 ↑ | — | — | |

↑; The arrow indicates that the rising edge of the enable pulse is used for reference.

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## ■ ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | — | — | 0.4 | V |
| | | | $I_{OL}=8mA$ | — | — | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}=5.25V$ | | — | 22 | 36 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

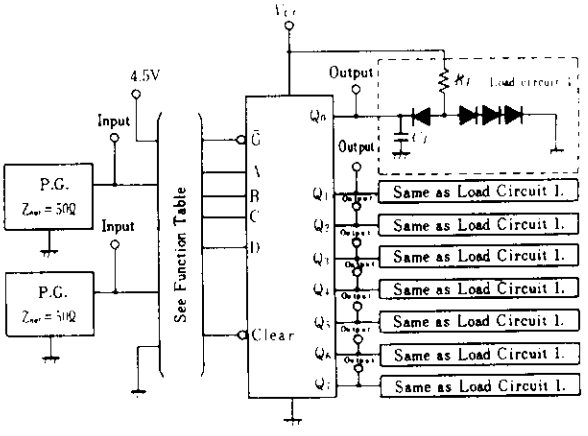
* $V_{CC}$=5V, $Ta$=25°C
** $I_{CC}$ is measured with all outputs open and all inputs grounded.

## ■ SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

| Item | Symbol | Inputs | Output | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PHL}$ | Clear | $Q_0 \sim Q_7$ | $C_L=15pF$, $R_L=2k\Omega$ | — | 17 | 27 | ns |
| | $t_{PLH}$ | Data | $Q_0 \sim Q_7$ | | — | 20 | 32 | ns |
| | $t_{PHL}$ | | | | — | 13 | 21 | |
| | $t_{PLH}$ | Address | $Q_0 \sim Q_7$ | | — | 24 | 38 | ns |
| | $t_{PHL}$ | | | | — | 18 | 29 | |
| | $t_{PLH}$ | Enable | $Q_0 \sim Q_7$ | | — | 22 | 35 | ns |
| | $t_{PHL}$ | | | | — | 15 | 24 | |

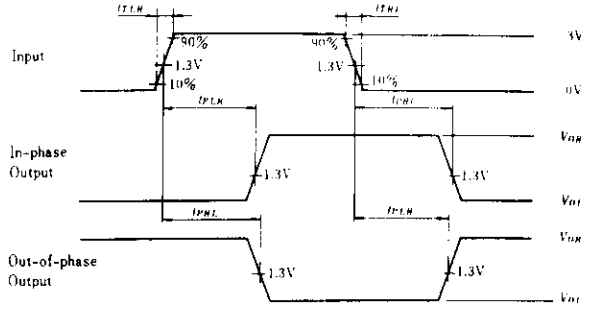
## ■ TESTING METHOD

### 1) Test Circuit




Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

### Waveform



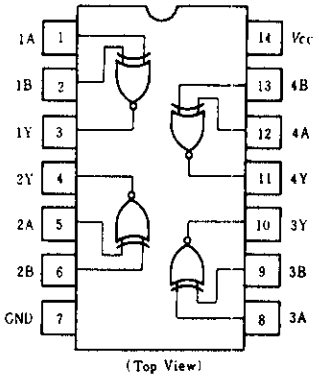

Input pulse; $t_{TLH} \leqq 15ns$, $t_{THL} \leqq 6ns$, $PRR=1MHz$ duty cycle 50%.



Home Print

# HD74LS266 ●Quadruple 2-input Exclusive-NOR Gates (with open collector outputs)

## ■PIN ARRANGEMENT



(Top View)

## ■FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | H |

H; high level, L; low level

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| High level output voltage | $V_{OH}$ | — | — | 5.5 | V |
| Low level output current | $I_{OL}$ | — | — | 8 | mA |

## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75℃)

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | |
| Output current | $I_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $V_{OH}$=5.5V | | — | — | 100 | μA |
| Output voltage | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | — | — | 0.4 | V |
| | | | $I_{OL}$=8mA | — | — | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 40 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.8 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.2 | mA |
| Supply current | $I_{CC}$** | $V_{CC}$=5.25V | | — | 8 | 13 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C
** $I_{CC}$ is measured with one input of each gate at 4.5V, the other inputs grounded, and the outputs open.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25℃)

| Item | Symbol | Inputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A or B | $C_L$=15pF, $R_L$=2kΩ | — | 18 | 30 | ns |
| | $t_{PHL}$ | | | — | 18 | 30 | |
| | $t_{PLH}$ | A or B | | — | 18 | 30 | |
| | $t_{PHL}$ | | | — | 18 | 30 | |

Note) Refer to Test Circuit and Waveform of the Common Item

Home Print

# HD74LS273 ●Octal D-type Positive-edge-triggered Flip-Flops (with Clear)

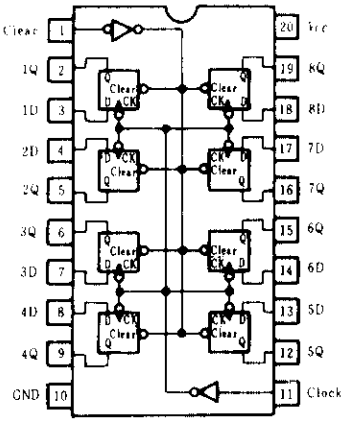
The HD74LS273, positive-edge-triggered flip-flops utilize LS TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse.

Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse.

When the clock input is at either the high or low level, the D input signal has no effect at the output.

## ■PIN ARRANGEMENT



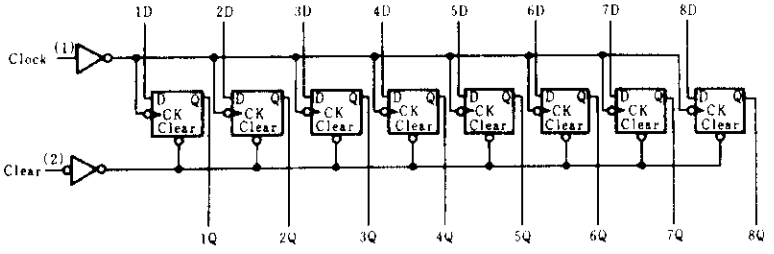

(Top View)

## ■FUNCTION TABLE

| Inputs | | | Output |
|---|---|---|---|
| Clear | Clock | D | Q |
| L | × | × | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | × | $Q_0$ |

Notes; H = high level, L = low level,
X = irrelevant
↑ = transition from low to high level
$Q_0$ = level of Q before the indicated steady-state input conditions were established.

## ■BLOCK DIAGRAM




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output current | | $I_{OH}$ | — | — | −400 | μA |
| | | $I_{OL}$ | — | — | 8 | mA |
| Clock frequency | | $f_{clock}$ | 0 | — | 30 | MHz |
| Clock and clear pulse width | | $t_w$ | 20 | — | — | ns |
| Setup time | Data | $t_{su}$ | 20 ↑ | — | — | ns |
| | Clear inactive-state | | 25 ↑ | — | — | |
| Data hold time | | $t_h$ | 5 ↑ | — | — | ns |

Note) ↑ : The arrow indicates the rising edge of clock pulse.



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## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | | 2.7 | — | | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, | $I_{OL}$=8mA | — | — | 0.5 | V |
| | | $V_{IL}$=0.8V | $I_{OL}$=4mA | — | — | 0.4 | |
| Input current | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.1 | mA |
| | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | — | −100 | mA |
| Supply current | $I_{CC}$** | $V_{CC}$=5.25V | | — | 17 | 27 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

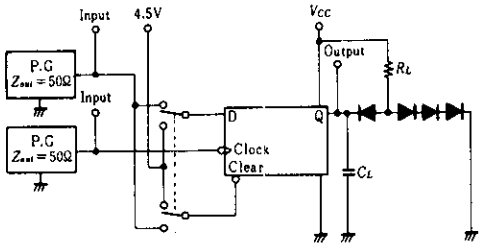
* $V_{CC}$=5V, $Ta$=25°C

** : With all outputs open and 4.5V applied to all data and clear inputs, $I_{CC}$ is measured after a momentary ground, then 4.5V is applied to clock.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

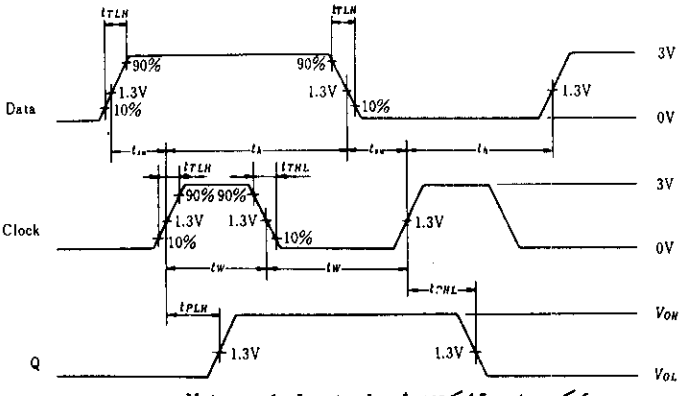
| Item | Symbol | Inputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | Clock | $C_L$=15pF, $R_L$=2kΩ | 30 | — | — | MHz |
| Propagation Delay Time | $t_{PHL}$ | Clear | | — | 18 | 27 | ns |
| | $t_{PLH}$ | Clock | | — | 17 | 27 | |
| | $t_{PHL}$ | | | — | 18 | 27 | |

## ■TESTING METHOD



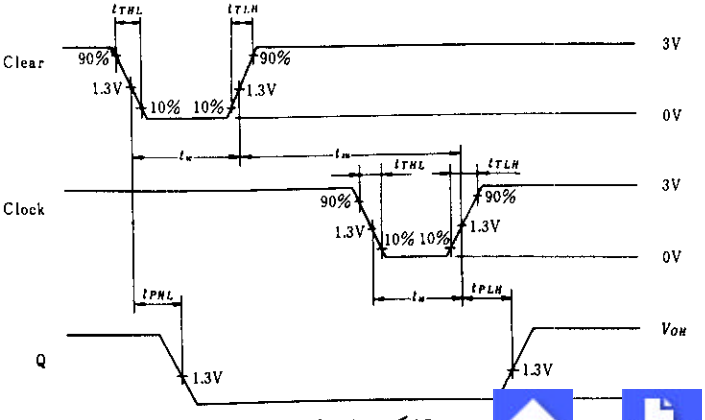

Notes: 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

Waveform-1




Notes: 1. Input pulse; $t_{TLH} \leqq 15$ns, $t_{TLH} \leqq 6$ns
Clock input; $PRR$ = 1MHz, duty cycle 50%
Data input; $PRR$ = 500kHz, duty cycle 50%

Waveform-2

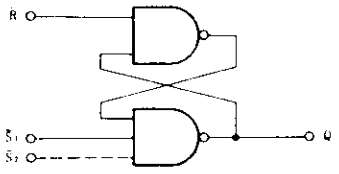



Note: Input pulse; $t_{TLH} \leqq 15$ns, $t_{TH}$ ... $PRR$ =

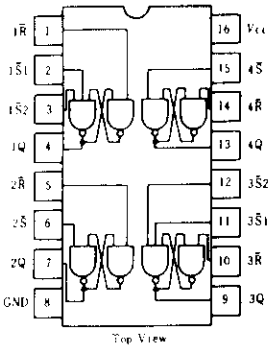
Home Print

# HD74LS279 ●Quadruple $\bar{S}$-$\bar{R}$ Latches

## ■BLOCK DIAGRAM(¼)




## ■PIN ARRANGEMENT




## ■FUNCTION TABLE

| Inputs | | Outputs |
|---|---|---|
| $\bar{S}$** | R | Q |
| H | H | $Q_0$ |
| L | H | H |
| H | L | L |
| L | L | H* |

Notes) 1. H; high level, L; low level
2. $Q_0$; The level of Q before the indicated input conditions were established.
3. *; This output level is psodo stable; that is, it may not persist when $\bar{S}$ and $\bar{R}$ inputs return to their inactive (high) level.
4. **; For latches with double $\bar{S}$ inputs: H; both $\bar{S}$ inputs high, L; one or both $\bar{S}$ inputs low.

## ■ELECTRICAL CHARACTERISTICS ($Ta=-20\sim+75℃$)

| Item | Symbol | Test Conditions | min | typ* | max | Unit |
|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | 2.0 | — | — | V |
| | $V_{IL}$ | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | 2.7 | — | — | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OL}$=4mA | — | — | 0.4 | V |
| | | $I_{OL}$=8mA | — | — | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | — | — | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | — | — | −0.6 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | — | — | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | −20 | — | −100 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}$=5.25V | — | 3.8 | 7 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IK}$=−18mA | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C
** $I_{CC}$ is measured with all $\bar{R}$ inputs grounded, all $\bar{S}$ inputs at 4.5V, and all outputs open.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25℃)

| Item | Symbol | Inputs | Output | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $\bar{S}$ | Q | $C_L$=15pF, $R_L$=2kΩ | — | 12 | 22 | ns |
| | $t_{PHL}$ | | | | — | 13 | 21 | ns |
| | $t_{PHL}$ | $\bar{R}$ | | | — | 15 | 27 | ns |

Note) Refer to Test Circuit and Waveform of the Common Item

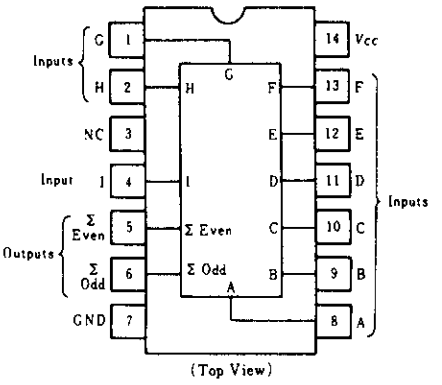


Home Print

# HD74LS280 ●9-bit Odd/Even Parity Generators/Checkers

This parity generator/checker offers the designer a trade-off between reduced power consumption and high performance. Although the HD74LS280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3.

## ■PIN ARRANGEMENT

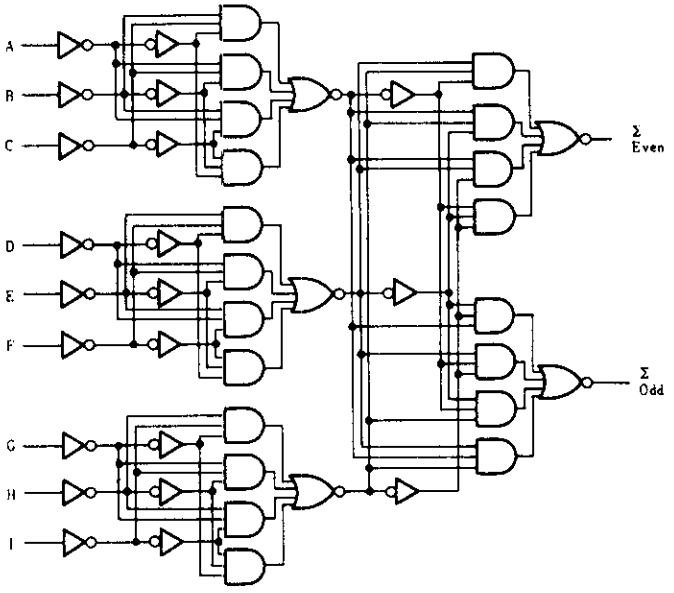


(Top View)

## ■FUNCTION TABLE

| Number of inputs A through I that are high | Outputs | |
|---|---|---|
| | Σ Even | Σ Odd |
| 0, 2, 4, 6, 8 | H | L |
| 1, 3, 5, 7, 9 | L | H |

## ■BLOCK DIAGRAM




## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | | 2.7 | — | — | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | — | — | 0.4 | V |
| | | | $I_{OL}$=8mA | — | — | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | — | −100 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}$=5.25V | | — | 16 | 27 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C
** $I_{CC}$ is measured with all outputs open and all inputs grounded.

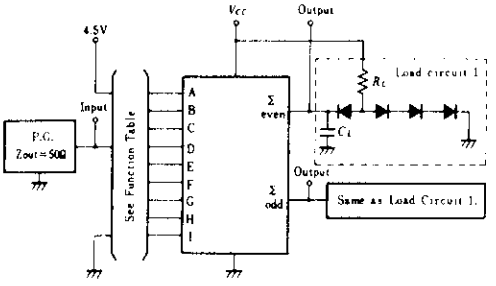
Home Print

## ■ SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | Σ Even | $C_L$=15pF, $R_L$=2kΩ | — | 33 | 50 | ns |
| | $t_{PHL}$ | | | — | 29 | 45 | ns |
| | $t_{PLH}$ | Σ Odd | | — | 23 | 45 | ns |
| | $t_{PHL}$ | | | — | 31 | 50 | ns |

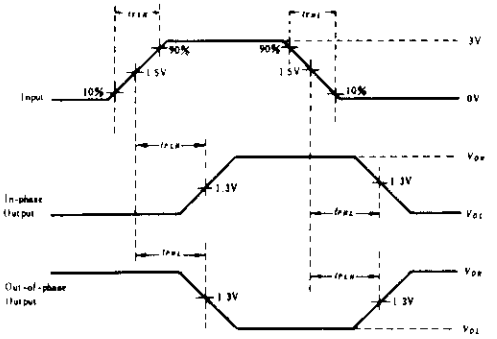
## ■ TESTING METHOD

### 1) Test circuit




Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ

### Waveform




Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns,
$PRR$=1MHz, duty cycle 50%.



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# HD74LS283 ●4-bit Binary Full Adders

The HD74LS283 adder is electrically and functionally identical to the HD74LS83A, respectively; only the arrangement of the terminals has been changed.

This improved full adder performs the addition of two 4-bit binary words.

The sum (Σ) outputs are provided for each bit and the resultant carry ($C_4$) is obtained from the fourth bit. This adder features full internal look-ahead across all four bits generating the carry term in then nanoseconds.

The adder logic, including the carry, is implemented in its true form.

End arround carry can be accomplished without the need for logic or level inversion.

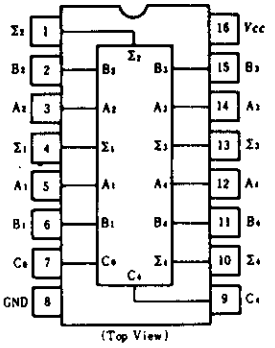
## ■FUNCTION TABLE

| Inputs | | | | Outputs | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | When $C_0$=L | | | When $C_0$=H | | |
| | | | | | | When $C_2$=L | | | When $C_2$=H |
| $A_1$ / $A_3$ | $B_1$ / $B_3$ | $A_2$ / $A_4$ | $B_2$ / $B_4$ | $\Sigma_1$ / $\Sigma_3$ | $\Sigma_2$ / $\Sigma_4$ | $C_2$ / $C_4$ | $\Sigma_1$ / $\Sigma_3$ | $\Sigma_1$ / $\Sigma_4$ | $C_2$ / $C_4$ |
| L | L | L | L | L | L | L | H | L | L |
| H | L | L | L | H | L | L | L | H | L |
| L | H | L | L | H | L | L | L | H | L |
| H | H | L | L | L | H | L | H | H | L |
| L | L | H | L | L | H | L | H | H | L |
| H | L | H | L | H | H | L | L | L | H |
| L | H | H | L | H | H | L | L | L | H |
| H | H | H | L | L | L | H | H | L | H |
| L | L | L | H | L | H | L | H | H | L |
| H | L | L | H | H | H | L | L | L | H |
| L | H | L | H | H | H | L | L | L | H |
| H | H | L | H | L | L | H | H | L | H |
| L | L | H | H | L | L | H | H | L | H |
| H | L | H | H | H | L | H | L | H | H |
| L | H | H | H | H | L | H | L | H | H |
| H | H | H | H | L | H | H | H | H | H |

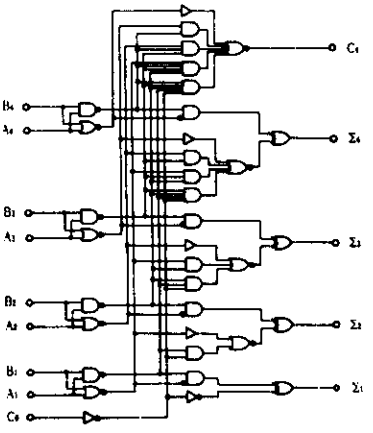
H; high level, L; low level

Notes) Input conditions at $A_1$, $B_1$, $A_2$, $B_2$, and $C_0$ are use to determine outputs $\Sigma_1$ and $\Sigma_2$ and the value of the internal carry $C_2$. The values at $C_2$, $A_3$, $B_3$, $A_4$, and $B_4$ are then used to determine outputs $\Sigma_3$, $\Sigma_4$, and $C_4$.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




Home Print

## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | — | — | 0.4 | V |
| | | | | $I_{OL}$=8mA | — | — | 0.5 | |
| Input current | except $C_0$ | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 40 | μA |
| | $C_0$ | | | | — | — | 20 | |
| | except $C_0$ | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.8 | mA |
| | $C_0$ | | | | — | — | −0.4 | |
| | except $C_0$ | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.2 | mA |
| | $C_0$ | | | | — | — | 0.1 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | — | −100 | mA |
| Supply current | | $I_{CC}$ | $V_{CC}$=5.25V | All inputs grounded | — | 22 | 39 | mA |
| | | | | All B low, other inputs at 4.5V | — | 19 | 34 | |
| | | | | All inputs at 4.5V | — | 19 | 34 | |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

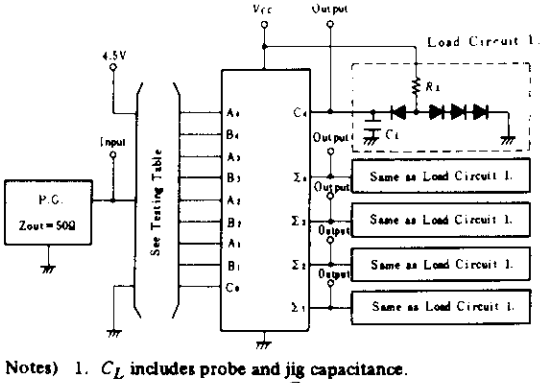
* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_0$ | Σi | $C_L$=15pF, $R_L$=2kΩ | — | 16 | 24 | ns |
| | $t_{PHL}$ | | | | — | 15 | 24 | ns |
| | $t_{PLH}$ | Ai, Bi | Σi | | — | 15 | 24 | ns |
| | $t_{PHL}$ | | | | — | 15 | 24 | ns |
| | $t_{PLH}$ | $C_0$ | $C_4$ | | — | 11 | 17 | ns |
| | $t_{PHL}$ | | | | — | 11 | 22 | ns |
| | $t_{PLH}$ | Ai, Bi | $C_4$ | | — | 11 | 17 | ns |
| | $t_{PHL}$ | | | | — | 12 | 17 | ns |

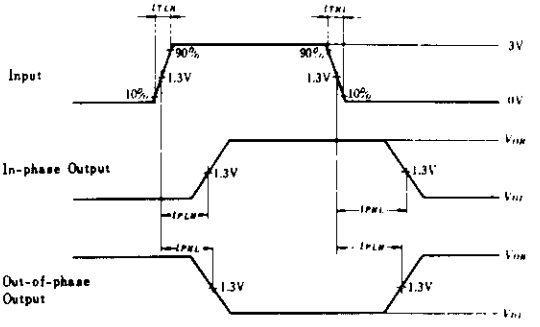
## ■TESTING METHOD

### 1) Test Circuit




Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

### Waveform




Input pulse; $t_{TLH}$≦15ns, $t_{THL}$≦6ns,
$PRR$=1MHz, duty cycle 50%.



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## 2) Testing Table

| Item | From input to output | Inputs | | | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $B_4$ | $A_4$ | $B_3$ | $A_3$ | $B_2$ | $A_2$ | $B_1$ | $A_1$ | $C_0$ | $C_4$ | $\Sigma_4$ | $\Sigma_3$ | $\Sigma_2$ | $\Sigma_1$ |
| $t_{PLH}$<br>$t_{PHL}$ | $C_0 \rightarrow \Sigma i$ or $C_4$ | GND | GND | GND | GND | GND | GND | GND | GND | IN | — | — | — | — | OUT |
| | | GND | 4.5V | GND | 4.5V | GND | 4.5V | GND | 4.5V | IN | OUT | OUT | OUT | OUT | OUT |
| | Ai or Bi $\rightarrow \Sigma i$ or $C_4$ | GND | GND | GND | GND | GND | GND | GND / IN | IN / GND | GND | — | — | — | — | OUT |
| | | GND | GND | GND | GND | GND / IN | IN / GND | GND | GND | GND | — | — | — | OUT | — |
| | | GND | GND | GND / IN | IN / GND | GND | GND | GND | GND | GND | — | — | OUT | — | — |
| | | GND / IN | IN / GND | GND | GND | GND | GND | GND | GND | GND | — | OUT | — | — | — |
| | | GND | GND | GND | GND | GND | GND | 4.5V / IN | IN / 4.5V | GND | — | — | — | OUT | OUT |
| | | GND | GND | GND | GND | 4.5V / IN | IN / 4.5V | GND | GND | GND | — | — | OUT | OUT | — |
| | | GND | GND | 4.5V / IN | IN / 4.5V | GND | GND | GND | GND | GND | — | OUT | OUT | — | — |
| | | 4.5V / IN | IN / 4.5V | GND | GND | GND | GND | GND | GND | GND | OUT | OUT | — | — | — |

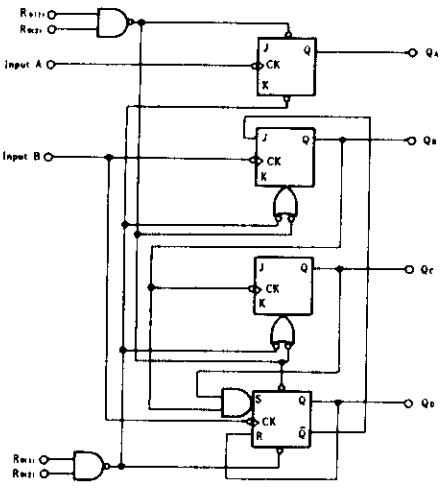
# HD74LS290 ●Decade Counters

This counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and divide-by-five counter.

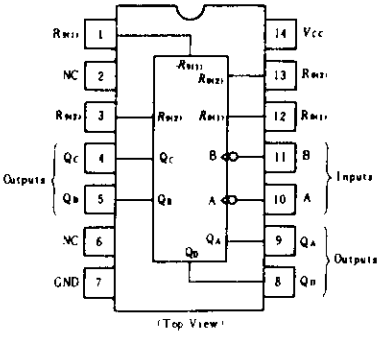
The HD74LS290 also has gated set-to-nine inputs for use in BCD nine's complement applications. To use the maximum count length of this counter, the B input is connected to the $Q_A$ output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table.

A symmetrical divide-by-ten count can be obtained from the HD74LS290 counter by connecting the $Q_D$ output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output $Q_A$.

## ■BLOCK DIAGRAM



## ■PIN ARRANGEMENT




## ■ABSOLUTE MAXIMUM RATINGS

| Item | | Symbol | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 7.0 | V |
| Input voltage | R Inputs | $V_{IN}$ | 7.0 | V |
| | A, B Inputs | | 5.5 | V |
| Operating temperature range | | $T_{opr}$ | −20 ~ +75 | °C |
| Storage temperature range | | $T_{stg}$ | −65 ~ +150 | °C |

## ■FUNCTION TABLE

### ● Reset/Count

| Reset Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| $R_{0(1)}$ | $R_{0(2)}$ | $R_{9(1)}$ | $R_{9(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | × | L | L | L | L |
| H | H | × | L | L | L | L | L |
| × | × | H | H | H | L | L | H |
| × | L | × | L | Count | | | |
| L | × | L | × | Count | | | |
| L | × | × | L | Count | | | |
| × | L | L | × | Count | | | |

### ● BCD Count Sequence (Notes 1)

| Count | Outputs | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

### ● Bi-Quinary Count Sequence (Notes 2)

| Count | Outputs | | | |
|---|---|---|---|---|
| | $Q_A$ | $Q_D$ | $Q_C$ | $Q_B$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

Notes) 1. Output $Q_A$ is connected to input B for BCD count.
2. Output $Q_D$ is connected to input A for bi-quinary count.
3. H; high level, L; low level, X; irrelevant

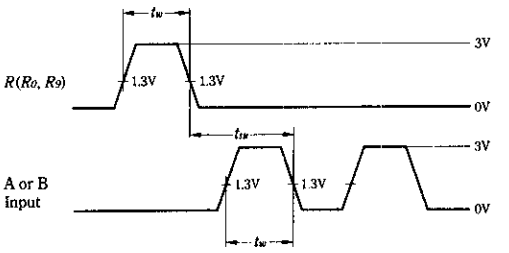


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## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Count frequency | A input | $f_{count}$ | 0 | — | 32 | MHz |
| | B input | | 0 | — | 16 | |
| Pulse width | A input | $t_w$ | 15 | — | — | ns |
| | B input | | 30 | — | — | |
| | Reset inputs | | 15 | — | — | |
| Setup time | | $t_{su}$ | 25 | — | — | ns |

## ■TIMING DEFINITION




## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA** | — | — | 0.4 | V |
| | | | | $I_{OL}$=8mA** | — | — | 0.5 | |
| Input current | Any Reset | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| | A input | | | | — | — | −2.4 | |
| | B input | | | | — | — | −3.2 | |
| | Any Reset | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | A input | | | | — | — | 40 | |
| | B input | | | | — | — | 80 | |
| | Any Reset | $I_I$ | $V_{CC}$=5.25V | $V_I$=7V | — | — | 0.1 | mA |
| | A input | | | $V_I$=5.5V | — | — | 0.2 | |
| | B input | | | | — | — | 0.4 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | — | −100 | mA |
| Supply current ••• | | $I_{CC}$ | $V_{CC}$=5.25V | | — | 9 | 15 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** $Q_A$ output is tested at specified $I_{OL}$ plus the limit value of $I_{IL}$ for the B input. This permits driving the B input while maintaining full fan-out capability.

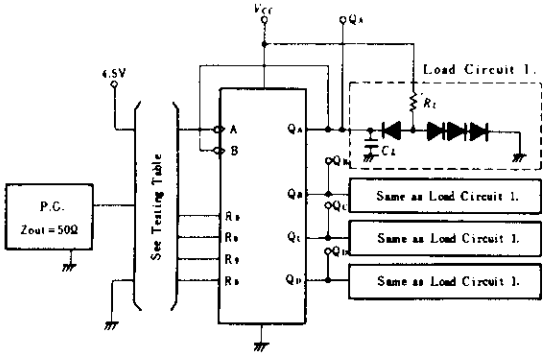
*** $I_{CC}$ is measured with all outputs open, both $R_0$ inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum count frequency | $f_{max}$ | A | $Q_A$ | $C_L$=15pF, $R_L$=2kΩ | 32 | 42 | — | MHz |
| | | B | $Q_B$ | | 16 | — | — | |
| Propagation delay time | $t_{PLH}$ | A | $Q_A$ | | — | 10 | 16 | ns |
| | $t_{PHL}$ | | | | — | 12 | 18 | |
| | $t_{PLH}$ | A | $Q_D$ | | — | 32 | 48 | ns |
| | $t_{PHL}$ | | | | — | 34 | 50 | |
| | $t_{PLH}$ | B | $Q_B$ | | — | 10 | 16 | ns |
| | $t_{PHL}$ | | | | — | 14 | 21 | |
| | $t_{PLH}$ | B | $Q_C$ | | — | 21 | 32 | ns |
| | $t_{PHL}$ | | | | — | 23 | 35 | |
| | $t_{PLH}$ | B | $Q_D$ | | — | 21 | 32 | ns |
| | $t_{PHL}$ | | | | — | 23 | 35 | |
| | $t_{PHL}$ | Set-to-0 | $Q_A$～$Q_D$ | | — | 26 | 40 | ns |
| | $t_{PLH}$ | Set-to-9 | $Q_A$, $Q_D$ | | — | 20 | 30 | ns |
| | $t_{PHL}$ | | $Q_B$, $Q_C$ | | — | 26 | 40 | |

## ■TESTING METHOD

### 1) Test Circuit



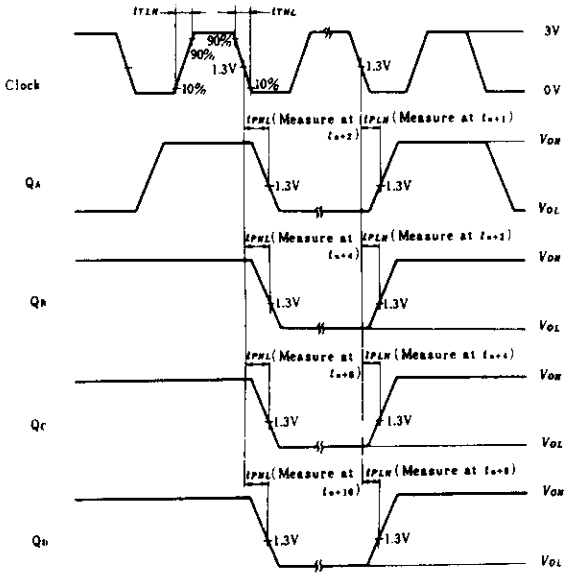

Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

### 2) Testing Table

| Item | From input to output | Inputs A | Inputs B | Inputs $R_0$ | Inputs $R_9$ | Outputs $Q_A$ | Outputs $Q_B$ | Outputs $Q_C$ | Outputs $Q_D$ |
|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | A→Q | IN | to $Q_A$ | GND | GND | OUT | OUT | OUT | OUT |
| | B→Q | 4.5V | IN | GND | GND | — | OUT | OUT | OUT |
| $t_{PLH}$ $t_{PHL}$ | A→$Q_A$ | IN | to $Q_A$ | GND | GND | OUT | — | — | — |
| | A→$Q_D$ | IN | to $Q_A$ | GND | GND | — | — | — | OUT |
| | B→$Q_B$ | 4.5V | IN | GND | GND | — | OUT | — | — |
| | B→$Q_C$ | 4.5V | IN | GND | GND | — | — | OUT | — |
| | B→$Q_D$ | 4.5V | IN | GND | GND | — | — | — | OUT |
| | $R_0$→Q** | IN* | to $Q_A$ | IN | GND | OUT | OUT | OUT | OUT |
| | $R_9$→Q** | IN* | to $Q_A$ | GND | IN | OUT | OUT | OUT | OUT |

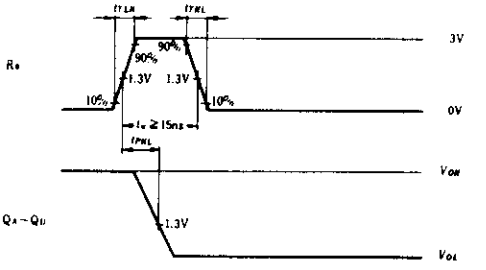
* For initialized
** Measured with each input and unused inputs at 4.5V.

### Waveform 1. $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Clock→Q)

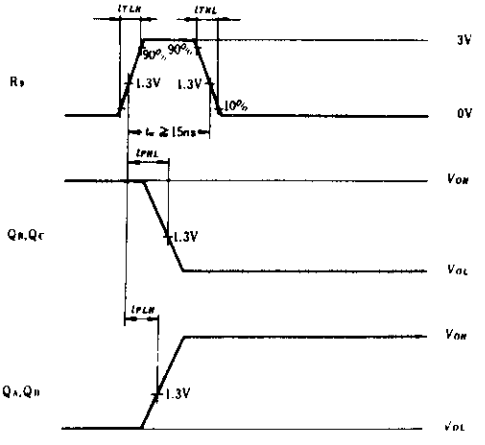



Notes) 1. Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 5$ns, $PRR$=1MHz, duty cycle=50% and: for $f_{max}$, $t_{TLH} = t_{THL} \leqq 2.5$ns.
2. $t_n$ is reference bit time when all outputs are low.

### Waveform 2. $t_{PHL}$ ($R_0$→Q)




### Waveform 3. $t_{PLH}$, $t_{PHL}$ ($R_9$→Q)



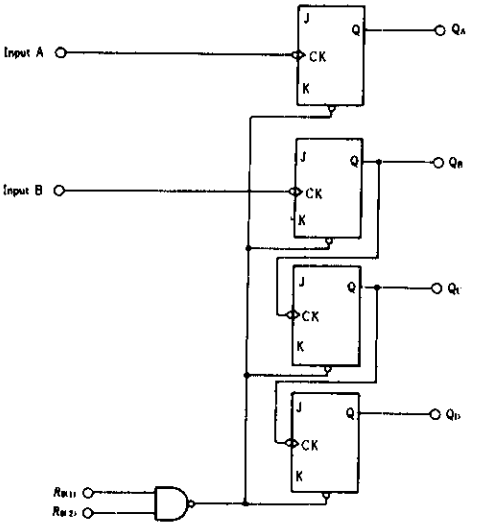



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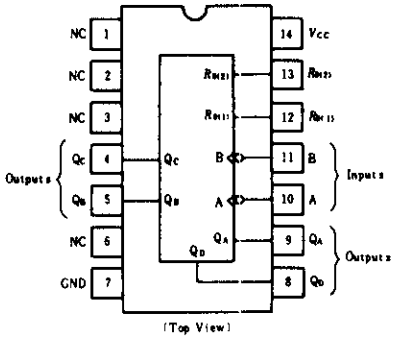
# HD74LS293 ●4-bit Binary Counters

This counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and divide-by-eight counter. This counter has a gated zero reset.To use the maximum count length of this counter, the B input is connected to the $Q_A$ output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




## ■ABSOLUTE MAXIMUM RATINGS

| Item | | Symbol | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 7.0 | V |
| Input voltage | $R_0$ Inputs | $V_{IN}$ | 7.0 | V |
| | A, B Inputs | | 5.5 | V |
| Operating temperature range | | $T_{opr}$ | −20～+75 | ℃ |
| Storage temperature range | | $T_{stg}$ | −65～+150 | ℃ |

## ■FUNCTION TABLE

### ● Reset/Count

| Reset Input | | Outputs | | | |
|---|---|---|---|---|---|
| $R_{0(1)}$ | $R_{0(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | L | L | L |
| L | × | Count | | | |
| × | L | Count | | | |

### ● BCD Count Sequence

| Count | Outputs | | | | Count | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ | | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L | 8 | H | L | L | L |
| 1 | L | L | L | H | 9 | H | L | L | H |
| 2 | L | L | H | L | 10 | H | L | H | L |
| 3 | L | L | H | H | 11 | H | L | H | H |
| 4 | L | H | L | L | 12 | H | H | L | L |
| 5 | L | H | L | H | 13 | H | H | L | H |
| 6 | L | H | H | L | 14 | H | H | H | L |
| 7 | L | H | H | H | 15 | H | H | H | H |

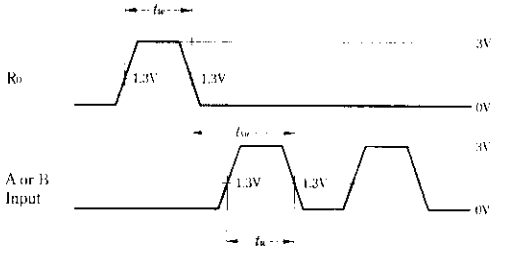
Notes) 1. H; high level, L; low level, X; irrelevant.
2. Output $Q_A$ is connected to input B.

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## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Output current | | $I_{OH}$ | — | — | −400 | μA |
| Output current | | $I_{OL}$ | — | — | 8 | mA |
| Count frequency | A input | $f_{count}$ | 0 | — | 32 | MHz |
| | B input | | 0 | — | 16 | |
| Pulse width | A input | $t_w$ | 15 | — | — | ns |
| | B input | | 30 | — | — | |
| | Reset inputs | | 15 | — | — | |
| Setup time | | $t_{su}$ | 25 | — | — | ns |

## ■TIMING DEFINITION




## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA** | — | — | 0.4 | V |
| | | | | $I_{OL}$=8mA** | — | — | 0.5 | |
| Input current | Any Reset | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| | A input | | | | — | — | −2.4 | |
| | B input | | | | — | — | −1.6 | |
| | Any Reset | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | A input | | | | — | — | 40 | |
| | B input | | | | — | — | 40 | |
| | Any Reset | $I_I$ | $V_{CC}$=5.25V | $V_I$=7V | — | — | 0.1 | mA |
| | A input | | | $V_I$=5.5V | — | — | 0.2 | |
| | B input | | | | — | — | 0.2 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | | −100 | mA |
| Supply current*** | | $I_{CC}$ | $V_{CC}$=5.25V | | — | 9 | 15 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** $Q_A$ output is tested at specified $I_{OL}$ plus the limit value of $I_{IL}$ for the B input. This permits driving the B input while maintaining full fan-out capability.

*** $I_{CC}$ is measured with all outputs open, both $R_0$ inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

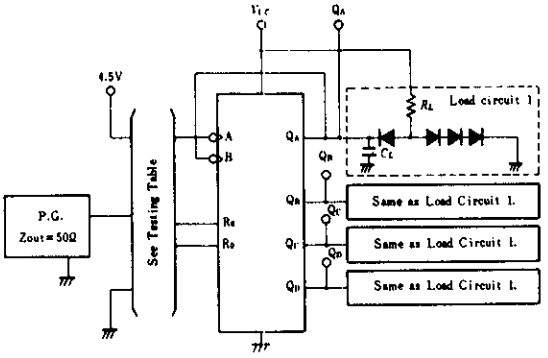
| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum count frequency | $f_{max}$ | A | $Q_A$ | $C_L$=15pF, $R_L$=2kΩ | 32 | 42 | — | MHz |
| | | B | $Q_B$ | | 16 | — | — | |
| Propagation delay time | $t_{PLH}$ | A | $Q_A$ | | — | 10 | 16 | ns |
| | $t_{PHL}$ | | | | — | 12 | 18 | |
| | $t_{PLH}$ | A | $Q_D$ | | — | 46 | 70 | ns |
| | $t_{PHL}$ | | | | — | 46 | 70 | |
| | $t_{PLH}$ | B | $Q_B$ | | — | 10 | 16 | ns |
| | $t_{PHL}$ | | | | — | 14 | 21 | |
| | $t_{PLH}$ | B | $Q_C$ | | — | 21 | 32 | ns |
| | $t_{PHL}$ | | | | — | 23 | 35 | |
| | $t_{PLH}$ | B | $Q_D$ | | — | 34 | 51 | ns |
| | $t_{PHL}$ | | | | — | 34 | 51 | |
| | $t_{PHL}$ | Set-to-0 | $Q_A$～$Q_D$ | | — | 26 | 40 | ns |



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## ■TESTING METHOD

### 1) Test Circuit



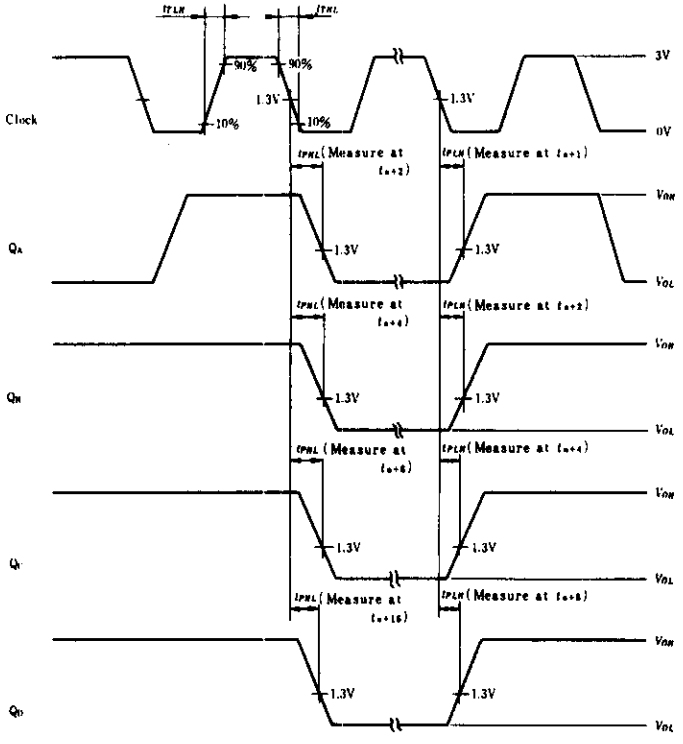

Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

### 2) Testing Table

| Item | From input to output | Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|
| | | A | B | $R_0$ | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| $f_{max}$ | A→Q | IN | to $Q_A$ | GND | OUT | OUT | OUT | OUT |
| | B→Q | 4.5V | IN | GND | — | OUT | OUT | OUT |
| $t_{PLH}$ $t_{PHL}$ | A→$Q_A$ | IN | to $Q_A$ | GND | OUT | — | — | — |
| | A→$Q_D$ | IN | to $Q_A$ | GND | — | — | — | OUT |
| | B→$Q_B$ | 4.5V | IN | GND | — | OUT | — | — |
| | B→$Q_C$ | 4.5V | IN | GND | — | — | OUT | — |
| | B→$Q_D$ | 4.5V | IN | GND | — | — | — | OUT |
| | $R_0$→Q** | IN* | to $Q_A$ | IN | OUT | OUT | OUT | OUT |

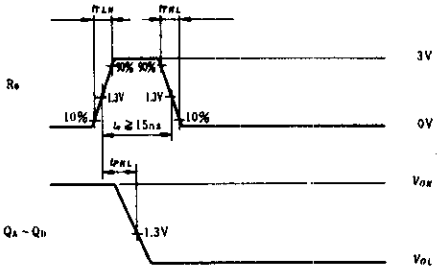
* For initialized.
** Measured with each input and unused inputs at 4.5V.

### Waveform 1. $f_{max}$, $t_{PLH}$, $t_{PHL}$ (Clock→Q)




Notes) 1. Input pulse: $t_{TLH}$≦15ns, $t_{THL}$≦5ns, $PRR$=1MHz, duty cycle=50% and: for $f_{max}$, $t_{TLH}$=$t_{THL}$≦2.5ns.
2. $t_n$ is reference bit time when all outputs are low.

### Waveform 2. $t_{PHL}$ ($R_0$→Q)



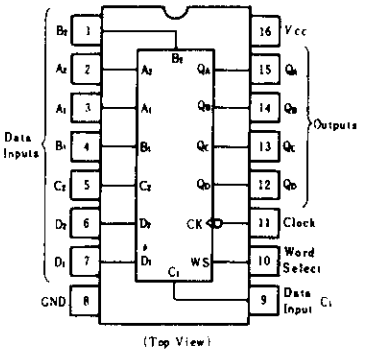

Note) $t_{TLH}$≦15ns, $t_{THL}$≦5ns

Home Print

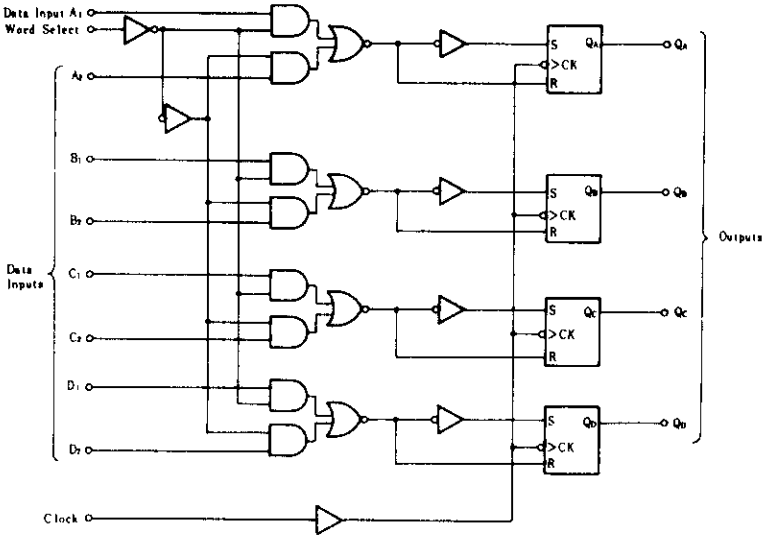
# HD74LS298 ●Quadruple 2-input Multiplexers (with storage)

This quadruple two-input multiplexer with storage provides essentially the equivalent functional capabilities of two separate MSI functions (HD74LS157 and HD74LS175). When the word-select input is low, word 1 ($A_1$, $B_1$, $C_1$, $D_1$) is applies to the flip-flops. A high input to word select will cause the selection of word 2 ($A_2$, $B_2$, $C_2$, $D_2$). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM




## ■FUNCTION TABLE

| Inputs | | Outputs | | | |
|---|---|---|---|---|---|
| Word Select | Clock | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| L | ↓ | $a_1$ | $b_1$ | $c_1$ | $d_1$ |
| H | ↓ | $a_2$ | $b_2$ | $c_2$ | $d_2$ |
| X | H | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |

Notes) 1. H; high level, L; low level, X; irrelevant (any input, including transition)
2. ↓; transition from high to low level
3. $a_1$, $a_2$, etc; the level of steady-state input at $A_1$, $A_2$, etc.
4. $Q_{A0}$, $Q_{B0}$, etc; the level of $Q_A$, $Q_B$, etc. entered on the most-recent ↓ transition of the clock input.

## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Clock pulse width | | $t_{w(CK)}$ | 20 | — | — | ns |
| Setup time | Data | $t_{su}$ | 15 | — | — | ns |
| | Word Select | | 25 | — | — | |
| Hold time | Data | $t_h$ | 5 | — | — | ns |
| | Word Select | | 0 | — | — | |



Home Print

## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | | 2.7 | — | — | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | — | — | 0.4 | V |
| | | | $I_{OL}$=8mA | — | — | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | — | −100 | mA |
| Supply current ** | $I_{CC}$ | $V_{CC}$=5.25V | | — | 13 | 21 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

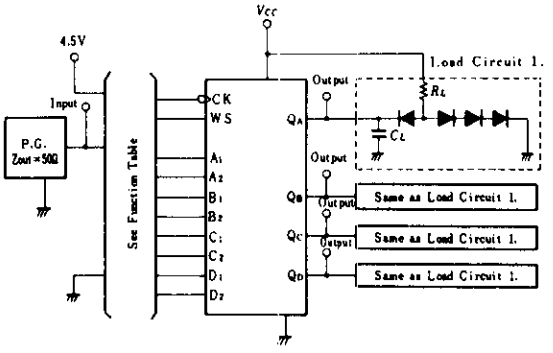
** With all outputs open and all inputs except clock low, $I_{CC}$ is measured after applying a momentary 4.5V, followed by ground, to the clock input.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$=15pF, $R_L$=2kΩ | — | 18 | 27 | ns |
| | $t_{PHL}$ | | — | 21 | 32 | ns |

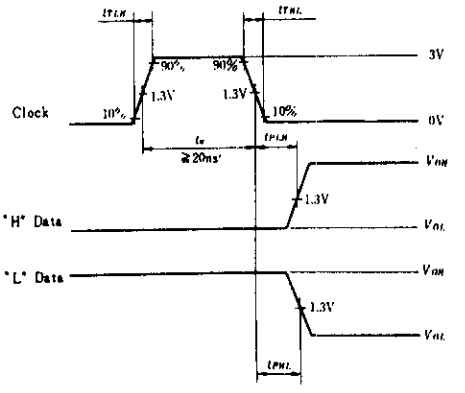
## ■TESTING METHOD

### 1) Test Circuit




Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

### Waveform




Input pulse; $t_{TLH}$≦15ns, $t_{THL}$≦6ns, $PRR$=1MHz.

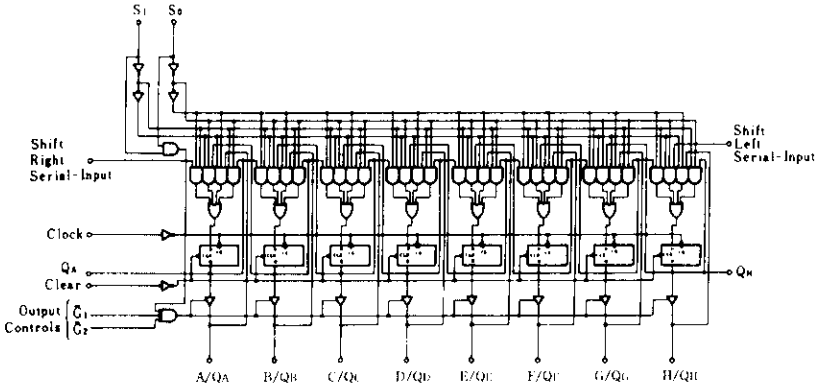
Home Print

# HD74LS299 ●8-bit Universal Shift/Storage Registers (with three-state outputs)

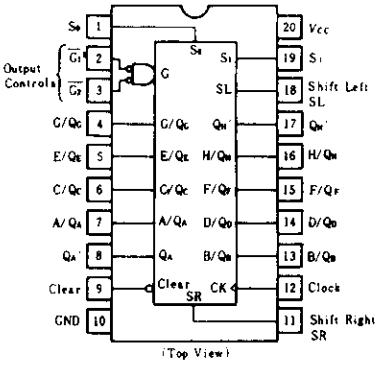
This eight-bit universal register features multiplexed inputs/outputs to achieve full eight bit data. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function select lines, $S_0$ and $S_1$, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




## ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7.0 | V |
| Input voltage | $V_{IN}$ | 7.0 | V |
| Output voltage (off-state) | $V_{O(off)}$ | 5.5 | V |
| Operating temperature range | $T_{opr}$ | −20～+75 | ℃ |
| Storage temperature range | $T_{stg}$ | −65～+150 | ℃ |

## ■FUNCTION TABLE

| Mode | Inputs | | | | | | | | Inputs/Outputs | | | | | | | | Outputs | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Clear | Function Select | | Output Control | | Clock | Serial | | A/$Q_A$ | B/$Q_B$ | C/$Q_C$ | D/$Q_D$ | E/$Q_E$ | F/$Q_F$ | G/$Q_G$ | H/$Q_H$ | $Q_A'$ | $Q_H'$ |
| | | $S_1$ | $S_0$ | $\overline{G}_1$ ↑ | $\overline{G}_2$ ↑ | | $S_L$ | $S_R$ | | | | | | | | | | |
| Clear | L | × | L | L | L | × | × | × | L | L | L | L | L | L | L | L | L | L |
| | L | L | × | L | L | × | × | × | L | L | L | L | L | L | L | L | L | L |
| Hold | H | L | L | L | L | × | × | × | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $Q_{E0}$ | $Q_{F0}$ | $Q_{G0}$ | $Q_{H0}$ | $Q_{A0}$ | $Q_{H0}$ |
| | H | × | × | L | L | L | × | × | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $Q_{E0}$ | $Q_{F0}$ | $Q_{G0}$ | $Q_{H0}$ | $Q_{A0}$ | $Q_{H0}$ |
| Shift Right | H | L | H | L | L | ↑ | × | H | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | H | $Q_{Gn}$ |
| | H | L | H | L | L | ↑ | × | L | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | L | $Q_{Gn}$ |
| Shift Left | H | H | L | L | L | ↑ | H | × | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | $Q_{Hn}$ | H | $Q_{Bn}$ | H |
| | H | H | L | L | L | ↑ | L | × | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | $Q_{Hn}$ | L | $Q_{Bn}$ | L |
| Load | H | H | H | × | × | ↑ | × | × | a | b | c | d | e | f | g | h | a | h |

Notes) 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. a~h; the level of steady-state input at inputs A through H, respectively. These data are loaded into the flip-flop outputs are isolated from the input/output terminals.
4. $Q_{A0}$~$Q_{H0}$; the level of $Q_A$ through $Q_H$, respectively, before the indicated steady-state input conditions were established.
5. $Q_{An}$~$Q_{Hn}$; the level of $Q_A$ through $Q_H$, respectively, before the most-recent ↑ transition of the clock.
6. ↑ =; When one or both output controls are high the eight input/output terminals are desabled to the high-impedance state, however, sequential operation or clearing of the register is not affected.



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## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Output current | $Q_A$~$Q_H$ | $I_{OH}$ | — | — | −2.6 | mA |
| | $Q_A'$ or $Q_H'$ | | — | — | −0.4 | |
| Output current | $Q_A$~$Q_H$ | $I_{OL}$ | — | — | 24 | mA |
| | $Q_A'$ or $Q_H'$ | | — | — | 8 | |
| Clock frequency | | $f_{clock}$ | 0 | — | 25 | MHz |
| Clock pulse width | Clock high | $t_{w(CK)}$ | 30 | — | — | ns |
| | Clock low | | 10 | — | — | |
| Clear pulse width | Clear low | $t_{w(CLR)}$ | 20 | — | — | ns |
| Setup time | Select | $t_{su}$ | 35 ↑ | — | — | ns |
| | High-level data | | 20 ↑ | — | — | |
| | Low-level data | | 20 ↑ | — | — | |
| | Clear inactive-state | | 20 ↑ | — | — | |
| Hold time | Select | $t_h$ | 10 ↑ | — | — | ns |
| | Data | | 10 ↑ | — | — | |

↑ The arrow indicates the rising edge.

## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20~+75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $Q_A$ thru $Q_H$ | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OH}$=−2.6mA | 2.4 | — | — | V |
| | $Q_A'$ or $Q_H'$ | | | $I_{OH}$=−400μA | 2.7 | — | — | |
| | $Q_A$ thru $Q_H$ | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=12mA | — | — | 0.4 | V |
| | $Q_A'$ or $Q_H'$ | | | $I_{OL}$=24mA | — | — | 0.5 | |
| | | | | $I_{OL}$=4mA | — | — | 0.4 | |
| | | | | $I_{OL}$=8mA | — | — | 0.5 | |
| Output current | $Q_A$ thru $Q_H$ | $I_{OZH}$ | $V_{CC}$=5.25V, $V_{IH}$=2V, $V_O$=2.7V | | — | — | 40 | μA |
| | $Q_A$ thru $Q_H$ | $I_{OZL}$ | $V_{CC}$=5.25V, $V_{IH}$=2V, $V_O$=0.4V | | — | — | −400 | μA |
| Input current | $S_0$, $S_1$, A~H | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 40 | μA |
| | Any other | | | | — | — | 20 | |
| | $S_0$, $S_1$ | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.8 | mA |
| | Any other | | | | — | — | −0.4 | |
| | $S_0$, $S_1$ | $I_I$ | $V_{CC}$=5.25V | $V_I$=7V | — | — | 0.2 | mA |
| | A~H | | | $V_I$=5.5V | — | — | 0.1 | |
| | Any other | | | $V_I$=7V | — | — | 0.1 | |
| Short-circuit output current | $Q_A$ thru $Q_H$ | $I_{OS}$ | $V_{CC}$=5.25V | | −30 | — | −130 | mA |
| | $Q_A'$ or $Q_H'$ | | | | −20 | — | −100 | |
| Supply current | | $I_{CC}$ | $V_{CC}$=5.25V | | — | 33 | 53 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$ = 5V, $Ta$ = 25°C

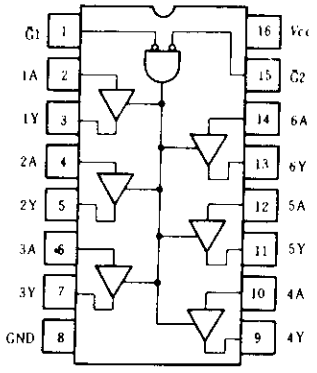
## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | | | $C_L$=15pF, $R_L$=2kΩ | 25 | 35 | — | MHz |
| Propagation delay time | $t_{PLH}$ | Clock | $Q_A'$ or $Q_H'$ | | — | 22 | 33 | ns |
| | $t_{PHL}$ | | | | — | 26 | 39 | |
| | $t_{PHL}$ | Clear | $Q_A'$ or $Q_H'$ | | — | 27 | 40 | |
| | $t_{PLH}$ | Clock | $Q_A$~$Q_H$ | $C_L$=45pF, $R_L$=665Ω | — | 17 | 25 | ns |
| | $t_{PHL}$ | | | | — | 26 | 39 | |
| | $t_{PHL}$ | Clear | $Q_A$~$Q_H$ | | — | 26 | 40 | ns |
| Output enable time | $t_{ZH}$ | $\overline{G}_1$, $\overline{G}_2$ | $Q_A$~$Q_H$ | | — | 13 | 21 | ns |
| | $t_{ZL}$ | | | | — | 19 | 30 | |
| Output disable time | $t_{HZ}$ | $\overline{G}_1$, $\overline{G}_2$ | $Q_A$~$Q_H$ | $C_L$=5pF, $R_L$=665Ω | — | 10 | 15 | ns |
| | $t_{LZ}$ | | | | — | 10 | 15 | |

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# HD74LS365A ●Hex Bus Drivers (with three-state outputs)

## ■PIN ARRANGEMENT



(Top View)

## ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7.0 | V |
| Input voltage | $V_{IN}$ | 7.0 | V |
| Output voltage (Off-state) | $V_{O(off)}$ | 5.5 | V |
| Operating temperature range | $T_{opr}$ | −20～+75 | ℃ |
| Storage temperature range | $T_{stg}$ | −65～+150 | ℃ |

## ■FUNCTION TABLE

| Inputs | | | Output |
|---|---|---|---|
| $\bar{G}_1$ | $\bar{G}_2$ | A | Y |
| H | × | × | Z |
| × | H | × | Z |
| L | L | L | L |
| L | L | H | H |

Note) H; high level, L; low level,
X; irrelevant
Z; off (high-impedance) state of a 3-state output

## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75℃)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−2.6mA | | 2.4 | — | — | V |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=24mA | — | — | 0.5 | |
| | | | | $I_{OL}$=12mA | — | — | 0.4 | |
| Output current | | $I_{OZH}$ | $V_{CC}$=5.25V, $V_{IH}$=2V, $V_{IL}$=0.8V | $V_O$=2.4V | — | — | 20 | μA |
| | | $I_{OZL}$ | | $V_O$=0.4V | — | — | −20 | |
| Input current | | $I_{IH}$ | $V_{CC}$=5.25V, $V_{IH}$=2.7V | | — | — | 20 | μA |
| | A inputs | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.5V, Either $\bar{G}$ inputs=2V | | — | — | −20 | μA |
| | | | $V_{CC}$=5.25V, $V_I$=0.4V, Both $\bar{G}$ inputs=0.4V | | — | — | −0.4 | mA |
| | $\bar{G}$ inputs | | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| | | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.1 | mA |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$=5.25V | | −40 | — | −225 | mA |
| Supply current | | $I_{CC}$** | $V_{CC}$=5.25V | | — | 14 | 24 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=5.25V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C
** With all outputs open, $I_{CC}$ is measured with all inputs grounded and all $\bar{G}$ inputs at 4.5V.



Home Print

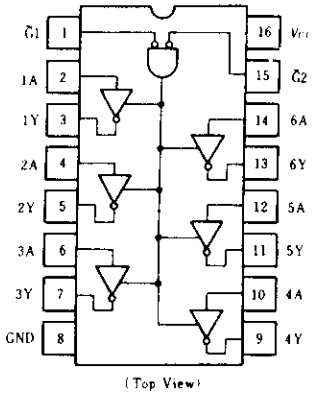
## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$=45pF<br>$R_L$=667Ω | — | 10 | 16 | ns |
| | $t_{PHL}$ | | — | 9 | 22 | |
| Output enable time | $t_{ZH}$ | | — | 19 | 35 | |
| | $t_{ZL}$ | | — | 24 | 40 | |
| Output disable time | $t_{HZ}$ | $C_L$=5pF<br>$R_L$=667Ω | — | — | 30 | |
| | $t_{LZ}$ | | — | — | 35 | |

Note) Refer to Test Circuit and Waveform of the Common Item

# HD74LS366A ●Hex Bus Drivers (with three-state outputs)

## ■PIN ARRANGEMENT



(Top View)

## ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7.0 | V |
| Input voltage | $V_{IN}$ | 7.0 | V |
| Output voltage (off-state) | $V_{O(off)}$ | 5.5 | V |
| Operating temperature range | $T_{opr}$ | −20~ +75 | °C |
| Storage temperature range | $T_{stg}$ | −65~ +150 | °C |

## ■FUNCTION TABLE

| Inputs | | | Output |
|---|---|---|---|
| $\overline{G}_1$ | $\overline{G}_2$ | A | Y |
| H | × | × | Z |
| × | H | × | Z |
| L | L | H | L |
| L | L | L | H |

Note)

H; high level, L; low level,
X; irrelevant
Z; off (high-impedance) state of a 3-state output

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Output current | $I_{OH}$ | — | — | −2.6 | mA |
| Output current | $I_{OL}$ | — | — | 24 | mA |



Home Print

## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75℃)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−2.6mA | | 2.4 | — | — | V |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, | $I_{OL}$=24mA | — | — | 0.5 | |
| | | | $V_{IL}$=0.8V | $I_{OL}$=12mA | — | — | 0.4 | |
| Output current | | $I_{OZH}$ | $V_{CC}$=5.25V, $V_{IH}$=2V, | $V_O$=2.4V | — | — | 20 | μA |
| | | $I_{OZL}$ | $V_{IL}$=0.8V | $V_O$=0.4V | — | — | −20 | |
| Input current | | $I_{IH}$ | $V_{CC}$=5.25V, $V_{IH}$=2.7V | | — | — | 20 | μA |
| | A inputs | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.5V, Either $\overline{G}$ inputs=2V | | — | — | −20 | μA |
| | | | $V_{CC}$=5.25V, $V_I$=0.4V, Both $\overline{G}$ inputs=0.4V | | — | — | −0.4 | mA |
| | $\overline{G}$ inputs | | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | |
| | | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.1 | mA |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$=5.25V | | −40 | — | −225 | mA |
| Supply current | | $I_{CC}$** | $V_{CC}$=5.25V | | — | 12 | 21 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C
** $I_{CC}$ is measured with data inputs grounded and output control inputs at 4.5V.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25℃)

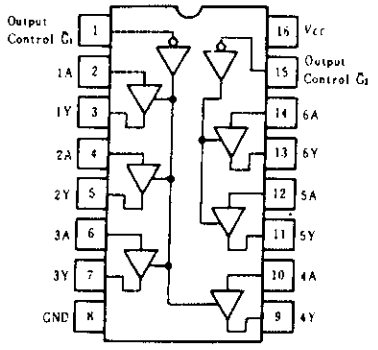
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$=45pF, $R_L$=667Ω | — | 7 | 15 | ns |
| | $t_{PHL}$ | | — | 12 | 18 | |
| Output enable time | $t_{ZH}$ | | — | 18 | 35 | |
| | $t_{ZL}$ | | — | 28 | 45 | |
| Output disable time | $t_{HZ}$ | $C_L$=5pF, $R_L$=667Ω | — | — | 32 | |
| | $t_{LZ}$ | | — | — | 35 | |

Note) Refer to Test Circuit and Waveform of the Common Item

# HD74LS367A

●Hex Bus Drivers
(non-inverted data outputs with three-state outputs)

## ■PIN ARRANGEMENT




(Top View)

## ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7.0 | V |
| Input voltage | $V_{IN}$ | 7.0 | V |
| Output voltage (off-state) | $V_{O(off)}$ | 5.5 | V |
| Operating temperature range | $T_{opr}$ | −20~+75 | °C |
| Storage temperature range | $T_{stg}$ | −65~+150 | °C |

## ■FUNCTION TABLE

| $\overline{G}$ | A | Y |
|---|---|---|
| H | X | Z |
| L | L | L |
| L | H | H |

Note) H; high level, L; low level,
X; irrelevant
Z; off (high-impedance) state of a 3-state output

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Output current | $I_{OH}$ | — | — | −2.6 | mA |
| Output current | $I_{OL}$ | — | — | 24 | mA |



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## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−2.6mA | | 2.4 | — | — | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=24mA | — | — | 0.5 | V |
| | | | $I_{OL}$=12mA | — | — | 0.4 | |
| Output current | $I_{OZ}$ | $V_{CC}$=5.25V, $V_{IH}$=2V, $V_{IL}$=0.8V | $V_O$=2.4V | — | — | 20 | μA |
| | | | $V_O$=0.4V | — | — | −20 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | $I_{IL}$ | A inputs $V_{CC}$=5.25V | $V_I$=0.5V, $\overline{G}$ inputs 2V | — | — | −20 | μA |
| | | | $V_I$=0.4V, $\overline{G}$ inputs 0.4V | — | — | −0.4 | mA |
| | | $\overline{G}$ inputs $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −40 | — | −225 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}$=5.25V | | — | 14 | 24 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C
** $I_{CC}$ is measured with data inputs grounded and output control inputs at 4.5V.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

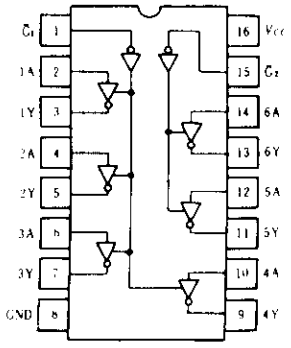
| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$=45pF, $R_L$=667Ω | — | 10 | 16 | ns |
| | $t_{PHL}$ | | — | 9 | 22 | |
| Output enable time | $t_{ZH}$ | | — | 19 | 35 | ns |
| | $t_{ZL}$ | | — | 24 | 40 | |
| Output disable time | $t_{HZ}$ | $C_L$=5pF, $R_L$=667Ω | — | — | 30 | ns |
| | $t_{LZ}$ | | — | — | 35 | |

Note) Refer to Test Circuit and Waveform of the Common Item

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# HD74LS368A ●Hex Bus Drivers (inverted data outputs with three-state outputs)

## ■PIN ARRANGEMENT




(Top View)

## ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7.0 | V |
| Input voltage | $V_{IN}$ | 7.0 | V |
| Output voltage (off-state) | $V_{O(off)}$ | 5.5 | V |
| Operating temperature range | $T_{opr}$ | −20 ~ +75 | °C |
| Storage temperature range | $T_{stg}$ | −65 ~ +150 | °C |

## ■FUNCTION TABLE

| $\bar{G}$ | A | Y |
|---|---|---|
| H | × | Z |
| L | L | H |
| L | H | L |

Note) H; high level, L; low level,
X; irrelevant
Z; off (high-impedance) state of a 3-state output

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Output current | $I_{OH}$ | — | — | −2.6 | mA |
| Output current | $I_{OL}$ | — | — | 24 | mA |



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## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−2.6mA | | 2.4 | — | — | V |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=12mA | — | — | 0.4 | |
| | | | | $I_{OL}$=24mA | | | 0.5 | |
| Output current | | $I_{OZ}$ | $V_{CC}$=5.25V, $V_{IH}$=2V, $V_{IL}$=0.8V | $V_O$=2.4V | — | — | 20 | μA |
| | | | | $V_O$=0.4V | — | — | −20 | |
| Input current | | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | A inputs | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.5V, $\overline{G}$ input at 2V | | — | — | −20 | μA |
| | $\overline{G}$ inputs | | $V_{CC}$=5.25V, $V_I$=0.4V, $\overline{G}$ inputs at 0.4V | | — | — | −0.4 | mA |
| | | | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | |
| | | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.1 | mA |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$=5.25V | | −40 | — | −225 | mA |
| Supply current ** | | $I_{CC}$ | $V_{CC}$=5.25V | | — | 12 | 21 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=5.25V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** With all outputs open, $I_{CC}$ is measured with all inputs grounded and all $\overline{G}$ inputs at 4.5V.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | $C_L$=45pF, $R_L$=667Ω | — | 7 | 15 | ns |
| | $t_{PHL}$ | | — | 12 | 18 | |
| Output enable time | $t_{ZH}$ | | — | 18 | 35 | |
| | $t_{ZL}$ | | — | 28 | 45 | |
| Output disable time | $t_{HZ}$ | $C_L$=5pF, $R_L$=667Ω | — | — | 32 | |
| | $t_{LZ}$ | | — | — | 35 | |

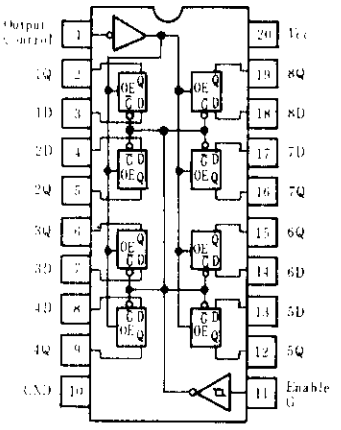
Note) Refer to Test Circuit and Waveform of the Common Item

# HD74LS373 ●Octal D-type Transparent Latches (with three-state outputs)

The HD74LS373, 8-bit register features totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capacity of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.

## ■PIN ARRANGEMENT



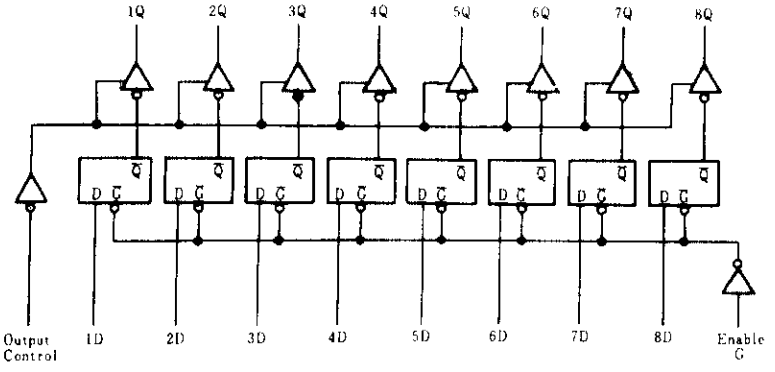

(Top View)

## ■FUNCTION TABLE

| Inputs | | | Output |
|---|---|---|---|
| Output control | Enable G | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | × | $Q_0$ |
| H | × | × | Z |

Notes: H = high level, L = low level,
X = irrelevant
$Q_0$ = level of Q before the indicated steady-state input conditions were established.
Z = off (high-impedance) state of a three-state output

## ■BLOCK DIAGRAM




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output voltage | | $V_{OH}$ | — | — | 5.5 | V |
| Output current | | $I_{OH}$ | — | — | −2.6 | mA |
| | | $I_{OL}$ | — | — | 24 | mA |
| Enable pulse width | "H" level | $t_w$ | 15 | — | — | ns |
| | "L" level | | 15 | — | — | |
| Data setup time | | $t_{su}$ | 5↓ | — | — | ns |
| Data hold time | | $t_h$ | 25↓ | — | — | ns |

Note) ↓ : The arrow indicates the falling edge of clock pulse.



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## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | Data inputs | | — | — | 0.7 | V |
| | | G, Output control inputs | | — | — | 0.8 | |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=$V_{IL\ max}$, $I_{OH}$=−2.6mA | | 2.4 | — | — | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=$V_{IL\ max}$ | $I_{OL}$=12mA | — | — | 0.4 | V |
| | | | $I_{OL}$=24mA | — | — | 0.5 | |
| Off-state output current | $I_{OZH}$ | $V_{CC}$=5.25V, $V_{IH}$=2V | $V_O$=2.7V | — | — | 20 | μA |
| | $I_{OZL}$ | | $V_O$=0.4V | — | — | −20 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −30 | — | −130 | mA |
| Supply current | $I_{CC}$ | $V_{CC}$=5.25V, $V_I$=4.5V (Output control) | | — | 24 | 40 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

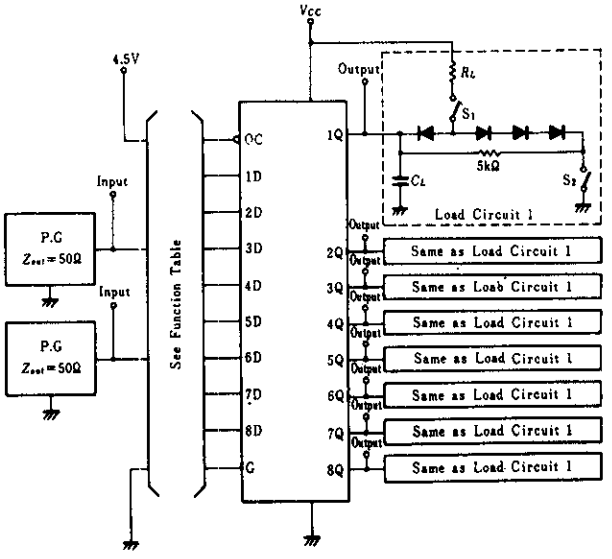
* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Input | Output | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | D | Q | $C_L$=45pF, $R_L$=667Ω | — | 12 | 18 | ns |
| | $t_{PHL}$ | | | | — | 12 | 18 | |
| | $t_{PLH}$ | G | Q | | — | 20 | 30 | |
| | $t_{PHL}$ | | | | — | 18 | 30 | |
| Output enable time | $t_{ZH}$ | OC | Q | | — | 15 | 28 | |
| | $t_{ZL}$ | | | | — | 25 | 36 | |
| Output disable time | $t_{HZ}$ | OC | Q | $C_L$=5pF, $R_L$=667Ω | — | 12 | 20 | |
| | $t_{LZ}$ | | | | — | 15 | 25 | |

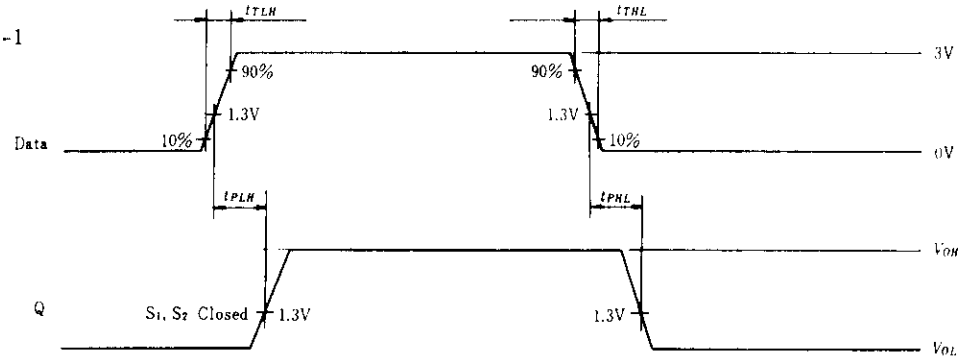
## ■TESTING METHOD

Test Circuit



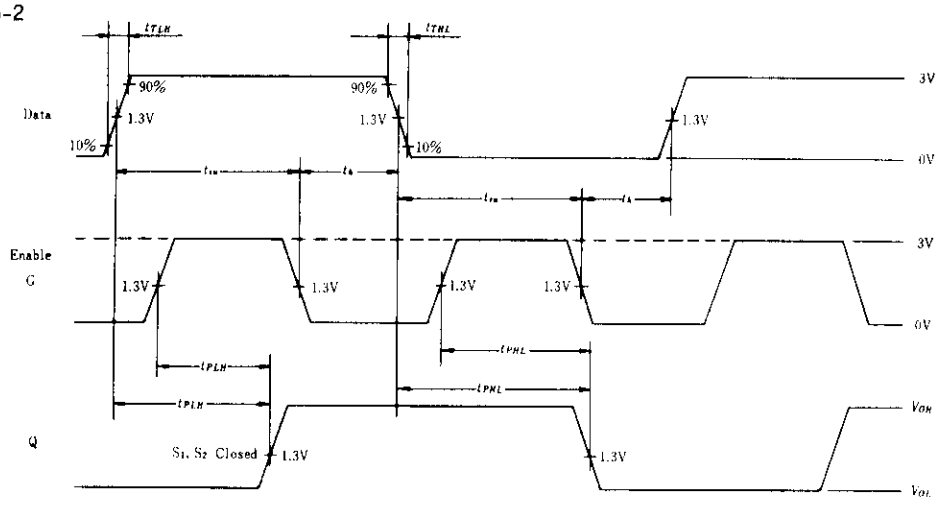

Notes: 1. $C_L$ includes probe jig capacitance.
2. All diodes are 1S2074 Ⓗ.

Waveform-1




**Notes:** Input pulse; $t_{TLH} \leqq 15ns$, $t_{THL} \leqq 6ns$, $PRR = 1MHz$, duty cycle 50%

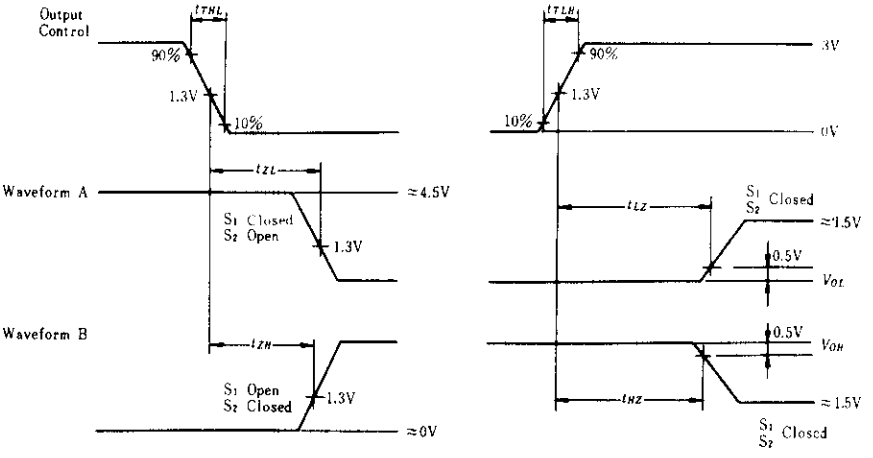
Waveform-2




**Note:** Enable input pulse; $t_{TLH} \leqq 15ns$, $t_{THL} \leqq 6ns$, $PRR = 1MHz$

Data input pulse; $t_{TLH} \leqq 15ns$, $t_{THL} \leqq 6ns$, $PRR = 1MHz$, G input is high.

Waveform-3




**Notes:**
1. Input pulse; $t_{TLH} \leqq 15ns$, $t_{THL} \leqq 6ns$, $PRR = 1MHz$, duty cycle 50%
2. Waveform A if for an output with internal conditions such that the output is low except when disabled by the output control. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.

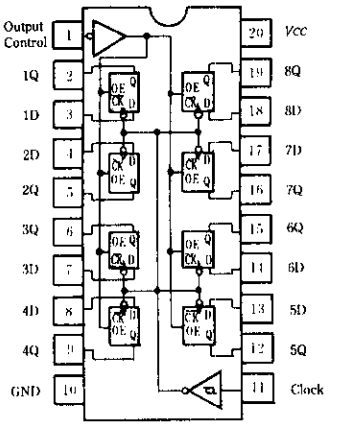


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# HD74LS374 ●Octal D-type Edge-triggered Flip-Flops (with three-state outputs)

The HD74LS374, 8-bit registers features totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The eight flip-flops are edge-triggered D-type flip-flops. On the positive transition the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

## ■PIN ARRANGEMENT



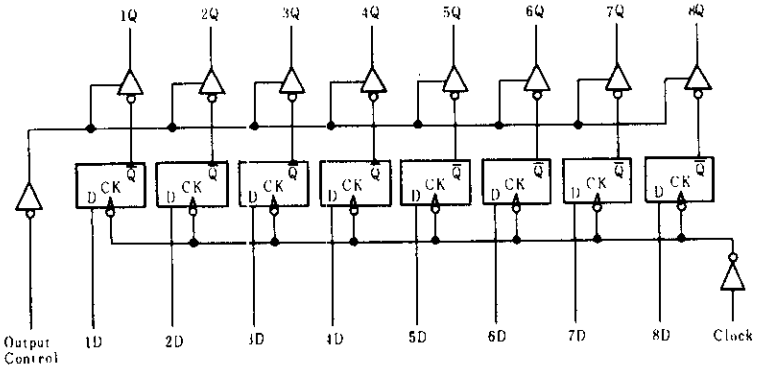

(Top View)

## ■FUNCTION TABLE

| Inputs | | | Output |
|---|---|---|---|
| Output control | Clock | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | × | $Q_0$ |
| H | × | × | Z |

Notes: H = high level, L = low level,
X = irrelevant
↑ = transition from low to high level
$Q_0$ = level of Q before the indicated steady-state input conditions were established
Z = off (high-impedance) state of a three-state output

## ■BLOCK DIAGRAM




## ■RECOMMENDED OPERATING CONDITION

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output voltage | | $V_{OH}$ | — | — | 5.5 | V |
| Output current | | $I_{OH}$ | — | — | −2.6 | mA |
| | | $I_{OL}$ | — | — | 24 | mA |
| Clock pulse width | "H" level | $t_w$ | 15 | — | — | ns |
| | "L" level | | 15 | — | — | |
| Data setup time | | $t_{su}$ | 20↑ | — | — | ns |
| Data hold time | | $t_h$ | 3↑ | — | — | ns |

Note) ↑ : The arrow indicates the rising edge of clock pulse.

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## ■ELECTRICAL CHARACTERISTICS ($Ta$= −20～+75°C)

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−2.6mA | | 2.4 | — | — | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=12mA | — | — | 0.4 | V |
| | | | $I_{OL}$=24mA | — | — | 0.5 | |
| Off-state output current | $I_{OZH}$ | $V_{CC}$=5.25V, $V_{IH}$=2V | $V_O$=2.7V | — | — | 20 | μA |
| | $I_{OZL}$ | | $V_O$=0.4V | — | — | −20 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.1 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −30 | — | −130 | mA |
| Supply current | $I_{CC}$ | $V_{CC}$=5.25V, $V_I$=4.5V (Output control) | | — | 27 | 40 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

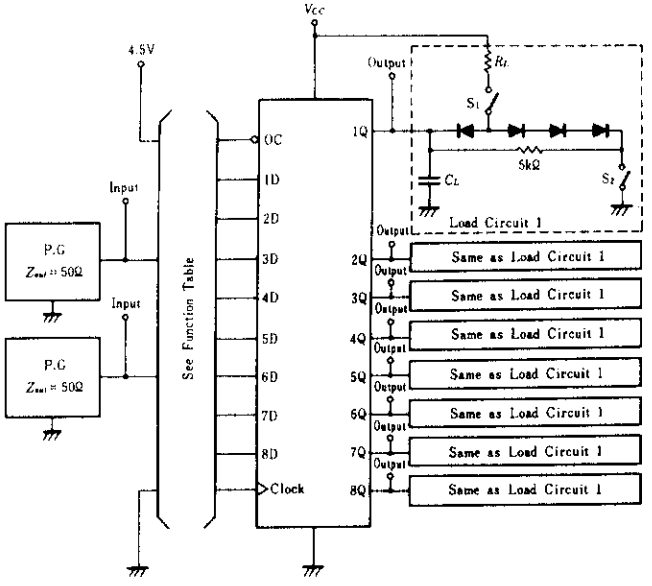
* $V_{CC}$=5V, $Ta$=25°C

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | $f_{max}$ | Clock | Q | $C_L$=45pF, $R_L$=667Ω | 35 | 50 | — | MHz |
| Propagation delay time | $t_{PLH}$ | Clock | Q | | — | 15 | 28 | ns |
| | $t_{PHL}$ | | | | — | 19 | 28 | |
| Output enable time | $t_{ZH}$ | OC | Q | | — | 20 | 28 | |
| | $t_{ZL}$ | | | | — | 21 | 28 | |
| Output disable time | $t_{HZ}$ | OC | Q | $C_L$=5pF, $R_L$=667Ω | — | 12 | 20 | |
| | $t_{LZ}$ | | | | — | 14 | 25 | |

## ■TESTING METHOD

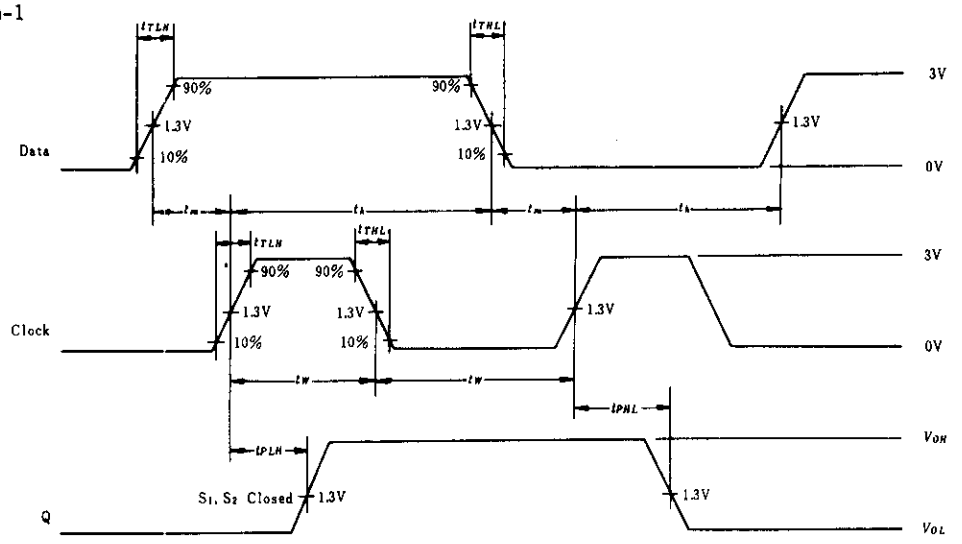
Test Circuit





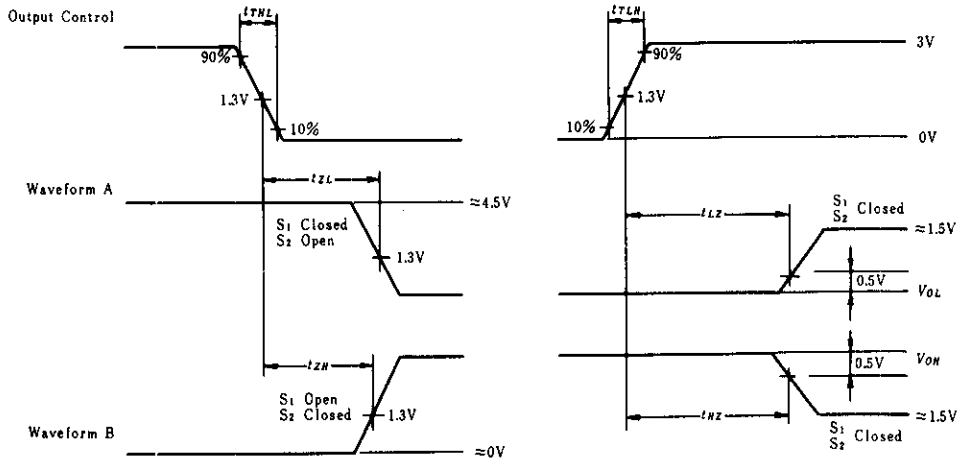

Home Print

Waveform-1




**Notes:** 1. Input pulse; $t_{TLH}$ = 15ns, $t_{THL}$ = 6ns
Clock input; $PRR$ = 1MHz, duty cycle 50%
Data input; $PRR$ = 500kHz, duty cycle 50%
2. $f_{max}$; $t_{TLH}$ = 2.5ns, $t_{THL}$ = 2.5ns

Waveform-2

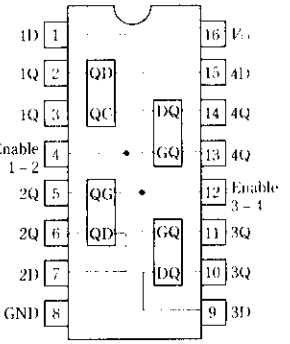



**Notes:** 1. Input pulse; $t_{TLH}$ = 15ns, $t_{THL}$ = 6ns, $PRR$ = 1MHz, duty cycle 50%
2. Waveform A is for an output with internal conditions such that the output is low except when disable by the output control. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.

# HD74LS375 ●Quadruple Bistable Latches

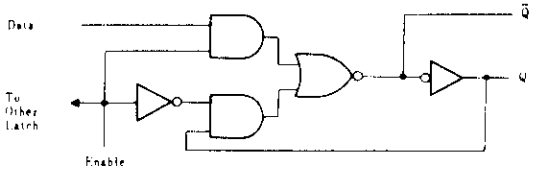
The HD74LS375 bistable latch is electrically and functionally identical to the HD74LS75, respectively. Only the arrangement of the terminals has been changed in the HD74LS375. This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable goes high.

## ■PIN ARRANGEMENT



(Top View)

## ■BLOCK DIAGRAM (1/4)




## ■FUNCTION TABLE

| Inputs | | Outputs | |
|---|---|---|---|
| D | G | Q | $\bar{Q}$ |
| L | H | L | H |
| H | H | H | L |
| × | L | $Q_0$ | $\bar{Q}_0$ |

Notes) H; high level, L; low level, X; irrelevant
$Q_0$ level of Q before the indicated steady-state input conditions were established.
$\bar{Q}_0$ complement of $Q_0$ or level of $\bar{Q}$ before the indicated steady-state input conditions were established.

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Pulse width | $t_W$ | 20 | — | — | ns |
| Setup time | $t_{su}$ | 20 | — | — | ns |
| Hold time | $t_h$ | 5 | — | — | ns |

## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | | 2.7 | — | — | V |
| | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | — | — | 0.4 | V |
| | | | $I_{OL}$=8mA | — | — | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | D | — | — | 20 | μA |
| | | | G | — | — | 80 | |
| | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | D | — | — | −0.4 | mA |
| | | | G | — | — | −1.6 | |
| | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | D | — | — | 0.1 | mA |
| | | | G | — | — | 0.4 | |
| Short-circuit output current | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | — | −100 | mA |
| Supply current ** | $I_{CC}$ | $V_{CC}$=5.25V | | — | 6.3 | 12 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C
** $I_{CC}$ is measured with all outputs open and all inputs grounded.



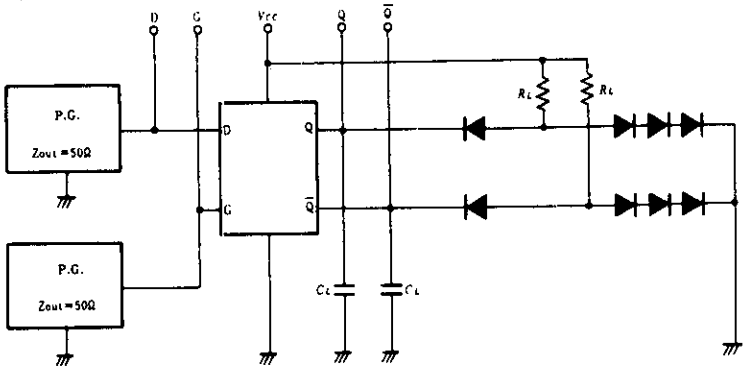
Home Print

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | D | Q | $R_L$=2kΩ<br>$C_L$=15pF | — | 15 | 27 | ns |
| | $t_{PHL}$ | | | | — | 9 | 17 | |
| | $t_{PLH}$ | D | $\overline{Q}$ | | — | 12 | 20 | |
| | $t_{PHL}$ | | | | — | 7 | 15 | |
| | $t_{PLH}$ | G | Q | | — | 15 | 27 | |
| | $t_{PHL}$ | | | | — | 14 | 25 | |
| | $t_{PLH}$ | G | $\overline{Q}$ | | — | 16 | 30 | |
| | $t_{PHL}$ | | | | — | 7 | 15 | |

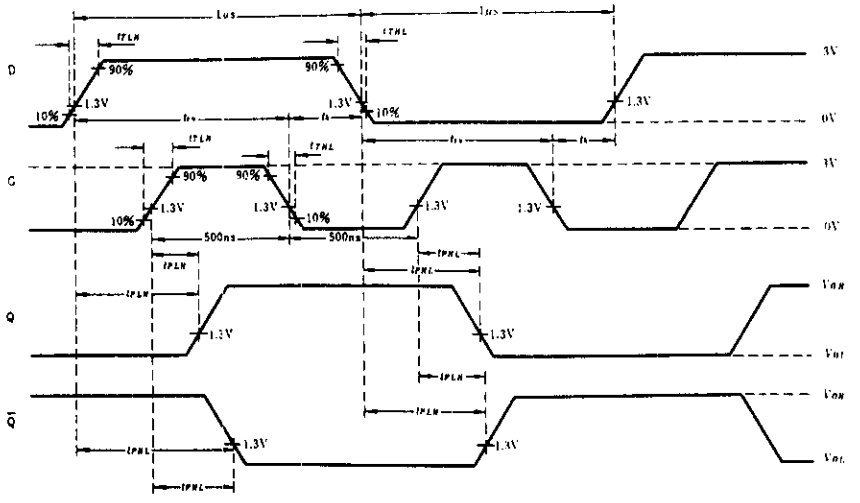
## ■TESTING METHOD

### 1) Test Circuit




Notes) 1. Test is put into the each latch.
2. All diodes are 1S2074 Ⓗ.
3. $C_L$ includes probe and jig capacitance.

### Waveform

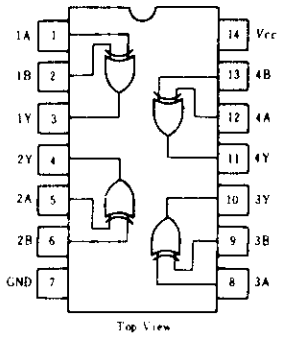



Notes) 1. Input pulse: D input: *PRR*=500kHz, G input: *PRR*=1MHz, $t_{THL}$≦10ns, $t_{TLH}$≦10ns.
2. When measuring propagation delay times from the D input, the corresponding G input must be held high.

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# HD74LS386 ●Quadruple 2-input Exclusive-OR Gates

## ■PIN ARRANGEMENT




## ■FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | B | |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

H; high level, L; low level.

## ■ELECTRICAL CHARACTERISTICS ($Ta=-20\sim+75°C$)

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$ | | 2.7 | — | — | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | — | — | 0.4 | V |
| | | | $I_{OL}=8mA$ | — | — | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 40 | $\mu A$ |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −0.8 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | — | — | 0.2 | mA |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −20 | — | −100 | mA |
| Supply current** | $I_{CC}$ | $V_{CC}=5.25V$ | | — | 6.1 | 10 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$
** $I_{CC}$ is measured with all outputs open and all inputs grounded.

## ■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

| Item | Symbol | Inputs | Test Conditions | | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A or B | Other inputs "L" | $C_L=15pF$, $R_L=2k\Omega$ | — | 12 | 23 | ns |
| | $t_{PHL}$ | | | | — | 10 | 17 | |
| | $t_{PLH}$ | A or B | Other inputs "H" | | — | 20 | 30 | ns |
| | $t_{PHL}$ | | | | — | 13 | 22 | |

Note) Refer to Test Circuit and Waveform of the Common Item

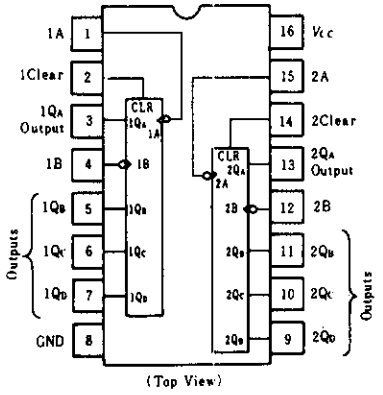


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# HD74LS390 ● Dual Decade Counters

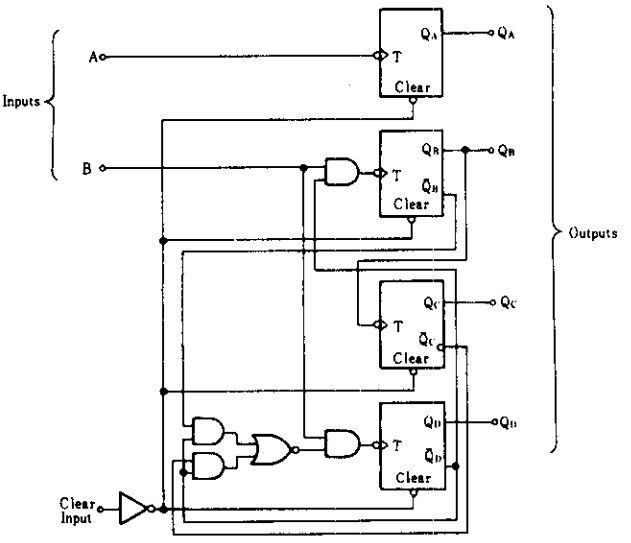
This circuit contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters. The HD74LS390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage.

## ■PIN ARRANGEMENT




(Top View)

## ■BLOCK DIAGRAM (½)




## ■ABSOLUTE MAXIMUM RATINGS

| Item | | Symbol | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 7 | V |
| Input voltage | Clear | $V_{IN}$ | 7 | V |
| | A, B | | 5.5 | V |
| Operating temperature range | | $T_{opr}$ | −20～+75 | ℃ |
| Storage temperature range | | $T_{stg}$ | −65～+150 | ℃ |

## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Output current | | $I_{OH}$ | — | — | −400 | μA |
| Output current | | $I_{OL}$ | — | — | 8 | mA |
| Count frequency | Input A | $f_{count}$ | 0 | — | 25 | MHz |
| | Input B | | 0 | — | 20 | |
| Pulse width | Input A | $t_w$ | 20 | — | — | ns |
| | Input B | | 25 | — | — | |
| | Clear | | 20 | — | — | |
| Setup time | | $t_{su}$ | 25↓ | — | — | ns |

↓; The arrow indicates that the falling edge of the clock pulse is used for reference.

## ■FUNCTION TABLE

### ●BCD Count Sequence (Notes 1)

| Count | Outputs | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

### ●Bi-Quinary (Notes 2)

| Count | Outputs | | | |
|---|---|---|---|---|
| | $Q_A$ | $Q_D$ | $Q_C$ | $Q_B$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

Notes)

1. Output $Q_A$ is connected to input B for BCD count.
2. Output $Q_D$ is connected to input A for bi-quinary count.
3. H; high level, L; low level, X; irrelevant

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## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | — | — | 0.4 | V |
| | | | | $I_{OL}$=8mA | — | — | 0.5 | |
| Input current | Clear | $I_I$ | $V_{CC}$=5.25V | $V_I$=7V | — | — | 0.1 | mA |
| | Input A | | | $V_I$=5.5V | — | — | 0.2 | |
| | Input B | | | | — | — | 0.4 | |
| | Clear | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | Input A | | | | — | — | 100 | |
| | Input B | | | | — | — | 200 | |
| | Clear | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| | Input A | | | | — | — | −1.6 | |
| | Input B | | | | — | — | −2.4 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | — | −100 | mA |
| Supply current | | $I_{CC}$** | $V_{CC}$=5.25V | | — | 15 | 26 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** $I_{CC}$ is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum count frequency | $f_{max}$ | A | $Q_A$ | $C_L$=15pF, $R_L$=2kΩ | 25 | 35 | — | MHz |
| | | B | $Q_B$ | | 20 | 30 | — | |
| Propagation delay time | $t_{PLH}$ | A | $Q_A$ | | — | 12 | 20 | ns |
| | $t_{PHL}$ | | | | — | 13 | 20 | |
| | $t_{PLH}$ | A | $Q_C$ | | — | 37 | 60 | |
| | $t_{PHL}$ | | | | — | 39 | 60 | |
| | $t_{PLH}$ | B | $Q_B$ | | — | 13 | 21 | |
| | $t_{PHL}$ | | | | — | 14 | 21 | |
| | $t_{PLH}$ | B | $Q_C$ | | — | 24 | 39 | |
| | $t_{PHL}$ | | | | — | 26 | 39 | |
| | $t_{PLH}$ | B | $Q_D$ | | — | 13 | 21 | |
| | $t_{PHL}$ | | | | — | 14 | 21 | |
| | $t_{PHL}$ | Clear | Any | | — | 24 | 39 | |

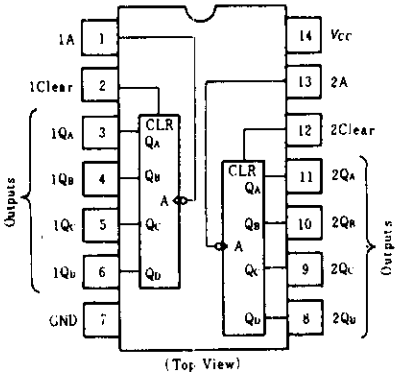


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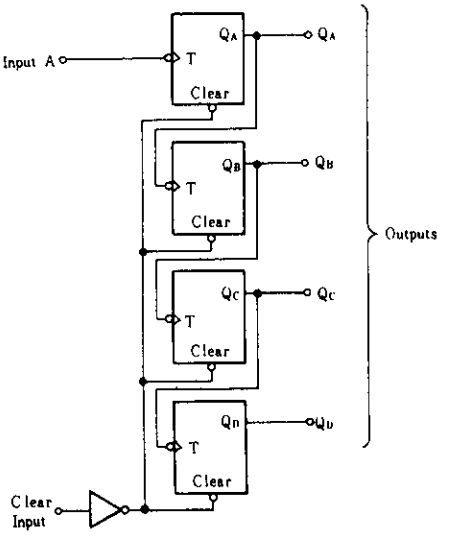
# HD74LS393 ●Dual 4-bit Binary Counters

This circuit contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters. The HD74LS393 comprises two independent four-bit binary counters each having a clear and a clock input.
N-bit binary counter can be implemented with each package providing the capability of divide-by-256.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM (1/2)




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Output current | | $I_{OH}$ | — | — | −400 | μA |
| Output current | | $I_{OL}$ | — | — | 8 | mA |
| Count frequency | A input | $f_{count}$ | 0 | — | 25 | MHz |
| Pulse width | A input high or low | $t_W$ | 20 | — | — | ns |
| | Clear high | | 20 | — | — | |
| Setup time | | $t_{su}$ | 25↓ | — | — | ns |

↓; The arrow indicates that the falling edge of the clock pulse is used for reference.

## ■ABSOLUTE MAXIMUM RATINGS

| Item | | Symbol | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 7 | V |
| Input voltage | Clear | $V_{IN}$ | 7 | V |
| | A | | 5.5 | |
| Operating temperature range | | $T_{opr}$ | −20～+75 | °C |
| Storage temperature range | | $T_{stg}$ | −65～+150 | °C |

## ■FUNCTION TABLE

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

H; high level, L; low level.

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## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | — | — | 0.4 | V |
| | | | | $I_{OL}$=8mA | — | — | 0.5 | |
| Input current | Clear | $I_I$ | $V_{CC}$=5.25V | $V_I$=7V | — | — | 0.1 | mA |
| | Input A | | | $V_I$=5.5V | — | — | 0.2 | |
| | Clear | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | Input A | | | | — | — | 100 | |
| | Clear | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| | Input A | | | | — | — | −1.6 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | — | −100 | mA |
| Supply current | | $I_{CC}$** | $V_{CC}$=5.25V | | — | 15 | 26 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** $I_{CC}$ is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum count frequency | $f_{max}$ | A | $Q_A$ | $C_L$=15pF, $R_L$=2kΩ | 25 | 35 | — | MHz |
| Propagation delay time | $t_{PLH}$ | A | $Q_A$ | | — | 12 | 20 | ns |
| | $t_{PHL}$ | | | | — | 13 | 20 | |
| | $t_{PLH}$ | A | $Q_D$ | | — | 40 | 60 | |
| | $t_{PHL}$ | | | | — | 40 | 60 | |
| | $t_{PHL}$ | Clear | Any | | — | 24 | 39 | |

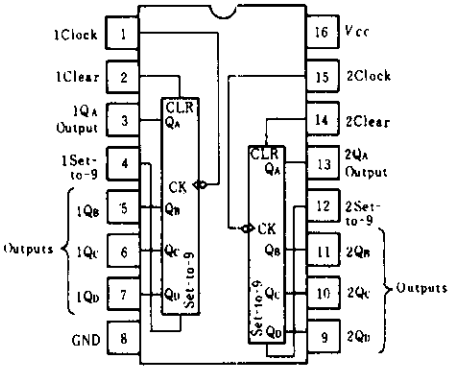


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# HD74LS490 ●Dual 4-bit Decade Counters

This circuit contains eight master-slave flip-flops and additional gating to implement two individual 4-bit decade counters. Each decade counter has individual clock, clear, and set-to-9 inputs. BCD count sequences of any length up to divide-by-100 may be implemented with a single HD74LS490. Buffering on each output is provided to ensure that susceptibility to collector communication is reduced significantly. All inputs are diode-clamped to reduce the effects of line ringing. The counters have parallel outputs from each counter stage so that submultiples of the input count frequency are available for system timing signals.

## ■PIN ARRANGEMENT




(Top View)

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Output current | $I_{OH}$ | — | — | −400 | μA |
| Output current | $I_{OL}$ | — | — | 8 | mA |
| Count frequency | $f_{count}$ | 0 | — | 25 | MHz |
| Pulse width | $t_W$ | 20 | — | — | ns |
| Setup time | $t_{su}$ | 25↓ | — | — | ns |

↓; The arrows indicates the falling edge from clock transition.

## ■FUNCTION TABLE

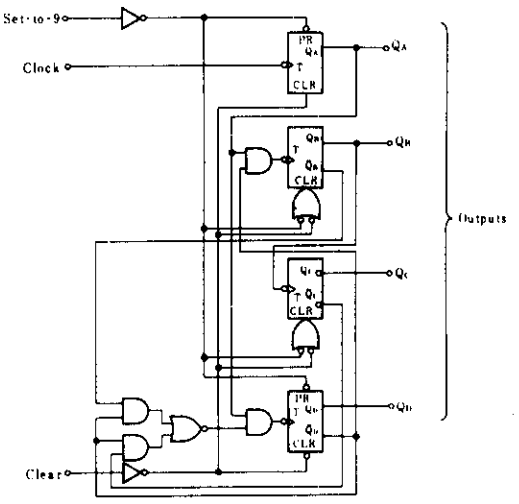
### ●CLEAR/SET-TO-9

| Inputs | | Outputs | | | |
|---|---|---|---|---|---|
| CLEAR | SET-TO-9 | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| H | L | L | L | L | L |
| L | H | H | L | L | H |
| L | L | Count | | | |

### ●BCD Count Sequence

| Count | Outputs | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

## ■BLOCK DIAGRAM (½)




## ■ABSOLUTE MAXIMUM RATINGS

| Item | | Symbol | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 7.0 | V |
| Input voltage | CLOCK | $V_{IN}$ | 5.5 | V |
| | CLEAR, SET-TO-9 | | 7.0 | |
| Operating temperature range | | $T_{opr}$ | −20～+75 | ℃ |
| Storage temperature range | | $T_{stg}$ | −65～+125 | ℃ |

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## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=400μA | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | — | — | 0.4 | |
| | | | | $I_{OL}$=8mA | — | — | 0.5 | |
| Input current | Clear<br>Set-to-9 | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | Clock | | | | — | — | 100 | |
| | Clear<br>Set-to-9 | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| | Clock | | | | — | — | −1.6 | |
| | Clear<br>Set-to-9 | $I_I$ | $V_{CC}$=5.25V | $V_I$=7V | — | — | 0.1 | mA |
| | Clock | | | $V_I$=5.5V | — | — | 0.2 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | — | −100 | mA |
| Supply current | | $I_{CC}$** | $V_{CC}$=5.25V | | — | 15 | 26 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** $I_{CC}$ is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum count frequency | $f_{max}$ | Clock | $Q_A$ | $C_L$=15pF, $R_L$=2kΩ | 25 | 35 | — | MHz |
| Propagation delay time | $t_{PLH}$ | Clock | $Q_A$ | | — | 12 | 20 | ns |
| | $t_{PHL}$ | | | | — | 13 | 20 | |
| | $t_{PLH}$ | Clock | $Q_B$, $Q_D$ | | — | 24 | 39 | |
| | $t_{PHL}$ | | | | — | 26 | 39 | |
| | $t_{PLH}$ | Clock | $Q_C$ | | — | 32 | 54 | |
| | $t_{PHL}$ | | | | — | 36 | 54 | |
| | $t_{PHL}$ | Clear | Any | | — | 24 | 39 | |
| | $t_{PLH}$ | Set-to-9 | $Q_A$, $Q_D$ | | — | 24 | 39 | |
| | $t_{PHL}$ | | $Q_B$, $Q_C$ | | — | 20 | 36 | |

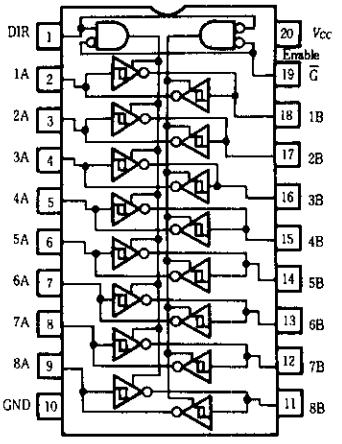


Home Print

# HD74LS640 ●Octal Bus Transceivers (inverted 3-state outputs)

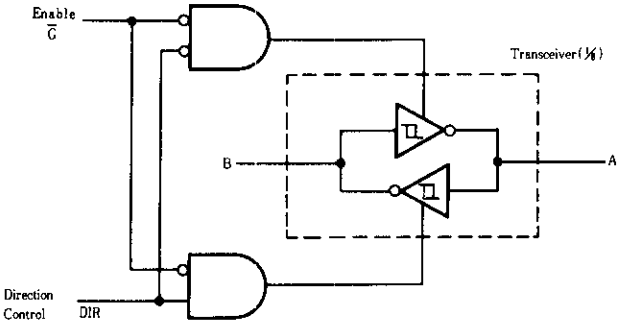
This octal bus transceivers is designed for asynchronous two-way communication between data buses. The device transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

## ■PIN ARRANGEMENT




(Top View)

## ■BLOCK DIAGRAM




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output Current | $I_{OH}$ | — | — | −15 | mA |
| Output Current | $I_{OL}$ | — | — | 24 | mA |
| Operating temperature range | $T_{opr}$ | −20 | 25 | 75 | ℃ |

## ■FUNCTION TABLE

| Enable | Direction Control | Operation |
|---|---|---|
| $\overline{G}$ | DIR | |
| L | L | $\overline{B}$ data to A bus |
| L | H | $\overline{A}$ data to B bus |
| H | × | Isolation |

Notes) H; high level, L; low level, X; irrelevant

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## ■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | | | V |
| | | $V_{IL}$ | | | | | 0.8 | V |
| Hysteresis | | $V_T^+ - V_T^-$ | $V_{CC}=4.75V$ | | 0.2 | — | — | V |
| Output voltage | | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OH}=-3mA$ | 2.4 | | | V |
| | | | | $I_{OH}=-15mA$ | 2 | | | V |
| | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=12mA$ | — | | 0.4 | V |
| | | | | $I_{OL}=24mA$ | — | — | 0.5 | V |
| Output current | | $I_{OZH}$ | $V_{CC}=5.25V$, $\overline{G}$ INPUT $=2V$ | $V_O=2.7V$ | — | — | 20 | μA |
| | | $I_{OZL}$ | | $V_O=0.4V$ | — | — | −400 | μA |
| Input current | | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | μA |
| | | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −400 | μA |
| | A or B | $I_I$ | $V_{CC}=5.25V$ | $V_I=5.5V$ | — | — | 0.1 | mA |
| | DIR or $\overline{G}$ | | | $V_I=7V$ | — | | 0.1 | mA |
| Short-circuit output current | | $I_{OS}$** | $V_{CC}=5.25V$ | | −40 | | −225 | mA |
| Supply current | | $I_{CCH}$ | $V_{CC}=5.25V$, OUTPUT OPEN | | — | 48 | 70 | mA |
| | | $I_{CCL}$ | | | — | 62 | 90 | mA |
| | | $I_{CCZ}$ | | | — | 64 | 95 | mA |
| Input clamp voitage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$
** Not more than one output shall be shorted at a time.
The duration of the short circuit shall not exceed one second.

## ■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

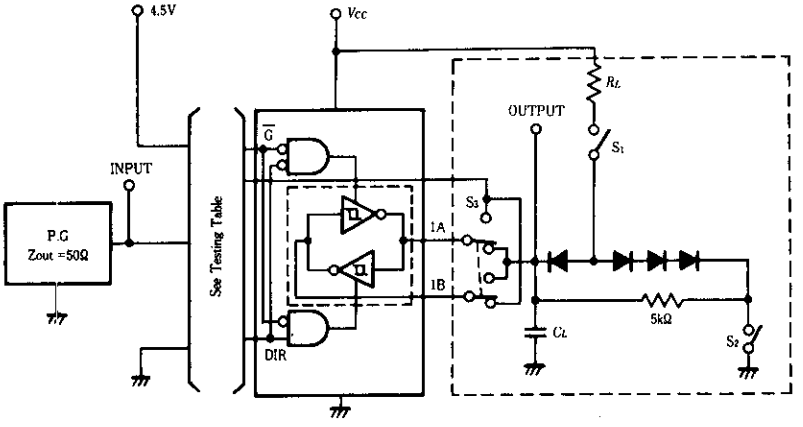
| Item | Symbol | INPUT | OUTPUT | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A | B | $C_L=45pF$, $R_L=667\Omega$ | — | 6 | 10 | ns |
| | | B | A | | — | 6 | 10 | ns |
| | $t_{PHL}$ | A | B | | | 8 | 15 | ns |
| | | B | A | | — | 8 | 15 | ns |
| Output enable time | $t_{ZL}$ | $\overline{G}$ | A | | — | 31 | 40 | ns |
| | | $\overline{G}$ | B | | — | 31 | 40 | ns |
| | $t_{ZH}$ | $\overline{G}$ | A | | — | 23 | 40 | ns |
| | | $\overline{G}$ | B | | — | 23 | 40 | ns |
| Output disable time | $t_{LZ}$ | $\overline{G}$ | A | $C_L=5pF$, $R_L=667\Omega$ | — | 15 | 25 | ns |
| | | $\overline{G}$ | B | | — | 15 | 25 | ns |
| | $t_{HZ}$ | $\overline{G}$ | A | | | 15 | 25 | ns |
| | | $\overline{G}$ | B | | — | 15 | 25 | ns |



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## ■TESTING METHOD

### Test Circuit

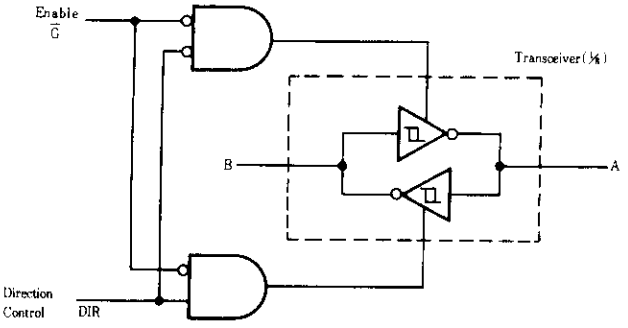



Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.
3. 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B, 7A-7B, 8A-8B are identical to above load circuit.
4. $S_3$ is a input-output switch.

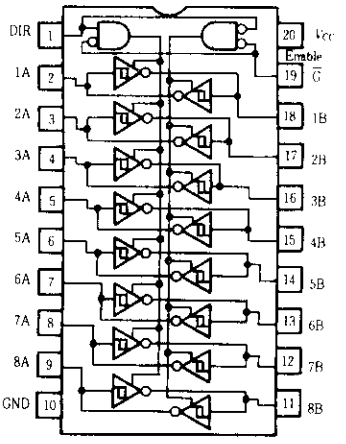
# HD74LS640-1 ●Octal Bus Transceivers (inverted 3-state outputs)

This octal bus transceivers is designed for asynchronous two-way communication between data buses. The device transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




(Top View)

## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output Current | $I_{OH}$ | — | — | −15 | mA |
| Output Current | $I_{OL}$ | — | — | 48 | mA |
| Operating temperature range | $T_{opr}$ | −20 | 25 | 75 | ℃ |

## ■FUNCTION TABLE

| Enable $\overline{G}$ | Direction Control DIR | Operation |
|---|---|---|
| L | L | $\overline{B}$ data to A bus |
| L | H | $\overline{A}$ data to B bus |
| H | × | Isclation |

Notes) H; high level, L; low level, X; irrelevant



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## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Hysteresis | | $V_T^+ - V_T^-$ | $V_{CC}$=4.75V | | 0.2 | — | — | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OH}$=−3mA | 2.4 | — | — | V |
| | | | | $I_{OH}$=−15mA | 2 | — | — | V |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=12mA | — | — | 0.4 | V |
| | | | | $I_{OL}$=24mA | — | — | 0.5 | V |
| | | | | $I_{OL}$=48mA | — | — | 0.5 | V |
| Output current | | $I_{OZH}$ | $V_{CC}$=5.25V, $\overline{G}$ INPUT=2V | $V_O$=2.7V | — | — | 20 | μA |
| | | $I_{OZL}$ | | $V_O$=0.4V | — | — | −400 | μA |
| Input current | | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −400 | μA |
| | A or B | $I_I$ | $V_{CC}$=5.25V | $V_I$=5.5V | — | — | 0.1 | mA |
| | DIR or $\overline{G}$ | | | $V_I$=7V | — | — | 0.1 | mA |
| Short-circuit output current | | $I_{OS}$** | $V_{CC}$=5.25V | | −40 | — | −225 | mA |
| Supply current | | $I_{CCH}$ | $V_{CC}$=5.25V, OUTPUT OPEN | | — | 48 | 70 | mA |
| | | $I_{CCL}$ | | | — | 62 | 90 | mA |
| | | $I_{CCZ}$ | | | — | 64 | 95 | mA |
| Input clamp voitage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

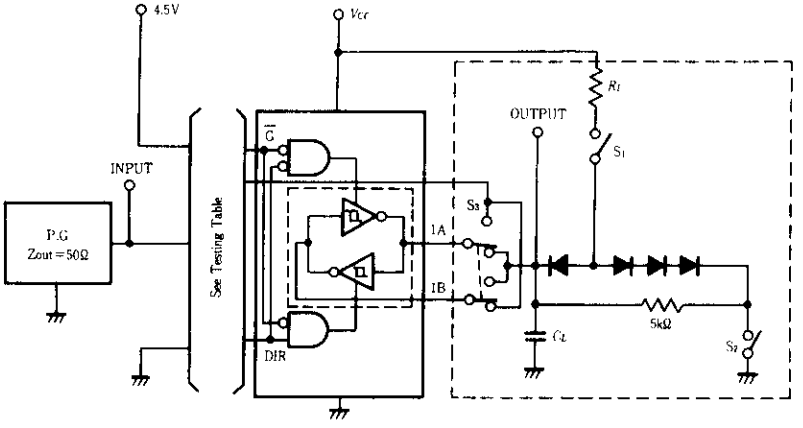
* $V_{CC}$ = 5V, $Ta$ = 25°C
** Not more than one output shall be shorted at a time.
The duration of the short circuit shall not exceed one second.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | INPUT | OUTPUT | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A | B | $C_L$=45pF, $R_L$=667Ω | — | 6 | 10 | ns |
| | | B | A | | — | 6 | 10 | ns |
| | $t_{PHL}$ | A | B | | — | 8 | 15 | ns |
| | | B | A | | — | 8 | 15 | ns |
| Output enable time | $t_{ZL}$ | $\overline{G}$ | A | | — | 31 | 40 | ns |
| | | $\overline{G}$ | B | | — | 31 | 40 | ns |
| | $t_{ZH}$ | $\overline{G}$ | A | | — | 23 | 40 | ns |
| | | $\overline{G}$ | B | | — | 23 | 40 | ns |
| Output disable time | $t_{LZ}$ | $\overline{G}$ | A | $C_L$=5pF, $R_L$=667Ω | — | 15 | 25 | ns |
| | | $\overline{G}$ | B | | — | 15 | 25 | ns |
| | $t_{HZ}$ | $\overline{G}$ | A | | — | 15 | 25 | ns |
| | | $\overline{G}$ | B | | — | 15 | 25 | ns |

## ■TESTING METHOD

### Test Circuit




Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.
3. 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B, 7A-7B, 8A-8B are identical to above load circuit.
4. $S_3$ is a input-output switch.

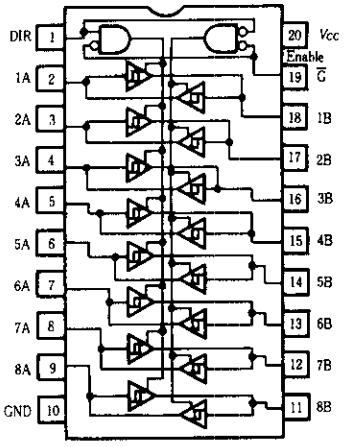


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# HD74LS641 ● Octal Bus Transceivers (non-inverted open-collector outputs)

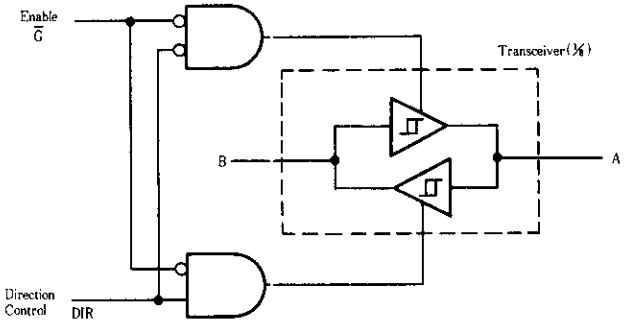
This octal bus transceivers is designed for asynchronous two-way communication between data buses. The devices transmit data, from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

## ■PIN ARRANGEMENT




(Top View)

## ■BLOCK DIAGRAM




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output voltage | $V_{OH}$ | — | — | 5.5 | V |
| Output current | $I_{OL}$ | — | — | 24 | mA |
| Operating temperature range | $T_{opr}$ | −20 | 25 | 75 | ℃ |

## ■FUNCTION TABLE

| Enable $\overline{G}$ | Direction Control DIR | Operation |
|---|---|---|
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | × | Isolation |

Notes) H; high level, L; low level, X; irrelevant

Home Print

## ■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | | | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Hysteresis | | $V_{T^+} - V_{T^-}$ | $V_{CC} = 4.75V$ | | 0.2 | — | — | V |
| Output current | | $I_{OH}$ | $V_{CC} = 4.75V$, $V_{IH} = 2V$, $V_{IL} = 0.8V$, $V_{OH} = 5.5V$ | | — | | 100 | μA |
| Output voltage | | $V_{OL}$ | $V_{CC} = 4.75V$, $V_{IH} = 2V$, $V_{IL} = 0.8V$ | $I_{OL} = 12mA$ | — | | 0.4 | V |
| | | | | $I_{OL} = 24mA$ | — | | 0.5 | V |
| Input current | | $I_{IH}$ | $V_{CC} = 5.25V$, $V_I = 2.7V$ | | | — | 20 | μA |
| | | $I_{IL}$ | $V_{CC} = 5.25V$, $V_I = 0.4V$ | | | — | −400 | μA |
| | A or B | $I_I$ | $V_{CC} = 5.25V$ | $V_I = 5.5V$ | — | | 0.1 | mA |
| | DIR or $\overline{G}$ | | | $V_I = 7V$ | — | | 0.1 | mA |
| Supply current | | $I_{CCH}$ | $V_{CC} = 5.25V$, output open | | — | 48 | 70 | mA |
| | | $I_{CCL}$ | | | — | 62 | 90 | mA |
| | | $I_{CCZ}$ | | | — | 64 | 95 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC} = 4.75V$, $I_{IN} = -18mA$ | | — | | −1.5 | V |

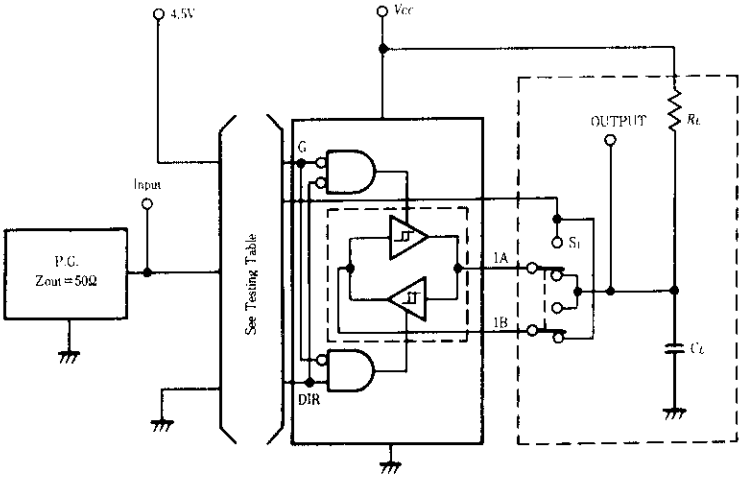
* $V_{CC} = 5V$, $Ta = 25°C$

## ■SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $Ta = 25°C$)

| Item | Symbol | INPUT | OUTPUT | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A | B | $C_L = 45pF$, $R_L = 667\ \Omega$ | — | 17 | 25 | ns |
| | | B | A | | — | 17 | 25 | ns |
| | $t_{PHL}$ | A | B | | — | 16 | 25 | ns |
| | | B | A | | — | 16 | 25 | ns |
| Output enable time | $t_{PLH}$ | $\overline{G}$ | A | | — | 23 | 40 | ns |
| | | $\overline{G}$ | B | | — | 25 | 40 | ns |
| | $t_{PHL}$ | $\overline{G}$ | A | | — | 34 | 50 | ns |
| | | $\overline{G}$ | B | | — | 37 | 50 | ns |

## ■TESTING METHOD

Test Circuit




Notes) 1. 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B, 7A-7B, 8A-8B, are identical to above load circuit.
2. $C_L$ includes probe and jig capacitance.
3. $S_1$ is a input-output switch.

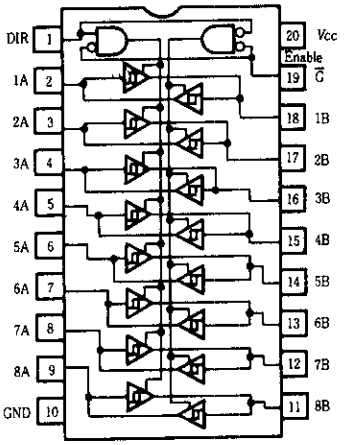


Home Print

# HD74LS641-1 ● Octal Bus Transceivers (non-inverted open-collector outputs)

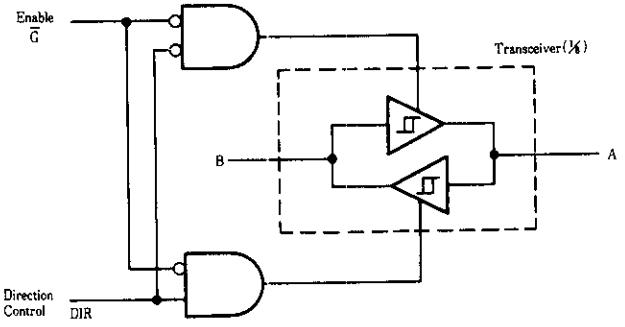
This octal bus transceivers is designed for asynchronous two-way communication between data buses. The devices transmit data, from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

## ■PIN ARRANGEMENT




(Top View)

## ■BLOCK DIAGRAM




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output voltage | $V_{OH}$ | — | — | 5.5 | V |
| Output current | $I_{OL}$ | — | — | 48 | mA |
| Operating temperature range | $T_{opr}$ | −20 | 25 | 75 | ℃ |

## ■FUNCTION TABLE

| Enable $\overline{G}$ | Direction Control DIR | Operation |
|---|---|---|
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | × | Isolation |

Notes) H; high level, L; low level, X; irrelevant

Home Print

## ■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Hysteresis | | $V_{T^+} - V_{T^-}$ | $V_{CC}=4.75V$ | | 0.2 | — | — | V |
| Output current | | $I_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$ | | — | — | 100 | μA |
| Output voltage | | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=12mA$ | — | — | 0.4 | V |
| | | | | $I_{OL}=24mA$ | — | — | 0.5 | V |
| | | | | $I_{OL}=48mA$ | — | — | 0.5 | V |
| Input current | | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | — | — | 20 | μA |
| | | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | — | — | −400 | μA |
| | A or B | $I_I$ | $V_{CC}=5.25V$ | $V_I=5.5V$ | — | — | 0.1 | mA |
| | DIR or $\overline{G}$ | | | $V_I=7V$ | — | — | 0.1 | mA |
| Supply current | | $I_{CCH}$ | $V_{CC}=5.25V$, output open | | — | 48 | 70 | mA |
| | | $I_{CCL}$ | | | — | 62 | 90 | mA |
| | | $I_{CCZ}$ | | | — | 64 | 95 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

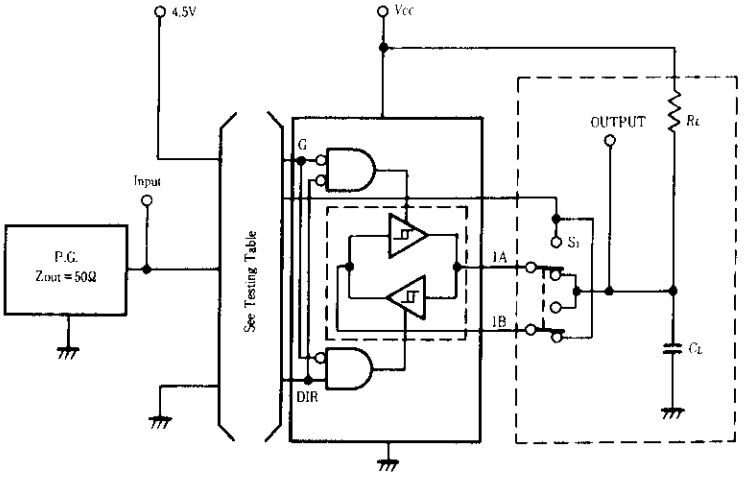
* $V_{CC}=5V$, $Ta=25°C$

## ■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

| Item | Symbol | INPUT | OUTPUT | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A | B | $C_L=45pF$, $R_L=667\Omega$ | — | 17 | 25 | ns |
| | | B | A | | — | 17 | 25 | ns |
| | $t_{PHL}$ | A | B | | — | 16 | 25 | ns |
| | | B | A | | — | 16 | 25 | ns |
| Output enable time | $t_{PLH}$ | $\overline{G}$ | A | | — | 23 | 40 | ns |
| | | $\overline{G}$ | B | | — | 25 | 40 | ns |
| | $t_{PHL}$ | $\overline{G}$ | A | | — | 34 | 50 | ns |
| | | $\overline{G}$ | B | | — | 37 | 50 | ns |

## ■TESTING METHOD

Test Circuit




Notes) 1. 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B, 7A-7B, 8A-8B, are identical to above load circuit.
2. $C_L$ includes probe and jig capacitance.
3. $S_1$ is a input-output switch.

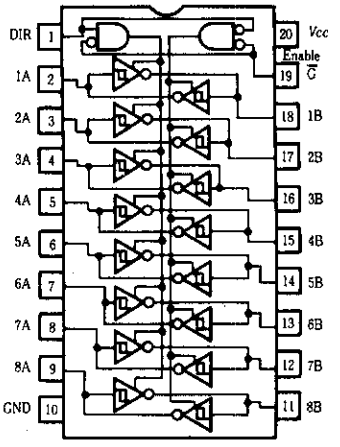


Home Print

# HD74LS642 ●Octal Bus Transceivers (inverted open-collector outputs)

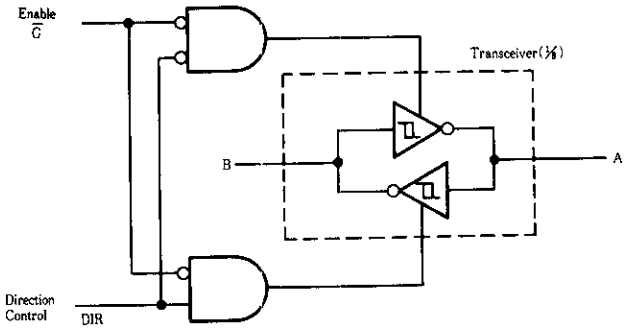
This octal bus transceiver is designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

## ■PIN ARRANGEMENT




(Top View)

## ■BLOCK DIAGRAM




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | unit |
|---|---|---|---|---|---|
| Output current | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output voltage | $V_{OH}$ | — | — | 5.5 | V |
| Output current | $I_{OL}$ | — | — | 24 | mA |
| Operating temperature range | $T_{opr}$ | −20 | 25 | 75 | ℃ |

## ■FUNCTION TABLE

| Enable $\overline{G}$ | Direction Control DIR | Operation |
|---|---|---|
| L | L | $\overline{B}$ data to A bus |
| L | H | $\overline{A}$ data to B bus |
| H | X | Isolation |

H; high level,
L; low level,
X; irrelevant

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## ■ELECTRICAL CHARACTERISTICS ($Ta$= −20~ +75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | | | V |
| | | $V_{IL}$ | | | | | 0.8 | |
| Hysteresis | | $V_{T^+}-V_{T^-}$ | $V_{CC}$=4.75V | | 0.2 | | | V |
| Output current | | $I_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $V_{OH}$=5.5V | | | | 100 | μA |
| Output voltage | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=12mA | | | 0.4 | V |
| | | | | $I_{OL}$=24mA | | | 0.5 | |
| Input current | | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | | | 20 | μA |
| | | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | | | −400 | μA |
| | A or B | $I_I$ | $V_{CC}$=5.25V | $V_I$=5.5V | | | 0.1 | mA |
| | DIR or $\overline{G}$ | | | $V_I$=7V | | | 0.1 | |
| Supply current** | | $I_{CCH}$ | $V_{CC}$=5.25V | | | 48 | 70 | mA |
| | | $I_{CCL}$ | | | | 62 | 90 | |
| | | $I_{CCZ}$ | | | | 64 | 95 | |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | | | −1.5 | V |

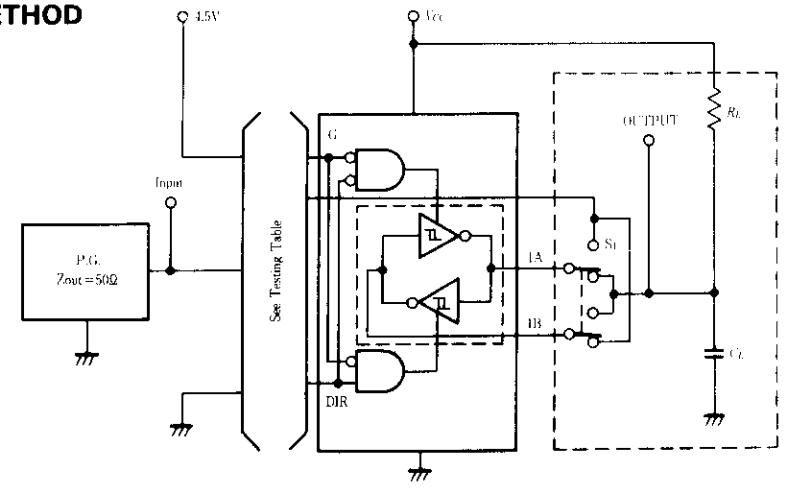
* $V_{CC}$ = 5V, $Ta$ = 25°C
** $I_{CC}$ is measured with all outputs open.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Input | Output | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A | B | $C_L$=45pF, $R_L$=667 Ω | — | 19 | 25 | ns |
| | | B | A | | | 19 | 25 | ns |
| | $t_{PHL}$ | A | B | | — | 14 | 25 | ns |
| | | B | A | | | 14 | 25 | ns |
| Output enable time | $t_{PLH}$ | $\overline{G}$ | A | | | 26 | 40 | ns |
| | | $\overline{G}$ | B | | | 28 | 40 | ns |
| | $t_{PHL}$ | $\overline{G}$ | A | | | 43 | 60 | ns |
| | | $\overline{G}$ | B | | | 39 | 60 | ns |

## ■TESTING METHOD

### Test Circuit




Notes) 1. 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B, 7A-7B, 8A-8B are identical to above load circuit.
2. $C_L$ includes probe and jig capacitance.
3. $S_1$ is a input-output switch.

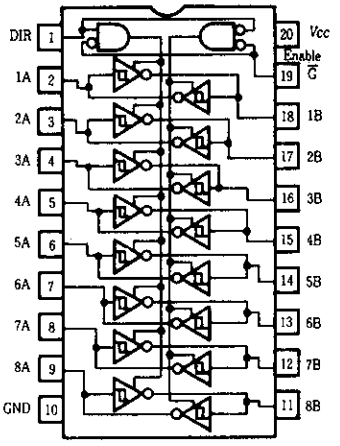


Home Print

# HD74LS642-1 ●Octal Bus Transceivers (inverted open-collector outputs)

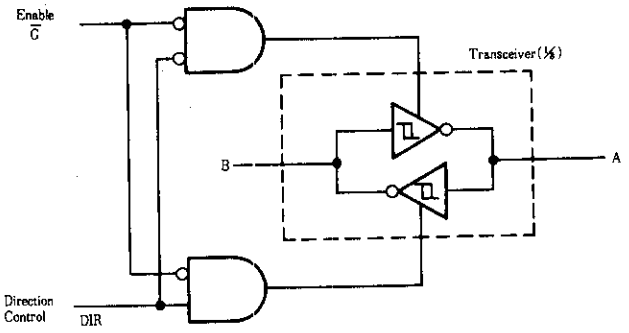
This octal bus transceiver is designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

## ■PIN ARRANGEMENT




(Top View)

## ■BLOCK DIAGRAM




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | unit |
|---|---|---|---|---|---|
| Output current | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output voltage | $V_{OH}$ | — | — | 5.5 | V |
| Output current | $I_{OL}$ | — | — | 48 | mA |
| Operating temperature range | $T_{opr}$ | −20 | 25 | 75 | ℃ |

## ■FUNCTION TABLE

| Enable $\overline{G}$ | Direction Control DIR | Operation |
|---|---|---|
| L | L | $\overline{B}$ data to A bus |
| L | H | $\overline{A}$ data to B bus |
| H | X | Isolation |

H; high level,
L; low level,
X; irrelevant

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## ■ELECTRICAL CHARACTERISTICS ($Ta$ = −20 ~ +75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | |
| Hysteresis | | $V_{T^+} - V_{T^-}$ | $V_{CC}$=4.75V | | 0.2 | — | — | V |
| Output current | | $I_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $V_{OH}$=5.5V | | — | — | 100 | μA |
| Output voltage | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=12mA | — | — | 0.4 | V |
| | | | | $I_{OL}$=24mA | — | — | 0.5 | |
| | | | | $I_{OL}$=48mA | — | — | 0.5 | |
| Input current | | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −400 | μA |
| | A or B | $I_I$ | $V_{CC}$=5.25V | $V_I$=5.5V | — | — | 0.1 | mA |
| | DIR or $\overline{G}$ | | | $V_I$=7V | — | — | 0.1 | |
| Supply current** | | $I_{CCH}$ | $V_{CC}$=5.25V | | — | 48 | 70 | mA |
| | | $I_{CCL}$ | | | — | 62 | 90 | |
| | | $I_{CCZ}$ | | | — | 64 | 95 | |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

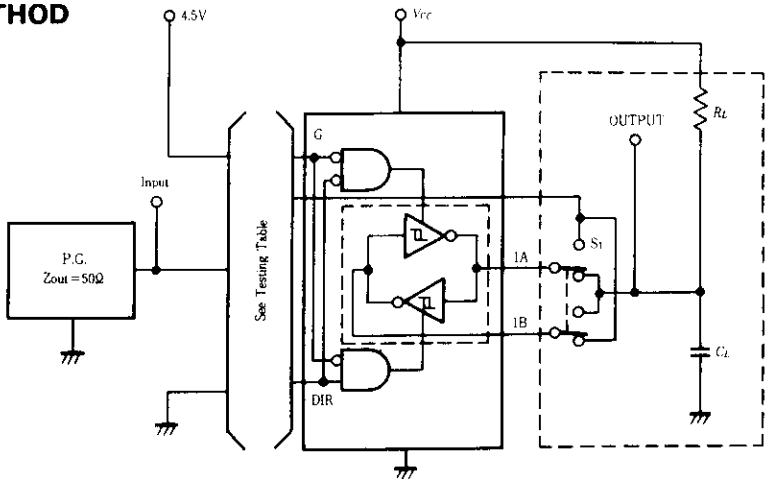
* $V_{CC}$ = 5V, $Ta$ = 25°C
** $I_{CC}$ is measured with all outputs open.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Input | Output | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A | B | $C_L$=45pF, $R_L$=667 Ω | — | 19 | 25 | ns |
| | | B | A | | — | 19 | 25 | ns |
| | $t_{PHL}$ | A | B | | — | 14 | 25 | ns |
| | | B | A | | — | 14 | 25 | ns |
| Output enable time | $t_{PLH}$ | $\overline{G}$ | A | | — | 26 | 40 | ns |
| | | $\overline{G}$ | B | | — | 28 | 40 | ns |
| | $t_{PHL}$ | $\overline{G}$ | A | | — | 43 | 60 | ns |
| | | $\overline{G}$ | B | | — | 39 | 60 | ns |

## ■TESTING METHOD

Test Circuit




Notes) 1. 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B, 7A-7B, 8A-8B are identical to above load circuit.
2. $C_L$ includes probe and jig capacitance.
3. $S_1$ is a input-output switch.

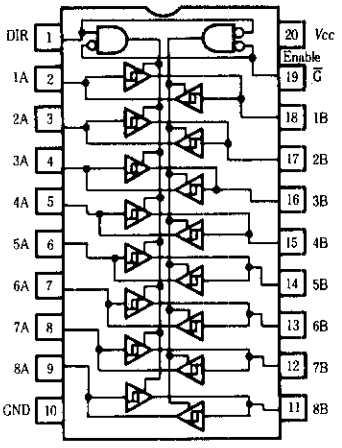


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# HD74LS645 ●Octal Bus Transceivers (non-inverted 3-state outputs)

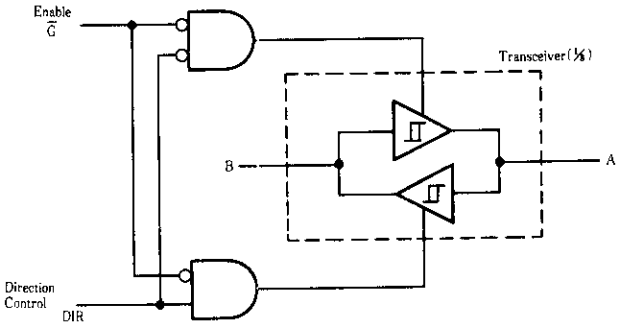
This octal bus transceiver is designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

## ■PIN ARRANGEMENT




(Top View)

## ■BLOCK DIAGRAM




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output current | $I_{OH}$ | — | — | −15 | mA |
| Output current | $I_{OL}$ | — | — | 24 | mA |
| Operating temperature range | $T_{opr}$ | −20 | 25 | 75 | ℃ |

## ■FUNCTIONAL TABLE

| Enable $\overline{G}$ | Direction Control DIR | Operation |
|---|---|---|
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

H; high level,
L; low level,
X; irrelevant

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## ■ELECTRICAL CHARACTERISTICS ($Ta$= −20~ +75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | | | V |
| | | $V_{IL}$ | | | — | — | 0.8 | |
| Hysteresis | | $V_{T^+}-V_{T^-}$ | $V_{CC}$=4.75V | | 0.2 | — | — | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, | $I_{OH}$=−3mA | 2.4 | — | — | V |
| | | | $V_{IL}$=0.8V | $I_{OH}$=−15mA | 2 | — | — | |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, | $I_{OL}$=12mA | — | — | 0.4 | V |
| | | | $V_{IL}$=0.8V | $I_{OL}$=24mA | — | — | 0.5 | |
| Output current | | $I_{OZH}$ | $V_{CC}$=5.25V | $V_O$=2.7V | — | — | 20 | μA |
| | | $I_{OZL}$ | $\overline{G}$ input =2V | $V_O$=0.4V | — | — | −400 | |
| Input current | | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −400 | μA |
| | A or B | $I_I$ | $V_{CC}$=5.25V | $V_I$=5.5V | — | — | 0.1 | mA |
| | DIR or $\overline{G}$ | | | $V_I$=7V | — | — | 0.1 | |
| Short-circuit output current | | $I_{OS}$*** | $V_{CC}$=5.25V | | −40 | — | −225 | mA |
| Supply current** | | $I_{CCH}$ | $V_{CC}$=5.25V, OUTPUT OPEN | | — | 48 | 70 | mA |
| | | $I_{CCL}$ | | | — | 62 | 90 | |
| | | $I_{CCZ}$ | | | — | 64 | 95 | |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$ = 5V, $Ta$ = 25°C
** $I_{CC}$ is measured with all outputs open.
*** Not more than one output should be shorted at a time, duration of short-circuit should not exceed one second.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

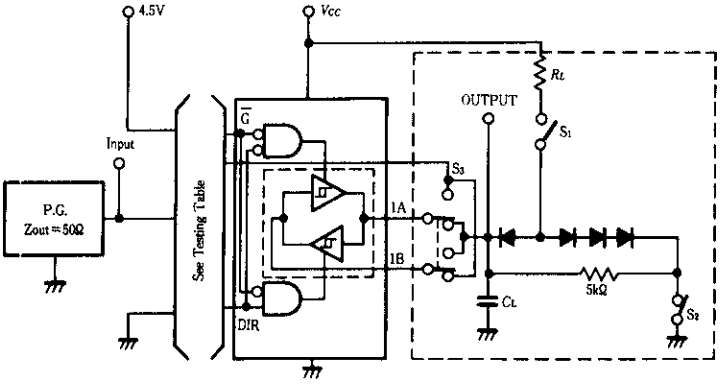
| Item | Symbol | Input | Output | Test Condition | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A | B | $C_L$=45pF, $R_L$=667Ω | — | 8 | 15 | ns |
| | | B | A | | — | 8 | 15 | ns |
| | $t_{PHL}$ | A | B | | — | 11 | 15 | ns |
| | | B | A | | — | 11 | 15 | ns |
| Output enable time | $t_{ZL}$ | $\overline{G}$ | A | | — | 31 | 40 | ns |
| | | $\overline{G}$ | B | | — | 31 | 40 | ns |
| | $t_{ZH}$ | $\overline{G}$ | A | | — | 26 | 40 | ns |
| | | $\overline{G}$ | B | | — | 26 | 40 | ns |
| Output disable time | $t_{LZ}$ | $\overline{G}$ | A | $C_L$=5pF, $R_L$=667Ω | — | 15 | 25 | ns |
| | | $\overline{G}$ | B | | — | 15 | 25 | ns |
| | $t_{HZ}$ | $\overline{G}$ | A | | — | 15 | 25 | ns |
| | | $\overline{G}$ | B | | — | 15 | 25 | ns |



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## ■TESTING METHOD

Test Circuit

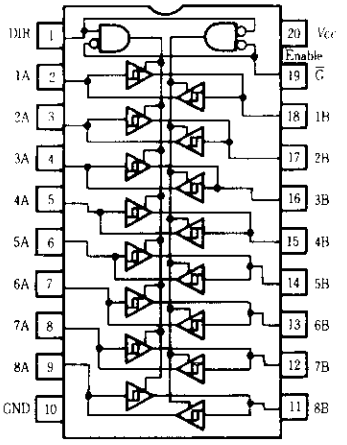



Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.
3. 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B, 7A-7B, 8A-8B are identical to above load circuit.
4. $S_3$ is a input-output switch.

# HD74LS645-1 ●Octal Bus Transceivers (non-inverted 3-state outputs)

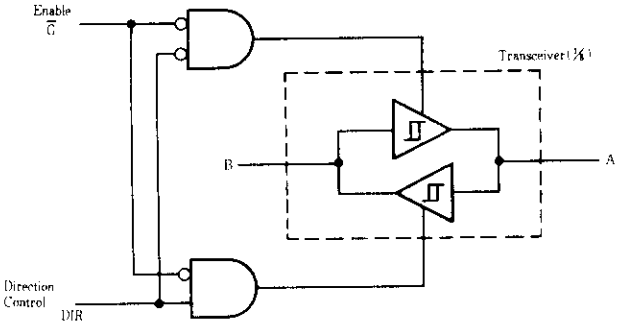
This octal bus transceiver is designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

## ■PIN ARRANGEMENT




(Top View)

## ■BLOCK DIAGRAM




## ■RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output current | $I_{OH}$ | — | — | −15 | mA |
| Output current | $I_{OL}$ | — | — | 48 | mA |
| Operating temperature range | $T_{opr}$ | −20 | 25 | 75 | ℃ |

## ■FUNCTIONAL TABLE

| Enable $\overline{G}$ | Direction Control DIR | Operation |
|---|---|---|
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

H; high level,
L; low level,
X; irrelevant



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## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2.0 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | |
| Hysteresis | | $V_T^+-V_T^-$ | $V_{CC}$=4.75V | | 0.2 | — | — | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OH}$=−3mA | 2.4 | — | — | V |
| | | | | $I_{OH}$=−15mA | 2 | — | — | |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=12mA | — | — | 0.4 | V |
| | | | | $I_{OL}$=24mA | — | — | 0.5 | |
| | | | | $I_{OL}$=48mA | — | — | 0.5 | |
| Output current | | $I_{OZH}$ | $V_{CC}$=5.25V, $\overline{G}$ input =2V | $V_O$=2.7V | — | — | 20 | μA |
| | | $I_{OZL}$ | | $V_O$=0.4V | — | — | −400 | |
| Input current | | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −400 | μA |
| | A or B | $I_I$ | $V_{CC}$=5.25V | $V_I$=5.5V | — | — | 0.1 | mA |
| | DIR or $\overline{G}$ | | | $V_I$=7V | — | — | 0.1 | |
| Short-circuit output current | | $I_{OS}$*** | $V_{CC}$=5.25V | | −40 | — | −225 | mA |
| Supply current** | | $I_{CCH}$ | $V_{CC}$=5.25V, OUTPUT OPEN | | — | 48 | 70 | mA |
| | | $I_{CCL}$ | | | — | 62 | 90 | |
| | | $I_{CCZ}$ | | | — | 64 | 95 | |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$ = 5V, $Ta$ = 25°C
** $I_{CC}$ is measured with all outputs open.
*** Not more than one output should be shorted at a time, duration of short-circuit should not exceed one second.

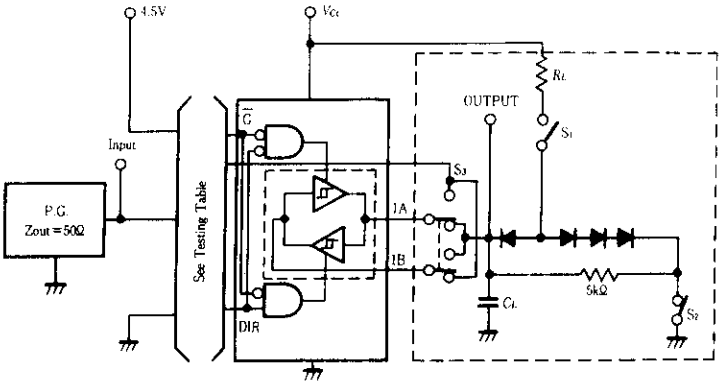
## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Input | Output | Test Condition | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A | B | $C_L$=45pF, $R_L$=667Ω | — | 8 | 15 | ns |
| | | B | A | | — | 8 | 15 | ns |
| | $t_{PHL}$ | A | B | | — | 11 | 15 | ns |
| | | B | A | | — | 11 | 15 | ns |
| Output enable time | $t_{ZL}$ | $\overline{G}$ | A | | — | 31 | 40 | ns |
| | | $\overline{G}$ | B | | — | 31 | 40 | ns |
| | $t_{ZH}$ | $\overline{G}$ | A | | — | 26 | 40 | ns |
| | | $\overline{G}$ | B | | — | 26 | 40 | ns |
| Output disable time | $t_{LZ}$ | $\overline{G}$ | A | $C_L$=5pF, $R_L$=667Ω | — | 15 | 25 | ns |
| | | $\overline{G}$ | B | | — | 15 | 25 | ns |
| | $t_{HZ}$ | $\overline{G}$ | A | | — | 15 | 25 | ns |
| | | $\overline{G}$ | B | | — | 15 | 25 | ns |

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## ■TESTING METHOD

Test Circuit




Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 (H).
3. 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B, 7A-7B, 8A-8B are identical to above load circuit.
4. $S_3$ is a input-output switch.



Home Print

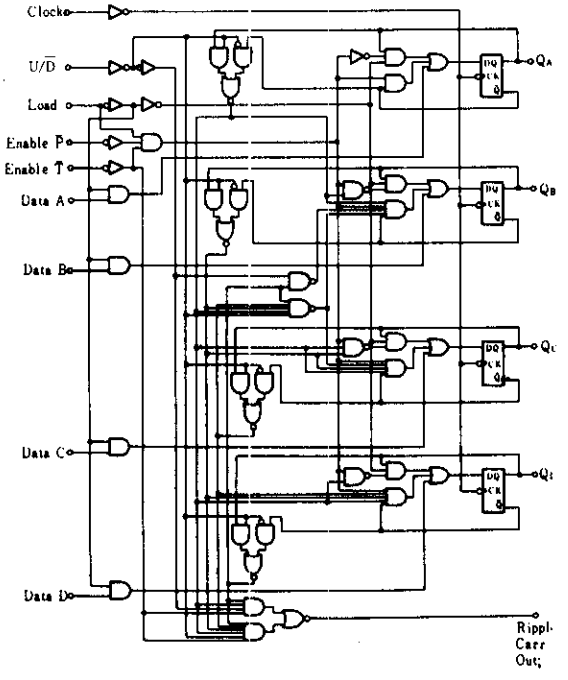
# HD74LS668 ●Synchronous Up/Down Decade Counters

This synchronous presettable decade counter features an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters.

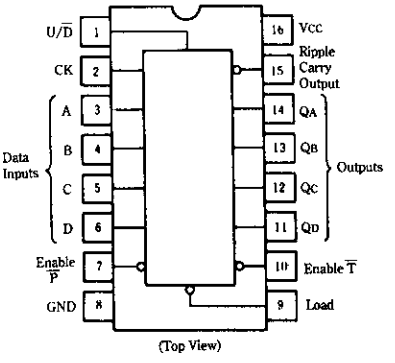
A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform. This counter is fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the $Q_A$ output when counting up and approximately equal to the low portion of the $Q_A$ output when counting down. This low level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. This counter features a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, Enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Output current | | $I_{OH}$ | — | — | −400 | μA |
| Output current | | $I_{OL}$ | — | — | 8 | mA |
| Clock frequency | | $f_{clock}$ | 0 | — | 25 | MHz |
| Clock pulse width | | $t_{w(ck)}$ | 25 | — | — | ns |
| Setup time | Input Data, A, B, C, D | $t_{su}$ | 25 | — | — | ns |
| | Enable $\overline{P}$, $\overline{T}$ | | 35 | — | — | |
| | Load | | 30 | — | — | |
| | Up/Down | | 35 | — | — | |
| Hold time | | $t_h$ | 0 | — | — | ns |

Home Print

## ■ELECTRICAL CHARACTERISTICS ($Ta$ = −20～+75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | — | — | 0.4 | V |
| | | | | $I_{OL}$=8mA | — | — | 0.5 | V |
| Input current | A, B, C, D, $\overline{P}$, U/$\overline{D}$ | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | Clock, $\overline{T}$ | | | | — | — | 20 | |
| | Load | | | | — | — | 40 | |
| | A, B, C, D, $\overline{P}$, U/$\overline{D}$ | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| | Clock, $\overline{T}$ | | | | — | — | −0.4 | |
| | Load | | | | — | — | −0.8 | |
| | A, B, C, D, $\overline{P}$, U/$\overline{D}$ | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.1 | mA |
| | Clock, $\overline{T}$ | | | | — | — | 0.1 | |
| | Load | | | | — | — | 0.2 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | — | −100 | mA |
| Supply current ** | | $I_{CC}$ | $V_{CC}$=5.25V | | — | 20 | 34 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** $I_{CC}$ is measured after applying a momentary 4.5V, then ground, to the clock input with all other inputs grounded the outputs open.

## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

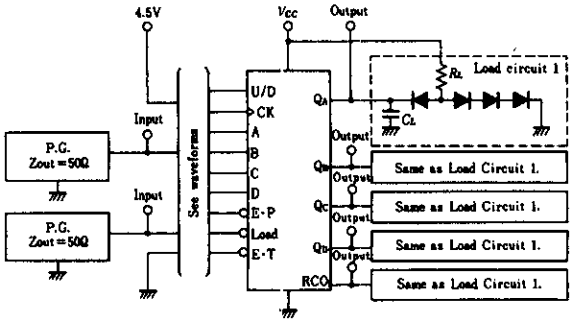
| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum count frequency | $f_{max}$ | | | $C_L$=15pF, $R_L$=2kΩ | 25 | 32 | — | MHz |
| Propagation delay time | $t_{PLH}$ | Clock | Ripple Carry | | — | 26 | 40 | ns |
| | $t_{PHL}$ | | | | — | 40 | 60 | |
| | $t_{PLH}$ | Clock | $Q_A$～$Q_D$ | | — | 18 | 27 | ns |
| | $t_{PHL}$ | | | | — | 18 | 27 | |
| | $t_{PLH}$ | Enable $\overline{T}$ | Ripple Carry | | — | 11 | 17 | ns |
| | $t_{PHL}$ | | | | — | 29 | 45 | |
| | $t_{PLH}$ | Up/Down | Ripple Carry | | — | 22 | 35 | ns |
| | $t_{PHL}$ | | | | — | 26 | 40 | |



Home Print

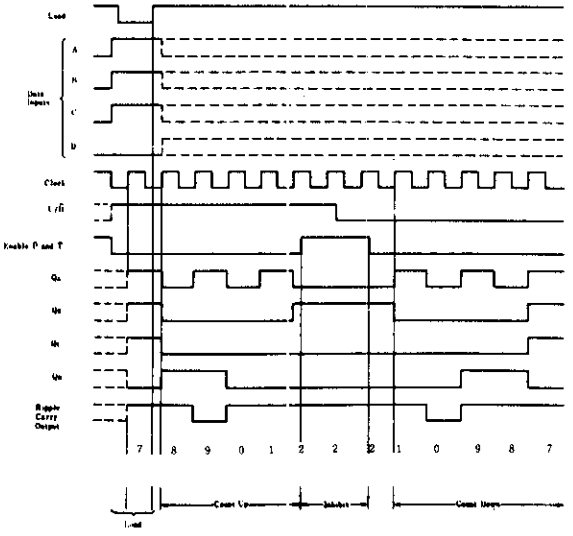
## ■TESTING METHOD

### 1) Test Circuit

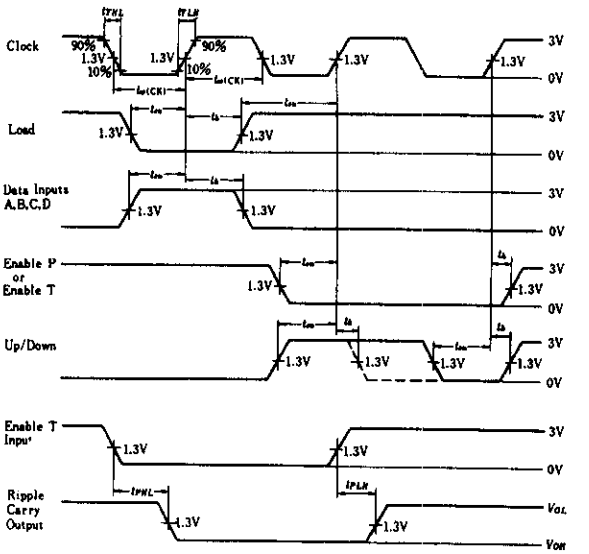



Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

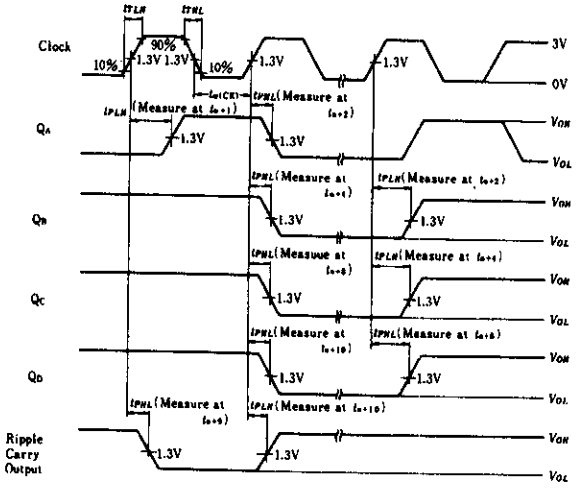
## ■COUNT SEQUENCE




### Waveform




Notes) 1. $t_{PLH}$ and $t_{PHL}$ from enable $\overline{T}$ input to ripple carry output assume that the counter is at the maximum count ($Q_A$ and $Q_D$ high).
2. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (9) the ripple carry output will be out of phase.
3. Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz




Notes) 1. Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz, duty cycle 50%.
2. For $f_{max}$, $t_{TLH} = t_{THL} \leqq 2.5$ns.
3. $t_n$ is the bit-time when all outputs are low.

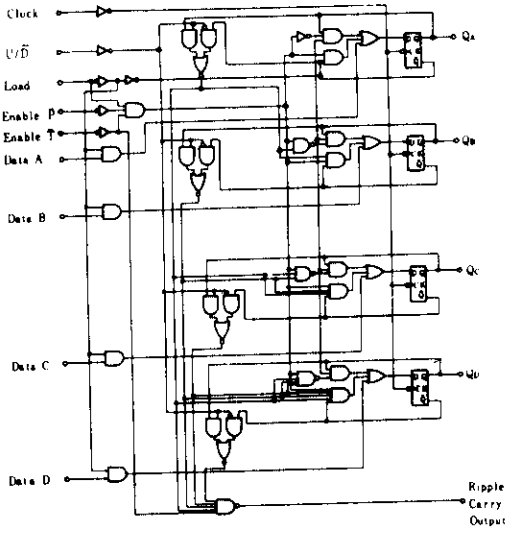
Home Print

# HD74LS669 ●Synchronous Up/Down 4-bit Binary Counters

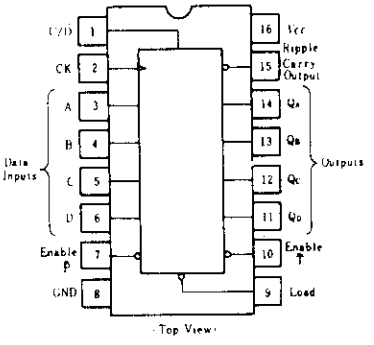
This synchronous presettable 4-bit binary counter features an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform. This counter is fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the $Q_A$ output when counting up and approximately equal to the low portion of the $Q_A$ output when counting down. This low level overflow carry pulse can be used to enable successive cascaded stages.

Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. This counter features a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

## ■BLOCK DIAGRAM




## ■PIN ARRANGEMENT




## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Output current | | $I_{OH}$ | — | — | −400 | μA |
| Output current | | $I_{OL}$ | — | — | 8 | mA |
| Clock frequency | | $f_{clock}$ | 0 | — | 25 | MHz |
| Clock pulse width | | $t_{w(CK)}$ | 25 | — | — | ns |
| Setup time | Input Data A, B, C, D | $t_{su}$ | 25 | — | — | ns |
| | Enable $\overline{P}$, $\overline{T}$ | | 35 | — | — | |
| | Load | | 30 | — | — | |
| | Up/Down | | 35 | — | — | |
| Hold time | | $t_h$ | 0 | — | — | ns |



Home Print

## ■ELECTRICAL CHARACTERISTICS ($Ta$=−20～+75°C)

| Item | | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | | | 2 | — | — | V |
| | | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | | $V_{OH}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V, $I_{OH}$=−400μA | | 2.7 | — | — | V |
| | | $V_{OL}$ | $V_{CC}$=4.75V, $V_{IH}$=2V, $V_{IL}$=0.8V | $I_{OL}$=4mA | — | — | 0.4 | V |
| | | | | $I_{OL}$=8mA | — | — | 0.5 | V |
| Input current | A, B, C, D, $\overline{P}$, U/$\overline{D}$ | $I_{IH}$ | $V_{CC}$=5.25V, $V_I$=2.7V | | — | — | 20 | μA |
| | Clock, $\overline{T}$ | | | | — | — | 20 | |
| | Load | | | | — | — | 40 | |
| | A, B, C, D, $\overline{P}$, U/$\overline{D}$ | $I_{IL}$ | $V_{CC}$=5.25V, $V_I$=0.4V | | — | — | −0.4 | mA |
| | Clock, $\overline{T}$ | | | | — | — | −0.4 | |
| | Load | | | | — | — | −0.8 | |
| | A, B, C, D, $\overline{P}$, U/$\overline{D}$ | $I_I$ | $V_{CC}$=5.25V, $V_I$=7V | | — | — | 0.1 | mA |
| | Clock, $\overline{T}$ | | | | — | — | 0.1 | |
| | Load | | | | — | — | 0.2 | |
| Short-circuit output current | | $I_{OS}$ | $V_{CC}$=5.25V | | −20 | — | −100 | mA |
| Supply current ** | | $I_{CC}$ | $V_{CC}$=5.25V | | — | 20 | 34 | mA |
| Input clamp voltage | | $V_{IK}$ | $V_{CC}$=4.75V, $I_{IN}$=−18mA | | — | — | −1.5 | V |

* $V_{CC}$=5V, $Ta$=25°C

** $I_{CC}$ is measured after applying a momentary 4.5V, then ground, to clock input with all other inputs grounded the outputs open.

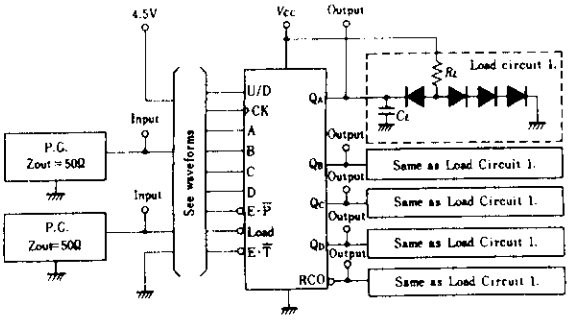
## ■SWITCHING CHARACTERISTICS ($V_{CC}$=5V, $Ta$=25°C)

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Maximum count frequency | $f_{max}$ | | | $C_L$=15pF, $R_L$=2kΩ | 25 | 32 | — | MHz |
| Propagation delay time | $t_{PLH}$ | Clock | Ripple Carry | | — | 26 | 40 | ns |
| | $t_{PHL}$ | | | | — | 40 | 60 | |
| | $t_{PLH}$ | Clock | $Q_A$～$Q_D$ | | — | 18 | 27 | ns |
| | $t_{PHL}$ | | | | — | 18 | 27 | |
| | $t_{PLH}$ | Enable $\overline{T}$ | Ripple Carry | | — | 11 | 17 | ns |
| | $t_{PHL}$ | | | | — | 29 | 45 | |
| | $t_{PLH}$ | Up/Down | Ripple Carry | | — | 22 | 35 | ns |
| | $t_{PHL}$ | | | | — | 26 | 40 | |

Home Print

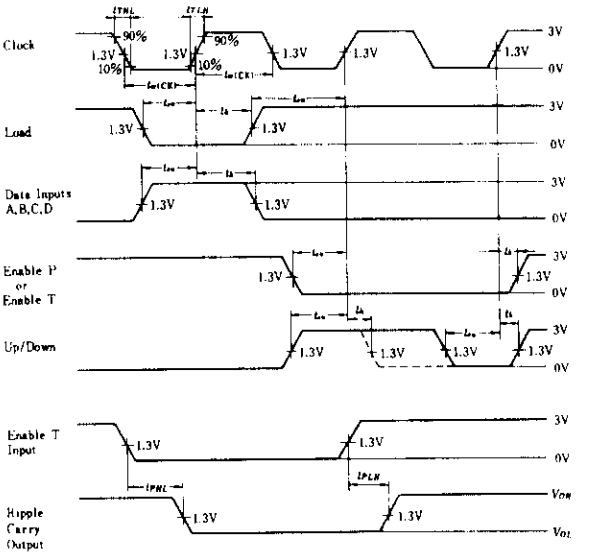
## ■TESTING METHOD

### 1) Test Circuit



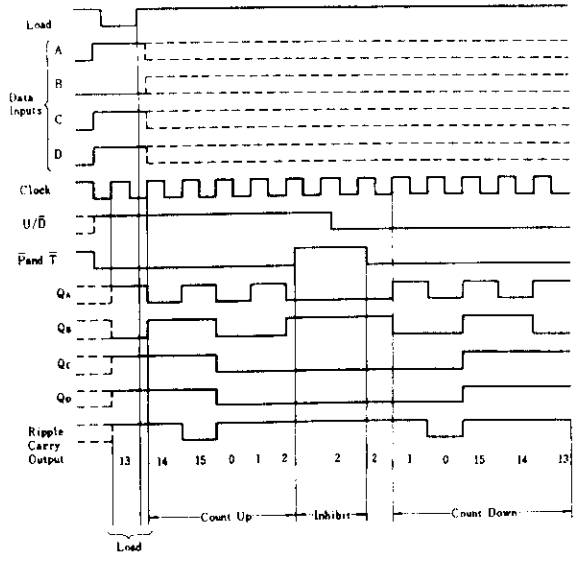

Notes) 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 (H).

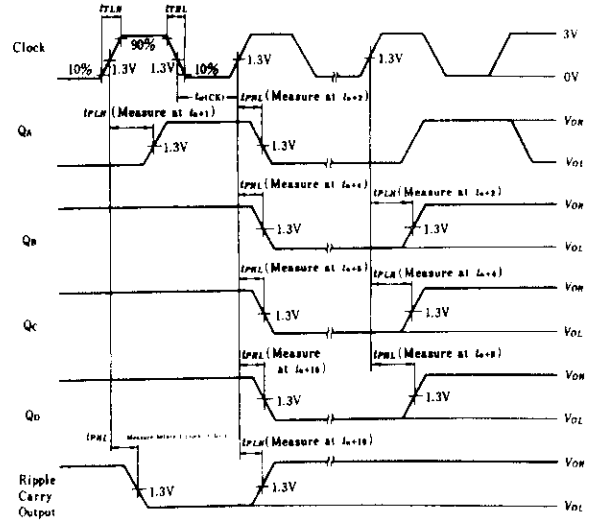
### Waveform




Notes) 1. $t_{PLH}$ and $t_{PHL}$ from enable $\overline{T}$ input to ripple carry output assume that the counter is at the maximum count ($Q_A$ through $Q_D$ high).
2. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) are ripple carry output transition will be in phase. If the count is maximum (15) the ripple carry output will be out of phase.
3. Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz

## ■COUNT SEQUENCE




Notes) 1. Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz, duty cycle 50%.
2. For $f_{max}$, $t_{TLH} = t_{THL} \leqq 2.5$ns.
3. $t_n$ is the bit-time when all outputs are low.



Home Print

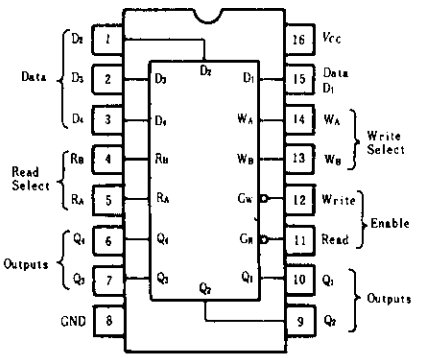
# HD74LS670 ●4-by-4 Register File (with three-state outputs)

The HD74LS670, 16-bit register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the the four word locations to either write-in or retrieve data.

This permits simultaneous writing into one location and reading from another word location. Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, $G_W$, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, $G_R$, is high, the data outputs are inhibited and go into the high-impedance state. The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word.

When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

## ■PIN ARRANGEMENT




(Top View)

## ■FUNCTION TABLE

| Write Inputs | | | Word | | | |
|---|---|---|---|---|---|---|
| $W_B$ | $W_A$ | $G_W$ | 0 | 1 | 2 | 3 |
| L | L | L | Q=D | $Q_0$ | $Q_0$ | $Q_0$ |
| L | H | L | $Q_0$ | Q=D | $Q_0$ | $Q_0$ |
| H | L | L | $Q_0$ | $Q_0$ | Q=D | $Q_0$ |
| H | H | L | $Q_0$ | $Q_0$ | $Q_0$ | Q=D |
| × | × | H | $Q_0$ | $Q_0$ | $Q_0$ | $Q_0$ |

| Read Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|
| $R_B$ | $R_A$ | $G_R$ | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ |
| L | L | L | $W_0 B_1$ | $W_0 B_2$ | $W_0 B_3$ | $W_0 B_4$ |
| L | H | L | $W_1 B_1$ | $W_1 B_2$ | $W_1 B_3$ | $W_1 B_4$ |
| H | L | L | $W_2 B_1$ | $W_2 B_2$ | $W_2 B_3$ | $W_2 B_4$ |
| H | H | L | $W_3 B_1$ | $W_3 B_2$ | $W_3 B_3$ | $W_3 B_4$ |
| × | × | H | Z | Z | Z | Z |

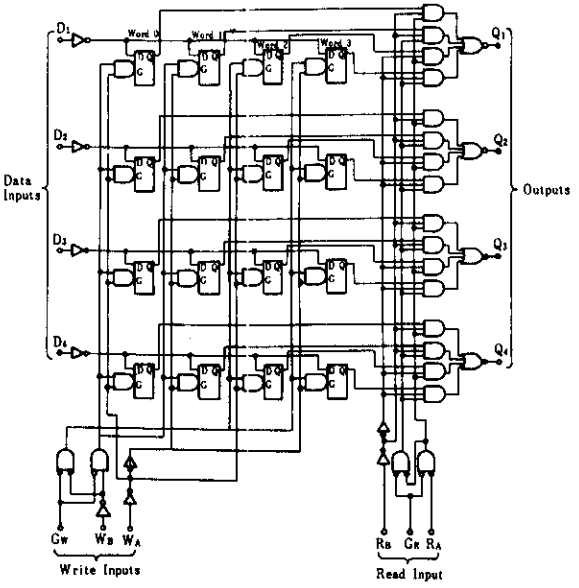
Notes: H = high level, L = low level, X = irrelevant, Z = high impedance (off)

(Q=D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

$Q_0$ = The level of Q before the indicated input conditions were established.

$W_0 B_1$ = The first bit of word 0, etc.

## ■BLOCK DIAGRAM




Home Print

## ■RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output current | | $I_{OH}$ | — | — | −2.6 | mA |
| | | $I_{OL}$ | — | — | 8 | mA |
| Pulse width | Read enable | $t_w$ | 25 | — | — | ns |
| | Write enable | | 60 | — | — | |
| Setup time | Data | $t_{su}$ | 10 | — | — | ns |
| | Write enable | | 15 | — | — | |
| Hold time | Data | $t_h$ | 15 | — | — | ns |
| | Write enable | | 5 | — | — | |
| Latch time | | $t_{latch}$ | 60 | — | — | ns |

## ■ELECTRICAL CHARACTERISTICS ($Ta=-20\sim+75°C$)

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | — | — | V |
| | $V_{IL}$ | | | — | — | 0.8 | V |
| Output voltage | $V_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-2.6mA$ | | 2.4 | — | — | V |
| | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | — | — | 0.4 | V |
| | | | $I_{OL}=8mA$ | — | — | 0.5 | |
| Off-state output current | $I_{OZH}$ | $V_{CC}=5.25V$, $V_{IH}=2V$ | $V_O=2.7V$ | — | — | 20 | μA |
| | $I_{OZL}$ | | $V_O=0.4V$ | — | — | −20 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | Any D, R or W | — | — | 20 | μA |
| | | | $G_W$ | — | — | 40 | |
| | | | $G_R$ | — | — | 60 | |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | Any D, R or W | — | — | −0.4 | mA |
| | | | $G_W$ | — | — | −0.8 | |
| | | | $G_R$ | — | — | −1.2 | |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | Any D, R or W | — | — | 0.1 | mA |
| | | | $G_W$ | — | — | 0.2 | |
| | | | $G_R$ | — | — | 0.3 | |
| Short-circuit output current | $I_{OS}$ | $V_{CC}=5.25V$ | | −30 | — | −130 | mA |
| Supply current | $I_{CC}$** | $V_{CC}=5.25V$ | | — | 30 | 50 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | — | — | −1.5 | V |

* $V_{CC}=5V$, $Ta=25°C$

** : Maximum $I_{CC}$ is guaranteed for the following worst case conditions: 4.5V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

## ■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

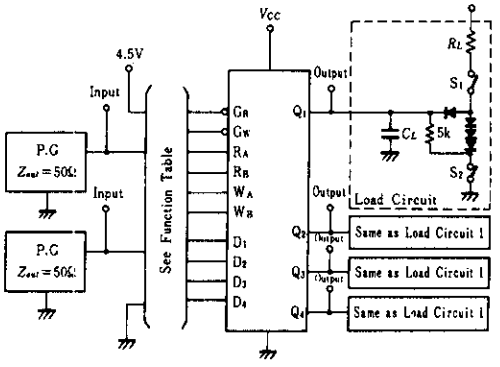
| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | Read select | $Q_1\sim Q_4$ | $C_L=15pF$, $R_L=2k\Omega$ | — | 23 | 40 | ns |
| | $t_{PHL}$ | | | | — | 25 | 45 | |
| | $t_{PLH}$ | Write enable | $Q_1\sim Q_4$ | | — | 26 | 45 | |
| | $t_{PHL}$ | | | | — | 28 | 50 | |
| | $t_{PLH}$ | Data | $Q_1\sim Q_4$ | | — | 25 | 45 | |
| | $t_{PHL}$ | | | | — | 23 | 40 | |
| Output enable time | $t_{ZH}$ | Read enable | $Q_1\sim Q_4$ | | — | 15 | 35 | |
| | $t_{ZL}$ | | | | — | 22 | 40 | |
| Output disable time | $t_{HZ}$ | | | $C_L=5pF$, $R_L=2k\Omega$ | — | 30 | 50 | |
| | $t_{LZ}$ | | | | — | 16 | 35 | |



Home Print

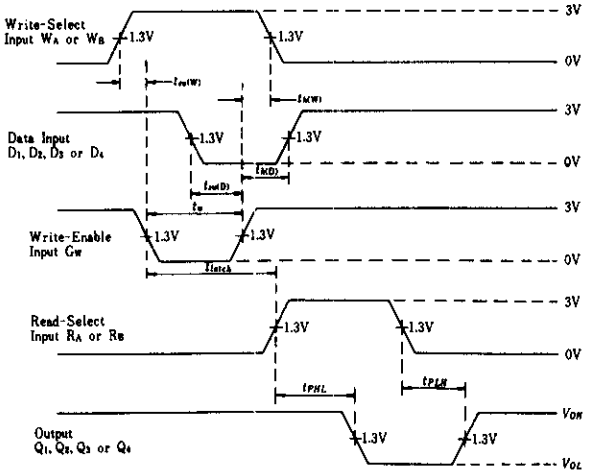
## ■TESTING METHOD

Test Circuit



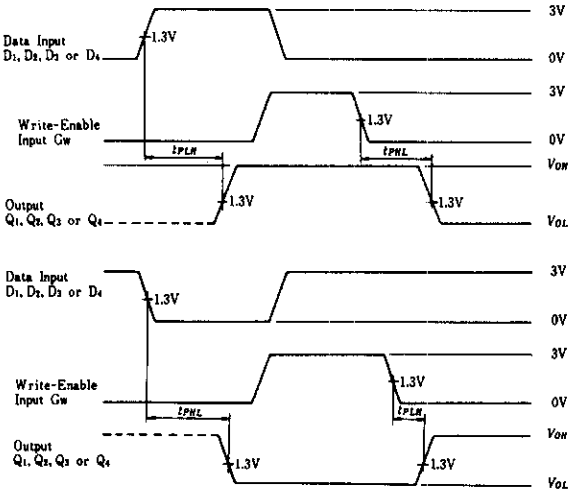

Notes: 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

Waveform-1



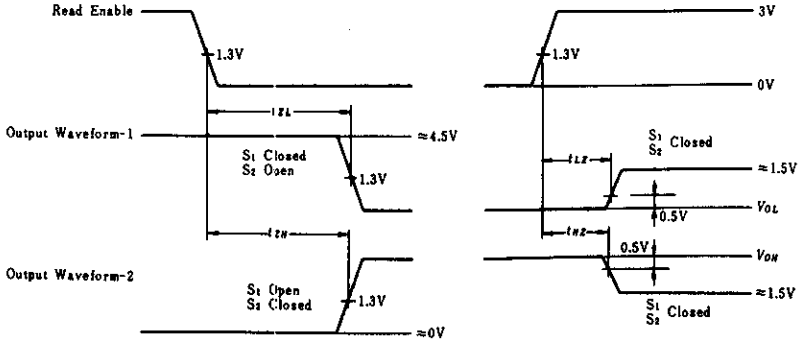

Notes: 1. High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.
2. When measuring delay times from a read-select inputs, the read-enable input is low.
3. Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz, duty cycle 50%

Waveform-2




Note: Each select address is tested. Prior to the start of each of the above test both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test $G_R$ is low.

Waveform-3




Waveform A is for an output with internal conditions such that the output is low except when disabled by the read-enable input. Waveform B is for an output with internal conditions such that the output is high except when disabled by the read-enable input.

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