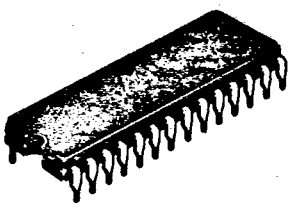
HD44007A

T-77-17

Sync Signal Generator for TV Cameras (NTSC, PAL/SECAM)

Functions

- Four times chroma sub-carrier oscillator frequency
- (B-Y) and (R-Y) chroma sub-carrier output circuit
- Active filter genlock phase detector
- Horizontal programmable logic array
- Vertical programmable logic array
- Horizontal/vertical programmable logic array



(DP-28)

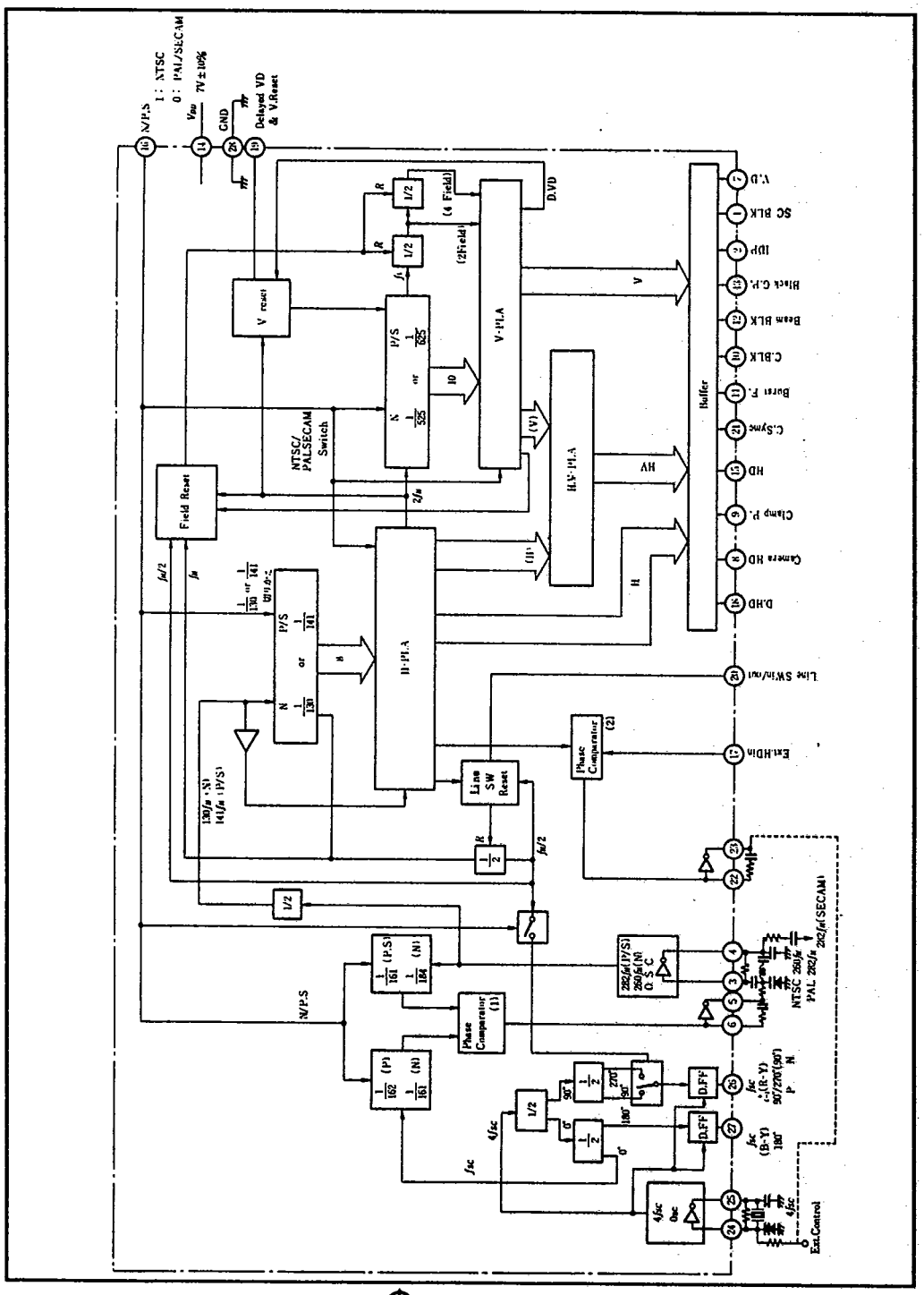
Ordering Information

Type No.	Package
HD44007A	DP-28

Pin Description

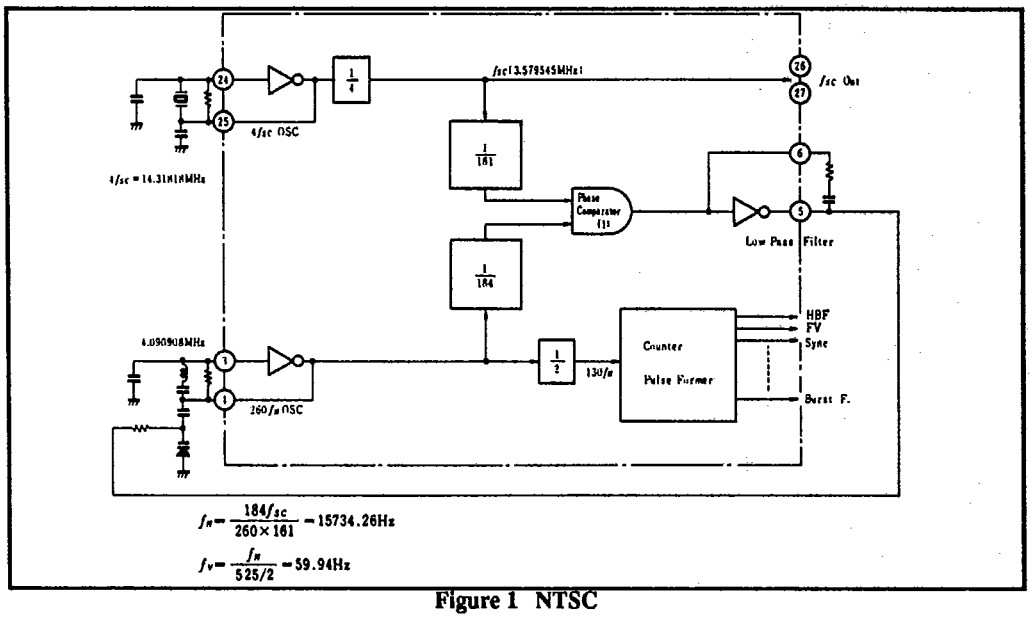
Pin No.	Function	Note	Max Output Current
1	SC. BLK	Identification pulse for SECAM	+250 µA
2	ID. P	Identification pulse for SECAM	+250 µA
3	260 f_H/282 f_H osc	In	
4	260 f_H/282 f_H osc	Out	
5	Filter	Out	
6	Filter	In	
7	VD		±250 µA
8	Camera HD		±500 µA
9	Clamp P		±500 µA
10	Composite BLK		±500 µA
11	Burst flag P		±100 µA
12	Beam BLK		±500 µA
13	Black gate P		±500 µA
14	V_{DD}	6.3 V to 7.0 V, typ 7.7 V	
15	HD		±500 µA
16	Selector input	High level for NTSC, low level for PAL and SECAM	
17	External HD in	H genlock input	
18	Delayed HD		±500 µA
19	Delayed VD in/out	In/out, output: $V_{OH} \geq 0.8\ V_{DD}$, $V_{OL} = 0.5\ V_{DD}$, input threshold $0.25\ V_{DD}$	–500 µA
20	Line SW in/out	In/out, pull-up resistor built-in	+250 µA
21	Composite Sync		
22	Filter	In	
23	Filter	Out	
24	4 f_{SC} osc	In	
25	4 f_{SC} osc	Out	
26	SC (90°/270°)	For NTSC, 90° only (high level at pin 16)	±100 µA
27	SC (180°)		±100 µA
28	GND		

Block Diagram



Operations

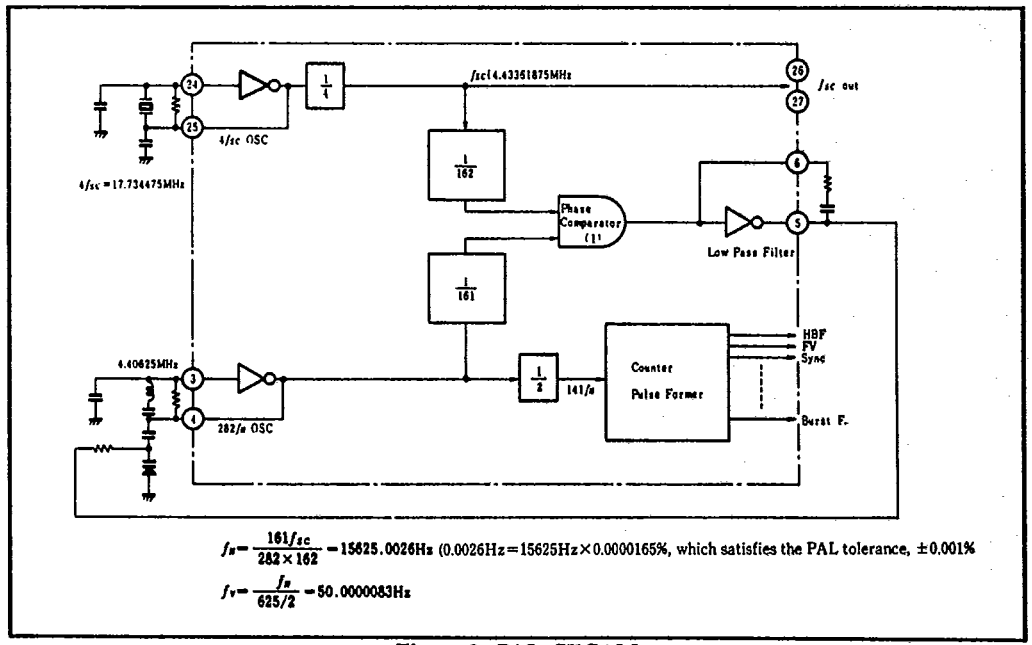
Interleave (external HS input, pin 17 and phase comparator 2 are not used.) See figures 1 and 2.



$$f_H = \frac{184 f_{sc}}{260 \times 161} = 15734.26\text{Hz}$$

$$f_V = \frac{f_H}{525/2} = 59.94\text{Hz}$$

Figure 1 NTSC



$$f_H = \frac{161 f_{sc}}{282 \times 162} = 15625.0026\text{Hz}$$ (0.0026Hz = 15625Hz × 0.0000165%, which satisfies the PAL tolerance, ±0.001%

$$f_V = \frac{f_H}{625/2} = 50.0000083\text{Hz}$$

Figure 2 PAL, SECAM

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Genlock

In genlock mode, the operating principles of NTSC and PAL/SECAM are the same, so only NTSC is described below. See figure 3.

Phase comparator 1 is not used. See figure 4.

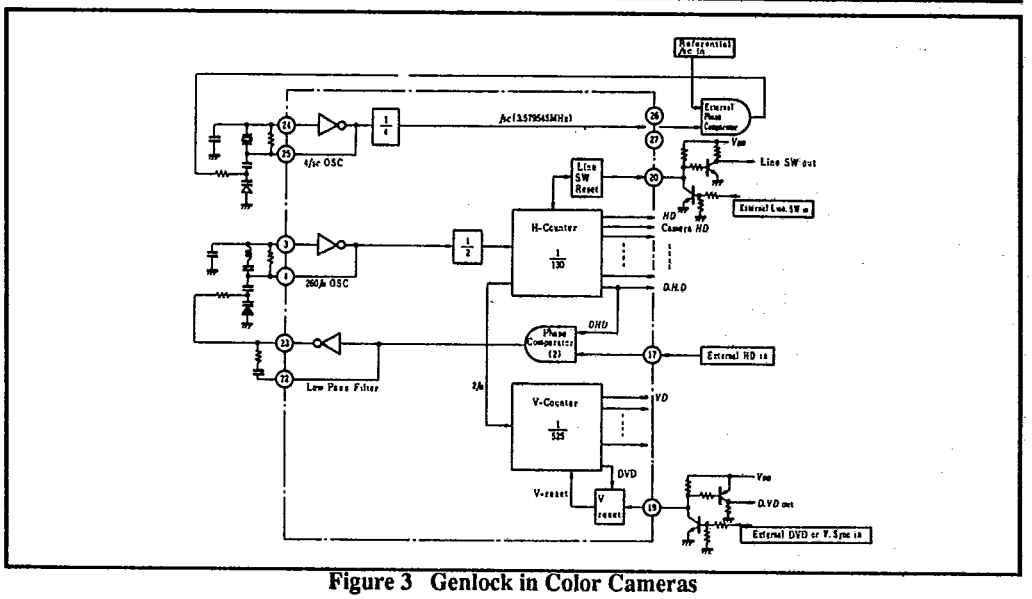
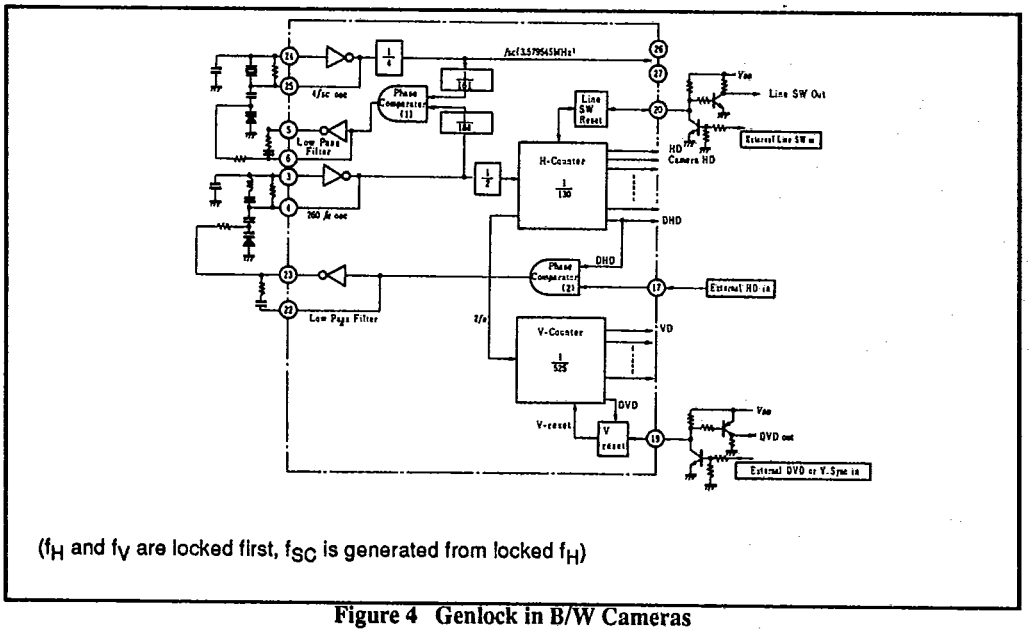


Figure 3 Genlock in Color Cameras



(f_H and f_V are locked first, f_{SC} is generated from locked f_H)

Figure 4 Genlock in B/W Cameras

Special Input/Output Terminals

Pin 20 is for line SW input and output (figure 5). Figure 6 shows the internal circuit and IC operation. The LC oscillator uses a CMOS inverter and crystal oscillator. There is no internal DC feedback resistor, so an external resistor for feedback should be connected, as in figure 7.

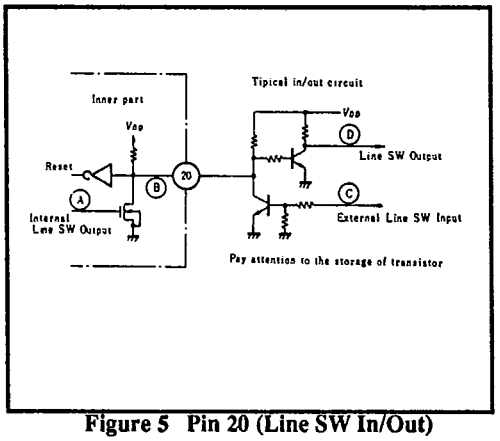


Figure 5 Pin 20 (Line SW In/Out)

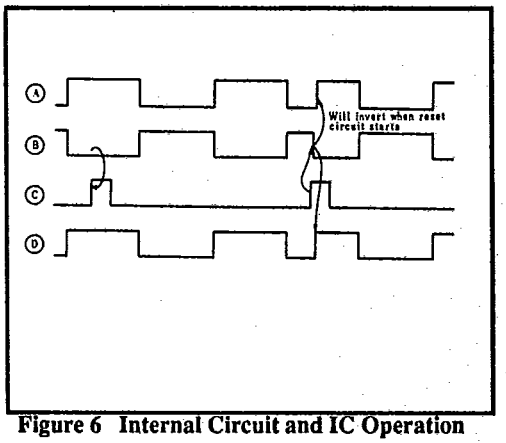


Figure 6 Internal Circuit and IC Operation

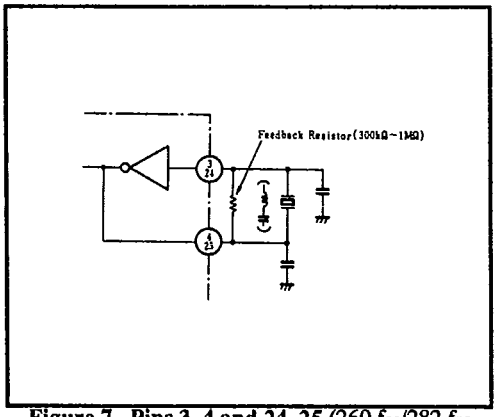


Figure 7 Pins 3, 4 and 24, 25 (260 f_H/282 f_H osc, 4 f_{SC} osc)

Pin 19 is for VD output and V reset input. Figure 8 shows the internal circuit and IC operation. Output impedance is 500 Ω to 2 kΩ when pin 19 output is $V_{DD}/2$.

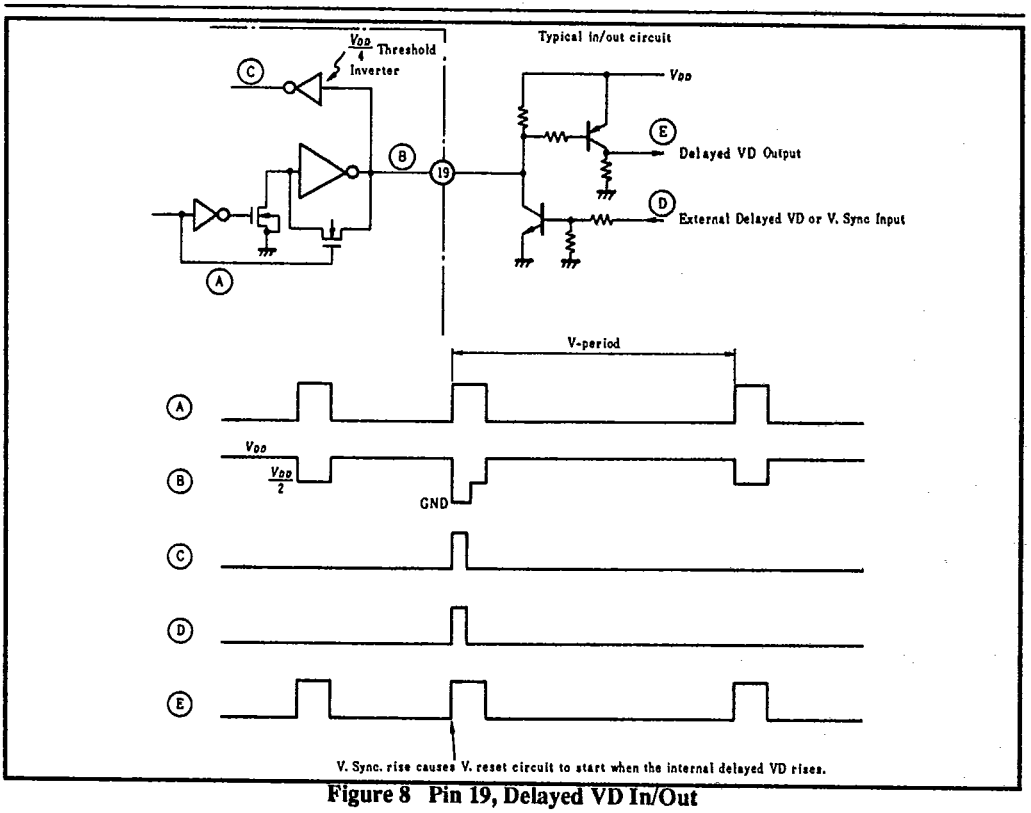


Figure 8 Pin 19, Delayed VD In/Out

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	10	V
Input Voltage	V_{IN}	–0.3 to VDD + 0.3	V
Power Dissipation (Ta = 85°C)	P_T	450	mW
Operating Temperature	T_{opr}	–30 to +85	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Operating Supply Voltage	V_{DD}	6.3	7.0	7.7	V	
Supply Current	I_{DD}	—	—	40	mA	Output pins open, under oscillation
Input Voltage	V_{IH}	0.8 Vp-p	—	V_{DD} + 0.3	V	Pins 16, 17, and 20
	V_{IL}	–0.3	—	0.2 V_{DD}	V	
Input Threshold Voltage	V_{IH}	0.2 V_{DD}	0.25 V_{DD}	0.3 V_{DD}	V	Pin 19
Output Voltage	V_{OH}	0.8 V_{DD}	—	—	V	Pins11, 26, and 27, I_{OH} = –100 µA
		0.8 V_{DD}	—	—	V	Pins1, 2, and 7, I_{OH} = –250 µA
		0.8 V_{DD}	—	—	V	Pins 8, 9, 10, 12, 13, 15, 18, 19 and 21, I_{OH} = –500 µA
	V_{OL}	—	—	0.2 V_{DD}	V	Pins 11, 26, and 27, I_{OL} = 100 µA
		—	—	0.2 V_{DD}	V	Pins 1, 2, 7, and 20, I_{OL} = 250 µA
		—	—	0.2 V_{DD}	V	Pins 8, 9, 10, 12, 13, 15, 18, and 21, I_{OL} = 500 µA
		0.4 V_{DD}	0.5 V_{DD}	0.6 V_{DD}	V	Pin 19, open
Output Impedance	Z_{out}	500	1000	2000	Ω	Low output level at pin 19
Pull-Up Resistance	I_R	–200	–100	–50	µA	High output level at pin 20, pin 20 grounded

Electrical Characeristics (cont)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Maximum Clock Pulse Frequency	$f_{C\ max}$	20	—	—	MHz	V_{DD} = 6.3 V, 20 MHz crystal resonator between pins 24 and 25, output at pins 26 and 27 (20/4 = 5 MHz output)
Maximum Divider Operating Frequency	$f_{D\ max}$	5.0	—	—	MHz	V_{DD} = 6.3 V, LC between pins 3 and 4, normal oscillation frequency at output terminal
Pin 26 Output Phase Angle (NTSC)	ϕN	88	90	92	deg	Pin 26 output phase referred to 180° (= pin 27 output phase), pin 16: V_{DD}, V_{DD} = 6.3–7.7 V
Pin 26 Output Phase Angle (PAL 1)	$\phi P1$	88	90	92	deg	Pin 26 output phase referred to 180° (= pin 27 output phase), pin 16: GND, high level line output
Pin 26 Output Phase Angle (PAL 2)	$\phi P2$	268	270	272	deg	Pin 26 output phase referred to 180° (= pin 27 output phase), pin 16: GND, low level line output

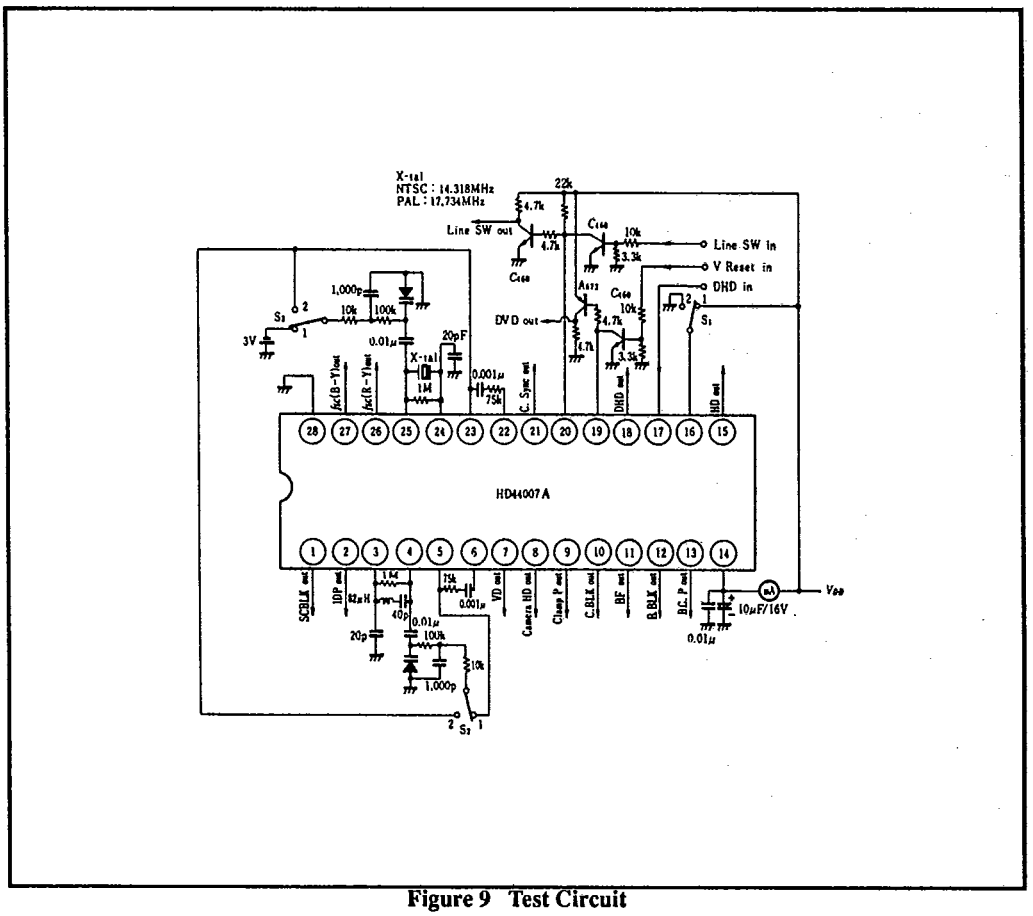


Figure 9 Test Circuit

Table 1 Test Circuit

	S_2	S_3
Interleave	1	1
Genlock	2	2

	S_1	x-tal
NTSC	1	14.318 MHz
PAL/SECAM	2	17.734 MHz

Timing Charts

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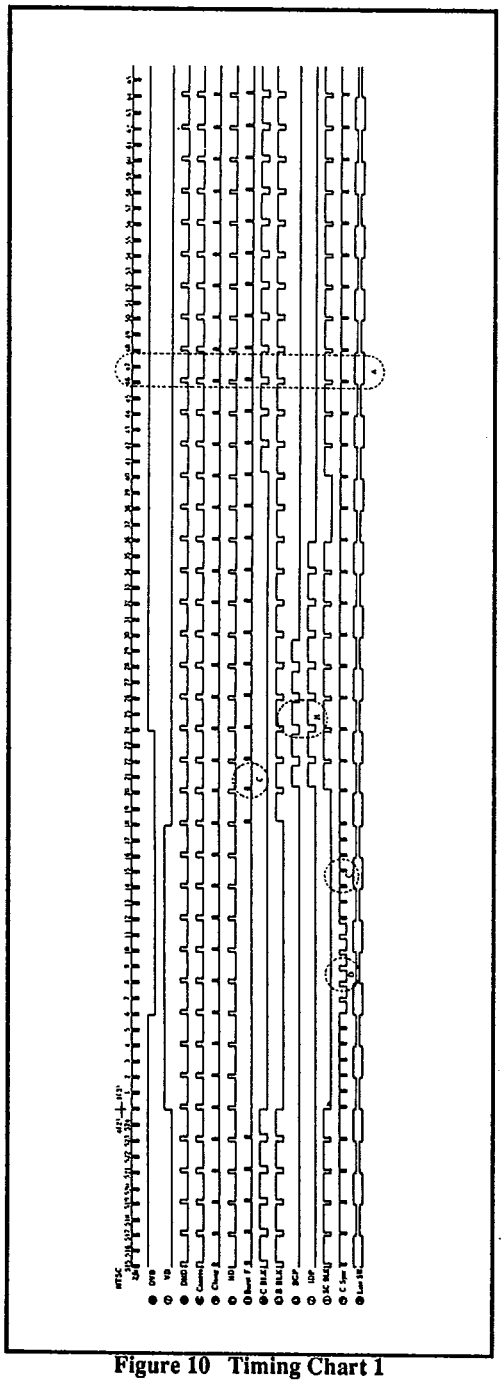

Figure 10 Timing Chart 1

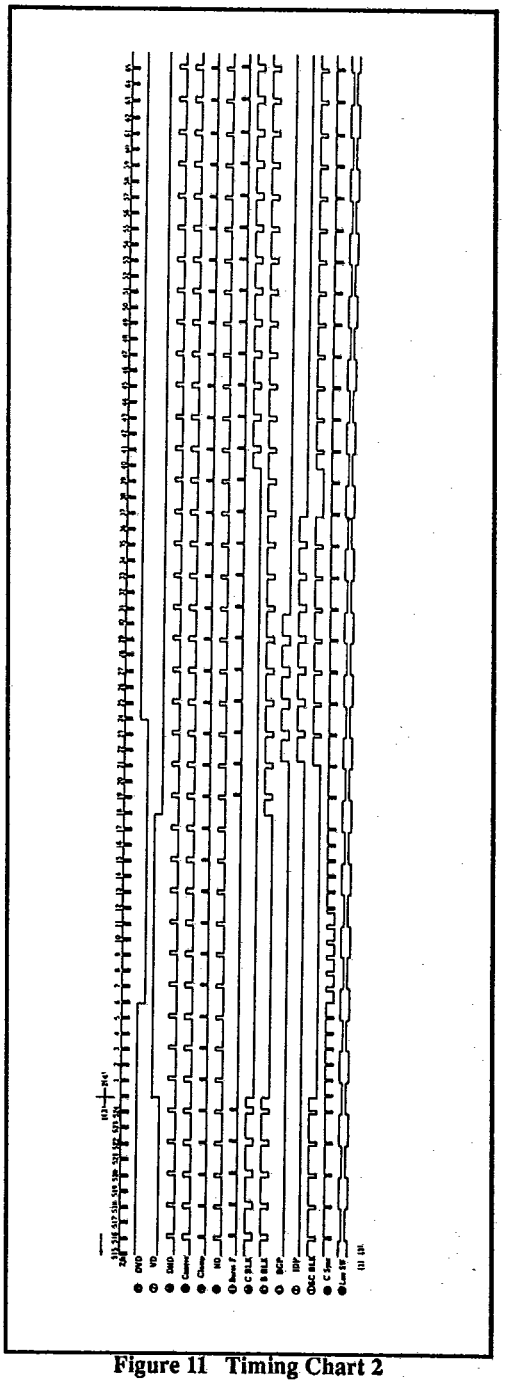

Figure 11 Timing Chart 2

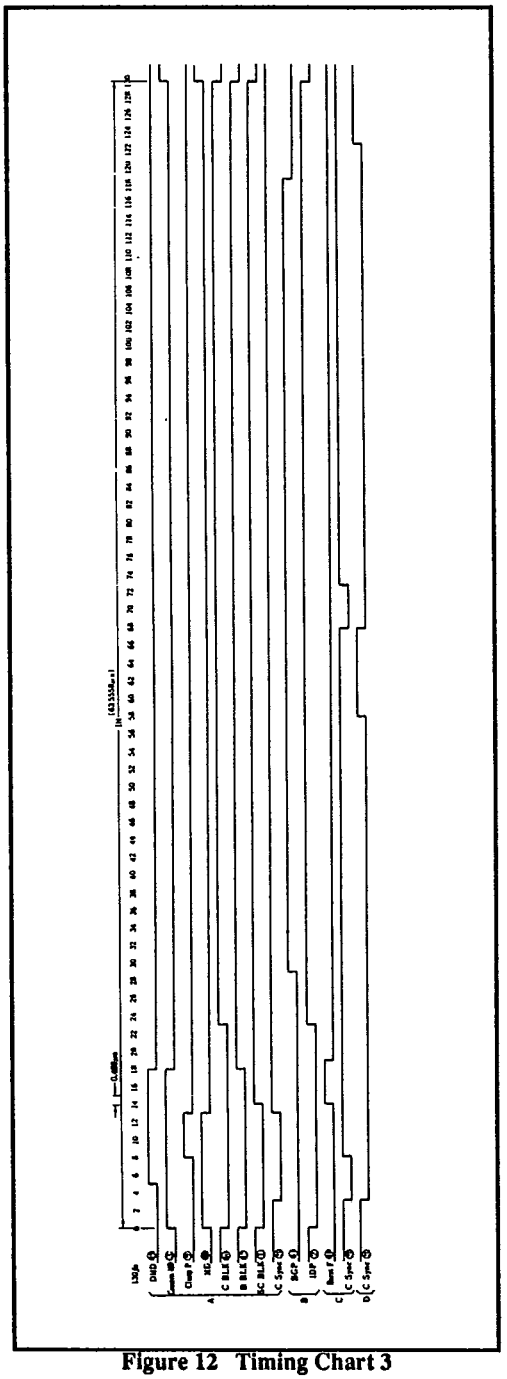

Figure 12 Timing Chart 3

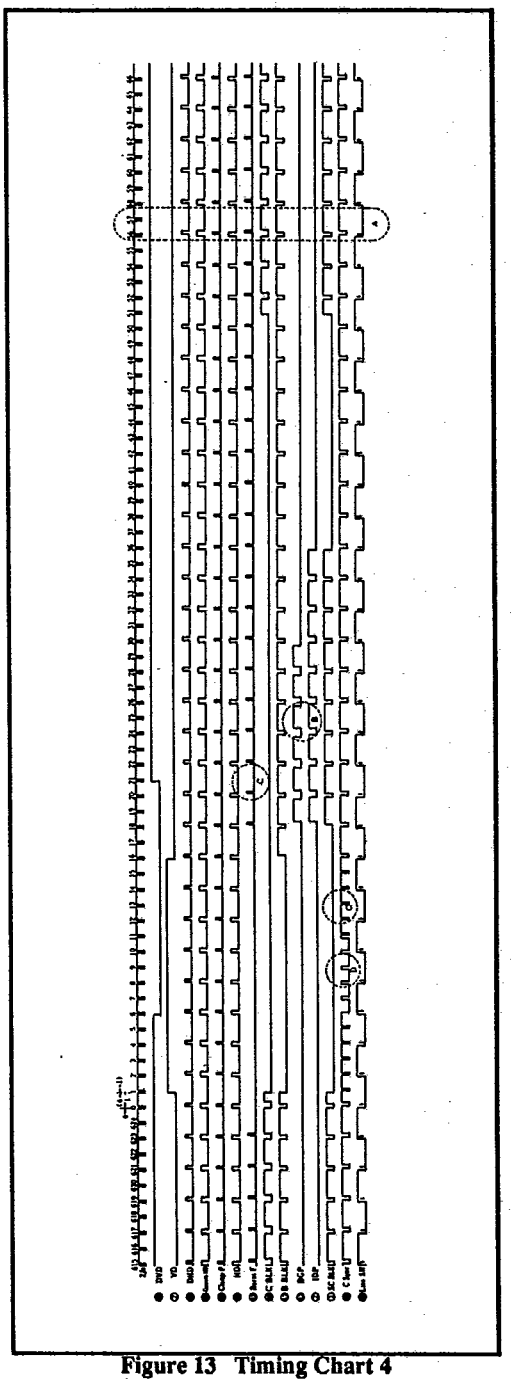

Figure 13 Timing Chart 4

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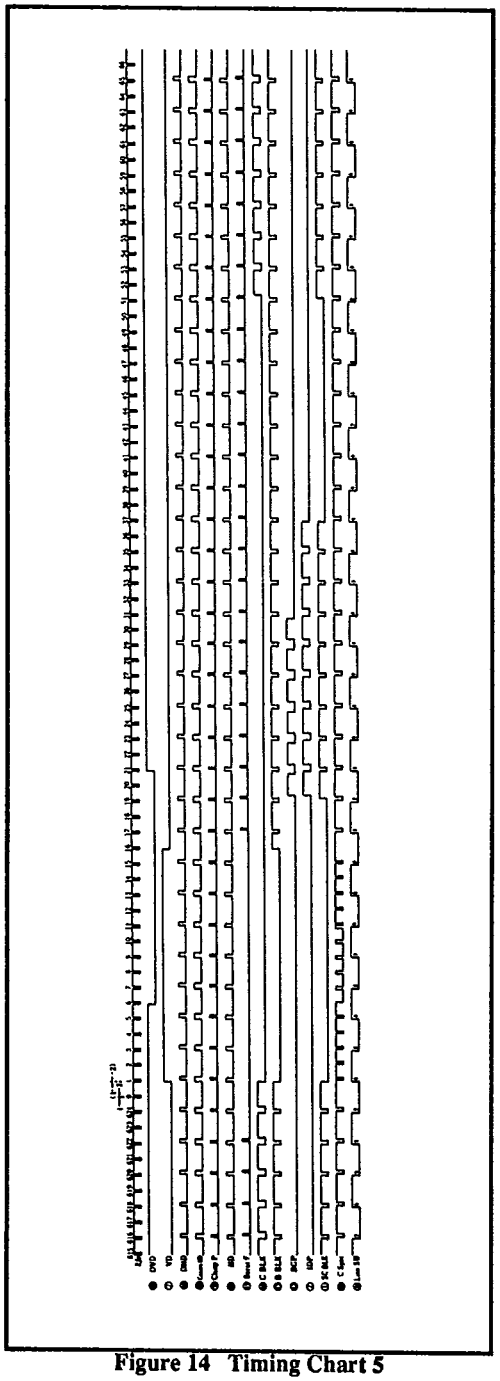

Figure 14 Timing Chart 5

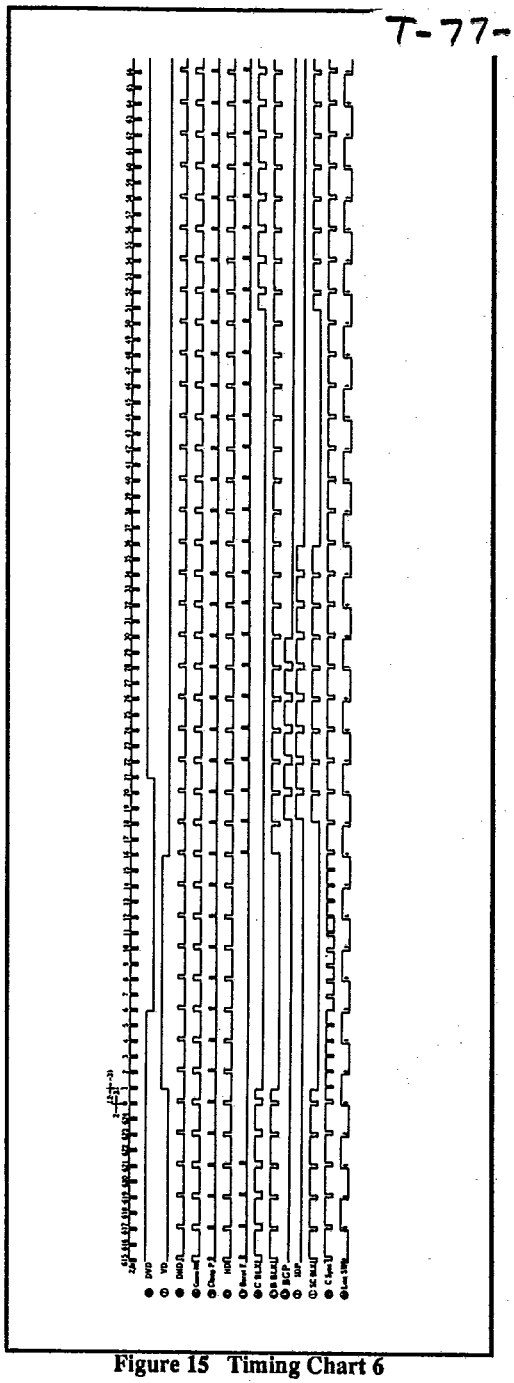

Figure 15 Timing Chart 6

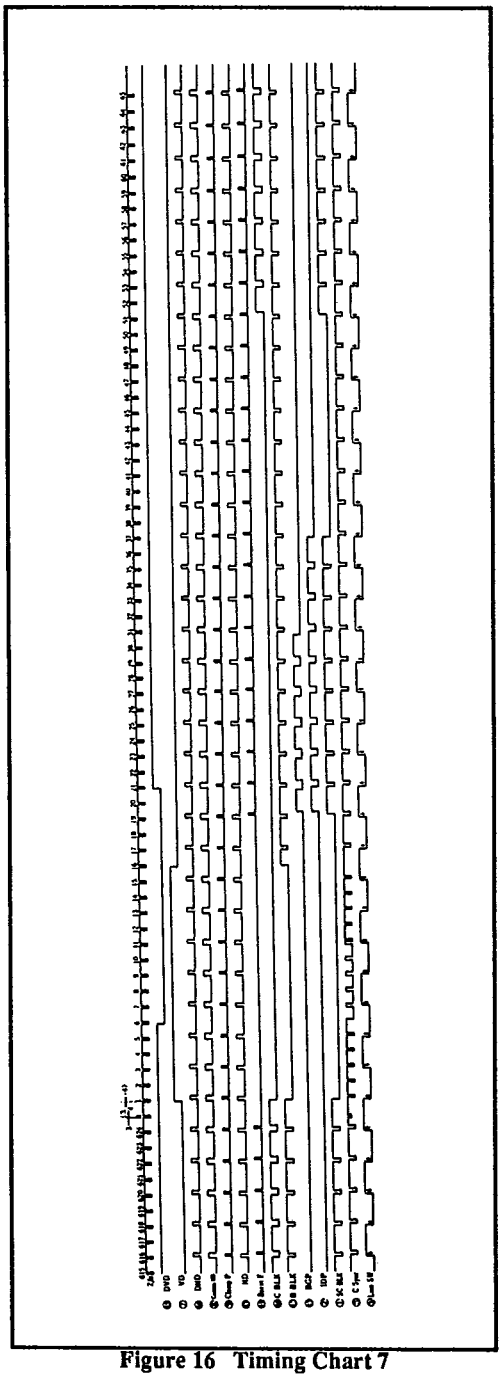

Figure 16 Timing Chart 7

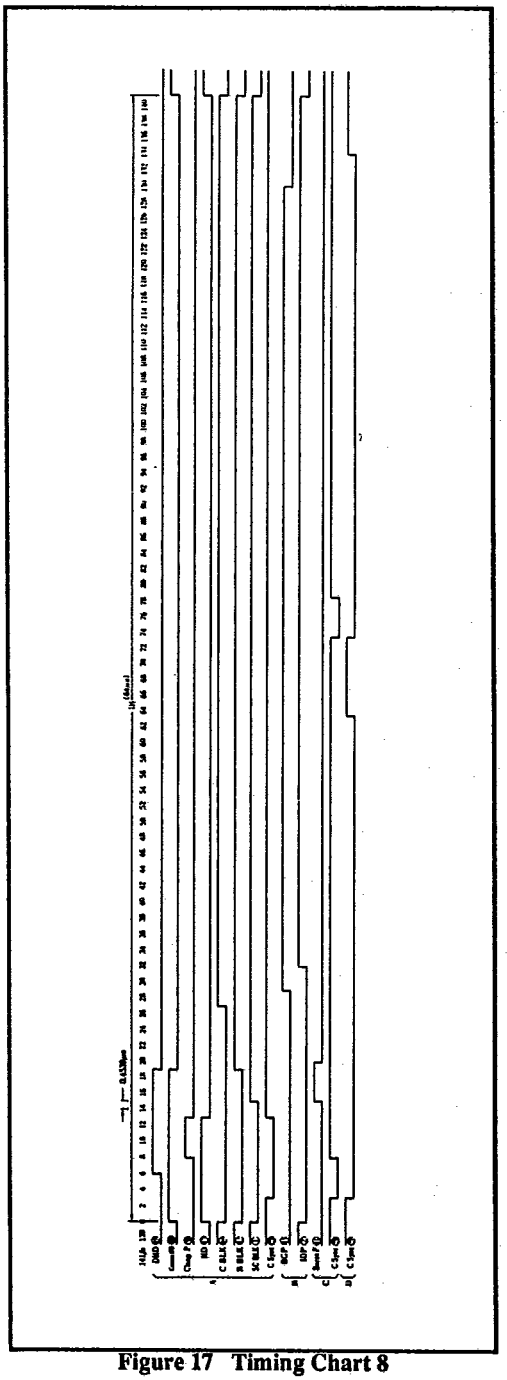

Figure 17 Timing Chart 8