# HD151TS207SS

## Mother Board Clock Generator for Intel P4+ Chipset (Springdale)

REJ03D0006-0100Z
Preliminary
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### Description

The HD151TS207SS is Intel CK409T type high-performance, low-skew, low-jitter, PC motherboard clock generator. It is specifically designed for Intel Pentium®4+ chipset.

### Features

- 3 differential pairs of current mode control CPU clocks
- 1 differential pair of Serial Reference Clock (SRC), selectable 100 MHz/200 MHz
- 6 copies PCI clocks and 3 copies PCIF clocks @3.3V, 33.3 MHz
- 1 copy PCI clock @3.3 V, selectable 33.3 MHz/25 MHz
- 1 copy USB clock @3.3 V, selectable 48 MHz/24 MHz
- 1 copy DOT clock @3.3 V, 48 MHz
- 4 copies of 3V66 clocks @3.3 V, 66.6 MHz
- 1 copy of 3V66/VCH clock @3.3 V, selectable 66.6 MHz/48 MHz
- 2 copies of REF clocks @3.3 V, 14.318 MHz
- Power save and clock stop function
- $I^2C^{TM}$ serial port programming
- Programmable Clock Control (Spread Spectrum Percentage, Clock Output Skew, Slew Rate)
- Watchdog timer and reset output
- 56pin SSOP (300 mils)

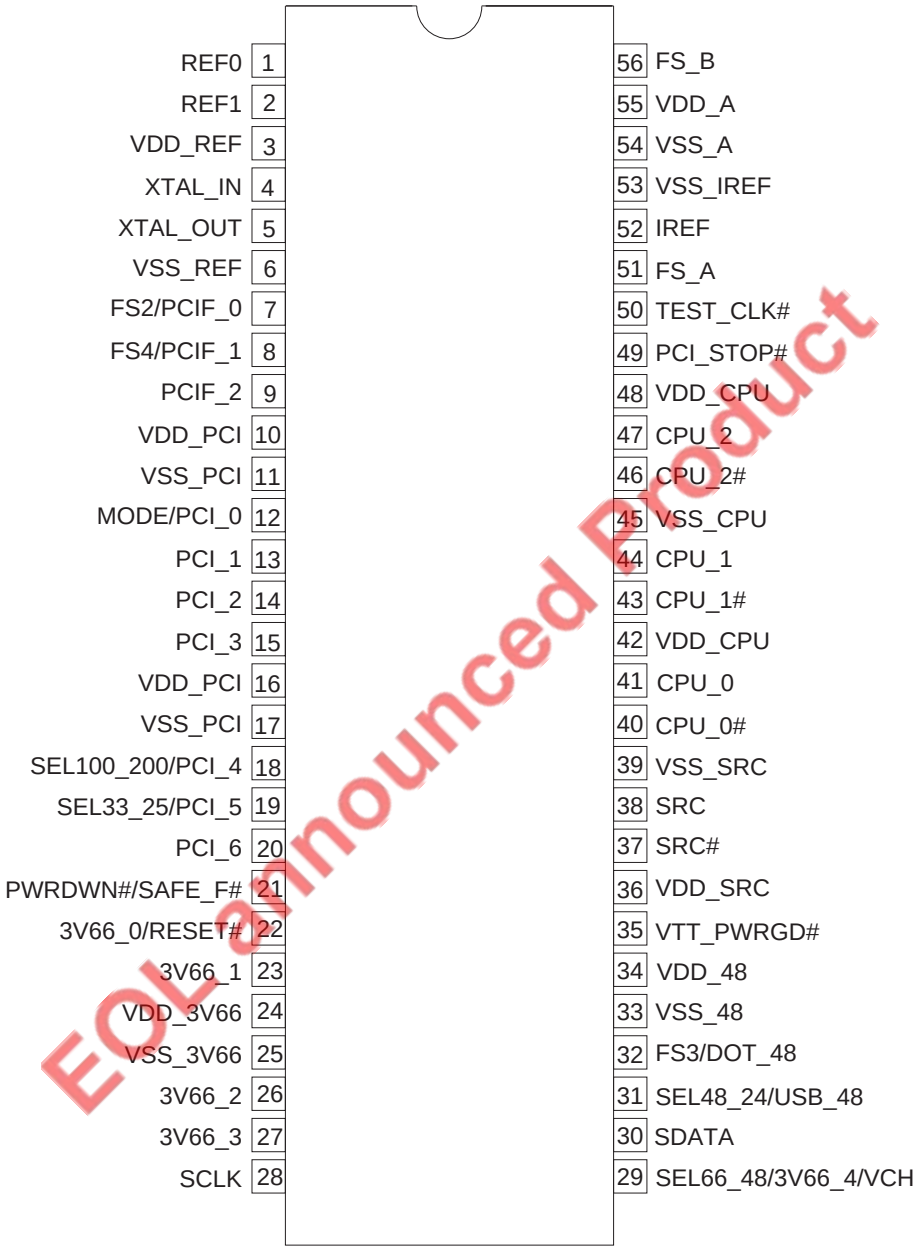
Note: $I^2C$ is a trademark of Philips Corporation.
Pentium is registered trademark of Intel Corporation

## Key Specifications

- Supply Voltages: VDD = 3.3 V±5%
- CPU clock cycle to cycle jitter = |125ps| (SSC Disabled)
- CPU clock group Skew = 100ps
- 3V66 clock group Skew = 250psmax
- PCI clock group Skew = 500psmax

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## Pin Arrangement




(Top view)

PCI_STOP#, PWRDWN# = 150 kΩ Internal Pull-up

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## Pin Descriptions

| Pin name | No. | Type | Description |
|---|---|---|---|
| VSS_A | 54 | Ground | Ground for PLL |
| VSS_CPU | 45 | | Ground for outputs |
| VSS_IREF | 53 | | Ground for current reference |
| VSS_SRC | 39 | | Ground for outputs |
| VSS_3V66 | 25 | | |
| VSS_PCI | 11, 17 | | |
| VSS_REF | 6 | | |
| VSS_48 | 33 | | |
| VDD_A | 55 | Power | 3.3 V Power Supply for PLL |
| VDD_CPU | 42, 48 | | 3.3 V Power Supply for outputs |
| VDD_SRC | 36 | | |
| VDD_3V66 | 24 | | |
| VDD_PCI | 10, 16 | | |
| VDD_REF | 3 | | |
| VDD_48 | 34 | | |
| REF0 | 1 | OUTPUT | 3.3 V 14.318 MHz reference clock. |
| REF1 | 2 | | |
| XTAL_IN | 4 | INPUT | 14.318 MHz XTAL input. |
| XTAL_OUT | 5 | OUTPUT | 14.318 MHz XTAL output.<br>Don't connect when an external clock is applied at XTAL_IN. |
| FS2/PCIF_[0:1] | 7,8 | INPUT/<br>OUTPUT | Frequency select latch input pin.<br>/Free running PCI clock 3.3 V output. |
| PCIF_2 | 9 | OUTPUT | Free running PCI clock 3.3 V output. |
| **MODE/PCI_0 | 12 | INPUT/<br>OUTPUT | Function select latch input pin for pin 22,<br>1 = Reset#, 0 = clock output.<br>/PCI clock 3.3 V output. |
| PCI_[1:3] | 13,14,<br>15 | OUTPUT | PCI clock 3.3 V outputs. |
| **SEL100_200/<br>PCI_4 | 18 | INPUT/<br>OUTPUT | Latched select input for SRC output.<br>1 = 200 MHz, 0 = 100 MHz<br>/PCI clock 3.3 V output. |
| **SEL33_25/PCI_5 | 19 | INPUT/<br>OUTPUT | Latched select input for PCI5 output.<br>1 = 25 MHz, 0 = 33 MHz<br>/PCI clock 3.3 V output. |
| PCI_6 | 20 | OUTPUT | PCI clock 3.3 V outputs. |

Note: (*): Those pins are 150 kΩ internal pulled-UP.
(**): Those pins are 150 kΩ internal pulled-DOWN.

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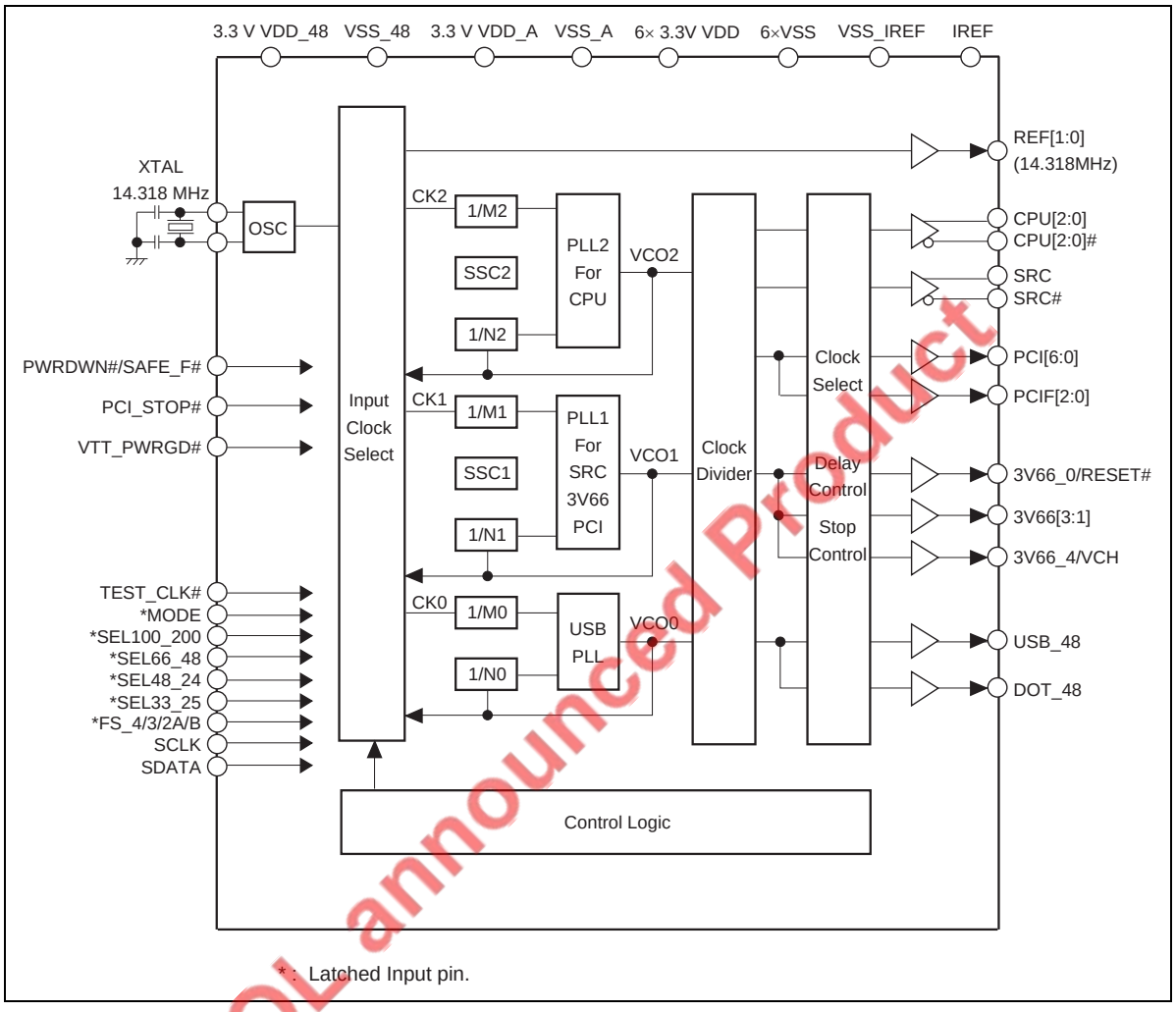
## Pin Descriptions (cont.)

| Pin name | No. | Type | Description |
|---|---|---|---|
| PWRDWN#/ SAFE_F# | 21 | INPUT PULL–UP* | PWRDWN# / SAFE_F# selectable input.<br>Default is PWRDWN# input.<br>Byte15[5] = “1” : SAFE_F# input.<br>PWRDWN# is all clocks stop pin.<br>Asynchronous active “Low” input.<br>When asserted low, all output clocks are disabled.<br>SAFE_F# is active “Low” input.<br>When SAFE_F# is “Low” ,frequency mode is changed to the predefined frequency mode. |
| 3V66_0/RESET# | 22 | OUTPUT | 3V66 / Watchdog RESET# selectable output.<br>Default is 3V66 output.<br>This signal is active low and selected by Mode latch input. |
| 3V66_[1:3] | 23,26, 27 | OUTPUT | 3V66 clock 3.3V outputs. |
| SCLK | 28 | INPUT PULL-UP* | Clock input for $I^2C$ logic. |
| **SEL66_48/ 3V66_4/VCH | 29 | INPUT/ OUTPUT | Latched select input for 3V66/VCH output 1 = 48 MHz, 0 = 66.66 MHz. /3V66 or VCH clock output. |
| SDATA | 30 | IN/OUTPUT PULL-UP* | Data input for $I^2C$ logic. |
| **SEL48_24/ USB_48 | 31 | INPUT/ OUTPUT | Latched select input for 48_24 MHz output<br>1 = 24 MHz, 0 = 48 MHz / 24_48 MHz clock 3.3 V output. |
| FS3/DOT_48 | 32 | INPUT/ OUTPUT | Frequency select latch input pin.<br>/DOT_48 clock 3.3 V output. |
| VTT_PWRGD# | 35 | INPUT PULL-UP* | Qualifying input that latches FS_A and FS_B.<br>When asserted low, FS_A and FS_B are latched. |
| SRC# | 37 | OUTPUT | “Complementary” clock of Differential Serial Reference Clock. |
| SRC | 38 | OUTPUT | “True” clock of Differential Serial Reference Clock. |
| CPU_[0:2]# | 40,43, 46 | OUTPUT | “Complementary” clock of differential CPU clock. |
| CPU_[0:2] | 41,44, 47 | OUTPUT | “True” clock of differential CPU clock. |
| PCI_STOP# | 49 | INPUT PULL–UP* | PCI clocks stop pin. Active “Low” input.<br>When asserted low, PCI[6:0] and SRC clocks are synchronously disabled in low state.<br>Usually this pin does not give to effect PCIF[2:0] clock outputs. |
| TEST_CLK# | 50 | INPUT PULL-UP* | Test clock mode pin. Active “Low” input. |
| FS_[A:B] | 51,52 | INPUT | CPU clocks frequency select latch input. |
| IREF | 52 | INPUT | A precision resistor is attached to this pin which is connected to internal current reference.<br>A resistor is connected between this pin and GNDIREF. |

Note: (*): Those pins are 150 kΩ internal pulled-UP.
(**): Those pins are 150 kΩ internal pulled-DOWN

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## Block Diagram




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## I²C Controlled Register Bit Map

Byte0 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | Reserved | | R | 0 | |
| 6 | Reserved | | R | 0 | |
| 5 | Reserved | | R | 0 | |
| 4 | Reserved | | R | 0 | |
| 3 | PCI_Stop Reflects the current value of the external PCI_STOP# pin | 0 = PCI_STOP# pin is Low<br>1 = PCI_STOP# pin is High | R | X | |
| 2 | Reserved | | R | X | |
| 1 | FS_B Reflects the value of the FS_B pin sampled on power up | 0 = FS_B Low at power up<br>1 = FS_B High at power up | R | X | See Table 1 |
| 0 | FS_A Reflects the value of the FS_A pin sampled on power up | 0 = FS_A Low at power up<br>1 = FS_A High at power up | R | X | |

Table1 Clock Frequency Function Table

| Byte6 Bit5 | FS_A | FS_B | CPU [MHz] | SRC [MHz] | 3V66 [MHz] | PCIF PCI [MHz] | REF0 REF1 [MHz] | USB DOT [MHz] | Note |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 100 | 100/200 | 66 | 33 | 14.318 | 48 | |
| 0 | 0 | 1 | 200 | 100/200 | 66 | 33 | 14.318 | 48 | |
| 0 | 1 | 0 | 133 | 100/200 | 66 | 33 | 14.318 | 48 | |
| 0 | 1 | 1 | 166 | 100/200 | 66 | 33 | 14.318 | 48 | |
| 1 | 0 | 0 | 200 | 100/200 | 66 | 33 | 14.318 | 48 | |
| 1 | 0 | 1 | 400 | 100/200 | 66 | 33 | 14.318 | 48 | |
| 1 | 1 | 0 | 266 | 100/200 | 66 | 33 | 14.318 | 48 | |
| 1 | 1 | 1 | 333 | 100/200 | 66 | 33 | 14.318 | 48 | |

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Table2 Test Clock select table

| TEST_CLK# | CPU [MHz] | SRC [MHz] | 3V66 [MHz] | PCIF PCI [MHz] | REF0 REF1 [MHz] | USB DOT [MHz] | Note |
|---|---|---|---|---|---|---|---|
| 1 | REF/2 | REF/2 | REF/4 | REF/8 | REF | REF/2 | See Note1, Table3 |
| 0 | Hi–Z | Hi–Z | Hi–Z | Hi–Z | Hi–Z | Hi–Z | |

Note: 1. REF is a clock over driven on the XIN during test mode.

## I²C Controlled Register Bit Map (cont.)

Table3 FS_A and FS_B pin Input level

| Logic Level | Min Voltage | Max Voltage |
|---|---|---|
| 0 (Low) | — | 0.35V |
| 1 (High) | 0.70V | — |

Byte1 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | Allow control of SCR with assertion of PCI_STOP# | 0 = Free running<br>1 = Stopped with PCI_STOP# | RW | 0 | See Table5 |
| 6 | SRC Output enable | 0 = Disabled (tristate)<br>1 = Enabled | RW | 1 | |
| 5 | Reserved | | RW | 1 | |
| 4 | Reserved | | RW | 1 | |
| 3 | Reserved | | RW | 1 | |
| 2 | CPU2 Output enable | 0 = Disabled (tristate)<br>1 = Enabled | RW | 1 | |
| 1 | CPU1 Output enable | 0 = Disabled (tristate)<br>1 = Enabled | RW | 1 | |
| 0 | CPU0 Output enable | 0 = Disabled (tristate)<br>1 = Enabled | RW | 1 | |

Byte2 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | SRC_Pwrdwn drive mode | 0 = Driven in power down,<br>1 = Tristate | RW | 0 | See Table5 |
| 6 | SRC_Stop drive mode | 0 = Driven when stopped,<br>1 = Tristate | RW | 0 | |
| 5 | CPU2_Pwrdwn drive mode | 0 = Driven in power down,<br>1 = Tristate | RW | 0 | See Table4 |
| 4 | CPU1_Pwrdwn drive mode | 0 = Driven in power down,<br>1 = Tristate | RW | 0 | |
| 3 | CPU0_Pwrdwn drive mode | 0 = Driven in power down,<br>1 = Tristate | RW | 0 | |
| 2 | Reserved | | RW | 0 | |
| 1 | Reserved | | RW | 0 | |
| 0 | Reserved | | RW | 0 | |

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## I²C Controlled Register Bit Map (cont.)

Table4 CPU Clock Power Management Truth Table

| Signal | Pin PWRDWN# | PWRDWN# Tristate Bit Byte2[5:3] | Non-Stop Outputs Byte1[5:3] = 1 | Note |
|---|---|---|---|---|
| CPU[2:0] | 1 | X | Running | |
| CPU[2:0] | 0 | 0 | Driven @ Iref x2 | See Note1 |
| CPU[2:0] | 0 | 1 | Tristate | |

Note: 1. Iref = VDD/(3Rr) = 3.3/(3x475) = 2.32 mA,
Iref x2 = 4.6 mA (Voh @Z: 0.23 V @50 Ω)

Table5 SRC Clock Power Management Truth Table

| Signal | Pin PWRDWN# | Pin PCI_STOP# | PCI_STOP# Tristate Bit Byte2[6] | PWRDWN# Tristate Bit Byte2[7] | Non-Stop Outputs Byte1[7] = 1 | Stoppable Outputs Byte1[7] = 0 | Note |
|---|---|---|---|---|---|---|---|
| SRC | 1 | 1 | X | X | Running | Running | |
| SRC | 1 | 0 | 0 | X | Running | Driven @ Iref x6 | See Note1 |
| SRC | 1 | 0 | 1 | X | Running | Tristate | |
| SRC | 0 | X | X | 0 | Driven @ Iref x2 | Driven @ Iref x2 | See Note1 |
| SRC | 0 | X | X | 1 | Tristate | Tristate | |

Note: 1. Iref = VDD/(3Rr) = 3.3/(3x475) = 2.32 mA
Iref x6 = 13.9 mA (Voh @Z: 0.7 V @50 Ω)
Iref x2 = 4.6 mA (Voh @Z: 0.23 V @50 Ω)

Byte3 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | PCI_Stop control | 0 = Enabled, all stoppable PCI and SRC clocks are stopped.<br>1 = Disabled | RW | 1 | |
| 6 | PCI_6 Output enable | 0 = Disabled, 1 = Enabled | RW | 1 | |
| 5 | PCI_5 Output enable | 0 = Disabled, 1 = Enabled | RW | 1 | |
| 4 | PCI_4 Output enable | 0 = Disabled, 1 = Enabled | RW | 1 | |
| 3 | PCI_3 Output enable | 0 = Disabled, 1 = Enabled | RW | 1 | |
| 2 | PCI_2 Output enable | 0 = Disabled, 1 = Enabled | RW | 1 | |
| 1 | PCI_1 Output enable | 0 = Disabled, 1 = Enabled | RW | 1 | |
| 0 | PCI_0 Output enable | 0 = Disabled, 1 = Enabled | RW | 1 | |

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## I²C Controlled Register Bit Map (cont.)

Byte4 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | USB_48 2x output drive | 0 = 2x Drive strength,<br>1 = Normal | RW | 0 | |
| 6 | USB_48MHz Output Enable | 0 = Disabled,<br>1 = Enabled | RW | 1 | |
| 5 | Allow control of PCIF_2 with assertion of PCI_STOP# | 0 = Free Running<br>1 = Stopped with PCI_STOP# | RW | 0 | |
| 4 | Allow control of PCIF_1 with assertion of PCI_STOP# | 0 = Free Running<br>1 = Stopped with PCI_STOP# | RW | 0 | |
| 3 | Allow control of PCIF_0 with assertion of PCI_STOP# | 0 = Free Running<br>1 = Stopped with PCI_STOP# | RW | 0 | |
| 2 | PCIF_2 Output enable | 0 = Disabled, 1 = Enabled | RW | 1 | |
| 1 | PCIF_1 Output enable | 0 = Disabled, 1 = Enabled | RW | 1 | |
| 0 | PCIF_0 Output enable | 0 = Disabled, 1 = Enabled | RW | 1 | |

Byte5 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | DOT_48MHz Output Enable | 0 = Disabled, 1 = Enabled | RW | 1 | |
| 6 | Reserved | | RW | 1 | |
| 5 | VCH Select 66MHz / 48MHz | 0 = 3V66 mode<br>1 = VCH (48 MHz) mode | RW | 0 | |
| 4 | 3V66_4/VCH Output Enable | 0 = Disabled (tristate),<br>1 = Enabled | RW | 1 | |
| 3 | 3V66_3 Output Enable | 0 = Disabled, 1 = Enabled | RW | 1 | |
| 2 | 3V66_2 Output Enable | 0 = Disabled, 1 = Enabled | RW | 1 | |
| 1 | 3V66_1 Output Enable | 0 = Disabled, 1 = Enabled | RW | 1 | |
| 0 | 3V66_0 Output Enable | 0 = Disabled, 1 = Enabled | RW | 1 | |

Byte6 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | Test Clock Mode | 0 = Disabled, 1 = Enabled | RW | 0 | |
| 6 | Reserved | | RW | 0 | |
| 5 | FS_A & FS_B Operation | 0 = Normal, 1 = Test mode | RW | 0 | |
| 4 | SRC Frequency Select | 0 = 100MHz, 1 = 200 MHz | RW | 0 | |
| 3 | Reserved | | RW | 0 | |
| 2 | Spread Spectrum Mode | 0 = Spread OFF<br>1 = Spread ON | RW | 0 | See B9[7:6] |
| 1 | REF1 Output Enable | 0 = Disabled, 1 = Enabled | RW | 1 | |
| 0 | REF0 Output Enable | 0 = Disabled, 1 = Enabled | RW | 1 | |

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## I²C Controlled Register Bit Map (cont.)

Byte7 Vendor Identification Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | Revision Code Bit3 | Vendor Specific | R | 0 | |
| 6 | Revision Code Bit2 | Vendor Specific | R | 0 | |
| 5 | Revision Code Bit1 | Vendor Specific | R | 0 | |
| 4 | Revision Code Bit0 | Vendor Specific | R | 1 | |
| 3 | Vendor ID Bit3 | Vendor Specific | R | 1 | |
| 2 | Vendor ID Bit2 | Vendor Specific | R | 1 | |
| 1 | Vendor ID Bit1 | Vendor Specific | R | 1 | |
| 0 | Vendor ID Bit0 | Vendor Specific | R | 1 | |

Byte8 Read Back Byte Count Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | Read back byte count Bit7 | Writing to this register will configure byte Count and how many bytes will be read back.<br>Default is 1Ehex = 30 bytes. | RW | 0 | |
| 6 | Read back byte count Bit6 | | RW | 0 | |
| 5 | Read back byte count Bit5 | | RW | 0 | |
| 4 | Read back byte count Bit4 | | RW | 1 | |
| 3 | Read back byte count Bit3 | | RW | 1 | |
| 2 | Read back byte count Bit2 | | RW | 1 | |
| 1 | Read back byte count Bit1 | | RW | 1 | |
| 0 | Read back byte count Bit0 | | RW | 0 | |

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## I²C Controlled Register Bit Map (cont.)

Byte9 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | SSC2 Enable Bit | B6[2] = 0 or B9[7] = 1 : SSC2 =OFF<br>B6[2] = 1 & B9[7] = 0 : SSC2 = ON | RW | 0 | |
| 6 | SSC1 Enable Bit | B6[2] = 0 or B9[6] = 1 : SSC1 = OFF<br>B6[2] = 1 & B9[6] = 0 : SSC1 = ON | RW | 0 | |
| 5 | Clock Frequency Control Bit4 | Latched input PCIF_1 at Power ON | RW | X | See Table 6 |
| 4 | Clock Frequency Control Bit3 | Latched input DOT48 at Power ON | RW | X | |
| 3 | Clock Frequency Control Bit2 | Latched input PCIF_0 at Power ON | RW | X | |
| 2 | Clock Frequency Control Bit1 | Latched input FS_A at Power ON | RW | X | |
| 1 | Clock Frequency Control Bit0 | Latched input FS_B at Power ON | RW | X | |
| 0 | Frequency Select Mode Bit | 0 = Freq. is selected by latched input FS_A and FS_B<br>1 = Freq. is selected by I²C B9[5:1] | RW | 0 | |

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## I²C Controlled Register Bit Map (cont.)

Table6 Clock Frequency Function Table

| No. | FS_4 | FS_3 | FS_2 | FS_A | FS_B | CPU [MHz] | SRC [MHz] | 3V66 [MHz] | PCI [MHz] |
|---|---|---|---|---|---|---|---|---|---|
| | B9[5] | B9[4] | B9[3] | B9[2] | B9[1] | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 100.02 | 100.02 | 66.68 | 33.34 |
| 1 | 0 | 0 | 0 | 0 | 1 | 200.03 | 100.02 | 66.68 | 33.34 |
| 2 | 0 | 0 | 0 | 1 | 0 | 133.36 | 100.02 | 66.68 | 33.34 |
| 3 | 0 | 0 | 0 | 1 | 1 | 166.69 | 100.02 | 66.68 | 33.34 |
| 4 | 0 | 0 | 1 | 0 | 0 | 200.03 | 100.02 | 66.68 | 33.34 |
| 5 | 0 | 0 | 1 | 0 | 1 | 400.07 | 100.02 | 66.68 | 33.34 |
| 6 | 0 | 0 | 1 | 1 | 0 | 266.71 | 100.02 | 66.68 | 33.34 |
| 7 | 0 | 0 | 1 | 1 | 1 | 333.39 | 100.02 | 66.68 | 33.34 |
| 8 | 0 | 1 | 0 | 0 | 0 | 138.69 | 100.02 | 66.68 | 33.34 |
| 9 | 0 | 1 | 0 | 0 | 1 | 142.25 | 100.02 | 66.68 | 33.34 |
| 10 | 0 | 1 | 0 | 1 | 0 | 145.80 | 100.02 | 66.68 | 33.34 |
| 11 | 0 | 1 | 0 | 1 | 1 | 149.36 | 100.02 | 66.68 | 33.34 |
| 12 | 0 | 1 | 1 | 0 | 0 | 152.91 | 100.02 | 66.68 | 33.34 |
| 13 | 0 | 1 | 1 | 0 | 1 | 156.47 | 100.02 | 66.68 | 33.34 |
| 14 | 0 | 1 | 1 | 1 | 0 | 160.03 | 100.02 | 66.68 | 33.34 |
| 15 | 0 | 1 | 1 | 1 | 1 | 163.58 | 100.02 | 66.68 | 33.34 |
| 16 | 1 | 0 | 0 | 0 | 0 | 167.14 | 100.02 | 66.68 | 33.34 |
| 17 | 1 | 0 | 0 | 0 | 1 | 170.70 | 100.02 | 66.68 | 33.34 |
| 18 | 1 | 0 | 0 | 1 | 0 | 174.25 | 100.02 | 66.68 | 33.34 |
| 19 | 1 | 0 | 0 | 1 | 1 | 177.81 | 100.02 | 66.68 | 33.34 |
| 20 | 1 | 0 | 1 | 0 | 0 | 181.36 | 100.02 | 66.68 | 33.34 |
| 21 | 1 | 0 | 1 | 0 | 1 | 184.92 | 100.02 | 66.68 | 33.34 |
| 22 | 1 | 0 | 1 | 1 | 0 | 186.70 | 100.02 | 66.68 | 33.34 |
| 23 | 1 | 0 | 1 | 1 | 1 | 189.36 | 100.02 | 66.68 | 33.34 |
| 24 | 1 | 1 | 0 | 0 | 0 | 192.03 | 100.02 | 66.68 | 33.34 |
| 25 | 1 | 1 | 0 | 0 | 1 | 194.70 | 100.02 | 66.68 | 33.34 |
| 26 | 1 | 1 | 0 | 1 | 0 | 197.37 | 100.02 | 66.68 | 33.34 |
| 27 | 1 | 1 | 0 | 1 | 1 | 200.03 | 100.02 | 66.68 | 33.34 |
| 28 | 1 | 1 | 1 | 0 | 0 | 202.70 | 100.02 | 66.68 | 33.34 |
| 29 | 1 | 1 | 1 | 0 | 1 | 205.37 | 100.02 | 66.68 | 33.34 |
| 30 | 1 | 1 | 1 | 1 | 0 | 208.03 | 100.02 | 66.68 | 33.34 |
| 31 | 1 | 1 | 1 | 1 | 1 | 210.70 | 100.02 | 66.68 | 33.34 |

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## I²C Controlled Register Bit Map (cont.)

Byte10 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | SSC Spread Select Bit[2:0] | Bit[2:0] =<br>000 = –0.500%, 100 = ±0.250%<br>001 = –0.750%, 101 = ±0.375%<br>010 = –1.000%, 110 = ±0.500%<br>011 = –1.500%, 111 = ±0.750% | RW | 0 | |
| 6 | | | RW | 0 | |
| 5 | | | RW | 0 | |
| 4 | Backup of latch Input FS_4 at Power ON | When SAFE_F# is Enable (B15[5]=1) PWRDWN#/SAFE_F# pin to “Low”, and if B23[1]=0, frequency selection is changed to these setting and PWRDWN#/SAFE_F# pin to “High”, frequency selection is changed back to the last mode. | R | X | |
| 3 | Backup of latch Input FS_3 at Power ON | | R | X | |
| 2 | Backup of latch Input FS_2 at Power ON | | R | X | |
| 1 | Backup of latch Input FS_A at Power ON | | R | X | |
| 0 | Backup of latch Input FS_B at Power ON | | R | X | |

Byte11 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | PCI_STOP# Enable Control Bit | 0 = Enable , 1 = Disable | RW | 0 | |
| 6 | CPU_STOP# Enable Control Bit | 0 = Enable , 1 = Disable | RW | 0 | |
| 5 | PWRDWN# Enable Control Bit | 0 = Enable , 1 = Disable | RW | 0 | |
| 4 | Backup of B9[5] written by I²C | When SAFE_F# is Enable (B15[5]=1) PWRDWN#/SAFE_F# pin to “Low”, and if B23[1]=1, frequency selection is changed to these setting and PWRDWN#/SAFE_F# pin to “High”, frequency selection is changed back to the last mode. | R | X | |
| 3 | Backup of B9[4] written by I²C | | R | X | |
| 2 | Backup of B9[3] written by I²C | | R | X | |
| 1 | Backup of B9[2] written by I²C | | R | X | |
| 0 | Backup of B9[1] written by I²C | | R | X | |

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## I²C Controlled Register Bit Map (cont.)

Byte12 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | Reserved | | R/W | 0 | |
| 6 | Reserved | | R/W | 0 | |
| 5 | Reserved | | R/W | 0 | |
| 4 | Reserved | | R/W | 0 | |
| 3 | Reserved | | R/W | 0 | |
| 2 | PLL1 Output (VCO1) Frequency Control Bit<br>(M1/N1 Divider Control Bit)<br>PLL1 : for SRC/3V66/PCI_PLL | 0 = Normal mode<br>PLL1 M1[6:0] and N1[9:0] are changed on Table 5 selection decided by FS4/3/2/A/B or B9[5:1]<br>1 = Over or Down clocking mode<br>PLL1 M1[6:0] and N1[9:0] are changed by B12[1:0], B13[7:0] and B14[6:0].<br>B12[1:0], B13[7:0] and B14[6:0] are able to be changed at B12[2] = 1. | R/W | 0 | See. Note 1 |
| 1 | PLL1 N1 Divider Control Bit9 | N1[9] | R/W | 0 | |
| 0 | PLL1 N1 Divider Control Bit8 | N1[8] | R/W | 0 | |

Note: 1. B12[1:0], B13[7:0] and B14[6:0] must be written together (at writing B14) in every case.

Byte13 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | PLL1 N1 Divider Control Bit7 | N1[7] | R/W | 0 | See Note 1 |
| 6 | PLL1 N1 Divider Control Bit6 | N1[6] | R/W | 1 | |
| 5 | PLL1 N1 Divider Control Bit5 | N1[5] | R/W | 0 | |
| 4 | PLL1 N1 Divider Control Bit4 | N1[4] | R/W | 0 | |
| 3 | PLL1 N1 Divider Control Bit3 | N1[3] | R/W | 1 | |
| 2 | PLL1 N1 Divider Control Bit2 | N1[2] | R/W | 0 | |
| 1 | PLL1 N1 Divider Control Bit1 | N1[1] | R/W | 1 | |
| 0 | PLL1 N1 Divider Control Bit0 | N1[0] | R/W | 1 | |

Note: 1. B12[1:0], B13[7:0] and B14[6:0] must be written together (at writing B14) in every case.

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## I²C Controlled Register Bit Map (cont.)

Byte14 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | Reserved | | R/W | 0 | See Note 1 |
| 6 | PLL1 M1 Divider Control Bit6 | M1[6] | R/W | 0 | |
| 5 | PLL1 M1 Divider Control Bit5 | M1[5] | R/W | 0 | |
| 4 | PLL1 M1 Divider Control Bit4 | M1[4] | R/W | 1 | |
| 3 | PLL1 M1 Divider Control Bit3 | M1[3] | R/W | 0 | |
| 2 | PLL1 M1 Divider Control Bit2 | M1[2] | R/W | 0 | |
| 1 | PLL1 M1 Divider Control Bit1 | M1[1] | R/W | 1 | |
| 0 | PLL1 M1 Divider Control Bit0 | M1[0] | R/W | 0 | |

Note: 1. B12[1:0], B13[7:0] and B14[6:0] must be written together (at writing B14) in every case.

Byte15 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | PCI_5 Output Frequency Select Bit | 0 = 33.3 MHz, 1 = 25 MHz | R/W | 0 | |
| 6 | USB_48 Output Frequency Select Bit | 0 = 48MHz, 1 = 24 MHz | R/W | 0 | |
| 5 | SAFE_F# Input mode select Bit | 0 = PWRDWN# input mode<br>1 = SAFE_F# input mode<br>Default is PWRDWN# input.<br>SAFE_F# is active “Low” input.<br>When SAFE_F# is “Low”, frequency mode is changed to the predefined frequency mode.<br>Predefined frequency mode is selected by B23[1]. | R/W | 0 | |
| 4 | Clock Divider Control Bit | 0 = Normal mode<br>Clock dividers are changed by Table 5 selection decided B9[5:1]<br>1 = Over or Down clocking mode<br>Clock dividers are changed by B15[3:0] and B16[7:0].<br>B15[3:0] and B16[7:0] are able to be changed at B15[4] = 1. | R/W | 0 | |
| 3 | CPU Divider Control Bit3 | 0001 = 1/1, 0111 = 1/7<br>0010 = 1/2, 1000 = 1/8<br>0011 = 1/3, 1001 = 1/9<br>0100 = 1/4, 1010 = 1/10<br>0101 = 1/5, 1011 = 1/11<br>0110 = 1/6, | R/W | X | |
| 2 | CPU Divider Control Bit2 | | R/W | X | |
| 1 | CPU Divider Control Bit1 | | R/W | X | |
| 0 | CPU Divider Control Bit0 | | R/W | X | |

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## I²C Controlled Register Bit Map (cont.)

Byte16 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | 3V66 / PCI / PCIF Divider Control Bit3 | 3V66 divider ratio =<br>0010 = 1/2, 0111 = 1/7<br>0011 = 1/3, 1000 = 1/8<br>0100 = 1/4, 1001 = 1/9<br>0101 = 1/5, 1010 = 1/10<br>0110 = 1/6, 1011 = 1/11 | R/W | X | |
| 6 | 3V66 / PCI / PCIF Divider Control Bit2 | | R/W | X | |
| 5 | 3V66 / PCI / PCIF Divider Control Bit1 | PCI / PCIF divider ratio = 3v66 x 1/2 | R/W | X | |
| 4 | 3V66 / PCI / PCIF Divider Control Bit0 | | R/W | X | |
| 3 | SRC Divider Control Bit3 | 0001 = 1/1, 0111 = 1/7<br>0010 = 1/2, 1000 = 1/8<br>0011 = 1/3, 1001 = 1/9<br>0100 = 1/4, 1010 = 1/10<br>0101 = 1/5, 1011 = 1/11<br>0110 = 1/6 | R/W | X | |
| 2 | SRC Divider Control Bit2 | | R/W | X | |
| 1 | SRC Divider Control Bit1 | | R/W | X | |
| 0 | SRC Divider Control Bit0 | | R/W | X | |

Byte17 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | Reserved | | R/W | 0 | |
| 6 | Reserved | | R/W | 0 | |
| 5 | Reserved | | R/W | 0 | |
| 4 | PLL2 Output (VCO2) Frequency Control Bit<br>(M2 / N2 Divider Control Bit)<br>PLL2 : for CPU | 0 = Normal mode<br>VCO2 frequency is changed on Table 5 selection decided by FS4/3/2/A/B or B9[5:1].<br>1 = Over or Down clocking mode<br>VCO2 frequency is changed by B17[3:0] and B18[7:0] with decimal.<br>B17[3:0] and B18[7:0] are able to be changed at B17[4] = 1. | R/W | 0 | See Note 1 |
| 3 | VCO2 Frequency Control Bit11 | These bits are 100MHz digit of VCO2 frequency.<br>0000 = 0, 0001 = 1 …. 1001 = 9 | R/W | 0 | |
| 2 | VCO2 Frequency Control Bit10 | | R/W | 1 | |
| 1 | VCO2 Frequency Control Bit9 | | R/W | 0 | |
| 0 | VCO2 Frequency Control Bit8 | | R/W | 0 | |

Note: 1. B17[3:0] and B18[7:0] must be written together (at writing B18) in every case.

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## I²C Controlled Register Bit Map (cont.)

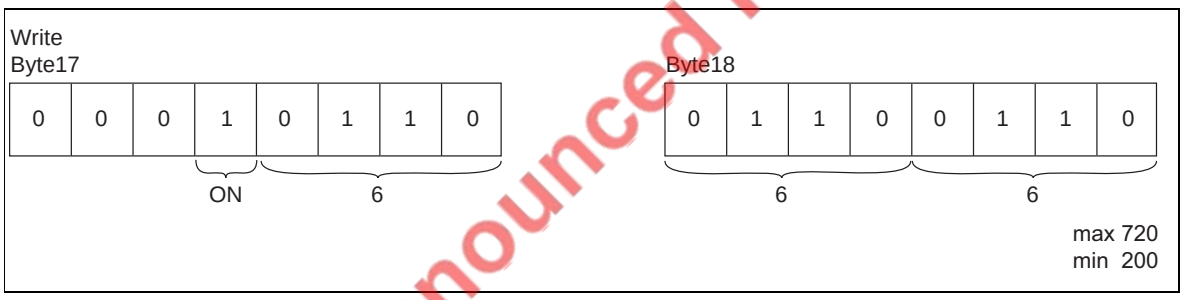
Byte18 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | VCO2 Frequency Control Bit7 | These bits are 10MHz digit of VCO2 frequency. 0000 = 0, 0001 = 1 …. 1001 = 9 | R/W | 0 | See Note 1 |
| 6 | VCO2 Frequency Control Bit6 | | R/W | 0 | |
| 5 | VCO2 Frequency Control Bit5 | | R/W | 0 | |
| 4 | VCO2 Frequency Control Bit4 | | R/W | 0 | |
| 3 | VCO2 Frequency Control Bit3 | These bits are 1MHz digit of VCO2 frequency. 0000 = 0, 0001 = 1 …. 1001 = 9 | R/W | 0 | |
| 2 | VCO2 Frequency Control Bit2 | | R/W | 0 | |
| 1 | VCO2 Frequency Control Bit1 | | R/W | 0 | |
| 0 | VCO2 Frequency Control Bit0 | | R/W | 0 | |

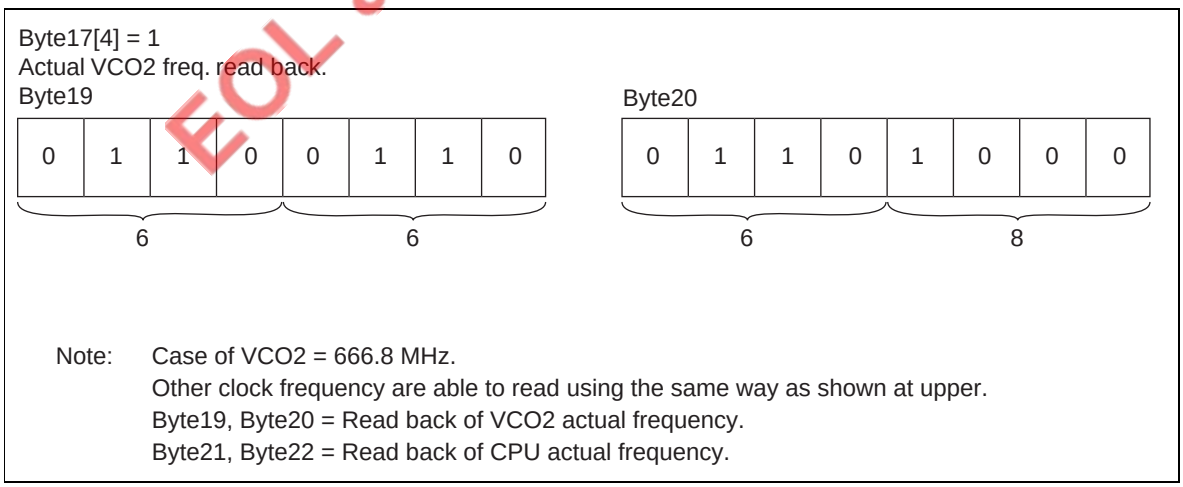
Note: 1. B17[3:0] and B18[7:0] must be written together (at writing B18) in every case.

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How to set VCO2 frequency to 666 MHz.




How to read actual frequency of VCO2 and CPU clock




Note: Case of VCO2 = 666.8 MHz.
Other clock frequency are able to read using the same way as shown at upper.
Byte19, Byte20 = Read back of VCO2 actual frequency.
Byte21, Byte22 = Read back of CPU actual frequency.

## I²C Controlled Register Bit Map (cont.)

Byte19 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | VCO2 Frequency Read Bit15 | Calculation result of VCO2 frequency.<br>100 MHz digit<br>0000 = 0, 0001 = 1 …. 1001 = 9 | R | 0 | |
| 6 | VCO2 Frequency Read Bit14 | | R | 0 | |
| 5 | VCO2 Frequency Read Bit13 | | R | 0 | |
| 4 | VCO2 Frequency Read Bit12 | | R | 0 | |
| 3 | VCO2 Frequency Read Bit11 | Calculation result of VCO2 frequency.<br>10 MHz digit<br>0000 = 0, 0001 = 1 …. 1001 = 9 | R | 0 | |
| 2 | VCO2 Frequency Read Bit10 | | R | 0 | |
| 1 | VCO2 Frequency Read Bit9 | | R | 0 | |
| 0 | VCO2 Frequency Read Bit8 | | R | 0 | |

Byte20 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | VCO2 Frequency Read Bit7 | Calculation result of VCO2 frequency.<br>1 MHz digit<br>0000 = 0, 0001 = 1 …. 1001 = 9 | R | 0 | |
| 6 | VCO2 Frequency Read Bit6 | | R | 0 | |
| 5 | VCO2 Frequency Read Bit5 | | R | 0 | |
| 4 | VCO2 Frequency Read Bit4 | | R | 0 | |
| 3 | VCO2 Frequency Read Bit3 | Calculation result of VCO2 frequency.<br>0.1 MHz digit<br>0000 = 0, 0001 = 1 …. 1001 = 9 | R | 0 | |
| 2 | VCO2 Frequency Read Bit2 | | R | 0 | |
| 1 | VCO2 Frequency Read Bit1 | | R | 0 | |
| 0 | VCO2 Frequency Read Bit0 | | R | 0 | |

Byte21 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | CPU Frequency Read Bit15 | Calculation result of CPU frequency.<br>100 MHz digit<br>0000 = 0, 0001 = 1 …. 1001 = 9 | R | 0 | |
| 6 | CPU Frequency Read Bit14 | | R | 0 | |
| 5 | CPU Frequency Read Bit13 | | R | 0 | |
| 4 | CPU Frequency Read Bit12 | | R | 0 | |
| 3 | CPU Frequency Read Bit11 | Calculation result of CPU frequency.<br>10 MHz digit<br>0000 = 0, 0001 = 1 …. 1001 = 9 | R | 0 | |
| 2 | CPU Frequency Read Bit10 | | R | 0 | |
| 1 | CPU Frequency Read Bit9 | | R | 0 | |
| 0 | CPU Frequency Read Bit8 | | R | 0 | |

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## I²C Controlled Register Bit Map (cont.)

Byte22 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | CPU Frequency Read Bit7 | Calculation result of CPU frequency.<br>1 MHz digit<br>0000 = 0, 0001 = 1 …. 1001 = 9 | R | 0 | |
| 6 | CPU Frequency Read Bit6 | | R | 0 | |
| 5 | CPU Frequency Read Bit5 | | R | 0 | |
| 4 | CPU Frequency Read Bit4 | | R | 0 | |
| 3 | CPU Frequency Read Bit3 | Calculation result of CPU frequency.<br>0.1 MHz digit<br>0000 = 0, 0001 = 1 …. 1001 = 9 | R | 0 | |
| 2 | CPU Frequency Read Bit2 | | R | 0 | |
| 1 | CPU Frequency Read Bit1 | | R | 0 | |
| 0 | CPU Frequency Read Bit0 | | R | 0 | |

Byte23 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | Watchdog Enable Control Bit | 0 = Disable , Pin22 = 3V66_0 output<br>1 = Enable , Pin22 = RESET# output | R/W | 0 | |
| 6 | RESET# Reverse Control Bit | 0 = Normal , 1 = Reverse | R/W | 0 | |
| 5 | Watchdog Timer Count Bit3 | These 4 bits corresponds to how many watchdog timer will wait from becoming "Alarm mode" (B23[0] = 1) to outputting RESET# pin to "Low".<br>Default is 586ms x8 = 4.7s at Power ON | R/W | 1 | |
| 4 | Watchdog Timer Count Bit2 | | R/W | 0 | |
| 3 | Watchdog Timer Count Bit1 | | R/W | 0 | |
| 2 | Watchdog Timer Count Bit0 | | R/W | 0 | |
| 1 | Backup Frequency Select Bit | 0 = B10[4:0] , 1 = B11[4:0]<br>When SAFE_F# is "Low" , frequency mode is changed to the predefined frequency mode decided by B10[4:0] or B11[4:0]. | R/W | 0 | |
| 0 | Watchdog Status Bit | 0 = Normal mode, 1 = Alarm mode | R/W | 0 | |

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## I²C Controlled Register Bit Map (cont.)

Byte24 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | Reserved | | R/W | 0 | |
| 6 | PCI_STOP# Stop PCI_6 Control Bit | 0 = Stoppable, 1 = Free running | R/W | 0 | |
| 5 | PCI_STOP# Stop PCI_5 Control Bit | 0 = Stoppable, 1 = Free running | R/W | 0 | |
| 4 | PCI_STOP# Stop PCI_4 Control Bit | 0 = Stoppable, 1 = Free running | R/W | 0 | |
| 3 | PCI_STOP# Stop PCI_3 Control Bit | 0 = Stoppable, 1 = Free running | R/W | 0 | |
| 2 | PCI_STOP# Stop PCI_2 Control Bit | 0 = Stoppable, 1 = Free running | R/W | 0 | |
| 1 | PCI_STOP# Stop PCI_1 Control Bit | 0 = Stoppable, 1 = Free running | R/W | 0 | |
| 0 | PCI_STOP# Stop PCI_0 Control Bit | 0 = Stoppable, 1 = Free running | R/W | 0 | |

Byte25 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | CPU Clock Skew1 Control Bit3 | Delay Ahead<br>1000 = +0.00ns, 0111 = –0.20ns<br>1001 = +0.20ns, 0110 = –0.40ns<br>1010 = +0.40ns, 0101 = –0.60ns<br>1011 = +0.60ns, 0100 = –0.80ns<br>1100 = +0.80ns, 0011 = –1.00ns<br>1101 = +1.00ns, 0010 = –1.20ns<br>1110 = +1.20ns, 0001 = –1.40ns<br>1111 = +1.40ns, 0000 = –1.60ns | R/W | 1 | See Note 1 |
| 6 | CPU Clock Skew1 Control Bit2 | | R/W | 0 | |
| 5 | CPU Clock Skew1 Control Bit1 | | R/W | 0 | |
| 4 | CPU Clock Skew1 Control Bit0 | | R/W | 0 | |
| 3 | CPU Clock Skew2 Control Bit3 | Delay Ahead<br>1000 = +0.00ns, 0111 = –0.15ns<br>1001 = +0.15ns, 0110 = –0.30ns<br>1010 = +0.30ns, 0101 = –0.45ns<br>1011 = +0.45ns, 0100 = –0.60ns<br>1100 = +0.60ns, 0011 = –0.75ns<br>1101 = +0.75ns, 0010 = –0.90ns<br>1110 = +0.90ns, 0001 = –1.05ns<br>1111 = +1.05ns, 0000 = –1.20ns | R/W | 1 | See Note 1 |
| 2 | CPU Clock Skew2 Control Bit2 | | R/W | 0 | |
| 1 | CPU Clock Skew2 Control Bit1 | | R/W | 0 | |
| 0 | CPU Clock Skew2 Control Bit0 | | R/W | 0 | |

Note: 1. Total CPU Clock Skew is Skew1+Skew2.

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## I²C Controlled Register Bit Map (cont.)

Byte26 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | PCIF / PCI Clock Skew2 Control Bit3 | Skew2 is “Late” Skew that is Delay Time from “Normal” Skew1.<br>0000 = +0.0ns, 1000 = +3.2ns<br>0001 = +0.4ns, 1001 = +3.6ns<br>0010 = +0.8ns, 1010 = +4.0ns<br>0011 = +1.2ns, 1011 = +4.4ns<br>0100 = +1.6ns, 1100 = +4.8ns<br>0101 = +2.0ns, 1101 = +5.2ns<br>0110 = +2.4ns, 1110 = +5.6ns<br>0111 = +2.8ns, 1111 = +6.0ns | R/W | 0 | See Note 1 |
| 6 | PCIF / PCI Clock Skew2 Control Bit2 | | R/W | 0 | |
| 5 | PCIF / PCI Clock Skew2 Control Bit1 | | R/W | 0 | |
| 4 | PCIF / PCI Clock Skew2 Control Bit0 | | R/W | 0 | |
| 3 | PCIF / PCI Clock Skew1 Control Bit3 | Skew1 is “Normal” Skew.<br>Delay Ahead<br>1000 = +0.0ns, 0111 = –0.4ns<br>1001 = +0.4ns, 0110 = –0.8ns<br>1010 = +0.8ns, 0101 = –1.2ns<br>1011 = +1.2ns, 0100 = –1.6ns<br>1100 = +1.6ns, 0011 = –2.0ns<br>1101 = +2.0ns, 0010 = –2.4ns<br>1110 = +2.4ns, 0001 = –2.8ns<br>1111 = +2.8ns, 0000 = –3.2ns | R/W | 1 | See Note 1 |
| 2 | PCIF / PCI Clock Skew1 Control Bit2 | | R/W | 0 | |
| 1 | PCIF / PCI Clock Skew1 Control Bit1 | | R/W | 0 | |
| 0 | PCIF / PCI Clock Skew1 Control Bit0 | | R/W | 0 | |

Note: 1. PCIF / PCI Clock Skew is Skew1 (= Normal) or Skew1+Skew2 (= Late).

Byte27 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | Reserved | | R/W | 0 | |
| 6 | PCIF_2 Skew Select Bit | 0 = Normal, 1 = Late | R/W | 0 | See Note 1 |
| 5 | PCIF_1 Skew Select Bit | 0 = Normal, 1 = Late | R/W | 0 | |
| 4 | PCIF_0 Skew Select Bit | 0 = Normal, 1 = Late | R/W | 0 | |
| 3 | 3V66 Clock Skew Control Bit3 | Delay Ahead<br>1000 = +0.0ns, 0111 = –0.4ns<br>1001 = +0.4ns, 0110 = –0.8ns<br>1010 = +0.8ns, 0101 = –1.2ns<br>1011 = +1.2ns, 0100 = –1.6ns<br>1100 = +1.6ns, 0011 = –2.0ns<br>1101 = +2.0ns, 0010 = –2.4ns<br>1110 = +2.4ns, 0001 = –2.8ns<br>1111 = +2.8ns, 0000 = –3.2ns | R/W | 1 | |
| 2 | 3V66 Clock Skew Control Bit2 | | R/W | 0 | |
| 1 | 3V66 Clock Skew Control Bit1 | | R/W | 0 | |
| 0 | 3V66 Clock Skew Control Bit0 | | R/W | 0 | |

Note: 1. Normal = Skew1(B26[3:0]), Late = Skew1(B26[3:0]) +Skew2 (B26[7:4]).

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## I²C Controlled Register Bit Map (cont.)

Byte28 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | Reserved | 0 = Normal, 1 = Late | R/W | 0 | |
| 6 | PCI_6 Skew Select Bit | 0 = Normal, 1 = Late | R/W | 0 | See Note 1 |
| 5 | PCI_5 Skew Select Bit | 0 = Normal, 1 = Late | R/W | 0 | |
| 4 | PCI_4 Skew Select Bit | 0 = Normal, 1 = Late | R/W | 0 | |
| 3 | PCI_3 Skew Select Bit | 0 = Normal, 1 = Late | R/W | 0 | |
| 2 | PCI_2 Skew Select Bit | 0 = Normal, 1 = Late | R/W | 0 | |
| 1 | PCI_1 Skew Select Bit | 0 = Normal, 1 = Late | R/W | 0 | |
| 0 | PCI_0 Skew Select Bit | 0 = Normal, 1 = Late | R/W | 0 | |

Note: 1. Normal = Skew1(B26[3:0]), Late = Skew1(B26[3:0]) +Skew2 (B26[7:4]).

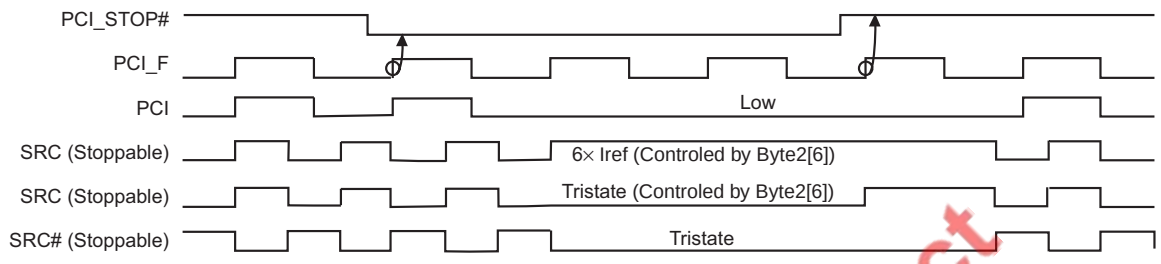
Byte29 Control Register

| Bit | Description | Contents | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | VCH Slew Rate Control Bit1 | 00 = Normal, 10 = "++" 01 = "+" , 11 = "–" | R/W | 1 | |
| 6 | VCH Slew Rate Control Bit0 | | R/W | 0 | |
| 5 | PCI Slew Rate Control Bit1 | 00 = Normal, 10 = "++" 01 = "+" , 11 = "–" | R/W | 1 | |
| 4 | PCI Slew Rate Control Bit0 | | R/W | 0 | |
| 3 | PCIF Slew Rate Control Bit1 | 00 = Normal, 10 = "++" 01 = "+" , 11 = "–" | R/W | 1 | |
| 2 | PCIF Slew Rate Control Bit0 | | R/W | 0 | |
| 1 | 3V66 Slew Rate Control Bit1 | 00 = Normal, 10 = "++" 01 = "+" , 11 = "–" | R/W | 1 | |
| 0 | 3V66 Slew Rate Control Bit0 | | R/W | 0 | |

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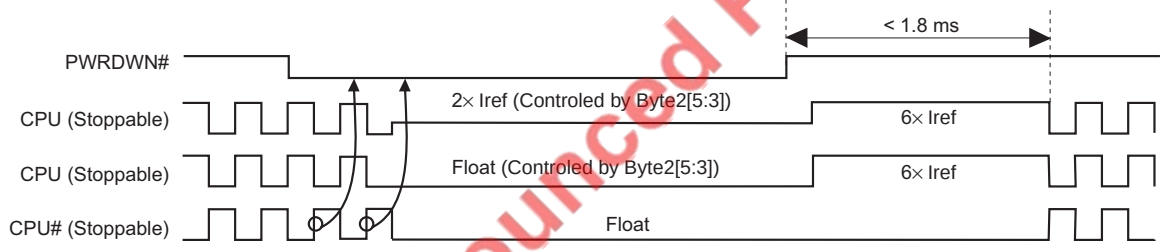
## Clock Stop Timing Diagram

PCI_STOP# Assertion/De-assersion




PCI_STOP# Assertion/De-assertion Waveforms

PWRDWN# Assertion/De-assersion




PWRDWN# Assertion/De-assertion Waveforms

PWRDWN# Functionality

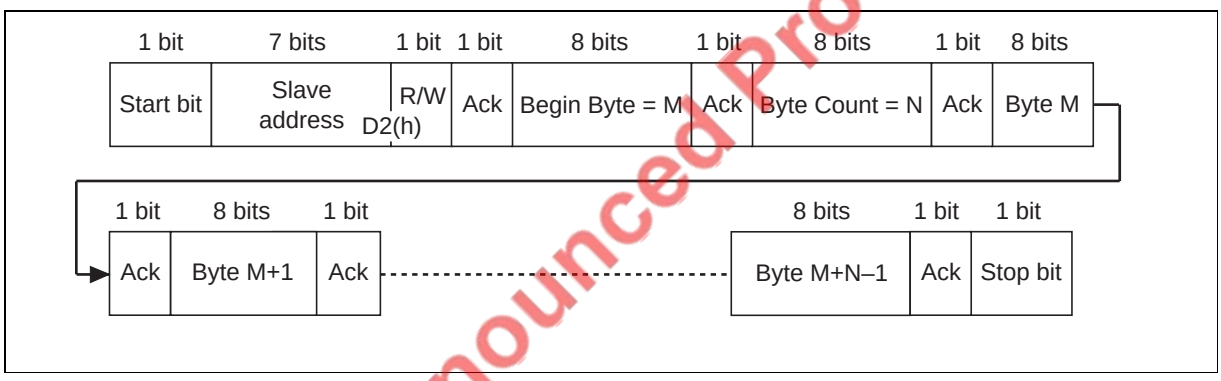
| PWRDWN# | CPU | CPU# | SRC | SRC# | 3V66 | PCIF/PCI | USB/DOT | REF |
|---|---|---|---|---|---|---|---|---|
| 1 | Normal | Normal | Normal | Normal | 66MHz | 33MHz | 48MHz | 14.318MHz |
| 0 | Iref:2 or Float | Float | Iref:2 or Float | Float | Low | Low | Low | Low |

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## Renesas clock generator I²C Serial Interface Operation

**1. Write mode**

1.1 Controller (host) sends a start bit.
1.2 Controller (host) sends the write address D2 (h).
1.3 Renesas clock generator will acknowledge (Renesas clock gen. sends “Low”).
1.4 Controller (host) sends a begin byte M.
1.5 Renesas clock generator will acknowledge (Renesas clock gen. sends “Low”).
1.6 Controller (host) sends a byte count N.
1.7 Renesas clock generator will acknowledge (Renesas clock gen. sends “Low”).
1.8 Controller (host) sends data from byte M to byte M+N–1.
1.9 Renesas clock generator will acknowledge each byte one at a time.
1.10 Controller (host) sends a stop bit.

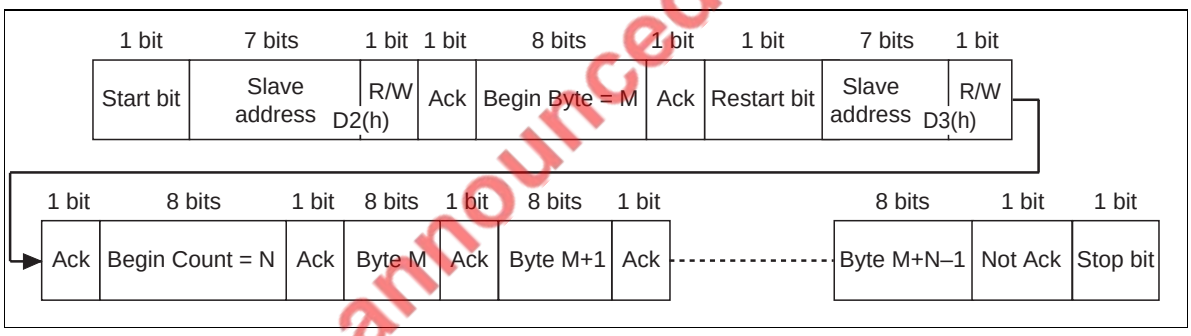



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## Renesas clock generator I²C Serial Interface Operation (cont.)

**2. Read mode**

2.1 Controller (host) sends a start bit.
2.2 Controller (host) sends the write address D2 (h).
2.3 Renesas clock generator will acknowledge (Renesas clock gen. sends “Low”).
2.4 Controller (host) sends a begin byte M.
2.5 Renesas clock generator will acknowledge (Renesas clock gen. sends “Low”).
2.6 Controller (host) sends a restart bit.
2.7 Controller (host) sends the read address D3 (h).
2.8 Renesas clock generator will acknowledge (Renesas clock gen. sends “Low”).
2.9 Renesas clock generator will send the byte count N.
2.10 Controller (host) will acknowledge.
2.11 Renesas clock generator will send data from byte M to byte M+N–1.
2.12 When Renesas clock generator sends the last byte, controller (host) will not acknowledge.
2.13 Controller (host) sends a stop bit.




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Notes: 1. Renesas clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for the verification.
2. The data transfer rate supported by this clock generator is 100k bits/sec or less (standard mode).
3. The input is operating at 3.3 V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only block-write from the controller.
6. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The data is loaded until a stop sequence is issued.
7. At power-on, all registers are set to a default condition, as shown.

## Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit | Conditions |
|---|---|---|---|---|
| Supply voltage | VDD | –0.5 to 4.6 | V | |
| Input voltage | $V_I$ | –0.5 to 4.6 | V | |
| Output voltage *1 | $V_O$ | –0.5 to VDD +0.5 | V | |
| Input clamp current | $I_{IK}$ | –50 | mA | $V_I < 0$ |
| Output clamp current | $I_{OK}$ | –50 | mA | $V_O < 0$ |
| Continuous output current | $I_O$ | ±50 | mA | $V_O$ = 0 to VDD |
| Maximum power dissipation at Ta = 55°C (in still air) | | 0.7 | W | |
| Storage temperature | Tstg | –65 to +150 | °C | |

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## Recommended Operating Conditions

| Item | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Supply voltage | VDD | 3.135 | 3.3 | 3.465 | V | |
| Supply voltage | VDDA | 3.135 | 3.3 | 3.465 | V | |
| DC input signal voltage | | –0.3 | — | VDD+0.3 | V | |
| High level input voltage | $V_{IH}$ | 2.0 | — | VDD+0.3 | V | |
| Low level input voltage | $V_{IL}$ | –0.3 | — | 0.8 | V | |
| Operating temperature | $T_a$ | 0 | — | 70 | °C | |

EOL announced Product

## DC Electrical Characteristics / Serial Input Port

Ta = 0°C to 70°C, VDD = 3.3 V

| Item | Symbol | Min | Typ *[1] | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | — | — | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | — | — | V | |
| Input Current | $I_I$ | –50 | — | +50 | µA | VI = 0 V or 3.465 V, VDD = 3.465 V |
| Input capacitance | $C_I$ | — | 10 | — | pF | SDATA & SCLK |

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

## AC Electrical Characteristics / Serial Input port

Ta = 0°C to 70°C, VDD = 3.3 V

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|
| SCLK Frequency | $F_{SCLK}$ | — | — | 100 | kHz | Normal Mode | |
| Start Hold Time | $t_{STHD}$ | 4.0 | — | — | µs | | |
| SCLK Low Time | $t_{LOW}$ | 4.7 | — | — | µs | | |
| SCLK High Time | $t_{HIGH}$ | 4.0 | — | — | µs | | |
| Data Setup Time | $t_{DSU}$ | 250 | — | — | ns | | |
| Data Hold Time | $t_{DHD}$ | 300 | — | — | ns | | |
| Stop Setup Time | $t_{STSU}$ | 4.0 | — | — | µs | | |
| BUS Free Time between Stop & Start Condition | $t_{SPF}$ | 4.7 | — | — | µs | | |

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## DC Electrical Characteristics CPU/CPU# Clock

Ta = 0°C to 70°C, VDD = 3.3 V, Iref = 475 Ω

| Item | Symbol | Min | Typ *[1] | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Output voltage | $V_O$ | — | — | 1.20 | V | Rp = 49.9 Ω, VDD = 3.3 V |
| Output Current | $I_O$ | — | I(nom) *[2] | — | mA | VDD = 3.3 V |
| Output resistance | | 3000 | — | — | Ω | $V_O$ = 1.2 V |

Notes: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditional (nom) is output current(Ioh) shown in below.

2. Ioh = VDD/(3Rr) = 3.3/(3x475) = 2.32 mA,
Ioh x6 = 13.89 mA (Voh @Z: 0.695 V @50 Ω),
Ioh x2 = 4.63 mA (Voh @Z: 0.232 V @50 Ω)

EOL announced Product

## AC Electrical Characteristics CPU/CPU# Clock (CPU at 0.7V Timing)

Ta = 0°C to 70°C, VDD = 3.3 V, $C_L$ = 2 pF, Rs = 33.2 Ω, Rp = 49.9 Ω

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|
| Cycle to cycle jitter | $t_{CCS}$ | — | \|125\| | — | ps | | Note1 |
| CPU Group Skew (CPU clock out to CPU clock out) | $t_{skS}$ | — | \|100\| | — | ps | | |
| Rise time | $t_r$ | 175 | — | 700 | ps | $V_O$ = 0.175 V to 0.525 V | 200MHz |
| Fall time | $t_f$ | 175 | — | 700 | ps | $V_O$ = 0.175 V to 0.525 V | 200MHz |
| Clock Duty Cycle | | 45 | 50 | 55 | % | | 200MHz |
| CPU clock period(100) | | — | 9.99 | — | ns | | |
| CPU clock period(133) | | — | 7.49 | — | ns | | |
| CPU clock period(166) | | — | 5.99 | — | ns | | |
| CPU clock period(200) | | — | 4.99 | — | ns | | |
| Cross point(0.7V) voltage | Vcross | 0.25 | — | 0.55 | V | | 200MHz |

Note: 1. Difference of cycle time between two adjoining cycles.

## DC Electrical Characteristics SRC/SRC# Clock

Ta = 0°C to 70°C, VDD = 3.3 V, Iref = 475 Ω

| Item | Symbol | Min | Typ *1 | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Output voltage | $V_O$ | — | — | 1.20 | V | Rp = 49.9 Ω, VDD = 3.3 V |
| Output Current | $I_O$ | — | I(nom) | — | mA | VDD = 3.3 V |
| Output resistance | | 3000 | — | — | Ω | $V_O$ = 1.2 V |

Notes: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions

2. I(nom) is output current(Ioh) shown in below.
Ioh = VDD/(3Rr) = 3.3/(3x475) = 2.32 mA,
Ioh x6 = 13.89 mA (Voh @Z: 0.695V @50 Ω),
Ioh x2 = 4.63 mA (Voh @Z: 0.232V @50 Ω)

## AC Electrical Characteristics SRC/SRC# Clock (SRC at 0.7V Timing)

Ta = 0°C to 70°C, VDD = 3.3 V, $C_L$ = 2 pF, Rs = 33.2 Ω, Rp = 49.9 Ω

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|
| Cycle to cycle jitter | $t_{CCS}$ | — | \|125\| | — | ps | | Note1 |
| Rise time | $t_r$ | 175 | — | 700 | ps | $V_O$ = 0.175 V to 0.525 V | 100 MHz |
| Fall time | $t_f$ | 175 | — | 700 | ps | $V_O$ = 0.175 V to 0.525 V | 100 MHz |
| Clock Duty Cycle | | 45 | 50 | 55 | % | | 100 MHz |
| SRC clock period(100) | | — | 9.99 | — | ns | | |
| SRC clock period(200) | | — | 4.99 | — | ns | | |
| Cross point(0.7V) voltage | Vcross | 0.25 | — | 0.55 | V | | 100 MHz |

Note: 1. Difference of cycle time between two adjoining cycles.

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## DC Electrical Characteristics / 3V66 Buffer (CK409T Type5 Buffer)

Ta = 0°C to 70°C, VDD = 3.3 V

| Item | Symbol | Min | Typ *1 | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Output Voltage | $V_{OH}$ | 3.1 | — | — | V | $I_{OH}$ = –1 mA, VDD = 3.3 V |
| | $V_{OL}$ | — | — | 50 | mV | $I_{OL}$ = 1 mA, VDD = 3.3 V |
| Output Current | $I_{OH}$ | — | — | –33 | mA | $V_{OH}$ = 1.0 V |
| | $I_{OL}$ | 30 | — | — | mA | $V_{OL}$ = 1.95 V |

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

## AC Electrical Characteristics / 3V66 Buffer

Ta = 0°C to 70°C, VDD = 3.3 V, $C_L$ = 30 pF

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|
| Cycle to cycle jitter | $t_{CCS}$ | — | \|250\| | — | ps | Fig.1 | Note1 |
| 3V66 Buffer (3V66 (4:0)) Group Skew | $t_{skS}$ | — | 0 | 250 | ps | Rising edge @1.5 V to 1.5 V Fig.2 | |
| Slew rate | $t_{SL}$ | 1.0 | — | 4.0 | V/ns | | 0.4V to 2.4 V |
| Clock Period | | — | 14.998 | — | ns | | |
| Clock Duty Cycle | | 45 | 50 | 55 | % | | |
| 3V66 (4:0) leads 33 MHz PCI | | 1.5 | — | 3.5 | ns | | |

Note: 1. Difference of cycle time between two adjoining cycles.

EOL announced Product

## DC Electrical Characteristics / PCI & PCIF Clock (CK409T Type5 Buffer)

Ta = 0°C to 70°C, VDD = 3.3 V

| Item | Symbol | Min | Typ *[1] | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Output Voltage | $V_{OH}$ | 3.1 | — | — | V | $I_{OH}$ = –1 mA, VDD = 3.3 V |
| | $V_{OL}$ | — | — | 50 | mV | $I_{OL}$ = 1 mA, VDD = 3.3 V |
| Output Current | $I_{OH}$ | — | — | –33 | mA | $V_{OH}$ = 1.0 V |
| | $I_{OL}$ | 30 | — | — | mA | $V_{OL}$ = 1.95 V |

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

## AC Electrical Characteristics / PCI & PCIF Clock

Ta = 0°C to 70°C, VDD = 3.3 V, $C_L$ = 30 pF

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|
| Cycle to cycle jitter | $t_{CCS}$ | — | \|250\| | — | ps | Fig.1 | Note1 |
| PCI Group Skew | tskS | — | 0 | 500 | ps | Rising edge @1.5V to 1.5 V Fig.2 | |
| Clock Period | | — | 29.996 | — | ns | | |
| Slew rate | $t_{SL}$ | 1.0 | — | 4.0 | V/ns | | 0.4 V to 2.4 V |
| Clock Duty Cycle | | 45 | 50 | 55 | % | | |

Note: 1. Difference of cycle time between two adjoining cycles.

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## DC Electrical Characteristics / USB & VCH 48MHz Clock (CK409T Type3A Buffer)

Ta = 0°C to 70°C, VDD = 3.3 V

| Item | Symbol | Min | Typ *[1] | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Output Voltage | $V_{OH}$ | 3.1 | — | — | V | $I_{OH}$ = –1 mA, VDD = 3.3 V |
| | $V_{OL}$ | — | — | 50 | mV | $I_{OL}$ = 1 mA, VDD = 3.3 V |
| Output Current | $I_{OH}$ | — | — | –29 | mA | $V_{OH}$ = 1.0 V |
| | $I_{OL}$ | 29 | — | — | mA | $V_{OL}$ = 1.95 V |

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

## AC Electrical Characteristics / USB & VCH 48MHz Clock

Ta = 0°C to 70°C, VDD = 3.3 V, $C_L$ = 20 pF

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|
| Cycle to cycle jitter | $t_{CCS}$ | — | \|350\| | — | ps | Fig.1 | Note1 |
| Clock Period | | — | 20.831 | — | ns | | |
| Slew rate | $t_{SL}$ | 1.0 | — | 2.0 | V/ns | | 0.4 V to 2.4 V |
| Clock Duty Cycle | | 45 | 50 | 55 | % | | |

Note: 1. Difference of cycle time between two adjoining cycles.

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## DC Electrical Characteristics / DOT Clock (CK409T Type3B Buffer)

Ta = 0°C to 70°C, VDD = 3.3 V

| Item | Symbol | Min | Typ *1 | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Output Voltage | $V_{OH}$ | 3.1 | — | — | V | $I_{OH}$ = –1 mA, VDD = 3.3 V |
| | $V_{OL}$ | — | — | 50 | mV | $I_{OL}$ = 1 mA, VDD = 3.3 V |
| Output Current | $I_{OH}$ | — | — | –29 | mA | $V_{OH}$ = 1.0 V |
| | $I_{OL}$ | 29 | — | — | mA | $V_{OL}$ = 1.95 V |

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

## AC Electrical Characteristics / DOT Clock

Ta = 0°C to 70°C, VDD = 3.3 V, $C_L$ = 10 pF

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|
| Cycle to cycle jitter | $t_{CCS}$ | — | \|350\| | — | ps | Fig.1 | **Note1** |
| Clock Period | | — | 20.831 | — | ns | | |
| Slew rate | $t_{SL}$ | 2.0 | — | 4.0 | V/ns | | 0.4V to 2.4V |
| Clock Duty Cycle | | 45 | 50 | 55 | % | | |

Note: 1. Difference of cycle time between two adjoining cycles.

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## DC Electrical Characteristics / REF Clock (CK409T Type5 Buffer)

Ta = 0°C to 70°C, VDD = 3.3 V

| Item | Symbol | Min | Typ *1 | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Output Voltage | $V_{OH}$ | 3.1 | — | — | V | $I_{OH}$ = –1 mA, VDD = 3.3 V |
| | $V_{OL}$ | — | — | 50 | mV | $I_{OL}$ = 1 mA, VDD = 3.3 V |
| Output Current | $I_{OH}$ | — | — | –33 | mA | $V_{OH}$ = 1.0 V |
| | $I_{OL}$ | 30 | — | — | mA | $V_{OL}$ = 1.95 V |

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

## AC Electrical Characteristics / REF Clock

Ta = 0°C to 70°C, VDD = 3.3 V, $C_L$ = 30 pF

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|
| Cycle to cycle jitter | $t_{CCS}$ | — | \|1000\| | — | ps | Fig.1 | **Note1** |
| Clock Period | | — | 69.841 | — | ns | | |
| Slew rate | $t_{SL}$ | 1.0 | — | 4.0 | V/ns | | 0.4 V to 2.4 V |
| Clock Duty Cycle | | 45 | 50 | 55 | % | | |

Note: 1. Difference of cycle time between two adjoining cycles.

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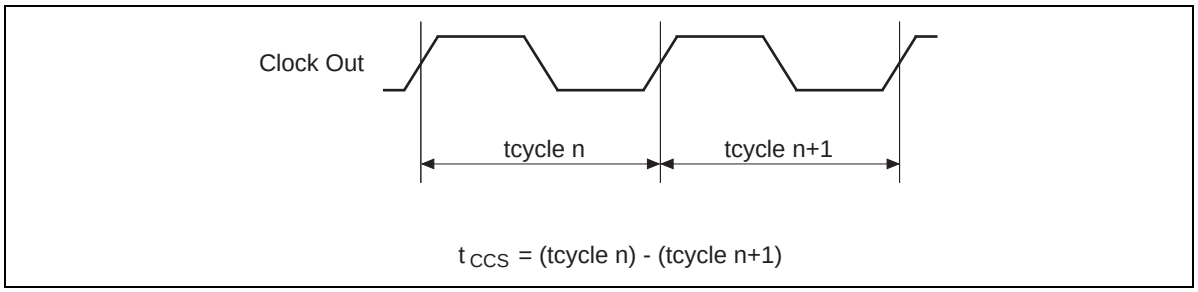



**Fig.1 Cycle to Cycle Jitter (3.3V Single Ended Clock Output)**

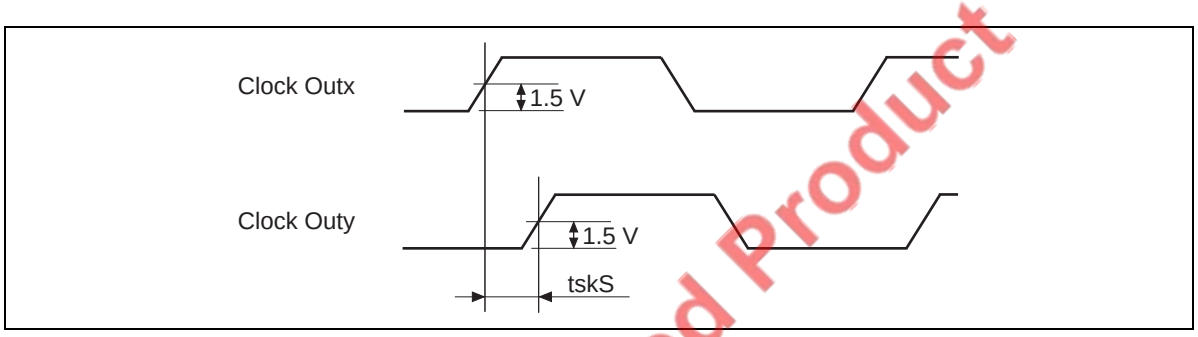



**Fig.2 Output Clock Skew (3.3V Single Ended Clock Output)**

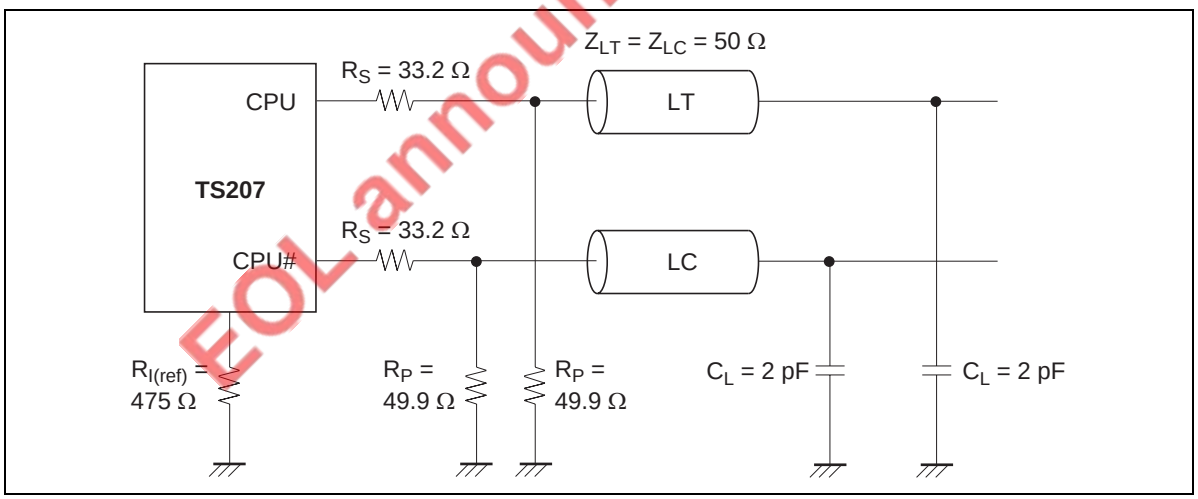
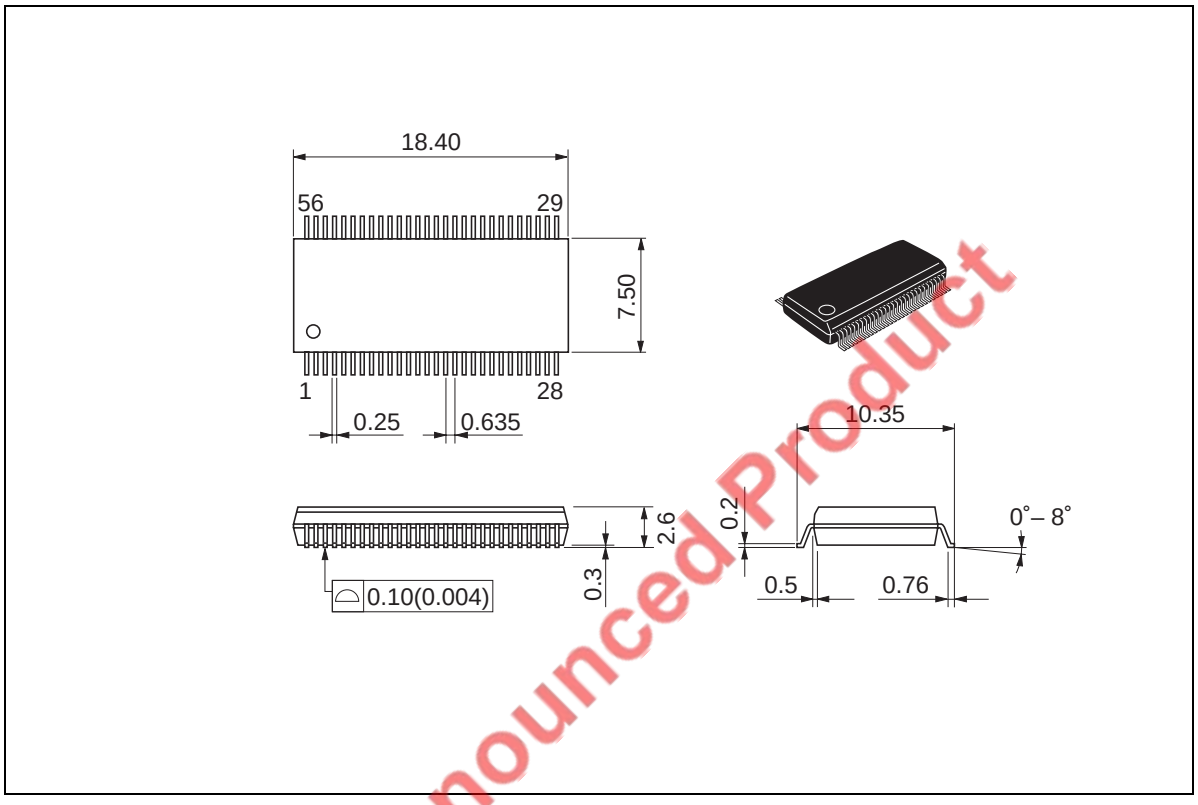



**Fig.3 Load Circuit for CPU/CPU#**

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## Package Dimensions

Unit : mm




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