

KEELOQ® Code Hopping Decoder

FEATURES

Security

- Encrypted storage of manufacturer's code
- Encrypted storage of encoder decryption keys
- Up to seven transmitters can be learned code hopping technology
- Normal and secure learning mechanisms

Operating

- 4.5V – 5.5V operation
- Internal oscillator
- Auto bit rate detection

Other

- Stand-alone decoder
- Internal EEPROM for transmitter storage
- Synchronous serial interface
- 1 Kbit user EEPROM
- 14-pin DIP/SOIC package

Typical Applications

- Automotive remote entry systems
- Automotive alarm systems
- Automotive immobilizers
- Gate and garage openers
- Electronic door locks
- Identity tokens
- Burglar alarm systems

Compatible Encoders

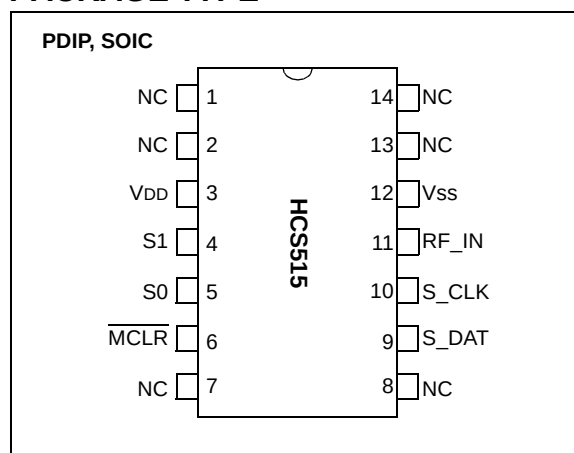
All encoders and transponders configured for the following setting:

- PWM modulation format (1/3-2/3)
- T_E in the range from 100 μ s to 400 μ s
- 10 x T_E Header
- 28-bit Serial Number
- 16-bit Synchronization counter
- Discrimination bits equal to Serial Number 8 LSbs
- 66- to 69-bit length code word.

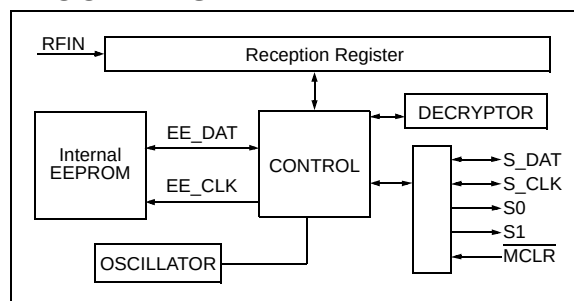
DESCRIPTION

The Microchip Technology Inc. HCS515 is a code hopping decoder designed for secure Remote Keyless Entry (RKE) systems. The HCS515 utilizes the patented code hopping system and high security learning mechanisms to make this a canned solution when used with the HCS encoders to implement a unidirectional remote and access control systems. The HCS515 can be used as a stand-alone decoder or in conjunction with a microcontroller.

PACKAGE TYPE



BLOCK DIAGRAM



The manufacturer's code, encoder decryption keys, and synchronization information are stored in encrypted form in internal EEPROM. The HCS515 uses the S_DAT and S_CLK inputs to communicate with a host controller device.

The HCS515 operates over a wide voltage range of 4.5V – 5.5V. The decoder employs automatic bit rate detection, which allows it to compensate for wide vari-

ations in transmitter data rate. The decoder contains sophisticated error checking algorithms to ensure only valid codes are accepted.

1.0 SYSTEM OVERVIEW

Key Terms

The following is a list of key terms used throughout this data sheet. For additional information on KEELoQ and Code Hopping, refer to Technical Brief 3 (TB003).

- **RKE** - Remote Keyless Entry
- **Button Status** - Indicates what button input(s) activated the transmission. Encompasses the 4 button status bits S3, S2, S1 and S0 (Figure 7-2).
- **Code Hopping** - A method by which a code, viewed externally to the system, appears to change unpredictably each time it is transmitted.
- **Code word** - A block of data that is repeatedly transmitted upon button activation (Figure 7-1).
- **Transmission** - A data stream consisting of repeating code words (Figure 7-1).
- **Crypt key** - A unique and secret 64-bit number used to encrypt and decrypt data. In a symmetrical block cipher such as the KEELoQ algorithm, the encryption and decryption keys are equal and will therefore be referred to generally as the crypt key.
- **Encoder** - A device that generates and encodes data.
- **Encryption Algorithm** - A recipe whereby data is scrambled using a crypt key. The data can only be interpreted by the respective decryption algorithm using the same crypt key.
- **Decoder** - A device that decodes data received from an encoder.
- **Decryption algorithm** - A recipe whereby data scrambled by an encryption algorithm can be unscrambled using the same crypt key.
- **Learn** – Learning involves the receiver calculating the transmitter's appropriate crypt key, decrypting the received hopping code and storing the serial number, synchronization counter value and crypt key in EEPROM. The KEELoQ product family facilitates several learning strategies to be implemented on the decoder. The following are examples of what can be done.
 - **Simple Learning**
The receiver uses a fixed crypt key, common to all components of all systems by the same manufacturer, to decrypt the received code word's encrypted portion.
 - **Normal Learning**
The receiver uses information transmitted during normal operation to derive the crypt key and decrypt the received code word's encrypted portion.

- **Secure Learn**

The transmitter is activated through a special button combination to transmit a stored 60-bit seed value used to generate the transmitter's crypt key. The receiver uses this seed value to derive the same crypt key and decrypt the received code word's encrypted portion.

- **Manufacturer's code** – A unique and secret 64-bit number used to generate unique encoder crypt keys. Each encoder is programmed with a crypt key that is a function of the manufacturer's code. Each decoder is programmed with the manufacturer code itself.

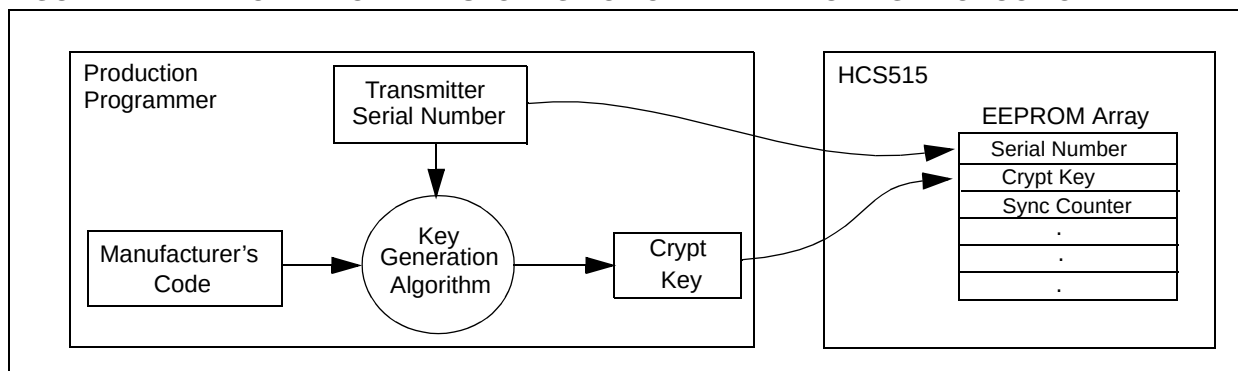
1.1 HCS Encoder Overview

The HCS encoders have a small EEPROM array which must be loaded with several parameters before use. The most important of these values are:

- A crypt key that is generated at the time of production
- A 16-bit synchronization counter value
- A 28-bit serial number which is meant to be unique for every encoder

The manufacturer programs the serial number for each encoder at the time of production, while the 'Key Generation Algorithm' generates the crypt key (Figure 1-1). Inputs to the key generation algorithm typically consist of the encoder's serial number and a 64-bit manufacturer's code, which the manufacturer creates.

Note: The manufacturer code is a pivotal part of the system's overall security. Consequently, all possible precautions must be taken and maintained for this code.

FIGURE 1-1: CREATION AND STORAGE OF CRYPT KEY DURING PRODUCTION

The 16-bit synchronization counter is the basis behind the transmitted code word changing for each transmission; it increments each time a button is pressed. Due to the code hopping algorithm's complexity, each increment of the synchronization value results in greater than 50% of the bits changing in the transmitted code word.

Figure 1-2 shows how the key values in EEPROM are used in the encoder. Once the encoder detects a button press, it reads the button inputs and updates the synchronization counter. The synchronization counter and crypt key are input to the encryption algorithm and the output is 32 bits of encrypted information. This data will change with every button press, its value appearing externally to 'randomly hop around', hence it is referred to as the hopping portion of the code word. The 32-bit hopping code is combined with the button information and serial number to form the code word transmitted to the receiver. The code word format is explained in greater detail in Section 7.2.

A receiver may use any type of controller as a decoder, but it is typically a microcontroller with compatible firmware that allows the decoder to operate in conjunction with an HCS515 based transmitter. Section 3.0 provides detail on integrating the HCS515 into a system.

A transmitter must first be 'learned' by the receiver before its use is allowed in the system. Learning includes calculating the transmitter's appropriate crypt key, decrypting the received hopping code and storing the serial number, synchronization counter value and crypt key in EEPROM.

In normal operation, each received message of valid format is evaluated. The serial number is used to determine if it is from a learned transmitter. If from a learned transmitter, the message is decrypted and the synchronization counter is verified. Finally, the button status is checked to see what operation is requested. Figure 1-3 shows the relationship between some of the values stored by the receiver and the values received from the transmitter.

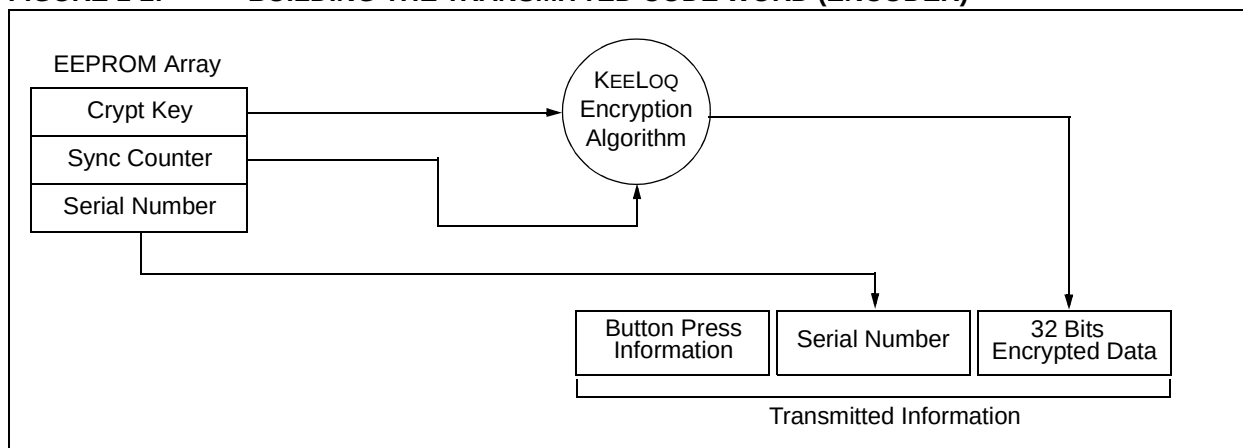
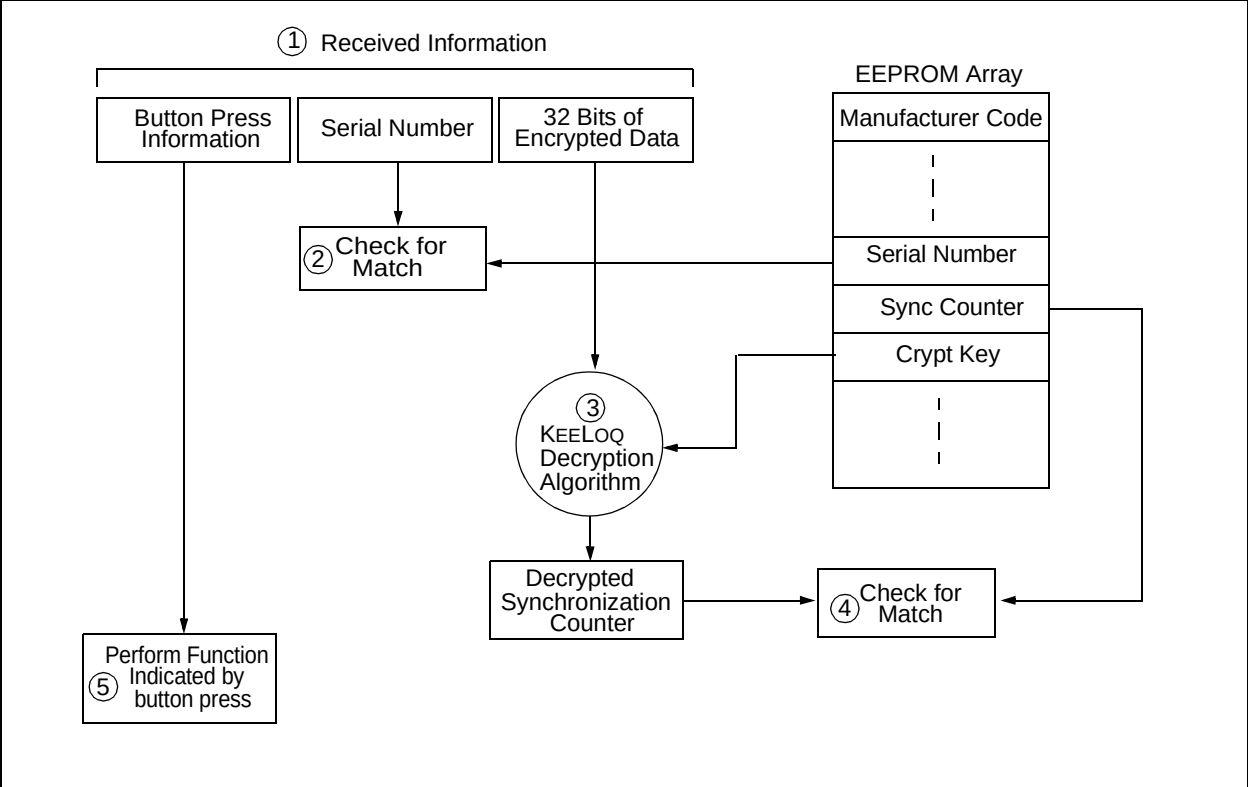
FIGURE 1-2: BUILDING THE TRANSMITTED CODE WORD (ENCODER)

FIGURE 1-3: BASIC OPERATION OF RECEIVER (DECODER)



NOTE: Circled numbers indicate the order of execution.

2.0 PIN ASSIGNMENT

PIN	Decoder Function	I/O ⁽¹⁾	Buffer Type ⁽¹⁾	Description
1	NC	—	—	No connection
2	NC	—	—	No connection
3	VDD	—	—	Power connection
4	S1	O	TTL	S1 function output
5	S0	O	TTL	S0 function output
6	MCLR	I	ST	Master clear input
7	NC	—	—	No connection
8	NC	—	—	No connection
9	S_DAT	I/O	TTL	Synchronous data from controller
10	S_CLK	I	TTL	Synchronous clock from controller
11	RF_IN	I	TTL	Input from RF receiver
12	GND	—	—	Ground connection
13	NC	—	—	No connection
14	NC	—	—	No connection

Note: P = power, I = in, O = out, and ST = Schmitt Trigger input.

3.0 DECODER OPERATION

3.1 Learning a Transmitter to a Receiver (Normal or Secure Learn)

Before the transmitter and receiver can work together, the receiver must first 'learn' and store the following information from the transmitter in EEPROM:

- A check value of the serial number
- The encoder decryption key
- The current synchronization counter value

The decoder must also store the manufacturer's code (Section 1.1) in protected memory. This code will typically be the same for all of the decoders in a system.

The HCS515 has seven memory slots, and, consequently, can store up to seven transmitters. During the learn procedure, the decoder searches for an empty memory slot for storing the transmitter's information. When all of the memory slots are full, the decoder will overwrite the last transmitter's information. To erase all of the memory slots at once, use the ERASE_ALL command (C3H).

3.1.1 LEARNING PROCEDURE

Learning is initiated by sending the ACTIVATE_LEARN (D2H) command to the decoder. The decoder acknowledges reception of the command by pulling the data line high.

For the HCS515 decoder to learn a new transmitter, the following sequence is required:

1. Activate the transmitter once.
2. Activate the transmitter a second time. (In Secure Learning mode, the seed transmission must be transmitted during the second stage of learn by activating the appropriate buttons on the transmitter.)
3. The HCS515 will transmit a learn-status string, indicating that the learn was successful.
4. The decoder has now learned the transmitter.
5. Repeat steps 1-3 to learn up to seven transmitters

Note 1: Learning will be terminated if two nonsequential codes were received or if two acceptable codes were not decoded within 30 seconds.

- 2: If more than seven transmitters are learned, the new transmitter will replace the last transmitter learned. It is, therefore, not possible to erase lost transmitters by repeatedly learning new transmitters. To remove lost or stolen transmitters, ERASE_ALL transmitters and relearn all available transmitters.

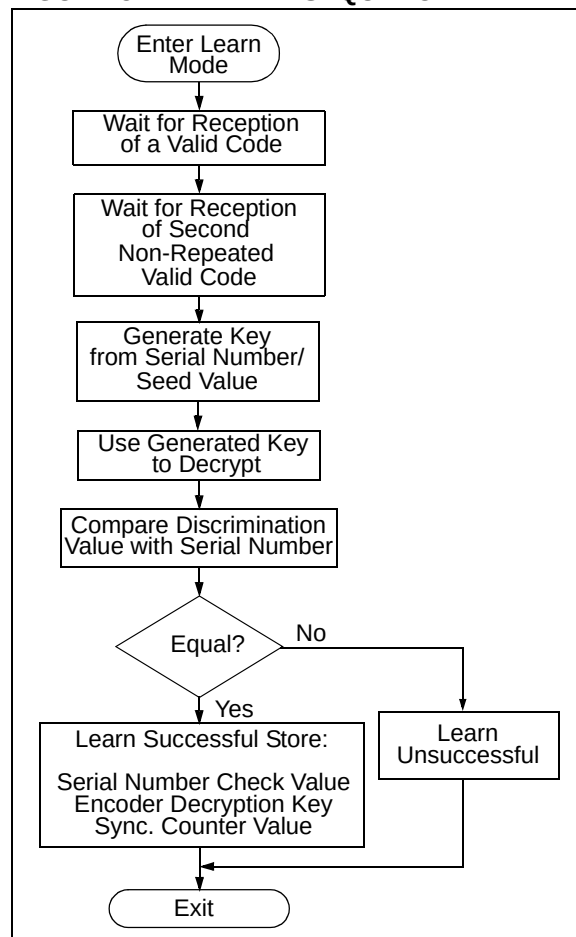
- 3: Learning a transmitter with an encoder decryption key that is identical to a transmitter already in memory replaces the existing transmitter. In practice, this means that all transmitters should have unique encoder decryption keys. Learning a previously learned transmitter does not use any additional memory slots.

The following checks are performed by the decoder to determine if the transmission is valid during learn:

- The first code word is checked for bit integrity.
- The second code word is checked for bit integrity.
- The encoder decryption key is generated according to the selected algorithm.
- The hopping code is decrypted.
- The discrimination value is checked.
- If all the checks pass, the key, serial number check value, and synchronization counter values are stored in EEPROM memory.

Figure 3-1 shows a flow chart of the learn sequence.

FIGURE 3-1: LEARN SEQUENCE



3.2 Validation of Codes

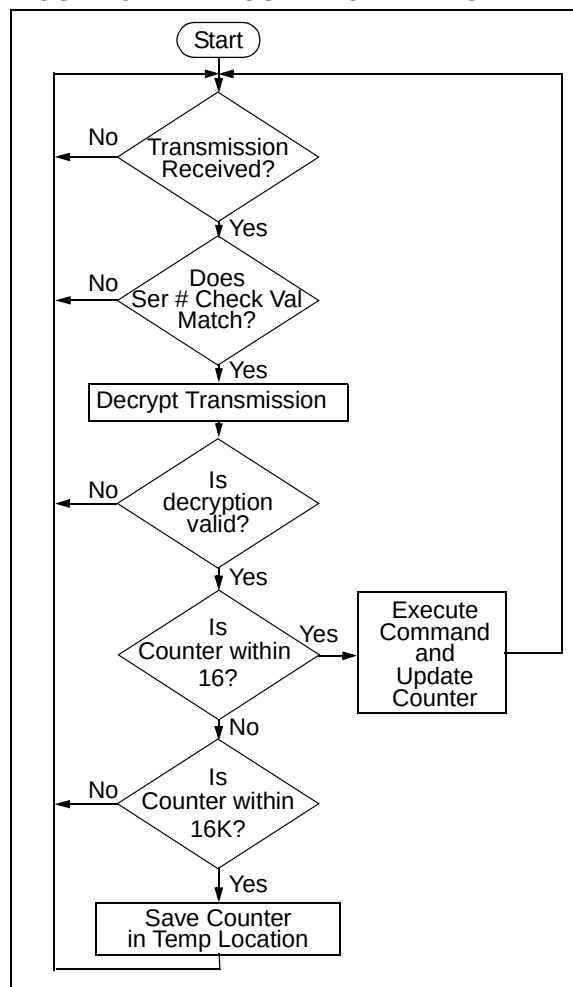
The decoder waits for a transmission and checks the serial number to determine if it is a learned transmitter. If it is, it takes the code hopping portion of the transmission and decrypts it, using the encoder decryption key. It uses the discrimination value to determine if the decryption was valid. If everything up to this point is valid, the synchronization counter value is evaluated.

3.3 Validation Steps

Validation consists of the following steps:

1. Search EEPROM to find the Serial Number Check Value Match
2. Decrypt the Hopping Code
3. Compare the 10 bits of the discrimination value with the lower 10 bits of serial number
4. Check if the synchronization counter value falls within the first synchronization window.
5. Check if the synchronization counter value falls within the second synchronization window.
6. If a valid transmission is found, update the synchronization counter, else use the next transmitter block, and repeat the tests.

FIGURE 3-2: DECODER OPERATION



3.4 Synchronization with Decoder (Evaluating the Counter)

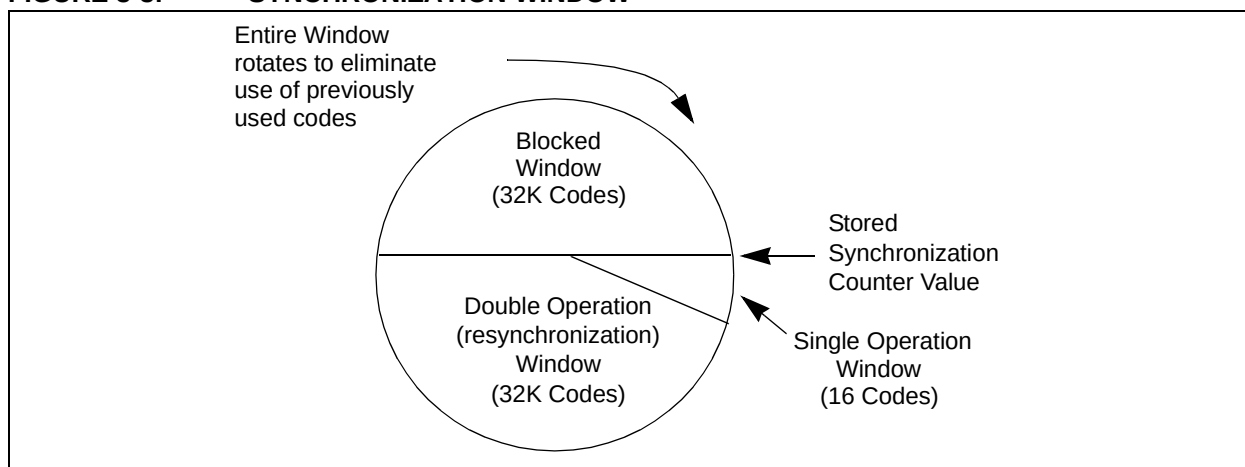
The KEELOQ technology patent scope includes a sophisticated synchronization technique that does not require the calculation and storage of future codes. The technique securely blocks invalid transmissions while providing transparent resynchronization to transmitters inadvertently activated away from the receiver.

Figure 3-3 shows a 3-partition, rotating synchronization window. The size of each window is optional but the technique is fundamental. Each time a transmission is authenticated, the intended function is executed and the transmission's synchronization counter value is stored in EEPROM. From the currently stored counter value there is an initial "Single Operation" forward window of 16 codes. If the difference between a received synchronization counter and the last stored counter is within 16, the intended function will be executed on the single button press and the new synchronization counter will be stored. Storing the new synchronization counter value effectively rotates the entire synchronization window.

A "Double Operation" (resynchronization) window further exists from the Single Operation window up to 32K codes forward of the currently stored counter value. It is referred to as "Double Operation" because a transmission with synchronization counter value in this window will require an additional, sequential counter transmission prior to executing the intended function. Upon receiving the sequential transmission the decoder executes the intended function and stores the synchronization counter value. This resynchronization occurs transparently to the user as it is human nature to press the button a second time if the first was unsuccessful.

The third window is a "Blocked Window" ranging from the double operation window to the currently stored synchronization counter value. Any transmission with synchronization counter value within this window will be ignored. This window excludes previously used, perhaps code-grabbed transmissions from accessing the system.

FIGURE 3-3: SYNCHRONIZATION WINDOW



HCS515

4.0 INTERFACING TO A MICROCONTROLLER

The HCS515 interfaces to a microcontroller via a synchronous serial interface. A clock and data line are used to communicate with the HCS515. The microcontroller controls the clock line. There are two groups of data transfer messages. The first is from the decoder whenever the decoder receives a valid transmission. The decoder signals reception of a valid code by taking the data line high (maximum of 500 ms). The microcontroller then services the request by clocking out a data string from the decoder. The data string contains the function code, the status bit, and block indicators. The second is from the controlling microcontroller to the decoder in the form of a defined command set.

Figure 4-1 shows the HCS515 decoder and the I/O interface lines necessary to interface to a microcontroller.

4.1 Valid Transmission Message

The decoder informs the microcontroller of a valid transmission by taking the data line high for up to 500 ms. The controlling microcontroller must acknowl-

edge by taking the clock line high. The decoder then takes the data line low. The microcontroller can then begin clocking a data stream out of the HCS515. The data stream consists of:

- START bit '0'.
- 2 status bits [REPEAT, VLow].
- 4-bit function code [S3 S2 S1 S0].
- STOP bit '1'.
- 4 bits indicating the number of transmitters learned into the decoder [CNT3...CNT0].
- 4 bits indicating which block was used [TX3...TX0].
- 64 bits of the received transmission with the hopping code decrypted.

Note: Data is always clocked in/out Least Significant bit (LSb) first.

The decoder will terminate the transmission of the data stream at any point where the clock is kept low for longer than 1 ms. Therefore, the microcontroller can only clock out the required bits. A maximum of 80 bits can be clocked out of the decoder.

FIGURE 4-1: HCS515 DECODER AND I/O INTERFACE LINES

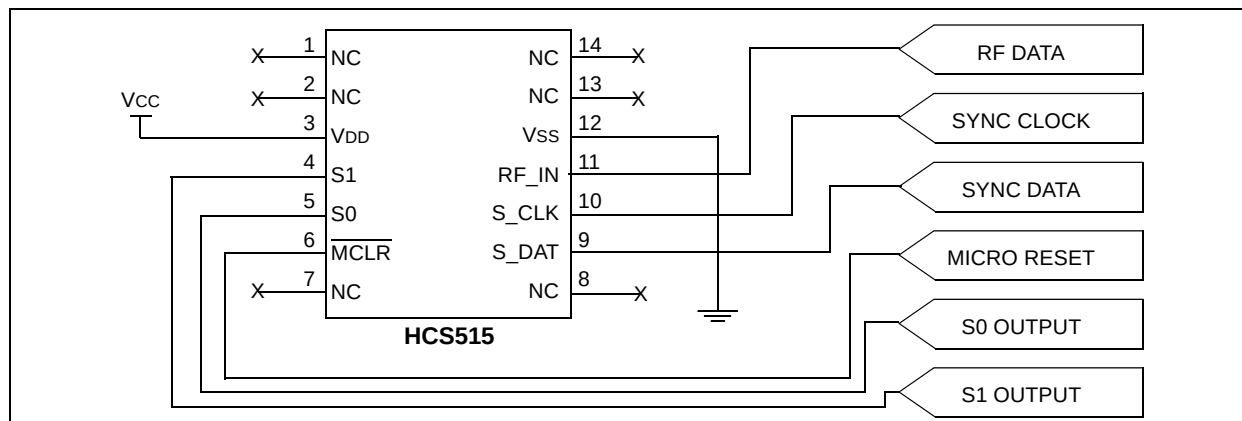
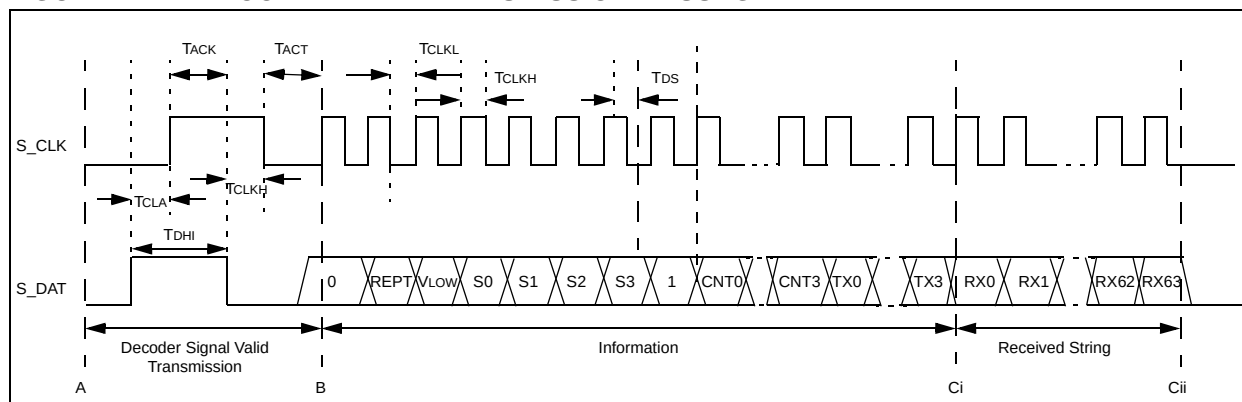


FIGURE 4-2: DECODER VALID TRANSMISSION MESSAGE



4.2.3 COMMAND ACTIVATION TIMES

The command activation time (Table 4-1) is defined as the maximum time the microcontroller has to wait for a response from the decoder. The decoder will abort and

service the command request. The response time depends on the state of the decoder when the Command mode is requested.

TABLE 4-1: COMMAND ACTIVATION TIMES

Decoder State	Min	Max
While receiving transmissions	—	2.5 ms BPWMAX = 2.7 ms
During the validation of a received transmission	—	3 ms
During the update of the sync counters	—	40 ms
During learn	—	170 ms

4.2.4 DECODER COMMANDS

The command byte specifies the operation required by the controlling microcontroller. Table 4-2 lists the commands.

TABLE 4-2: DECODER COMMANDS

Instruction	Command Byte	Operation
READ	F0 HEX	Read a byte from user EEPROM
WRITE	E1 HEX	Write a byte to user EEPROM
ACTIVATE_LRN	D2 HEX	Activate a learn sequence on the decoder
ERASE_ALL	C3 HEX	Activate an erase all function on the decoder
PROGRAM	B4 HEX	Program manufacturer's code and configuration byte

4.2.5 READ BYTE/S FROM USER EEPROM

The read command (Figure 4-4) is used to read bytes from the user EEPROM. The offset in the user EEPROM is specified by the address byte, which is truncated to 7 bits (C to D). After the address, a dummy byte must be clocked in (D to E). The EEPROM data byte is clocked out on the next rising edge of the clock line with the Least Significant bit first (E to F). Sequential reads are possible by repeating sequence E to F within 1 ms after the falling edge of the previous byte's Most Significant bit (MSb). During the sequential read, the address value will wrap after 128 bytes. The decoder will terminate the read command if no clock pulses are received for a period longer than 1.2 ms.

4.2.6 WRITE BYTE/S TO USER EEPROM

The write command (Figure 4-5) is used to write a location in the user EEPROM. The address byte is truncated to seven bits (C to D). The data is clocked in Least Significant bit (LSb) first. The clock line must be asserted to initiate the write. Sequential writes of bytes are possible by clocking in the byte and then asserting the clock line (D – F). The decoder will terminate the write command if no clock pulses are received for a period longer than 1.2 ms. After a successful write sequence, the decoder will acknowledge by taking the data line high and keeping it high until the clock line goes low.

FIGURE 4-4: READ BYTES FROM USER EEPROM

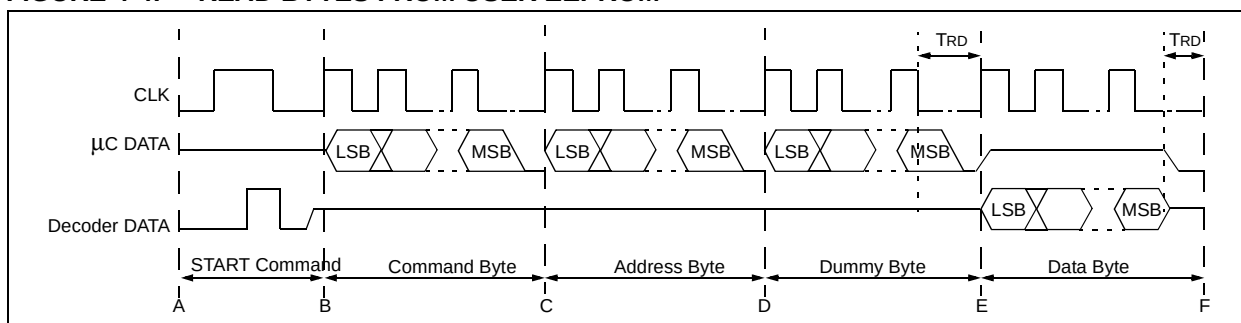
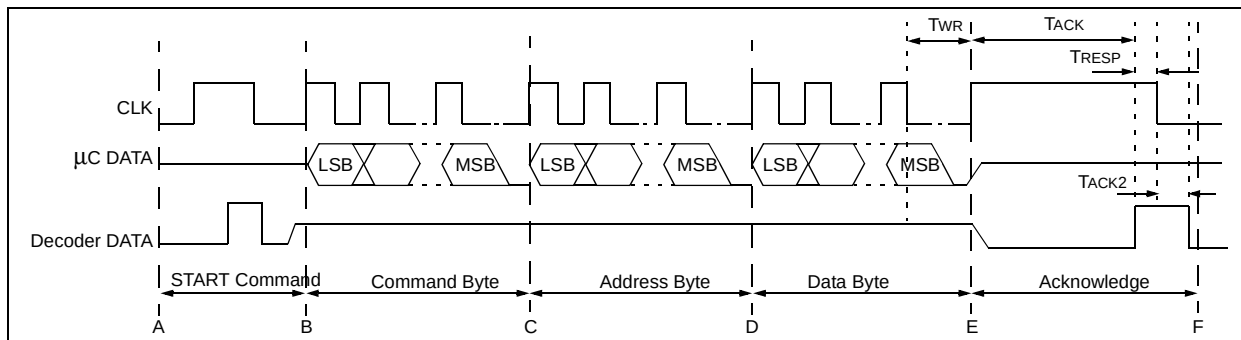


FIGURE 4-5: WRITE BYTES TO USER EEPROM

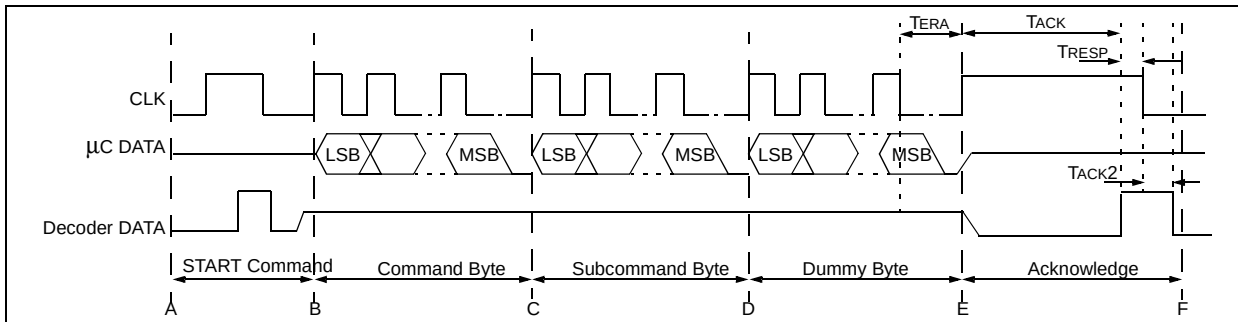


4.2.7 ERASE ALL

The erase all command (Figure 4-6) erases all the transmitters in the decoder. After the command and two dummy bytes are clocked in, the clock line must be

asserted to activate the command. After a successful completion of an erase all command, the data line is asserted until the clock line goes low.

FIGURE 4-6: ERASE ALL



4.2.8 ACTIVATE LEARN

The activate learn command (Figure 4-7) is used to activate a transmitter learning sequence on the decoder. The command consists of a Command mode activation sequence, a command byte, and two dummy bytes. The decoder will respond by taking the data line high to acknowledge that the command was valid and that learn is active.

Upon reception of the first transmission, the decoder will respond with a learn status message (Figure 4-8).

During learn, the decoder will acknowledge the reception of the first transmission by taking the data line high for 60 ms. The controlling microcontroller can clock out at most 8 bits, which will all be zeros. All of the bits of the status byte are zero, and this is used to distinguish between a learn time-out status string and the first transmission received string. The controlling microcontroller must ensure that the clock line does not go high 60 ms after the falling edge of the data line, for this will terminate learn.

Upon reception of the second transmission, the decoder will respond with a learn status message (Figure 4-9).

The learn status message after the second transmission consists of the following:

- 1 START bit.
- The function code [S3 : S0] of the message is zero, indicating that this is a status string.
- The RESULT bit indicates the result of the learn sequence. The RESULT bit is set if successful and cleared otherwise.
- The OVR bit will indicate whether an exiting transmitter is over written. The OVR bit will be set if an existing transmitter is learned over.
- The [CNT3...CNT0] bits will indicate the number of transmitters learned on the decoder.
- The [TX3...TX0] bits indicate the block number used during the learning of the transmitter.

FIGURE 4-7: LEARN MODE ACTIVATION

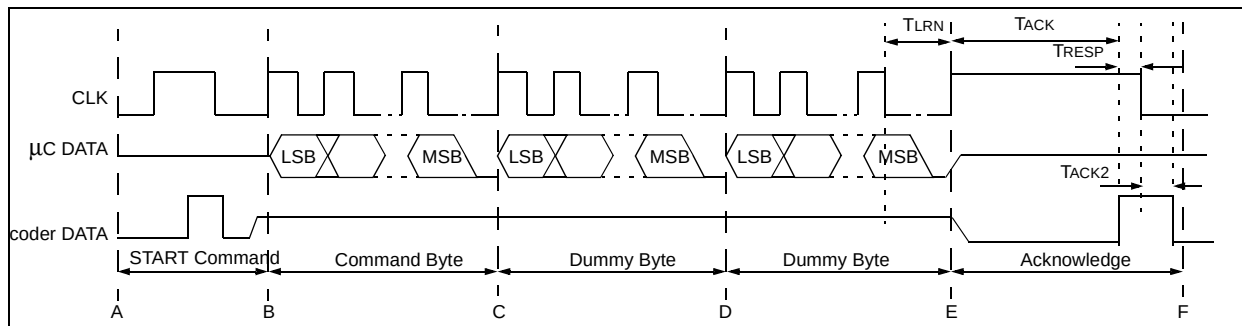
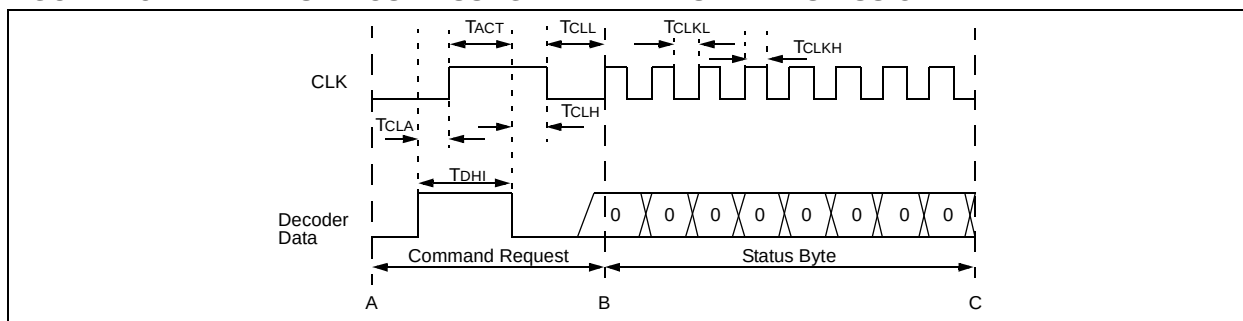
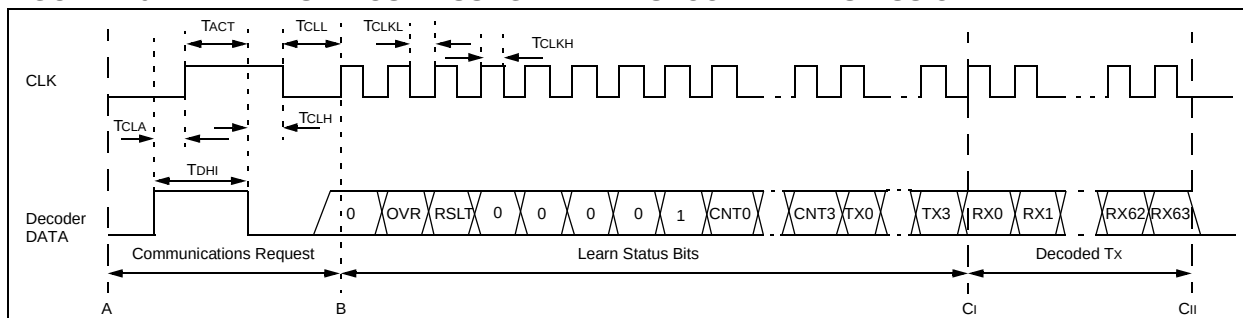


FIGURE 4-8: LEARN STATUS MESSAGE AFTER FIRST TRANSMISSION**FIGURE 4-9: LEARN STATUS MESSAGE AFTER SECOND TRANSMISSION**

4.3 Stand-Alone Mode

The HCS515 decoder can also be used in stand-alone applications. The HCS515 will activate the data line for up to 500 ms if a valid transmission was received, and this output can be used to drive a relay circuit. To activate learn or erase all commands, a button must be connected to the CLK input. User feedback is indicated on an LED connected to the S_DAT output line. If the CLK line is pulled high, using the learn button, the LED will switch on. After the CLK line is kept high for longer than 2 seconds, the decoder will switch the LED line off, indicating that learn will be entered if the button is released. If the CLK line is kept high for another 6 seconds, the decoder will activate an ERASE_ALL command.

Learn mode can be aborted by taking the clock line high until the data line goes high (LED switches on). During learn, the data line will give feedback to the user and, therefore, must not be connected to the relay drive circuitry.

Note: The Repeat bit must be cleared in the configuration byte in Stand-alone mode.

After taking the clock low and before a transmitter is learned, any low-to-high change on the clock line may terminate learn. This has learn implications when a switch with contact bounce is used.

4.4 Erase All Command and Erase Command

The Table 4-3 describes two versions of the Erase All command.

TABLE 4-3: ERASE ALL COMMAND

Command Byte	Subcommand Byte	Description
C3 HEX	00 HEX	Erase all transmitters.
C3 HEX	01 HEX	Erase all transmitters except 1. The first transmitter in memory is not erased.

Subcommand 01 can be used where a transmitter with permanent status is implemented in the microcontroller software. Use of subcommand 01 ensures that the permanent transmitter remains in memory even when all other transmitters are erased. The first transmitter learned after any of the following events is the first transmitter in memory and becomes the permanent transmitter:

1. Programming of the manufacturer's code.
2. Erasing of all transmitters (subcommand 00 only).

4.5 Test Mode

A special Test mode is activated after:

1. Programming of the manufacturer's code.
2. Erasing of all transmitters.

Test mode can be used to test a decoder before any transmitters are learned on it. Test mode enables testing of decoders without spending the time to learn a transmitter. Test mode is terminated after the first successful learning of an ordinary transmitter. In test mode, the decoder responds to a test transmitter. The test transmitter has the following properties:

1. Encoder decryption key = manufacturer's code.
2. Serial number = any value.
3. Discrimination bits = lower 10 bits of the serial number.

4. Synchronization counter value = any value (synchronization information is ignored).

Because the synchronization counter value is ignored in Test mode, any number of test transmitters can be used, even if their synchronization counter values are different.

4.6 Power Supply Supervisor

Reliable operation of the HCS515 requires that the contents of the EEPROM memory be protected against erroneous writes. To ensure that erroneous writes do not occur after supply voltage "brown-out" conditions, the use of a proper power supply supervisor device is imperative (Figure 4-11 and Figure 8-2).

FIGURE 4-10: STAND-ALONE MODE LEARN/ERASE-ALL TIMING

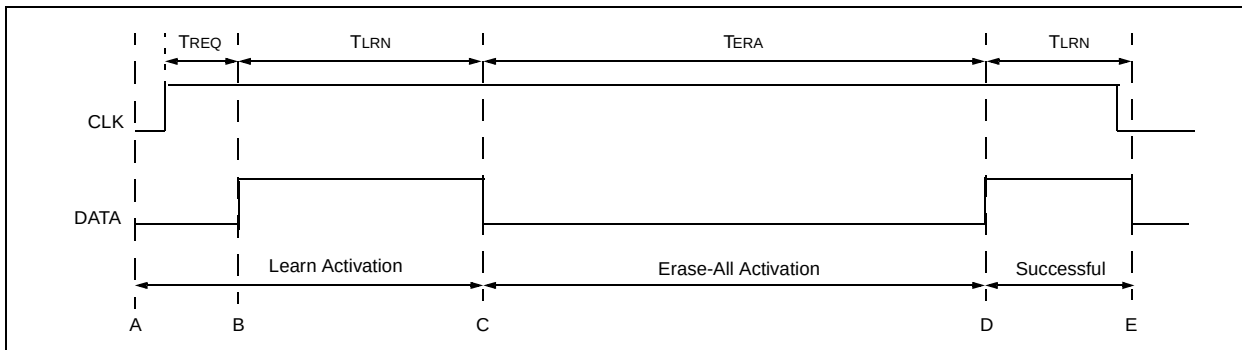
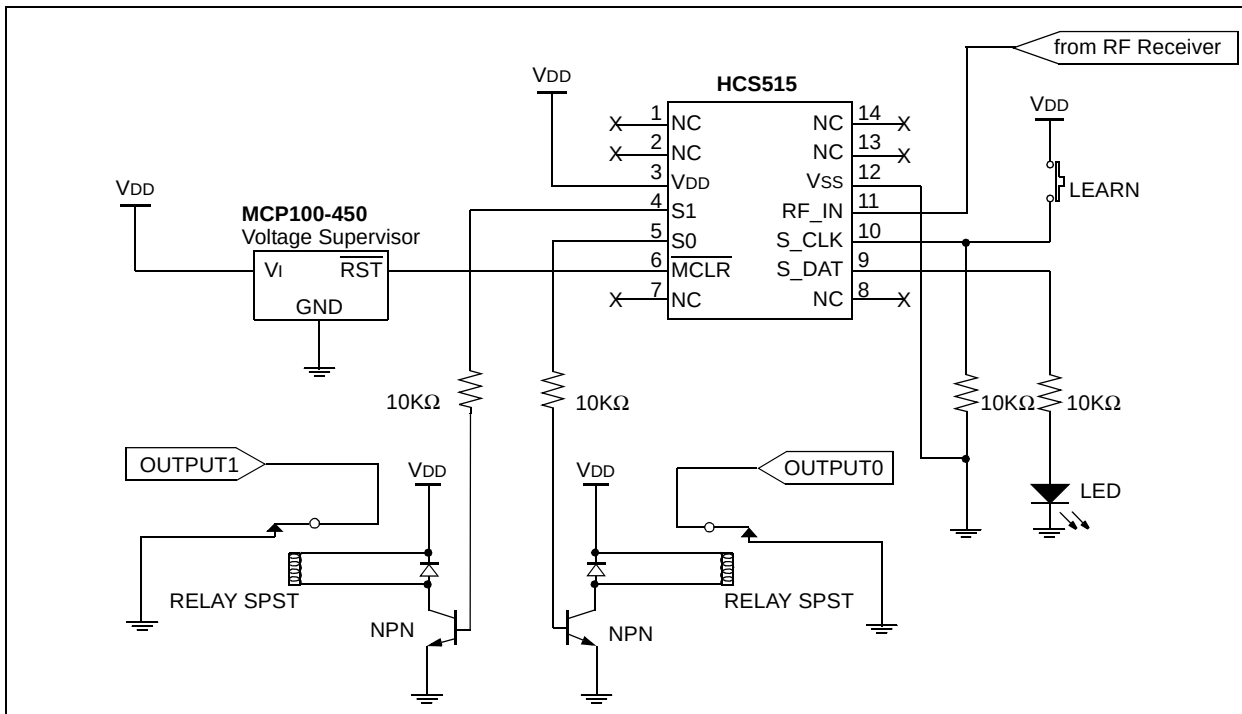


FIGURE 4-11: TYPICAL STAND-ALONE APPLICATION CIRCUIT



5.0 DECODER PROGRAMMING

The memory is divided between system memory that stores the transmitter information (read protected) and user memory (read/write). Commands to access the user memory are described in Sections 4.2.5 and 4.2.6.

The following information stored in system memory needs to be programmed before the decoder can be used:

- 64-bit manufacturer's code
- Decoder configuration byte

Note 1: These memory locations are read protected and can only be written to using the program command with the device powered up.

- 2:** The contents of the system memory is encrypted by a unique 64-bit key that is stored in the HCS515. To initialize the system memory, the HCS515's program command must be used.

5.1 Configuration Byte

The decoder is configured during initialization by setting the appropriate bits in the configuration byte. The following table list the options:

Bit	Mnemonic	Description
0	LRN_MODE	Learning mode selection LRN_MODE = 0 – Normal Learn LRN_MODE = 1 – Secure Learn
1	Not Used	Reserved
2	REPEAT	Repeat Transmission enable 0 = Disable 1 = Enabled
3	Not Used	Reserved
4	Not Used	Reserved
5	Not Used	Reserved
6	Not Used	Reserved
7	Not Used	Reserved

5.1.1 LRN_MODE

LRN_MODE selects between two learning modes. With LRN_MODE = 0, the Normal (serial number derived) mode is selected; with LRN_MODE = 1, the Secure (seed derived) mode is selected. See Section 6.0 for more detail on learning modes.

5.1.2 REPEAT

The HCS515 can be configured to indicate repeated transmissions. In a stand-alone configuration, repeated transmissions must be disabled.

5.2 Programming Waveform

The programming command consists of the following:

- Command Request Sequence (A to B)
- Command Byte (B to C)
- Configuration Byte (C to D)
- Manufacturer's Code Eight Data Bytes (D to G)
- Activation and Acknowledge Sequence (G to H)

5.3 Programming Data String

A total of 80 bits are clocked into the decoder. The 8-bit command byte is clocked in first, followed by the 8-bit configuration byte and the 64-bit manufacturer's code. The data must be clocked in Least Significant bit (LSb) first. The decoder will then encrypt the manufacturer's code using the decoder's unique 64-bit EEPROM encoder decryption key. After completion of the programming EEPROM, the decoder will acknowledge by taking the data line high (G to H). If the data line goes high within 30 ms after the clock goes high, programming also fails.

FIGURE 5-1: PROGRAMMING WAVEFORM

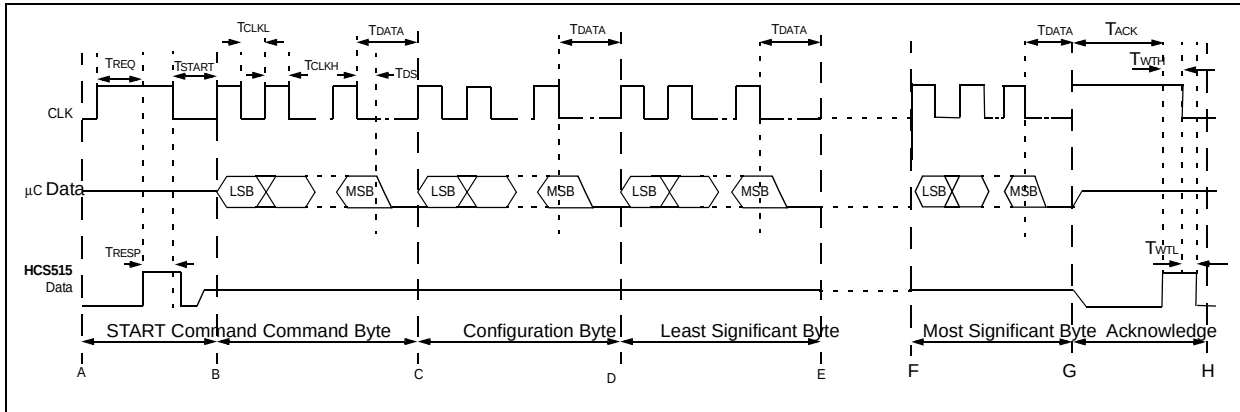


TABLE 5-1: PROGRAMMING COMMAND

Symbol	Parameters	Sugg. Value	Min.	Max.	Units
TREQ	Command request time	d.o.d.	0.005	500	ms
TRESP	Acknowledge time	100	10	1000	µs
TSTART	Command request to first command bit	100	20	1000	µs
TCLKH	Clock high time	100	20	1000	µs
TCLKL	Clock low time	100	20	1000	µs
TDS	Data hold time	50	14	1000	µs
TDATA	Command last bit to data first bit	100	10	1000	µs
TACK	Command acknowledge time	d.o.d.	30	240	ms
TWTH	Acknowledge respond time	100	20	1000	µs
TWTL	Clock low to next command	100	10	—	µs

Note: d.o.d. - depends on decoder status
These parameters are characterized but not tested

6.0 KEY GENERATION

The HCS515 supports two learning schemes which are selected during the initialization of the system EEPROM. The learning schemes are:

- Normal learn using the KEELOQ decryption algorithm
- Secure learn using the KEELOQ decryption algorithm

6.1 Normal (Serial Number derived) Learn using the Decryption Algorithm

This learning scheme uses the KEELOQ decryption algorithm and the 28-bit serial number of the transmitter to derive the encoder decryption key. The 28-bit serial number is patched with predefined values as indicated below to form two 32-bit seeds.

$$\begin{aligned}\text{SourceH} &= 60000000\ 00000000\text{H} + \text{Serial Number} \mid_{28\text{ bits}} \\ \text{SourceL} &= 20000000\ 00000000\text{H} + \text{Serial Number} \mid_{28\text{ bits}}\end{aligned}$$

Then, using the KEELOQ decryption algorithm and the manufacturer's code the encoder decryption key is derived as follows:

$$\begin{aligned}\text{KeyH}_{\text{Upper 32 bits}} &= F_{\text{KEELOQ Decryption}}(\text{SourceH}) \mid_{64\text{-bit Manufacturer's Code}} \\ \text{KeyL}_{\text{Lower 32 bits}} &= F_{\text{KEELOQ Decryption}}(\text{SourceL}) \mid_{64\text{-bit Manufacturer's Code}}\end{aligned}$$

6.2 Secure (Seed Derived) Learn using the Decryption Algorithm

This scheme uses the secure seed transmitted by the encoder to derive the two input seeds. The decoder always uses the lower 64 bits of the transmission to form a 60-bit seed. The upper 4 bits are always forced to zero.

For 32-bit seed encoders:

$$\begin{aligned}\text{SourceH} &= \text{Serial Number}_{\text{Lower 28 bits}} \\ \text{SourceL} &= \text{Seed}_{32\text{ bits}}\end{aligned}$$

For 48-bit seed encoders:

$$\begin{aligned}\text{SourceH} &= \text{Seed}_{\text{Upper 16 bits}} + \text{Serial Number}_{\text{Upper 16 bits (with upper 4 bits set to zero)}} \ll 16 \\ \text{SourceL} &= \text{Seed}_{\text{Lower 32 bits}}\end{aligned}$$

For 60-bit seed encoders:

$$\begin{aligned}\text{SourceH} &= \text{Seed}_{\text{Upper 28 bits with upper 4 bits set to zero}} \\ \text{SourceL} &= \text{Seed}_{\text{Lower 32 bits}}\end{aligned}$$

The KEELOQ decryption algorithm and the manufacturer's code is used to derive the encoder decryption key as follows:

$$\begin{aligned}\text{KeyH}_{\text{Upper 32 bits}} &= \text{Decrypt}(\text{SourceH})_{64\text{-bit Manufacturer's Code}} \\ \text{KeyL}_{\text{Lower 32 bits}} &= \text{Decrypt}(\text{SourceL})_{64\text{-bit Manufacturer's Code}}\end{aligned}$$

7.0 ENCODERS

7.1 Transmission Format (PWM)

The encoder transmission is made up of several parts (Figure 7-1). Each transmission begins with a preamble and a header, followed by the encrypted and then the fixed data. The actual data is 66/69 bits, which consist of 32 bits of encrypted data and 34/37 bits of non-encrypted data. Each transmission is followed by a guard period before another transmission can begin. The code hopping portion provides up to four billion changing code combinations and includes the button status bits (based on which buttons were activated), along with the synchronization counter value and some discrimination bits. The non-code hopping portion is comprised of the status bits, the function bits, and the 28-bit serial number. The encrypted and non-encrypted combined sections increase the number of combinations to 7.38×10^{19} .

7.2 Code Word Organization

The HCS encoder transmits a 66/69-bit code word when a button is pressed. The 66/69-bit word is constructed from a code hopping portion and a non-code hopping portion (Figure 7-2).

The **Encrypted Data** is generated from four button bits, two overflow counter bits, ten discrimination bits, and the 16-bit synchronization counter value.

The **Non-encrypted Data** is made up from 2 status bits, 4 function bits, and the 28/32-bit serial number.

FIGURE 7-1: TRANSMISSION FORMAT (PWM)

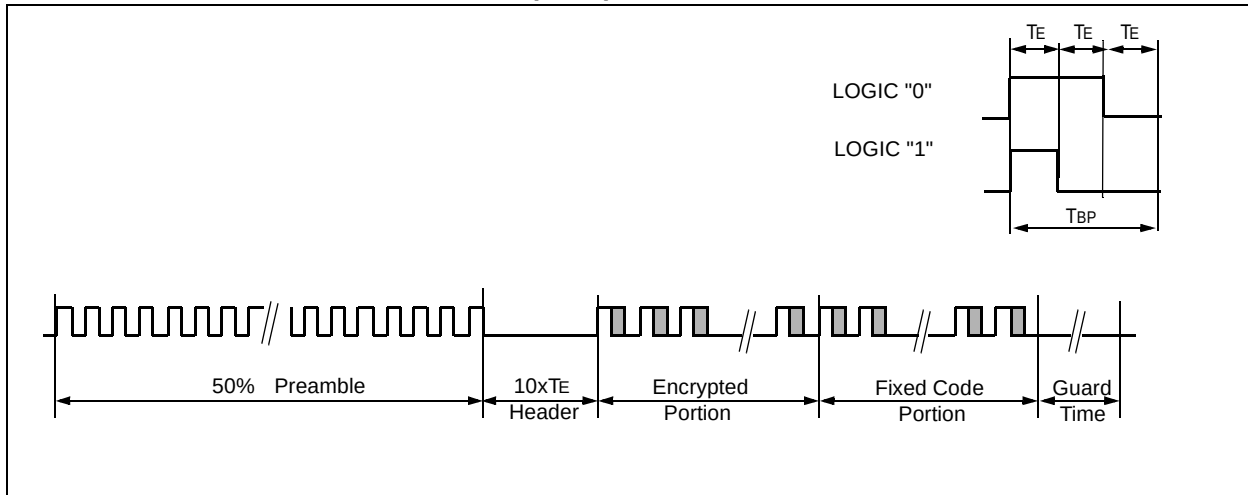
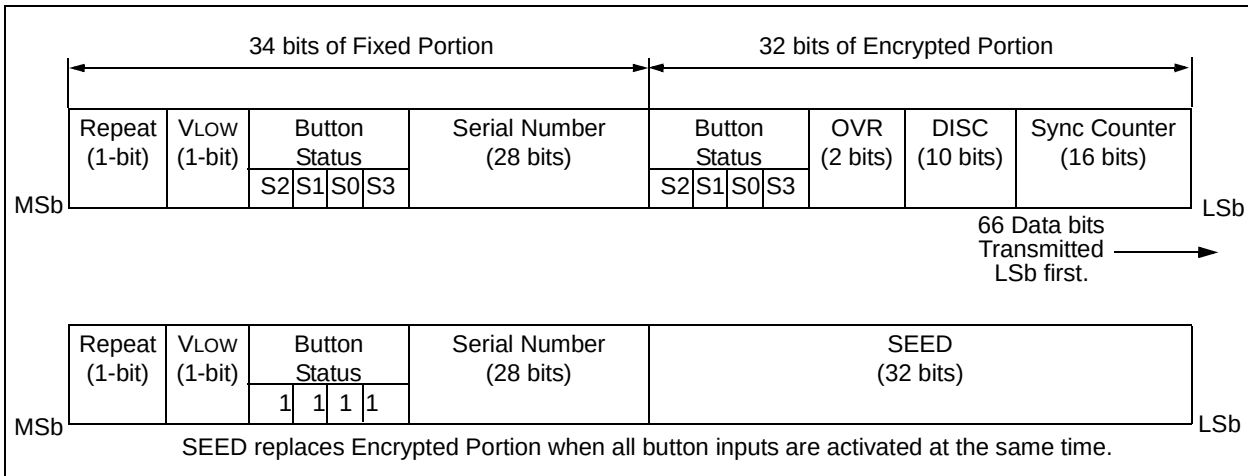


FIGURE 7-2: CODE WORD ORGANIZATION



8.0 ELECTRICAL CHARACTERISTICS FOR HCS515

Absolute Maximum Ratings[†]

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to Vss (except VDD)	-0.6V to VDD +0.6V
Voltage on VDD with respect to Vss	0 to +7.0V
Total power dissipation (Note)	700 mW
Maximum current out of Vss pin	200 mA
Maximum current into VDD pin	150 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > VDD)	± 20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > VDD)	± 20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA

Note: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

[†] **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 8-1: DC CHARACTERISTICS

		Standard Operating Conditions (unless otherwise stated)				
		Operating temperature				
		Commercial (C): 0°C ≤ TA ≤ +70°C				
		Industrial (I): -40°C ≤ TA ≤ +85°C				
Symbol	Parameters	Min.	Typ. ^(†)	Max.	Units	Conditions
VDD	Supply voltage	4.5	—	5.5	V	—
VPOR	VDD start voltage to ensure RESET	—	VSS	—	V	—
SVDD	VDD rise rate to ensure RESET	0.05*	—	—	V/ms	—
IDD	Supply current	—	1.8	2.	mA	FOSC = 4 MHz, VDD = 5.5V
IPD	Power-Down Current	—	10	50	μA	VDD = 4.5V
VIL	Input low voltage	VSS	—	—	V	MCLR = .2 VDD
		VSS	—	0.8	V	VDD between 4.5V and 5.5V
VIH	Input high voltage	0.25 VDD + 0.8	—	VDD	V	VDD between 4.5V and 5.5V
					V	Except MCLR = 0.80 VDD
VOL	Output low voltage	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
VOH	Output high voltage	VDD - 0.7	—	—	V	IOH = -3 mA, VDD = 4.5V

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

* These parameters are characterized but not tested.

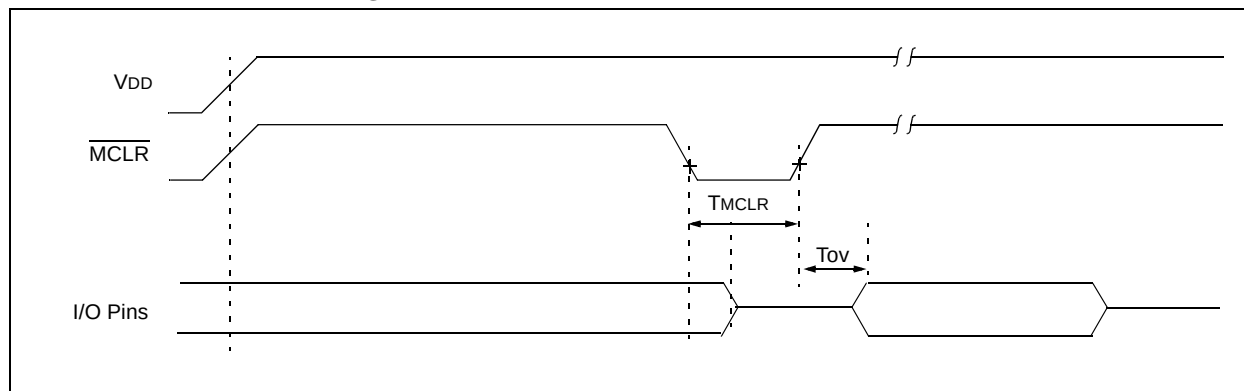
Note: Negative current is defined as coming out of the pin.

TABLE 8-2: AC CHARACTERISTICS

		Standard Operating Conditions (unless otherwise specified):				
		Commercial (C): 0°C ≤ TA ≤ +70°C				
		Industrial (I): -40°C ≤ TA ≤ +85°C				
Symbol	Parameters	Min.	Typ.	Max.	Units	Conditions
TE	Transmit elemental period	65	—	660	μs	—
TOD	Output delay	48	75	237	ms	—
TMCLR	MCLR low time	150	—	—	ns	—
TOV	Time output valid	—	150	222	ms	—

Note: These parameters are characterized but not tested.

FIGURE 8-1: RESET WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



8.1 AC Electrical Characteristics

8.1.1 VALID TRANSMISSION NOTIFICATION

		Standard Operating Conditions (unless otherwise specified) Commercial (C): $0^{\circ}\text{C} \leq \text{TA} \leq +70^{\circ}\text{C}$ Industrial (I): $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$			
Symbol	Parameters	Min.	Typ.	Max.	Units
TDHI	Command request time	0.0050	—	500	ms
TCLA	Micro request acknowledge time	0.0050	—	1	ms
TACK	Decoder Acknowledge time	—	—	4	μs
TACT	Start Command mode to first command bit	20	—	1200	μs
TCLKH	Clock high time	20	—	1000	μs
TCLKL	Clock low time	20	—	1000	μs
FCLK	Clock frequency	500	—	25000	Hz
TDS	Data hold time	14	—	1000	μs

Note: These parameters are characterized but not tested.

8.1.2 COMMAND MODE ACTIVATION

		Standard Operating Conditions (unless otherwise specified): Commercial (C): $0^{\circ}\text{C} \leq \text{TA} \leq +70^{\circ}\text{C}$ Industrial (I): $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$			
Symbol	Parameters	Min.	Typ.	Max.	Units
TREQ	Command request time	0.0050	—	500	ms
TRESP	Microcontroller request acknowledge time	—	—	1	ms
TACK	Decoder acknowledge time	—	—	4	μs
TSTART	Start Command mode to first command bit	20	—	1000	μs
TCLKH	Clock high time	20	—	1000	μs
TCLKL	Clock low time	20	—	1000	μs
FCLK	Clock frequency	500	—	25000	Hz
TDS	Data hold time	14	—	—	μs
TCMD	Command validate time	—	—	10	μs
TADDR	Address validate time	—	—	10	μs
TDATA	Data validate time	—	—	10	μs

Note: These parameters are characterized but not tested.

8.1.3 READ FROM USER EEPROM COMMAND

		Standard Operating Conditions (unless otherwise specified): Commercial (C): $0^{\circ}\text{C} \leq \text{TA} \leq +70^{\circ}\text{C}$ Industrial (I): $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$			
Symbol	Parameters	Min.	Typ.	Max.	Units
TRD	Decoder EEPROM read time	1000	—	2000	μs

Note: These parameters are characterized but not tested.

8.1.4 WRITE TO USER EEPROM COMMAND

		Standard Operating Conditions (unless otherwise specified): Commercial (C): 0°C ≤ TA ≤ +70°C Industrial (I): -40°C ≤ TA ≤ +85°C			
Symbol	Parameters	Min.	Typ.	Max.	Units
TWR	Write command activation time	20	—	1000	μs
TACK	EEPROM write acknowledge time	—	—	10	ms
TRESP	Microcontroller acknowledge response time	20	—	1000	μs
TACK2	Decoder response acknowledge time	—	—	10	μs

Note: These parameters are characterized but not tested.

8.1.5 ERASE ALL COMMAND

		Standard Operating Conditions (unless otherwise specified): Commercial (C): 0°C ≤ TA ≤ +70°C Industrial (I): -40°C ≤ TA ≤ +85°C			
Symbol	Parameters	Min.	Typ.	Max.	Units
TERA	Learn command activation time	20	—	1000	μs
TACK	Decoder acknowledge time	20	—	210	ms
TRESP	Microcontroller acknowledge response time	20	—	1000	μs
TACK2	Decoder data line low	—	—	10	μs

Note: These parameters are characterized but not tested.

8.1.6 ACTIVATE LEARN COMMAND IN MICRO MODE

		Standard Operating Conditions (unless otherwise specified): Commercial (C): 0°C ≤ TA ≤ +70 °C Industrial (I): -40°C ≤ TA ≤ +85°C			
Symbol	Parameters	Min.	Typ.	Max.	Units
TLRN	Learn command activation time	20	—	1000	μs
TACK	Decoder acknowledge time	—	—	20	μs
TRESP	Microcontroller acknowledge response time	20	—	1000	μs
TACK2	Decoder data line low	—	—	10	μs

Note: These parameters are characterized but not tested.

8.1.7 ACTIVATE LEARN COMMAND IN STAND-ALONE MODE

		Standard Operating Conditions (unless otherwise specified): Commercial (C): 0°C ≤ TA ≤ +70°C Industrial (I): -40°C ≤ TA ≤ +85°C			
Symbol	Parameters	Min.	Typ.	Max.	Units
TREQ	Command request time	—	—	100	ms
TLRN	Learn command activation time	—	—	2	s
TERA	Erase-all command activation time	—	—	6	s

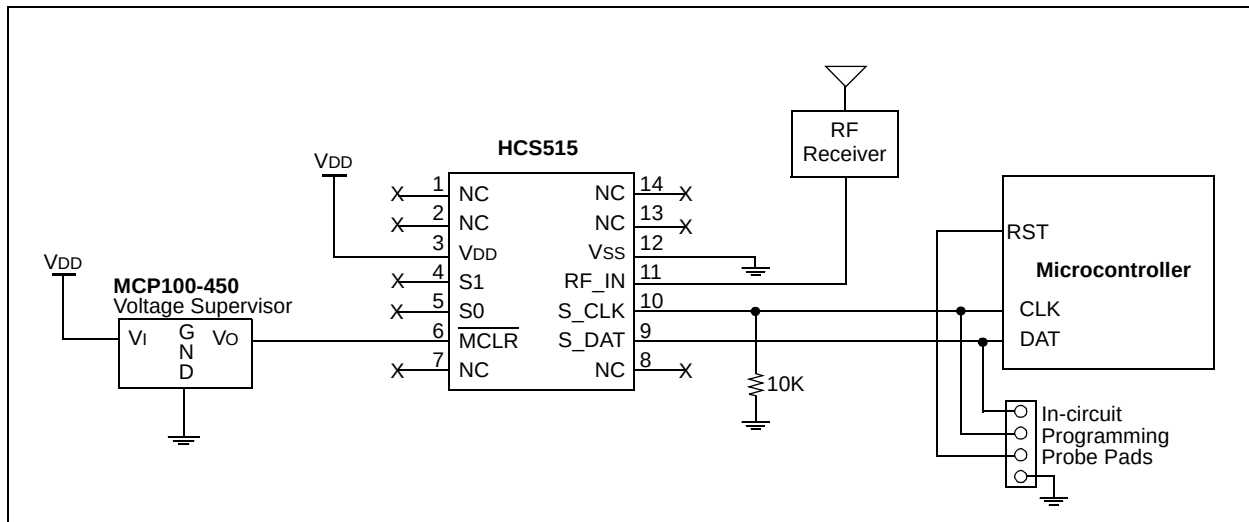
Note: These parameters are characterized but not tested.

8.1.8 LEARN STATUS STRING

		Standard Operating Conditions (unless otherwise specified):			
		Commercial (C): 0°C ≤ TA ≤ +70°C			
		Industrial (I): -40°C ≤ TA ≤ +85°C			
Symbol	Parameters	Min.	Typ.	Max.	Units
TDHI	Command request time	—	—	500	ms
TCLA	Microcontroller command request time	0.005	—	500	ms
TACT	Decoder request acknowledge time	—	—	10	μs
TCLH	Clock high hold time			1.2	ms
TCLL	Clock low hold time	0.020	—	1.2	ms
TCLKH	Clock high time	20	—	1000	μs
TCLKL	Clock low time	20	—	1000	μs
FCLK	Clock frequency	500	—	25000	Hz
TDS	Data hold time	—	—	5	μs

Note: These parameters are characterized but not tested.

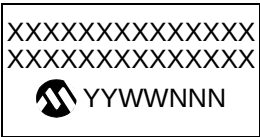
FIGURE 8-2: TYPICAL MICROCONTROLLER INTERFACE CIRCUIT



9.0 PACKAGING INFORMATION

9.1 Package Marking Information

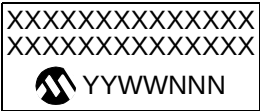
14-Lead PDIP (300 mil)



Example



14-Lead SOIC 150 mil)



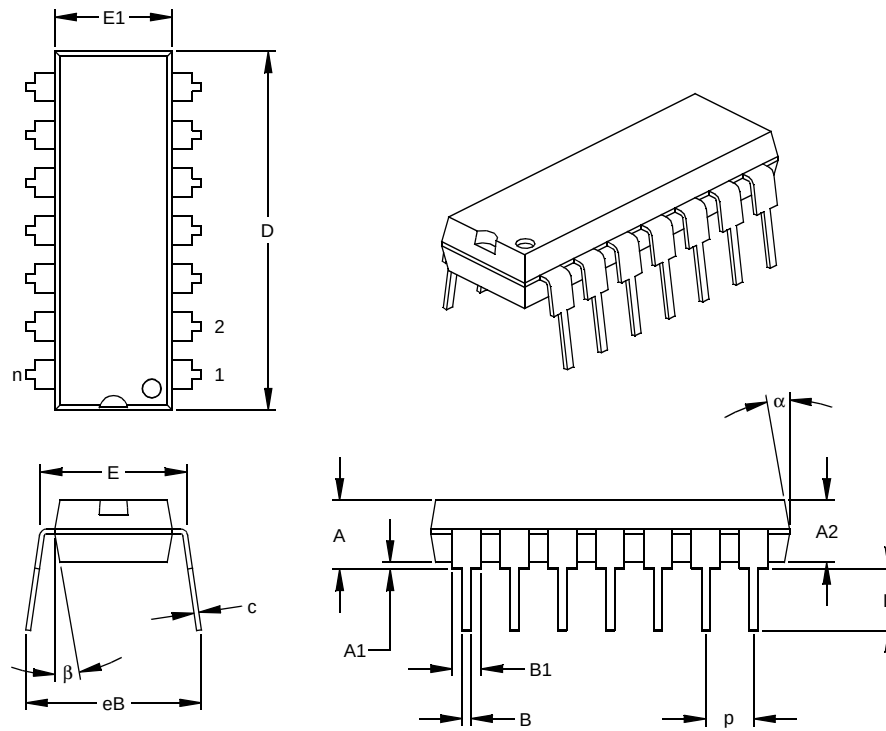
Example



Legend:	XX...X Customer specific information*
	YY Year code (last 2 digits of calendar year)
	WW Week code (week of January 1 is week '01')
	NNN Alphanumeric traceability code
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

* Standard OTP marking consists of Microchip part number, year code, week code, and traceability code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



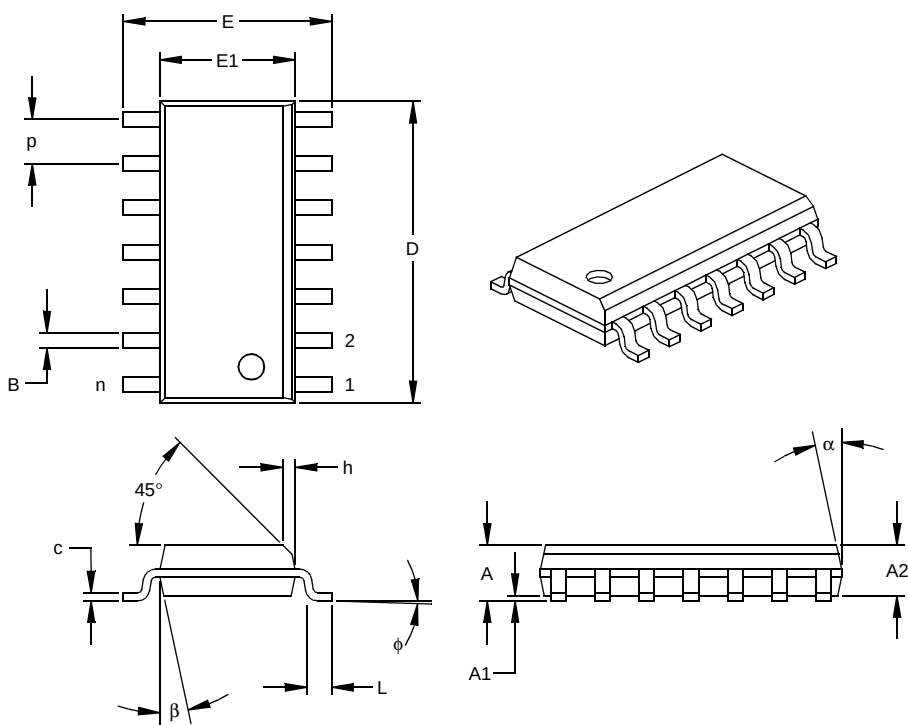
UNITS		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
 § Significant Characteristic

Notes:
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
 JEDEC Equivalent: MS-001
 Drawing No. C04-005

HCS515

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)



UNITS		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-065

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HCS515 — /P	Package:		P = Plastic DIP (300 mil Body), 14-lead
			SL = Plastic SOIC (150 mil Body), 14-lead
	Temperature Range:		Blank = 0°C to +70°C I = -40°C to +85°C
	Device:		HCS515 Code Hopping Decoder
			HCS515T Code Hopping Decoder (Tape and Reel)

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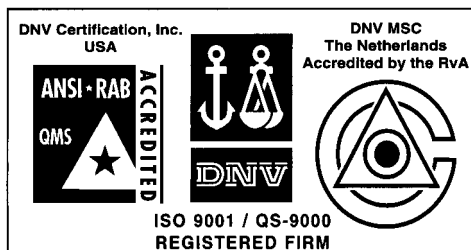
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Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing

Microchip Technology Consulting (Shanghai)
Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu

Microchip Technology Consulting (Shanghai)
Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-6766200 Fax: 86-28-6766599

China - Fuzhou

Microchip Technology Consulting (Shanghai)
Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Shanghai

Microchip Technology Consulting (Shanghai)
Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen

Microchip Technology Consulting (Shanghai)
Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

Hong Kong

Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessy Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan

Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark

Microchip Technology Nordic ApS
Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy

Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

01/18/02