HCPL-J314

0.6 Amp Output Current IGBT Gate Drive Optocoupler

AVAGO TECHNOLOGIES

Data Sheet

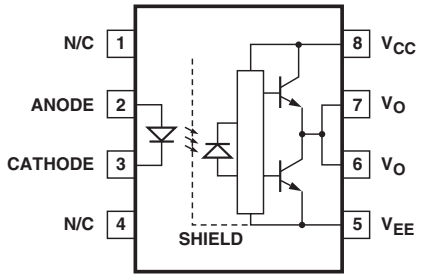
Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The HCPL-J314 family of devices consists of an AlGaAs LED optically coupled to an integrated circuit with a power output stage. These optocouplers are ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by this optocoupler makes it ideally suited for directly driving small or medium power IGBTs. For IGBTs with higher ratings the HCPL-3150 (0.6 A) or HCPL-3120 (2.5 A) optocouplers can be used.

Functional Diagram



HCPL-J314

Truth Table

LED	V_O
OFF	LOW
ON	HIGH

A 0.1 µF bypass capacitor must be connected between pins V_{CC} and V_{EE}.

Features

- 0.6 A maximum peak output current
- 0.4 A minimum peak output current
- High speed response:
  0.7 µs max. propagation delay over temperature range
- Ultra high CMR: min. 25 kV/µs at V_{CM} = 1.5 kV
- Bootstrappable supply current: max. 3 mA
- Wide operating temperature range: -40°C to 100°C
- Wide V_{CC} operating range: 10 V to 30 V over temperature range
- Available in DIP8 (single) and SO16 (dual) package
- Safety approvals: UL Recognized, 3750 Vrms for 1 minute. CSA Approval IEC/EN/DIN EN 60747-5-2 Approval. V_{IORM} = 891 V_{peak}

Applications

- Isolated IGBT/Power MOSFET gate drive
- AC and brushless DC motor drives
- Inverters for appliances
- Industrial inverters
- Switch Mode Power Supplies (SMPS)
- Uninterruptable Power Supplies (UPS)

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Selection Guide

Package Type	Part Number	Number of Channels
8-pin DIP (300 Mil)	HCPL-J314	1
SO16	HCPL-314J	2

Note: Please refer to HCPL-314J datasheet for more details

Ordering Information

HCPL-J314 is UL Recognized with 3750 Vrms for 1 minute per UL1577.

Part Number	Option		Package	Surface Mount	Gull Wing	Tape & Reel	IEC/EN/DIN EN 60747-5-2	Quantity
	RoHS Compliant	Non RoHS Compliant						
HCPL-J314	-000E	No option	300mil DIP-8				X	50 per tube
	-300E	#300		X	X		X	50 per tube
	-500E	#500		X	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1: HCPL-J314-500E to order product of 300 mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval in RoHS compliant.

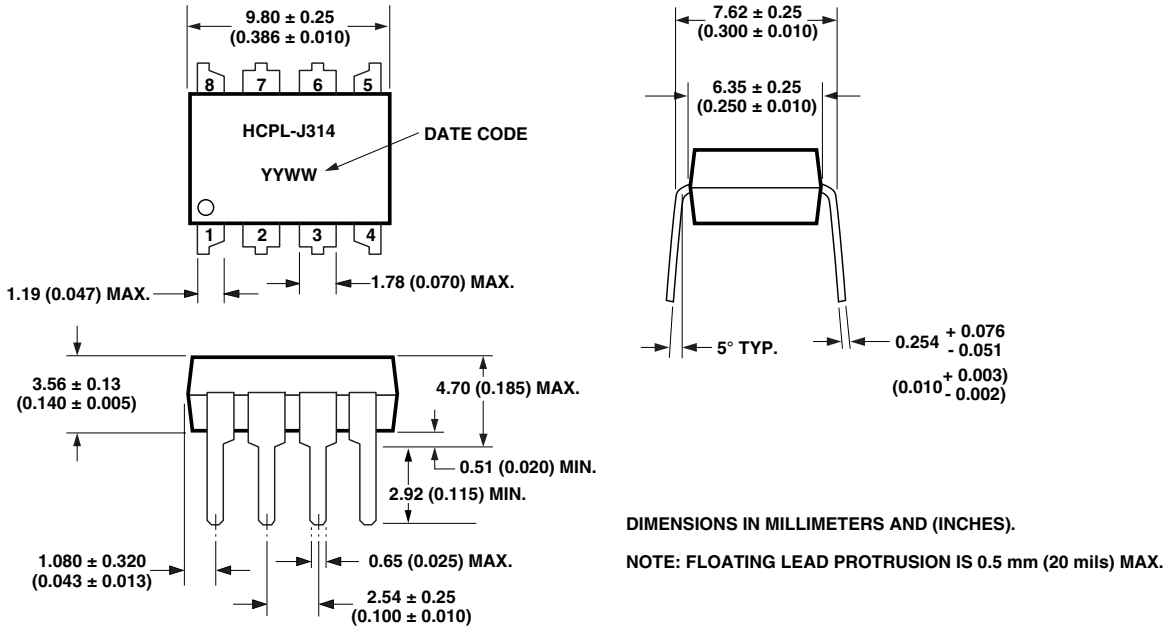
Example 2: HCPL-J314 to order product of 300 mil DIP package in tube packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval and non RoHS complaint

Option data sheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

HCPL-J314 Package Outline Drawings

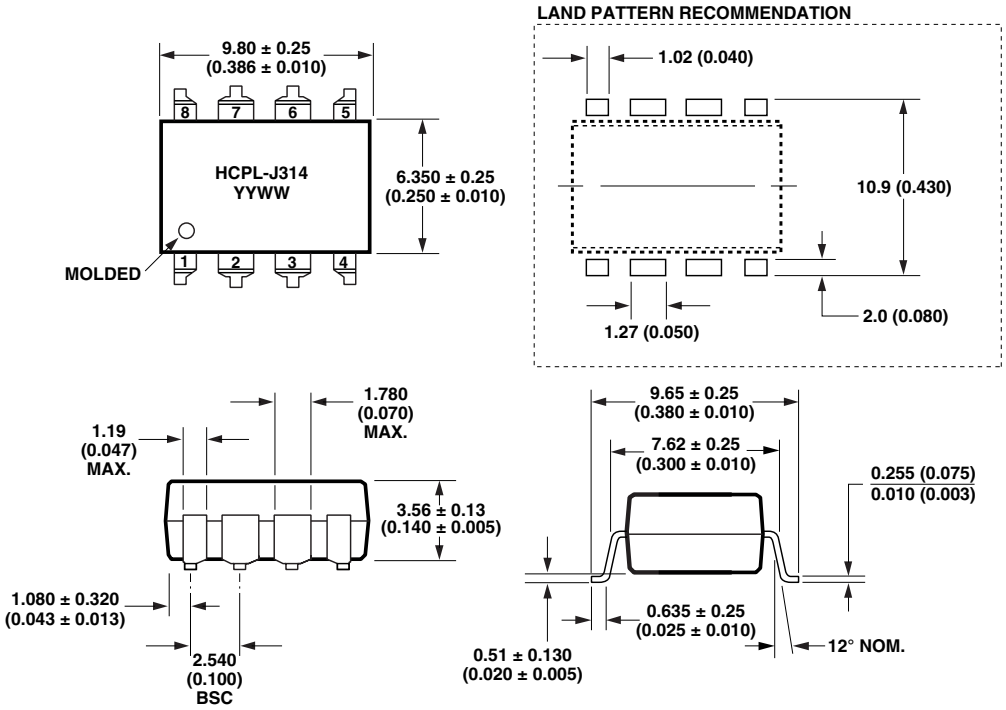
Standard DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

Gull Wing Surface Mount Option 300

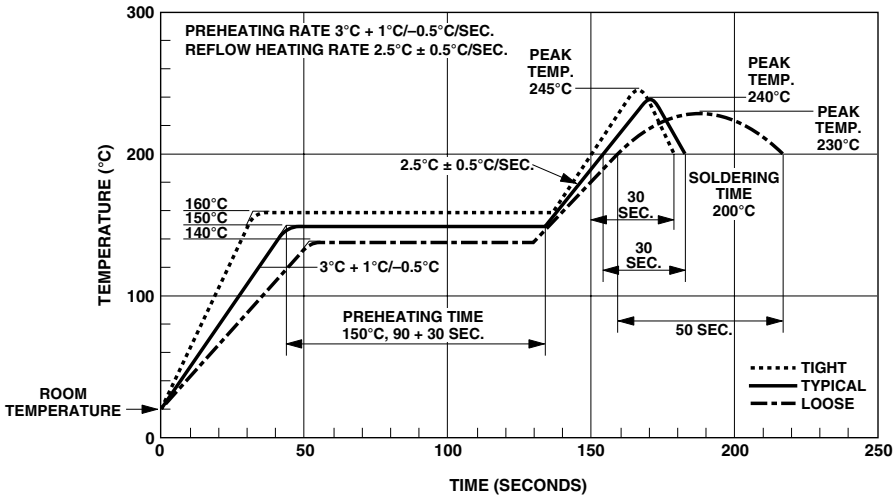


DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

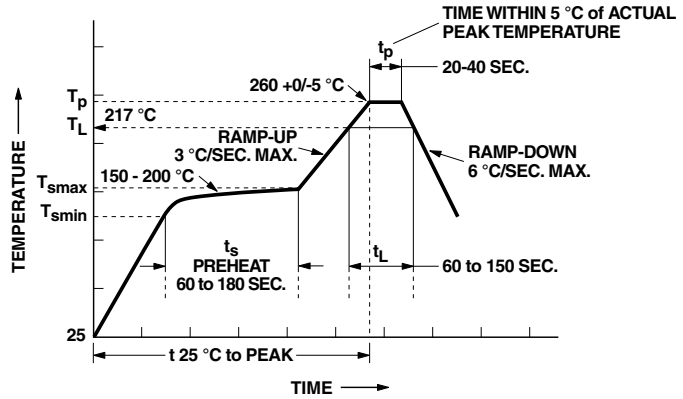
NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

Solder Reflow Temperature Profile



Note: Non-halide flux should be used.

Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

Note: Non-halide flux should be used.

Regulatory Information

The HCPL-J314 has been approved by the following organizations:

IEC/EN/DIN EN 60747-5-2

Approved under:
IEC 60747-5-2:1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01

UL

Approval under UL 1577, component recognition program up to V_{ISO} = 3750 Vrms. File E55361.

CSA

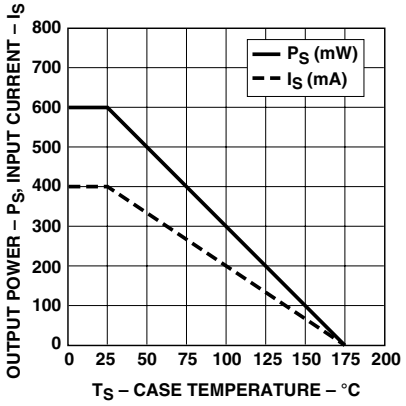
Approved under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-2 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 150 V_{rms}		I - IV	
for rated mains voltage ≤ 300 V_{rms}		I - IV	
for rated mains voltage ≤ 600 V_{rms}		I - III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	891	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	1670	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and Sample Test, t_m = 60 sec, Partial discharge < 5 pC	V_{PR}	1336	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 10 sec)	V_{IOTM}	6000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current**	$I_{S,INPUT}$	400	mA
Output Power**	$P_{S, OUTPUT}$	1200	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

*Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, IEC/EN/DIN EN 60747-5-2 for a detailed description of Method a and Method b partial discharge test profiles.

** Refer to the following figure for dependence of P_S and I_S on ambient temperature.



Insulation and Safety Related Specifications

Parameter	Symbol	HCPL-J314	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.4	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	100	°C	
Average Input Current	$I_{F(AVG)}$		25	mA	1
Peak Transient Input Current (<1 µs pulse width, 300pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	V_R		5	V	
"High" Peak Output Current	$I_{OH(PEAK)}$		0.6	A	2
"Low" Peak Output Current	$I_{OL(PEAK)}$		0.6	A	2
Supply Voltage	V_{CC} - V_{EE}	-0.5	35	V	
Output Voltage	$V_{O(PEAK)}$	-0.5	V_{CC}	V	
Output Power Dissipation	P_O		260	mW	3
Input Power Dissipation	P_I		105	mW	4
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Package Outline Drawings section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Power Supply	V_{CC} - V_{EE}	10	30	V	
Input Current (ON)	$I_{F(ON)}$	8	12	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	-3.6	0.8	V	
Operating Temperature	T_A	-40	100	°C	

Electrical Specifications (DC)

Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}	0.2			A	$V_O = V_{CC} - 4$	2	5
		0.4	0.5			$V_O = V_{CC} - 10$	3	2
Low Level Output Current	I_{OL}	0.2	0.4		A	$V_O = V_{EE} + 2.5$	5	5
		0.4	0.5			$V_O = V_{EE}+10$	6	2
High Level Output Voltage	V_{OH}	V_{CC}-4	V_{CC}-1.8		V	I_O = -100 mA	1	6,7
Low Level Output Voltage	V_{OL}		0.4	1	V	I_O = 100 mA	4	
High Level Supply Current	I_{CCH}		0.7	3	mA	I_O = 0 mA	7,8	14
Low Level Supply Current	I_{CCL}		1.2	3	mA	I_O = 0 mA		
Threshold Input Current Low to High	I_{FLH}			6	mA	I_O = 0 mA, V_O > 5 V	9,15	
Threshold Input Voltage Low to High	V_{FHL}	0.8			V			
Input Forward Voltage	V_F	1.2	1.5	1.8	V	I_F = 10 mA	16	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$		-1.6		mV/°C			
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA		
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V		

Switching Specifications (AC)

Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	0.1	0.2	0.7	µs	Rg = 47 Ω, Cg = 3 nF, f = 10 kHz, Duty Cycle = 50%, I_F = 8 mA, V_{CC} = 30 V	10,11, 12,13, 14,17	14
Propagation Delay Time to Low Output Level	t_{PHL}	0.1	0.3	0.7	µs			
Propagation Delay Difference Between Any Two Parts or Channels	PDD	-0.5		0.5	µs			10
Rise Time	t_R		50		ns			
Fall Time	t_F		50		ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	25	35		kV/µs	T_A = 25°C, V_{CM} = 1.5 kV	18	11
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	25	35		kV/µs		18	12

Package Characteristics

For each channel unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	3750			Vrms	T_A = 25°C, RH < 50% for 1 min.		8,9
Output-Output Momentary Withstand Voltage	V_{O-O}	1500			Vrms			15
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		9
Input-Output Capacitance	C_{I-O}		1.2		pF	Freq = 1 MHz		

Notes:

1. Derate linearly above 70°C free air temperature at a rate of 0.3 mA/°C.
2. Maximum pulse width = 10 µs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 0.4 A. See Application section for additional details on limiting I_{OL} peak.
3. Derate linearly above 85°C, free air temperature at the rate of 4.0 mW/°C.
4. Input power dissipation does not require derating.
5. Maximum pulse width = 50 µs, maximum duty cycle = 0.5%.
6. In this test, V_{OH} is measured with a DC load current. When driving capacitive load V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
7. Maximum pulse width = 1 ms, maximum duty cycle = 20%.
8. In accordance with UL 1577, each HCPL-J314 optocoupler is proof tested by applying an insulation test voltage ≥ 5000 Vrms for 1 second (leakage detection current limit I_{I-O} ≤ 5 µA). This test is performed before 100% production test for partial discharge (method B) shown in the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table, if applicable.
9. Device considered a two-terminal device: pins on input side shorted together and pins on output side shorted together.
10. PDD is the difference between t_{PHL} and t_{PLH} between any two parts or channels under the same test conditions.
11. Common mode transient immunity in the high state is the maximum tolerable |dVcm/dt| of the common mode pulse V_{CM} to assure that the output will remain in the high state (i.e. Vo > 6.0 V).
12. Common mode transient immunity in a low state is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e. Vo < 1.0 V).
13. This load condition approximates the gate load of a 1200 V/25 A IGBT.
14. For each channel. The power supply current increases when operating frequency and Qg of the driven IGBT increases.
15. Device considered a two terminal device: Channel one output side pins shorted together, and channel two output side pins shorted together.

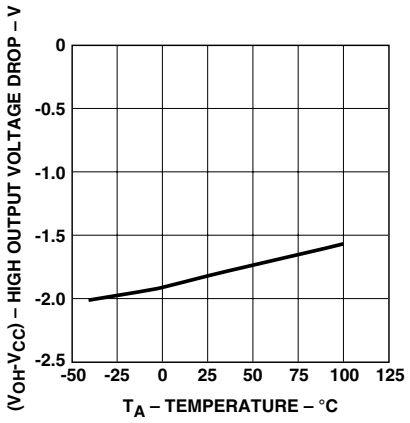


Figure 1. V_{OH} vs. temperature.

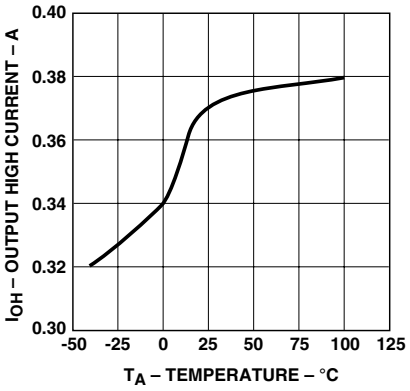


Figure 2. I_{OH} vs. temperature.

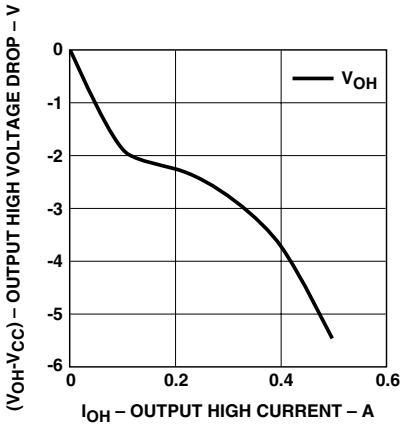


Figure 3. V_{OH} vs. I_{OH}.

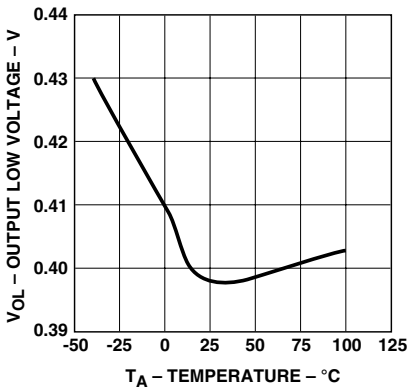


Figure 4. V_{OL} vs. temperature.

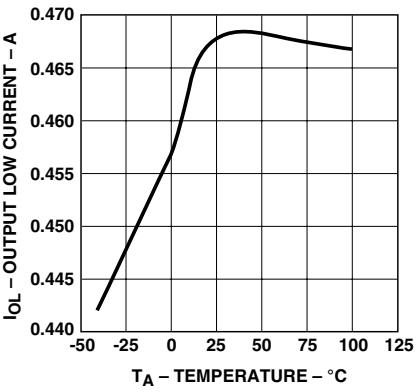


Figure 5. I_{OL} vs. temperature.

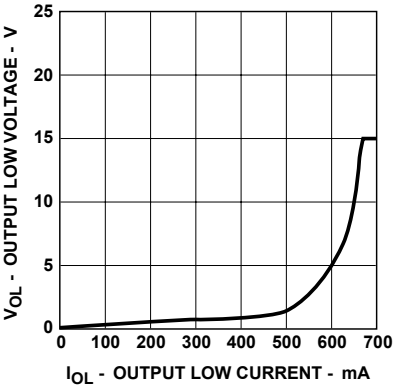


Figure 6. V_{OL} vs. I_{OL}.

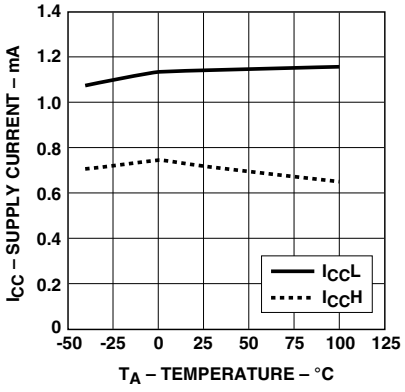


Figure 7. I_{CC} vs. temperature.

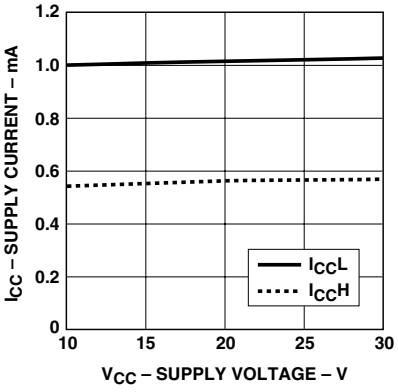


Figure 8. I_{CC} vs. V_{CC}.

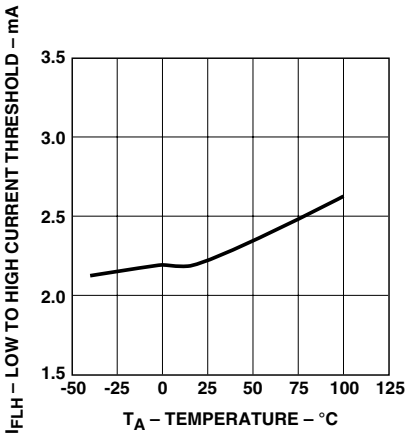


Figure 9. I_{FLH} vs. temperature.

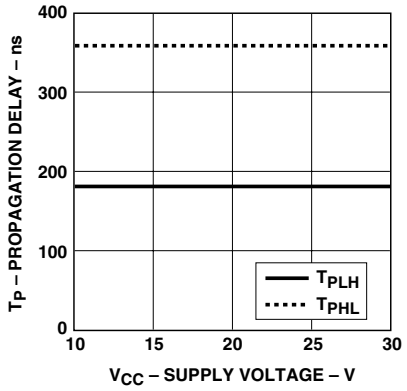


Figure 10. Propagation delay vs. V_{CC}.

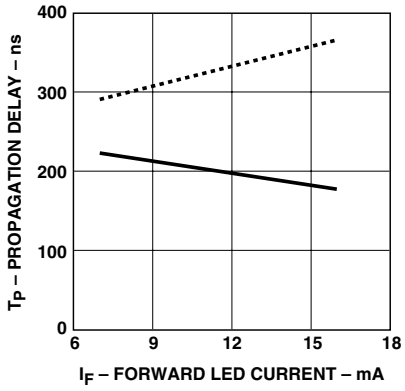


Figure 11. Propagation delay vs. I_F.

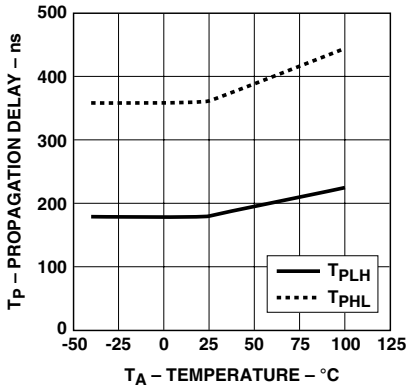


Figure 12. Propagation delay vs. temperature.

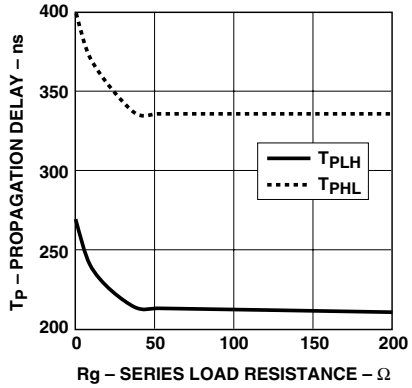


Figure 13. Propagation delay vs. Rg.

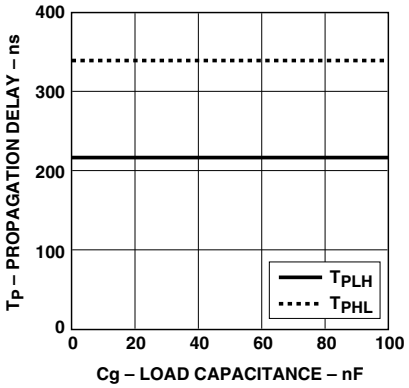


Figure 14. Propagation delay vs. Cg.

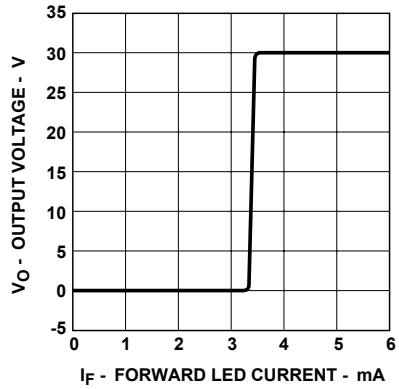


Figure 15. Transfer characteristics.

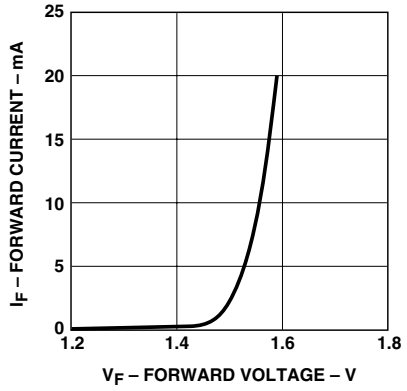


Figure 16. Input current vs. forward voltage.

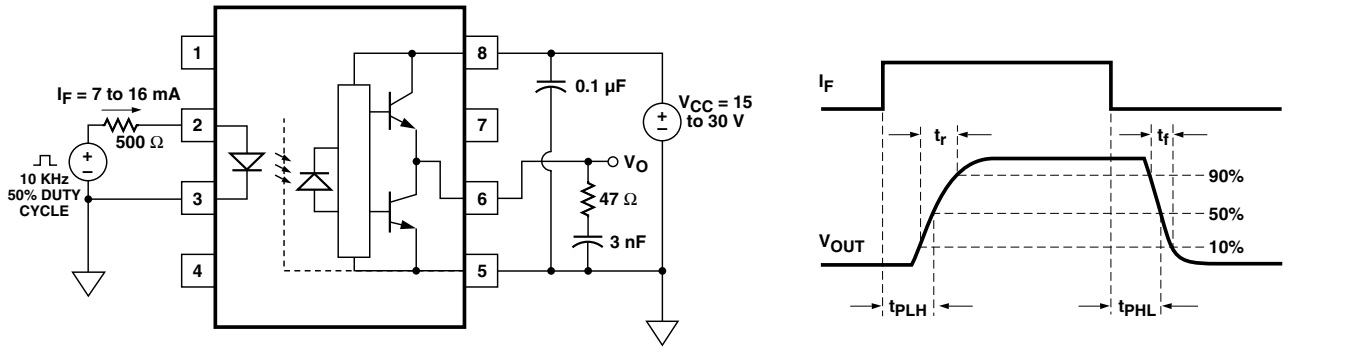


Figure 17. Propagation delay test circuit and waveforms.

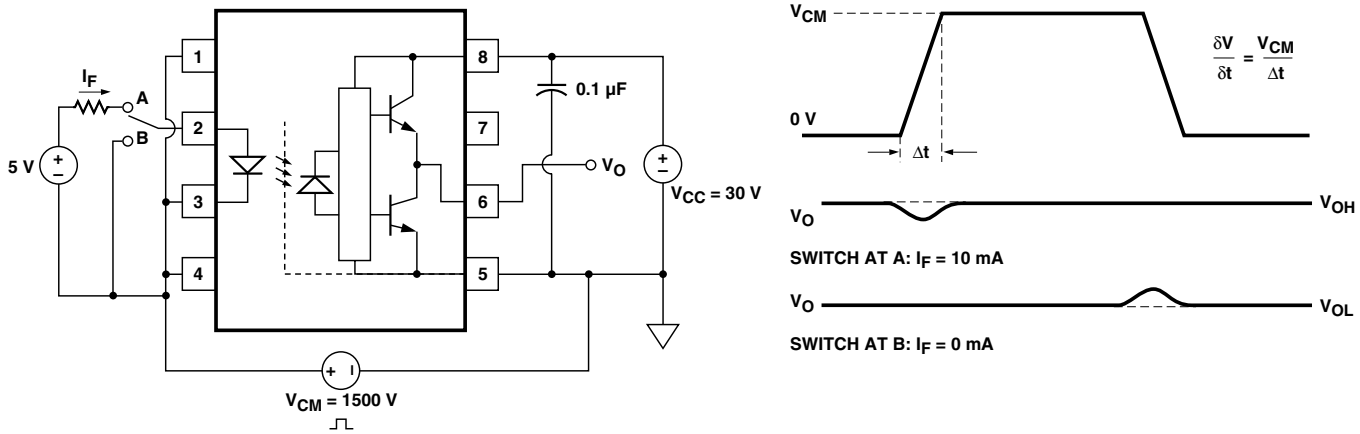


Figure 18. CMR test circuit and waveforms.

Applications Information

Eliminating Negative IGBT Gate Drive

To keep the IGBT firmly off, the HCPL-J314 has a very low maximum V_{OL} specification of 1.0 V. Minimizing Rg and the lead inductance from the HCPL-J314 to the IGBT gate and emitter (possibly by mounting the HCPL-J314 on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 19. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the HCPL-J314 input as this can result in unwanted coupling of transient signals into the input of HCPL-J314 and degrade performance. (If the IGBT drain must be routed near the HCPL-J314 input, then the LED should be reverse biased when in the off state, to prevent the transient signals coupled from the IGBT drain from turning on the HCPL-J314.)

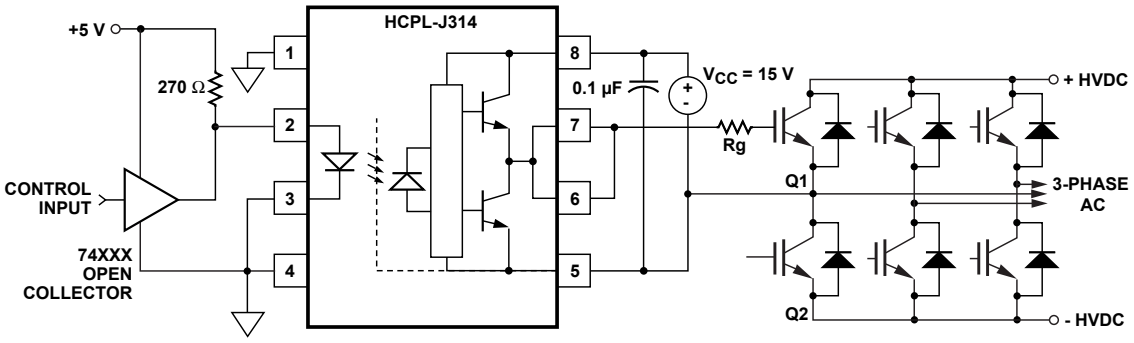


Figure 19. Recommended LED drive and application circuit for HCPL-J314.

Selecting the Gate Resistor (Rg)

Step 1: Calculate R_g minimum from the I_{OL} peak specification. The IGBT and Rg in Figure 19 can be analyzed as a simple RC circuit with a voltage supplied by the HCPL-J314.

$$Rg \geq \frac{V_{CC} - V_{OL}}{I_{OLPEAK}}$$

$$= \frac{24\ V - 5\ V}{0.6A}$$

$$= 32\ \Omega$$

The V_{OL} value of 5 V in the previous equation is the V_{OL} at the peak current of 0.6A. (See Figure 6).

Step 2: Check the HCPL-J314 power dissipation and increase Rg if necessary. The HCPL-J314 total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O).

$P_T = P_E + P_O$

$P_E = I_F \times V_F \times Duty\ Cycle$

$P_O = P_{O(BIAS)} + P_{O(SWITCHING)} = I_{CC} \times V_{CC} + E_{SW}(Rg,Qg) \times f$

$= (I_{CCBIAS} + K_{ICC} \times Qg \times f) \times V_{CC} + E_{SW}(Rg,Qg) \times f$

where $K_{ICC} \times Qg \times f$ is the increase in I_{CC} due to switching and K_{ICC} is a constant of 0.001 mA/(nC*kHz). For the circuit in Figure 19 with I_F (worst case) = 10 mA, Rg = 32 Ω, Max Duty Cycle = 80%, Qg = 100 nC, f = 20 kHz and T_{AMAX} = 85°C:

$P_E = 10\ mA \times 1.8\ V \times 0.8 = 14\ mW$

$P_O = (3\ mA + (0.001\ mA/(nC \times kHz)) \times 20\ kHz \times 100\ nC) \times 24\ V + 0.4\ \mu J \times 20\ kHz = 80\ mW$

$< 260\ mW\ (P_{O(MAX)} @ 85°C)$

The value of 3 mA for I_{CC} in the previous equation is the max. I_{CC} over entire operating temperature range.

Since P_O for this case is less than $P_{O(MAX)}$, Rg = 32 Ω is all right for the power dissipation.

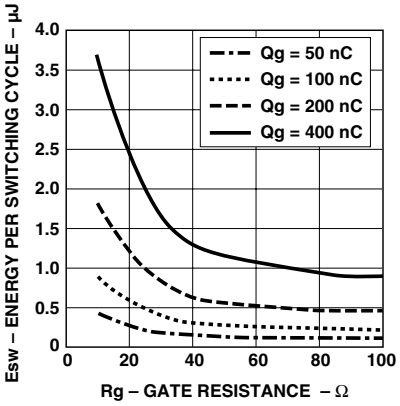


Figure 20. Energy dissipated in the HCPL-J314 and for each IGBT switching cycle.

LED Drive Circuit Considerations for Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 21. The HCPL-J314 improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5-8 as shown in Figure 22. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 19), can achieve 10 kV/µs CMR while minimizing component complexity.

Techniques to keep the LED in the proper state are discussed in the next two sections.

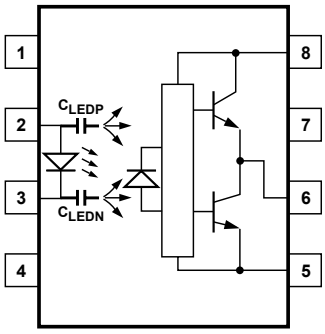


Figure 21. Optocoupler input to output capacitance model for unshielded optocouplers.

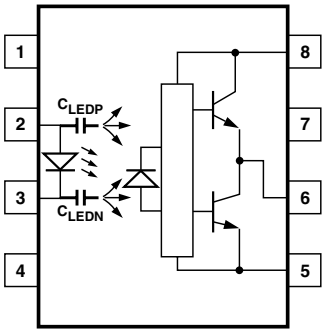


Figure 22. Optocoupler input to output capacitance model for shielded optocouplers.

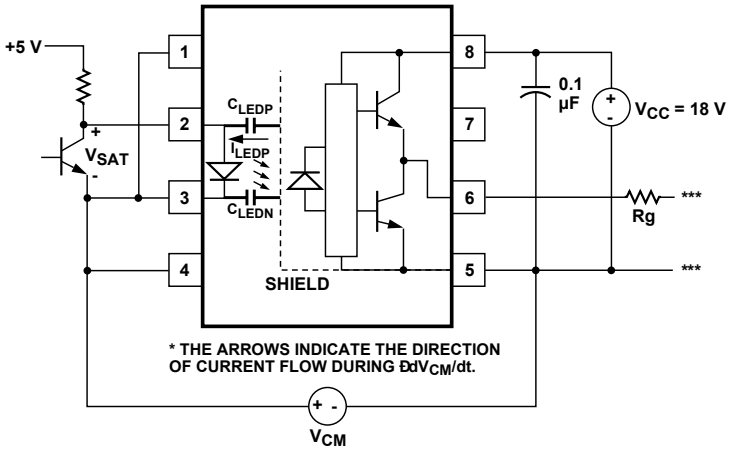


Figure 23. Equivalent circuit for Figure 17 during common mode transient.

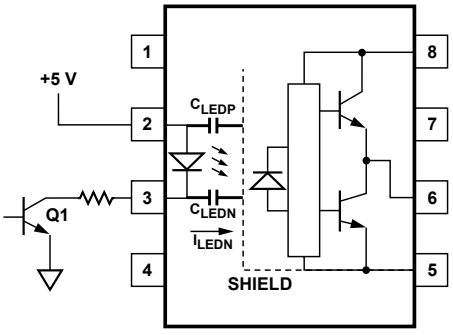


Figure 24. Not recommended open collector drive circuit.

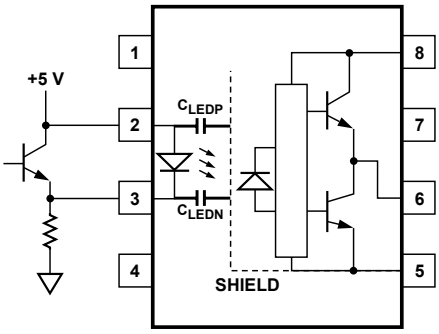


Figure 25. Recommended LED drive circuit for ultra-high CMR IPM dead time and propagation delay specifications.

CMR with the LED On (CMR_H)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 8 mA provides adequate margin over the maximum IFigure 26. Minimum LED Skew for Zero Dead Time.Figure 27. Waveforms for Dead Time. of 5 mA to achieve 10 kV/µs CMR.

CMR with the LED Off (CMR_L)

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $-dV_{CM}/dt$ transient in Figure 23, the current flowing through C_{LEDP} also flows through the RSAT and VSAT of the logic gate. As long as the low state voltage developed across the logic gate is less than $V_{F(OFF)}$ the LED will remain off and no common mode failure will occur.

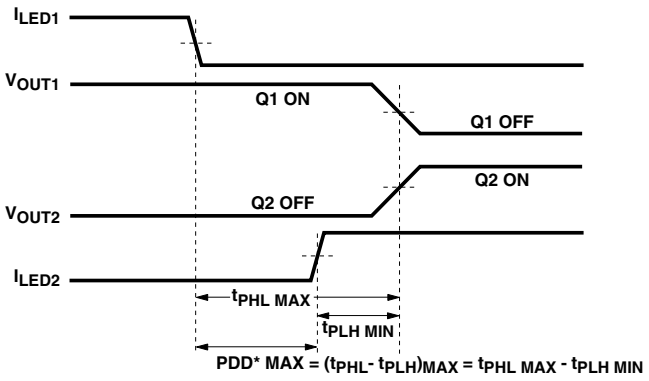
The open collector drive circuit, shown in Figure 24, can not keep the LED off during a $+dV_{CM}/dt$ transient, since all the current flowing through C_{LEDN} must be supplied by the LED, and it is not recommended for applications requiring ultra high CMR1 performance. The alternative drive circuit which like the recommended application circuit (Figure 19), does achieve ultra high CMR performance by shunting the LED in the off state.

IPM Dead Time and Propagation Delay Specifications

The HCPL-J314 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize “dead time” in their power inverter designs. Dead time is the time high and low side power transistors are off. Any overlap in Ql and Q2 conduction will result in large currents flowing through the power devices from the high-voltage to the low-voltage motor rails. To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 26. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD max, which is specified to be 500 ns over the operating temperature range of -40° to 100°C.

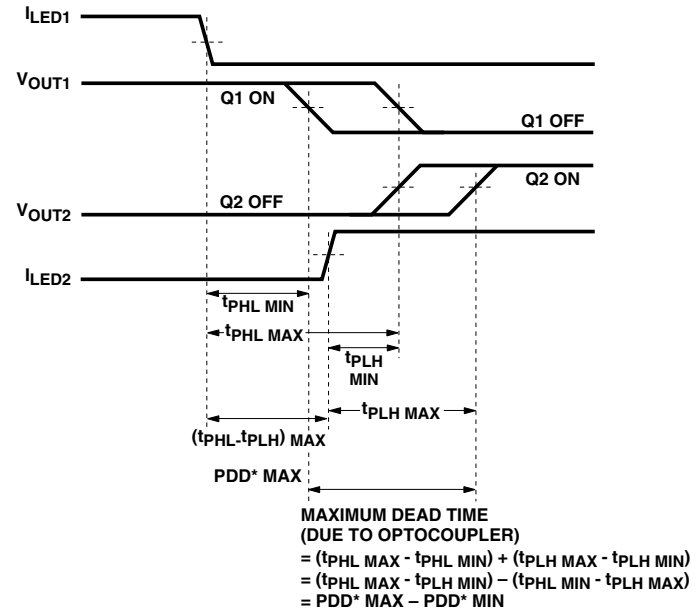
Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specification as shown in Figure 27. The maximum dead time for the HCPL-J314 is 1 µs (= 0.5 µs - (-0.5 µs)) over the operating temperature range of -40°C to 100°C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR PDD CALCULATIONS THE PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 26. Minimum LED skew for zero dead time.



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR DEAD TIME AND PDD CALCULATIONS ALL PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 27. Waveforms for dead time.

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