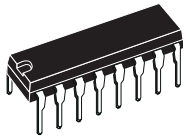
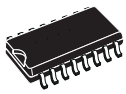
HCF40109B

QUAD LOW-TO-HIGH VOLTAGE LEVEL SHIFTER

- INDIPENDENCE OF POWER SUPPLY SEQUENCE CONSIDERATIONS - V_{CC} CAN EXCEED V_{DD}, INPUT SIGNALS CAN EXCEED BOTH V_{CC} AND V_{DD}
- UP AND DOWN LEVEL SHIFTING CAPABILITY
- THREE-STATE OUTPUTS WITH SEPARATE ENABLE CONTROLS
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP



SOP

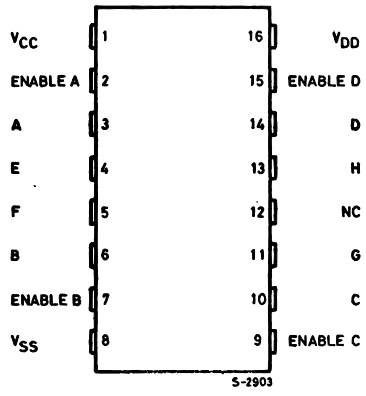
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF40109BEY	
SOP	HCF40109BM1	HCF40109M013TR

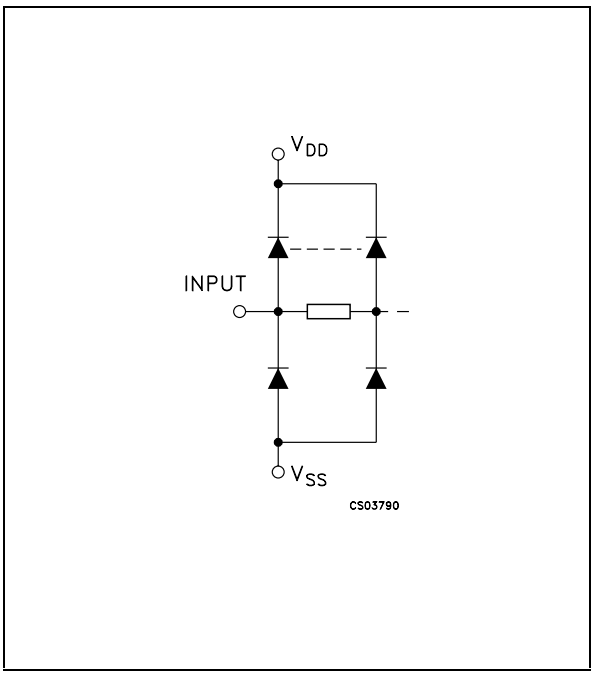
DESCRIPTION

HCF40109B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
HCF40109B contains four low-to-high voltage level shifting circuits. Each circuit will shift a low-voltage digital-logic input signal (A, B, C, D) with logical 1 = V_{CC} and logical 0 = V_{SS} to a higher voltage output signal (E, F, G, H) with logical 1 = V_{DD} and logical 0 = V_{SS}. HCF40109B, unlike other low-to-high level-shifting circuits, does not require the presence of the high voltage supply (V_{DD}) before the application of either the low-voltage supply (V_{CC}) or the input signals. There are no restrictions on the sequence of application of V_{DD}, V_{CC}, or the input signals. In addition, there are no restrictions on the relative magnitudes of the supply voltages or input signals within the device maximum ratings; V_{CC} may exceed V_{DD}, and input signals may exceed V_{CC} and V_{DD}. When operated in the mode V_{CC} V_{DD}, HCF40109B will operate as a high-to-low level-shifter. HCF40109B also features individual three-state output capability. A low level on any of the separately enabled three-state output controls produces a high-impedance state in the corresponding output.

PIN CONNECTION



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

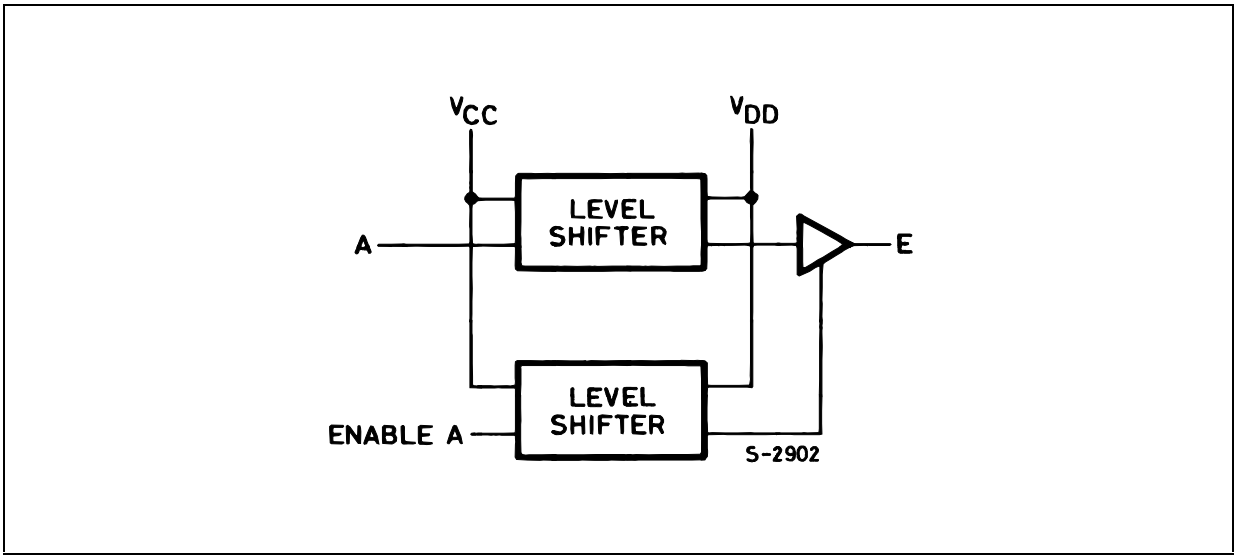
PIN No	SYMBOL	NAME AND FUNCTION
3, 6, 10, 14	A, B, C, D	Low Input Voltage
4, 5, 11, 13	E, F, G, H	High Input Voltage
2, 7, 9, 15	ENABLE A, B, C, D	Enable Input
12	NC	Not Connected
1	V_{CC}	Low Supply Voltage
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

TRUTH TABLE

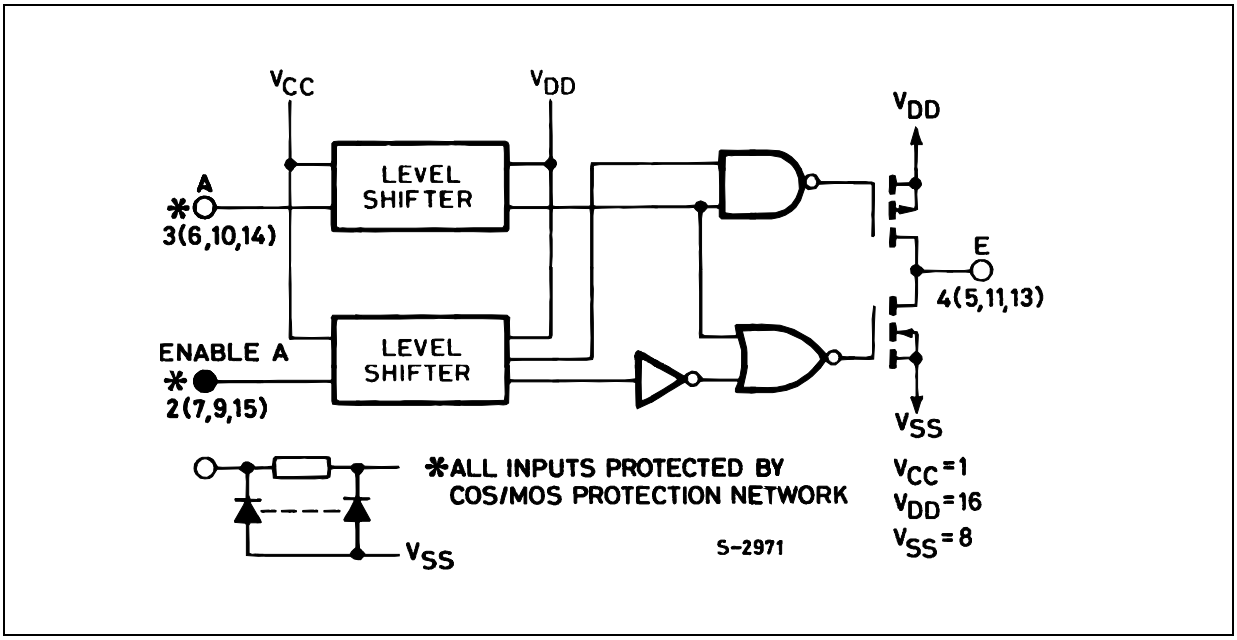
MODE	INPUTS		OUTPUT
	A, B, C, D	Enable A, B, C, D	E, F, G, H
Low to High Level Shift	L	H	L
	H	H	H
	X	L	Z

X : Don't Care
Z : High Impedance

FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

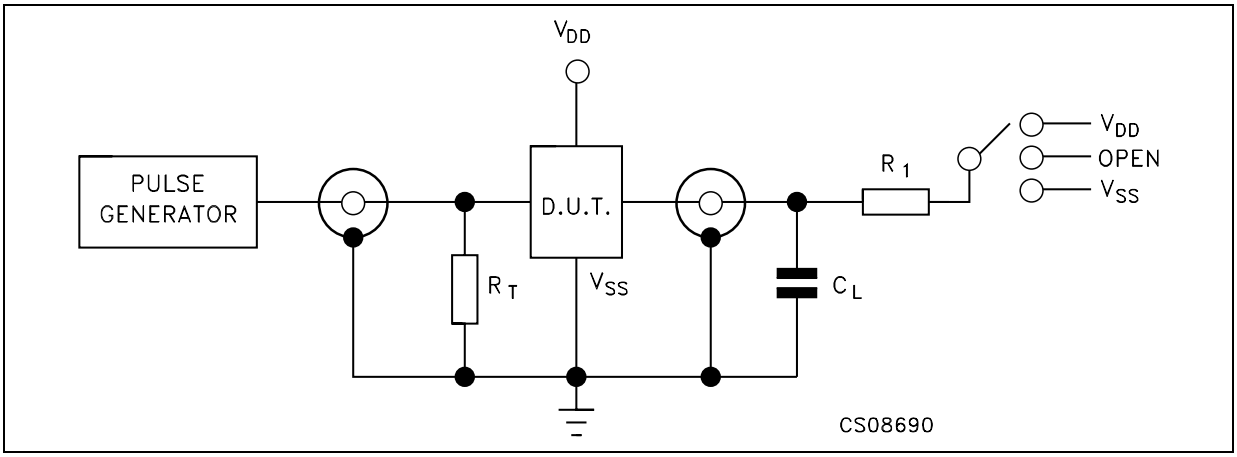
Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.02	1		30		30	μA
		0/10			10		0.02	2		60		60	
		0/15			15		0.02	4		120		120	
		0/20			20		0.04	20		600		600	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.53	-3.2		-1.36		-1.1		mA
		0/5	4.6	<1	5	-0.52	-1		-0.44		-0.36		
		0/10	9.5	<1	10	-1.3	-2.6		-1.1		-0.9		
		0/15	13.5	<1	15	-3.6	-6.8		-3.0		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.52	1		0.44		0.36		mA
		0/10	0.5	<1	10	1.3	2.6		1.1		0.9		
		0/15	1.5	<1	15	3.6	6.8		3.0		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition			Value (*)			Unit
		V_{CC} (V)	V_{DD} (V)	SHITFING MODE	Min.	Typ.	Max.	
t_{PHL} t_{PLH}	Propagation Delay Time : (Data input to output) High to Low Level	5	10	L - H		300	600	ns
		5	15			220	440	
		10	15			180	360	
		10	5	H - L		850	1600	
		15	5			850	1600	
		15	10			290	580	
	Low to High Level	5	10	L - H		130	260	ns
		5	15			120	240	
		10	15			70	140	
		10	5	H - L		230	460	
		15	5			230	460	
		15	10			80	160	
t_{PHZ}	3-State Disable DelayTime Output High to High Impedance	5	10	L - H		60	120	ns
		5	15			50	100	
		10	15			35	70	
		10	5	H - L		120	240	
		15	5			120	240	
		15	10			40	80	
t_{PZH}	High Impedance to Output High	5	10	L - H		320	640	ns
		5	15			230	460	
		10	15			180	360	
		10	5	H - L		800	1500	
		15	5			800	1500	
		15	10			280	560	
t_{PLZ}	Output Low to High Impedance	5	10	L - H		370	740	ns
		5	15			300	600	
		10	15			250	500	
		10	5	H - L		850	1600	
		15	5			850	1600	
		15	10			350	700	
t_{PZL}	High Impedance to Output Low	5	10	L - H		100	200	ns
		5	15			80	160	
		10	15			40	80	
		10	5	H - L		120	240	
		15	5			120	240	
		15	10			40	80	
t_{THL},t_{TLH}	Transition Time	5	10	L - H		50	100	ns
		5	15			40	80	
		10	15			40	80	
		10	5	H - L		100	200	
		15	5			100	200	
		15	10			50	100	

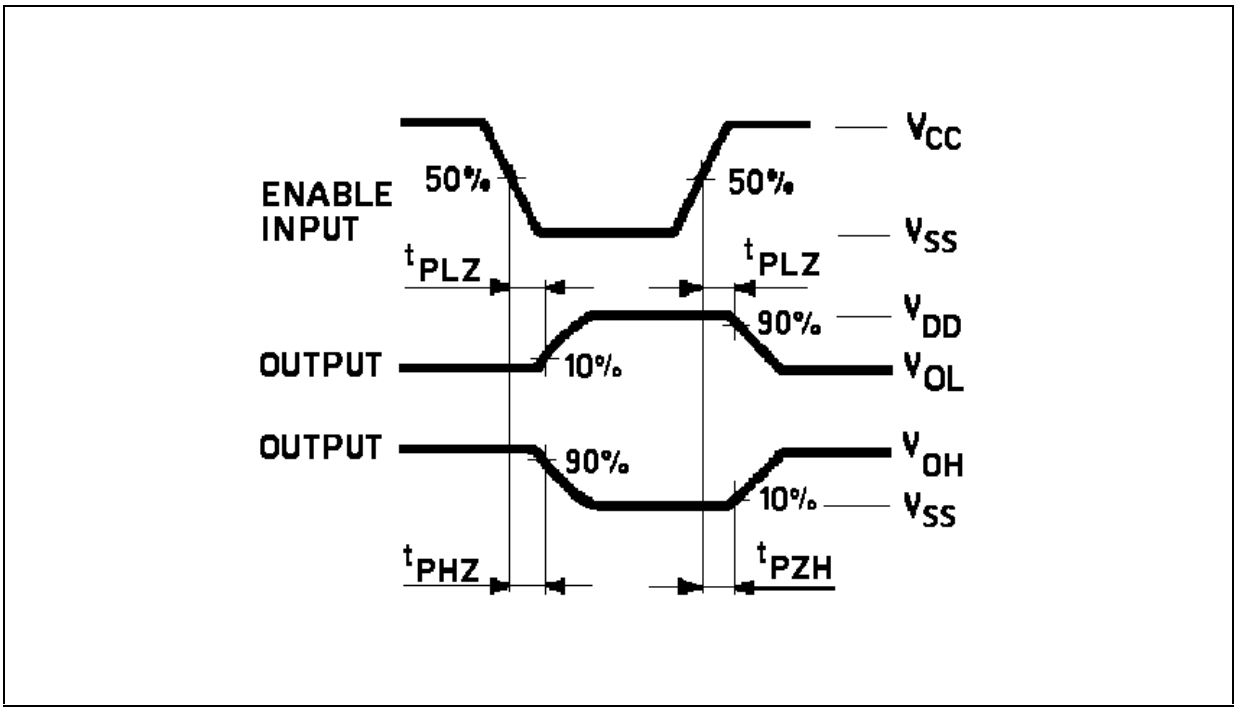
TEST CIRCUIT



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{DD}
t_{PZH}, t_{PHZ}	V_{SS}

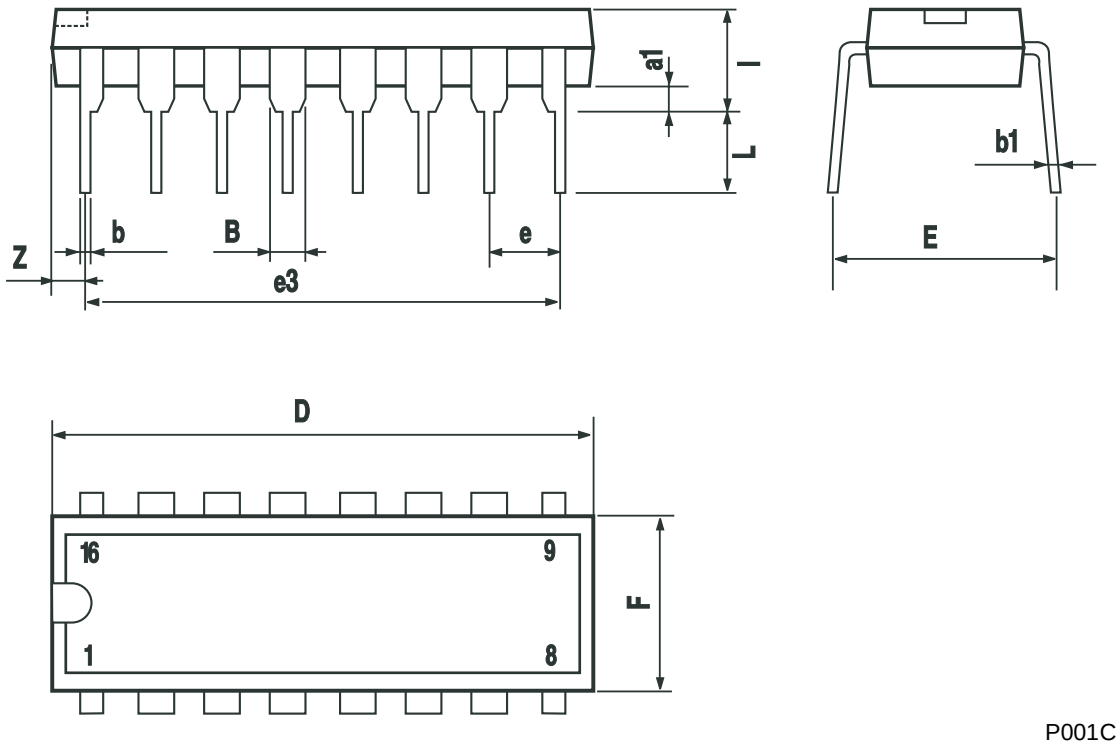
C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM : PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



Plastic DIP-16 (0.25) MECHANICAL DATA

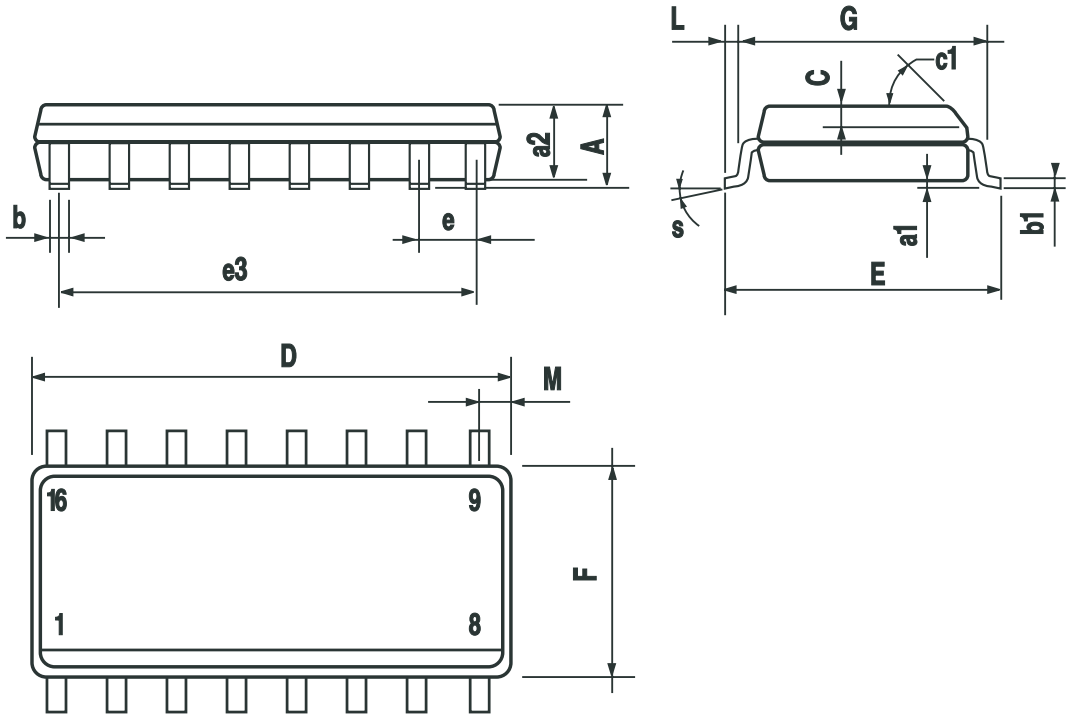
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

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