Data Sheet June 2004 FN4806.3

Low Cost SLIC For Large Telecom Switches

The HC5503PRC is a low cost SLIC optimized for large Telecom switches. It combines a flexible voltage feed architecture with the Intersil latch-free DI bonded wafer process, to provide a low component count, carrier class solution at very low cost. The re-configurable design permits simple, economical solutions for campus-wide call center and PBX applications. External components can be used in conjunction with the high battery voltage capability to meet the complex impedance and long loop drive requirements of Central Office switches, worldwide.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HC5503PRCB	0 to 70	24 Ld SOIC	M24.3
HC5503PRCBZ (Note)	0 to 70	24 Ld SOIC (Pb-free)	M24.3
HC5503PRCBZ96 (Note)	0 to 70	24 Ld SOIC Tape & Reel (Pb-free)	M24.3
HC5503PRCR	0 to 70	32 Ld 7x7 QFN	L32.7x7
HC5503PRCRZ (Note)	0 to 70	32 Ld 7x7 QFN (Pb-free)	L32.7x7
HC5503PRCRZ96 (Note)	0 to 70	32 Ld 7x7 QFN Tape & Reel (Pb-free)	L32.7x7

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Features

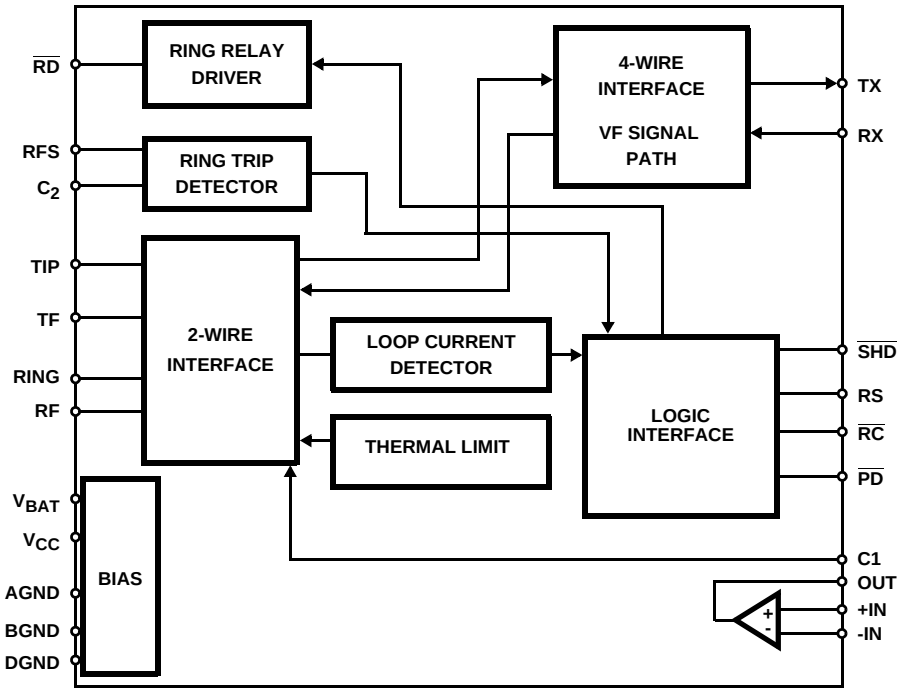
- Wide Operating Battery Range (-40V to -58V)
- Single Additional +5V Supply
- 30mA Short Loop Current Limit
- Ring Relay Driver
- Switch Hook and Ring Trip Detect
- Low On-Hook Power Consumption
- On-Hook Transmission
- ITU-T Longitudinal Balance Performance
- Loop Power Denial Function
- Thermal Protection
- Supports Tip, Ring or Balanced Ringing Schemes
- Low Profile SO and QFN Surface Mount Packaging
- Pb-free Available

Applications

- Central Office, PBX, Call Centers
- Related Literature
  - AN571, Using Ring Sync with HC-5502A and HC-5504 SLICs

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Block Diagram



Absolute Maximum Ratings

Maximum Continuous Supply Voltages
- (V_B-) . . . . . -60 to 0.5V
- (V_B+) . . . . . -0.5 to 7V
- (V_B+ - V_B-) 75V

Relay Drive Voltage (V_{RD}) . . . . . -0.5 to 15V

Operating Conditions

Operating Temperature Range . . . . . 0°C to 70°C
Relay Driver Voltage (V_{RD}) . . . . . 5V to 12V
Positive Supply Voltage (V_B+) . . . . . 4.75V to 5.25V
Negative Supply Voltage (V_B-) . . . . . -40V to -58V
High Level Logic Input Voltage 2.4V
Low Level Logic Input Voltage 0.6V
Subscriber Loop Resistance . . . . . 200Ω - 1800Ω

Thermal Information

Thermal Resistance (Typical, Note 2, 3)	θ_{JA} (°C/W)
24 Lead SOIC	75
32 Lead 7x7 QFN	32

Maximum Junction Temperature Plastic . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Die Characteristics

Transistor Count 185
Diode Count 36
Die Dimensions . . . . . 137 x 102
Substrate Potential . . . . . Connected
Process . . . . . Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. θ_{JA} for the QFN package is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features including conductive thermal vias. See Tech Brief TB379 and TB389 for additional information and board layout consideration

Electrical Specifications

Unless Otherwise Specified, V_B- = -48V, V_B+ = 5V, AG = BG = DG = 0V, R_P = 50Ω, R_S = 100Ω, Typical Parameters. T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	I_{LONG} = 0 (Note 4)	-	113	-	mW
Off Hook Power Dissipation	R_L = 600Ω, I_{LONG} = 0 (Notes 3, 4)	-	750	-	mW
On Hook I_B+	R_L = ∞, I_{LONG} = 0	-	1.4	-	mA
Off Hook I_B+	R_L = 600Ω, I_{LONG} = 0	-	2.8	-	mA
On Hook I_B-	R_L = ∞, I_{LONG} = 0	-	2.2	-	mA
Off Hook I_B-	R_L = 600Ω, I_{LONG} = 0	-	31	-	mA
Off Hook Loop Current	R_L = 1800Ω (I_{LOOP} = 0)	18	-	-	mA
Off Hook Loop Current	R_L = 200Ω, I_{LONG} = 0 (Note 3)	25	30	35	mA
Fault Currents					
TIP to Ground		-	27	-	mA
RING to Ground		-	55	-	mA
TIP to RING		-	30	-	mA
TIP and RING to Ground		-	69	-	mA
Ring Relay Drive V_{OL}	I_{OL} = 62mA	-	0.2	0.5	V
Ring Relay Driver Off Leakage	V_{RD} = 12V, $\overline{RC}$ = 1 = HIGH, T_A = 25°C	-	-	100	µA
DC Ring Trip Threshold		8.1	10.8	13.5	mA
Switch Hook Detection Threshold		5.0	7.5	10	mA
Loop Current During Power Denial	R_L = 200Ω	-	3.2	-	mA
Dial Pulse Distortion	(Note 4)	0	-	0.5	ms
Receive Input Impedance	(Note 4)	-	110	-	kΩ
Transmit Output Impedance	(Note 4)	-	10	20	Ω

Electrical Specifications Unless Otherwise Specified, V_B- = -48V, V_B+ = 5V, AG = BG = DG = 0V, R_P = 50Ω, R_S = 100Ω, Typical Parameters. T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
2-Wire Return Loss	(Referenced to 600Ω + 2.16μF), $R_P = R_S$ = 150Ω (Note 4)				
SR_L LO		-	15.5	-	dB
ER_L		-	24	-	dB
SR_L HI		-	31	-	dB
Longitudinal Balance	$1V_{RMS}$ 200Hz - 3400Hz, (Note 4) IEEE Method				
2-Wire Off Hook (Note 4)	0°C ≤ T_A ≤ 75°C, $R_P = R_S$ = 150Ω	53	58	-	dB
2-Wire On Hook (Note 4)		53	58	-	dB
4-Wire Off Hook		50	58	-	dB
Insertion Loss	At 1kHz, 0dBm Input Level, Referenced 600Ω,				
2-Wire to 4-Wire, 4-Wire to 2-Wire	$R_P = R_S$ = 150Ω	-	±0.05	±0.2	dB
Frequency Response	200 - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level, $R_P = R_S$ = 150Ω (Note 4)	-	±0.02	±0.05	dB
Idle Channel Noise	$R_P = R_S$ = 150Ω (Note 4)				
2-Wire to 4-Wire, 4-Wire to 2-Wire		-	1	5	dBrnC
		-	-89	-85	dBm0p
Absolute Delay	$R_P = R_S$ = 150Ω (Note 4)				
2-Wire to 4-Wire, 4-Wire to 2-Wire		-	-	2	μs
Trans Hybrid Loss	Balance Network Set Up for 600Ω Termination at 1kHz, $R_P = R_S$ = 150Ω (Note 4)	30	40	-	dB
Overload Level	V_B+ = +5V, $R_P = R_S$ = 150Ω (Note 4)				
2-Wire to 4-Wire, 4-Wire to 2-Wire		1.5	-	-	V_{PEAK}
Level Linearity	At 1kHz, (Note 4) Referenced to 0dBm Level,				
2-Wire to 4-Wire, 4-Wire to 2-Wire (Note 4)	$R_P = R_S$ = 150Ω				
+3 to -40dBm		-	-	±0.05	dB
-40 to -50dBm		-	-	±0.1	dB
-50 to -55dBm		-	-	±0.3	dB
Power Supply Rejection Ratio	$R_P = R_S$ = 150Ω (Note 4)				
V_B+ to 2-Wire	30 - 60Hz, R_L = 600Ω	15	-	-	dB
V_B+ to Transmit		15	-	-	dB
V_B- to 2-Wire		15	-	-	dB
V_B- to Transmit		15	-	-	dB
V_B+ to 2-Wire	200 - 16kHz, R_L = 600Ω, $R_P = R_S$ = 150Ω	30	-	-	dB
V_B+ to Transmit		30	-	-	dB
V_B- to 2-Wire		30	-	-	dB
V_B- to Transmit		30	-	-	dB
Logic Input Current (RS, $\overline{RC}$, $\overline{PD}$)	0V ≤ V_{IN} ≤ 5V	-	-	±100	μA
Logic Inputs					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} 800μA, V_B+ = 5V	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} 40μA, V_B+ = 5V	2.7	-	5.0	V

Electrical Specifications Unless Otherwise Specified, V_B- = -48V, V_B+ = 5V, AG = BG = DG = 0V, R_P = 50Ω, R_S = 100Ω, Typical Parameters. T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
UNCOMMITTED OP AMP SPECIFICATIONS					
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Input Bias Current		-	20	-	nA
Differential Input Resistance	(Note 4)	-	1	-	MΩ
Output Voltage Swing	R_L = 10K, V_B+ = 5V	-	±3	-	V_{PEAK}
Output Resistance	A_{VCL} = 1 (Note 4)	-	10	-	Ω
Small Signal GBW	(Note 4)	-	1	-	MHz

NOTES:

4. I_{LONG} = Longitudinal Current.
5. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

Pin Descriptions

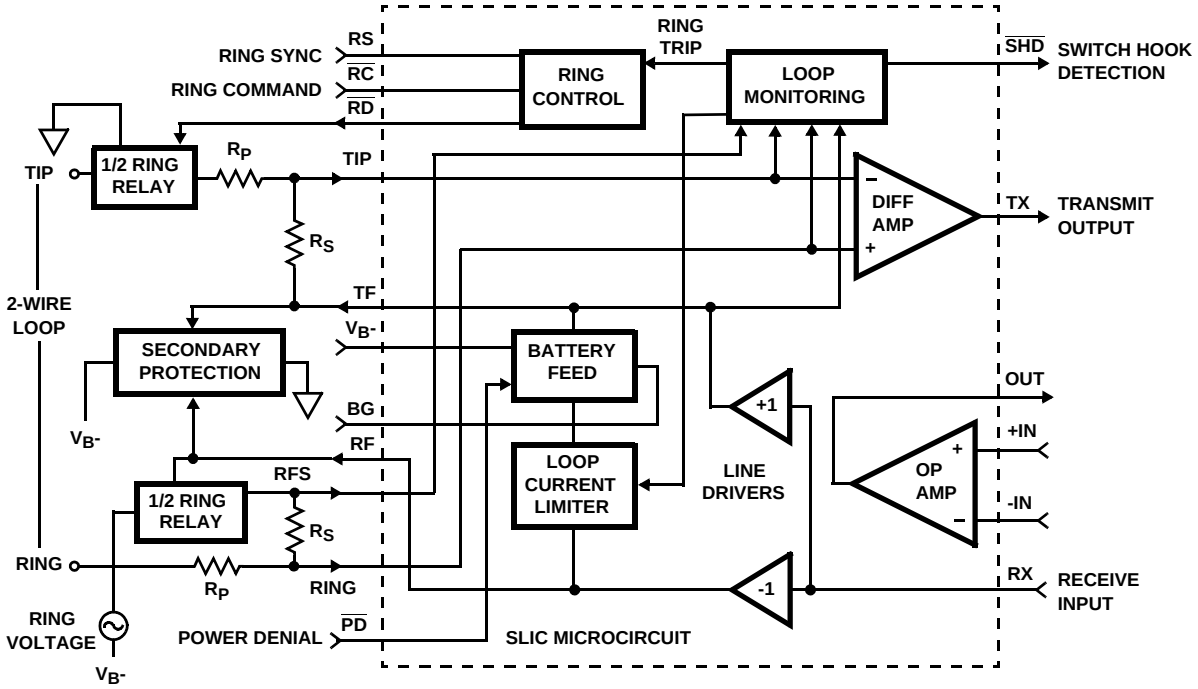
24 PIN DIP/SOIC	7 x 7 QFN	SYMBOL	DESCRIPTION
1	28	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a sense resistor (R_S) and a ring relay contact. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring purposes.
2	31	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a sense resistor (R_S) and a ring relay contact. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.
3	32	RFS	Senses ring side of loop for ground key and ring trip detection. During ringing, the ring signal is inserted into the line at this node and RF is isolated from RFS via a relay.
4	1	V_B+	Positive Voltage Source - Most positive supply. V_B+ is typically.
5	3	C_1	Capacitor #1 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V_B-. Typical value is 0.3µF, 30V.
6	4	DG	Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.
7	5	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock should be arranged such that a positive pulse transition occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring relay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to 5V.
8	6	$\overline{RD}$	Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.
9	7, 8	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a sense resistor (R_S). Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
10	9, 10	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a sense resistor (R_S). Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
11	11	V_B-	Negative Voltage Source - Most negative supply. V_B- is typically -48V with an operational range of -42V to -58V. Frequently referred to as “battery”.
12	12	BG	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
13	13	$\overline{SHD}$	Switch Hook Detection - A low active LS TTL - compatible logic output. This output is enabled for loop currents exceeding the switch hook threshold.
14	14,19	NC	Used during production test. Leave disconnected.

Pin Descriptions (Continued)

24 PIN DIP/SOIC	7 x 7 QFN	SYMBOL	DESCRIPTION
15	15	$\overline{PD}$	Power Denial - A low active TTL - Compatible logic input. When enabled, the ring feed voltage collapses to the tip feed voltage (~4V). The DC feed is disabled, but the AC transmission is maintained. The switch hook detect ($\overline{SHD}$) is not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.
16	16	$\overline{RC}$	Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next high level of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subscriber is not already off- hook ($\overline{SHD}$ = 0).
17		NC	Leave disconnected.
18	20	OUT	The analog output of the spare operational amplifier.
19	21	-IN	The inverting analog input of the spare operational amplifier.
20	22	+IN	The non-inverting analog input of the spare operational amplifier.
21	23	RX	Receive Input, Four Wire Side - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed terminals.
22	25	C_2	Capacitor #2 - An external capacitor to be connected between this terminal and analog ground. This capacitor is required for the proper operation of ring trip detection. Recommended value 0.82µF ±10% 10V non-polarized.
23	26	AG	Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
24	27	TX	Transmit Output, Four Wire Side - A low impedance analog output proportional to the loop current. Transhybrid balancing must be performed beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.
	2, 17, 18,24, 29, 30,	NC	No internal connection.

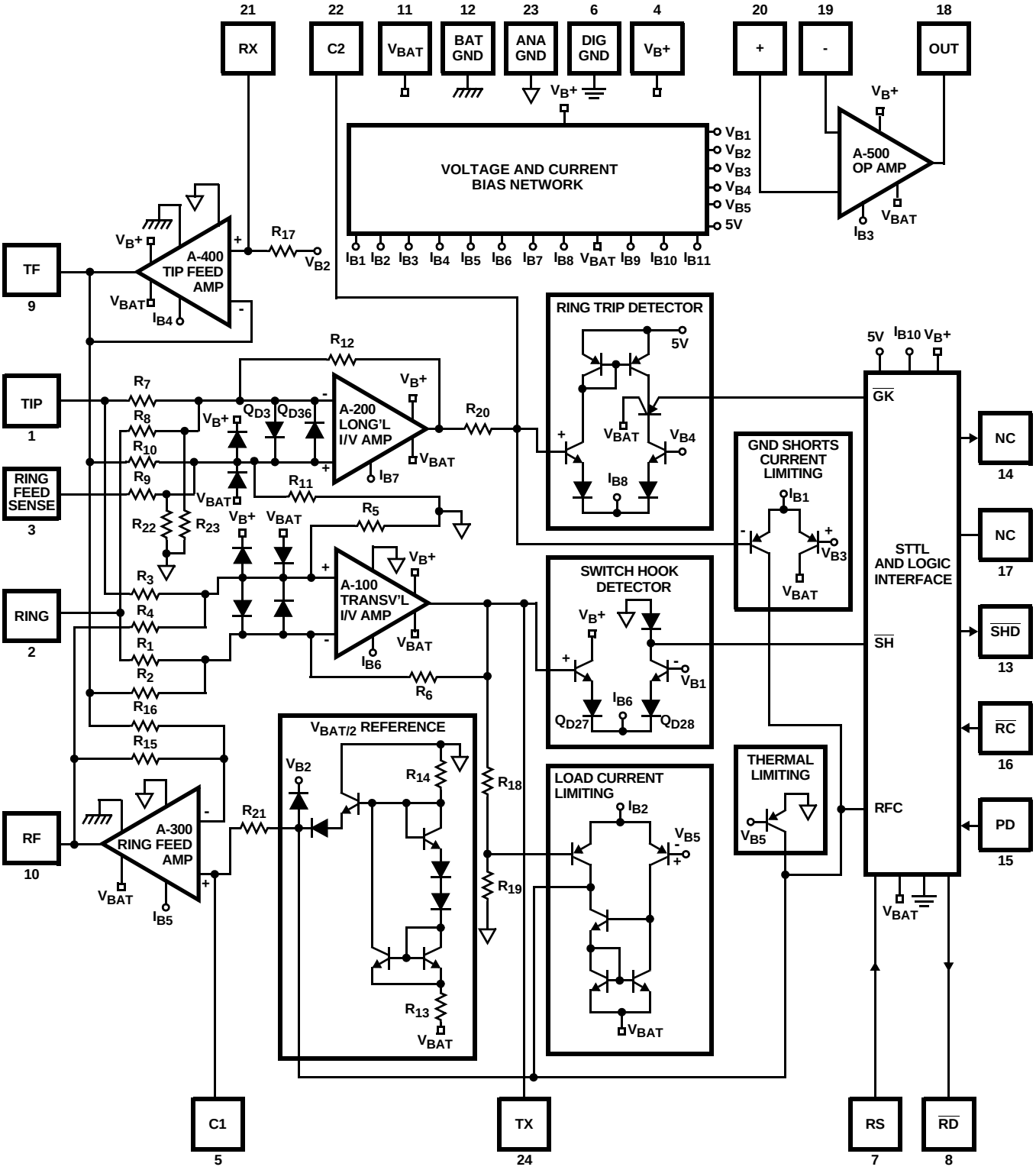
NOTE: All grounds (AG, BG, and DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Functional Diagram

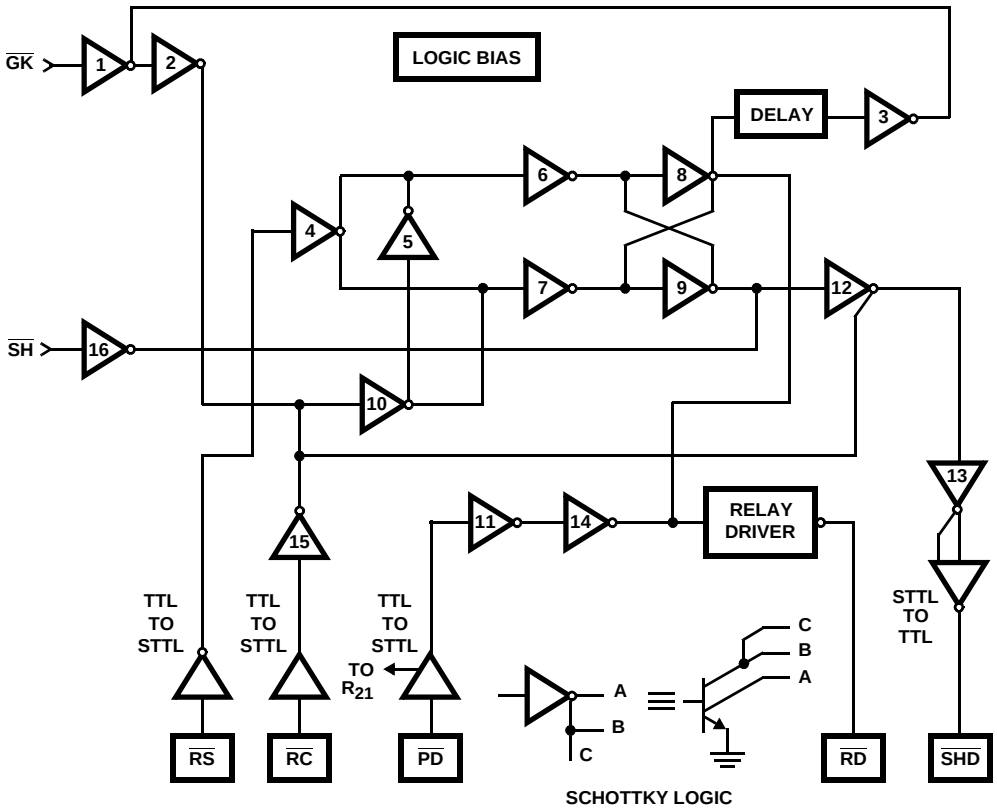


R_S: 100Ω; 1/2W to 2W depending on surge requirements
R_P: 50Ω; 1/2W to 2W depending on surge requirements

SLIC FUNCTIONAL SCHEMATIC
SOIC PIN NUMBERS SHOWN



LOGIC GATE SCHEMATIC



Surge Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

The voltage withstand capability of pins 'Tip', 'Ring' and 'RFs' is ±450V with respect to ground, as shown in Table 1.

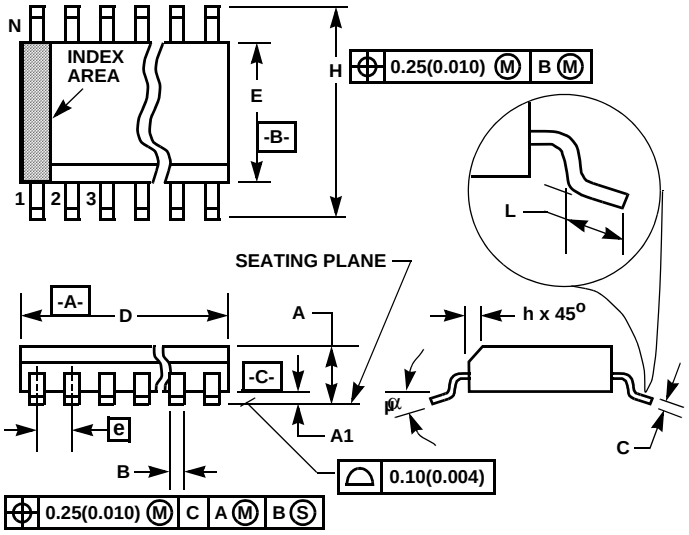
TABLE 1.

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±450 (Plastic)	V_{PEAK}
Metallic Surge	10µs Rise/ 1000µs Fall	±450 (Plastic)	V_{PEAK}
T/GND R/GND	10µs Rise/ 1000µs Fall	±450 (Plastic)	V_{PEAK}
50/60Hz Current T/GND R/GND	11 Cycles Limited to $10A_{RMS}$	315 (Plastic)	V_{RMS}

This device is intended for use with an appropriate secondary protection circuit scheme.

The SLIC will withstand longitudinal currents up to a maximum or $30mA_{RMS}$, $15mA_{RMS}$ per leg, without any performance degradation.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0^o	8^o	0^o	8^o	-

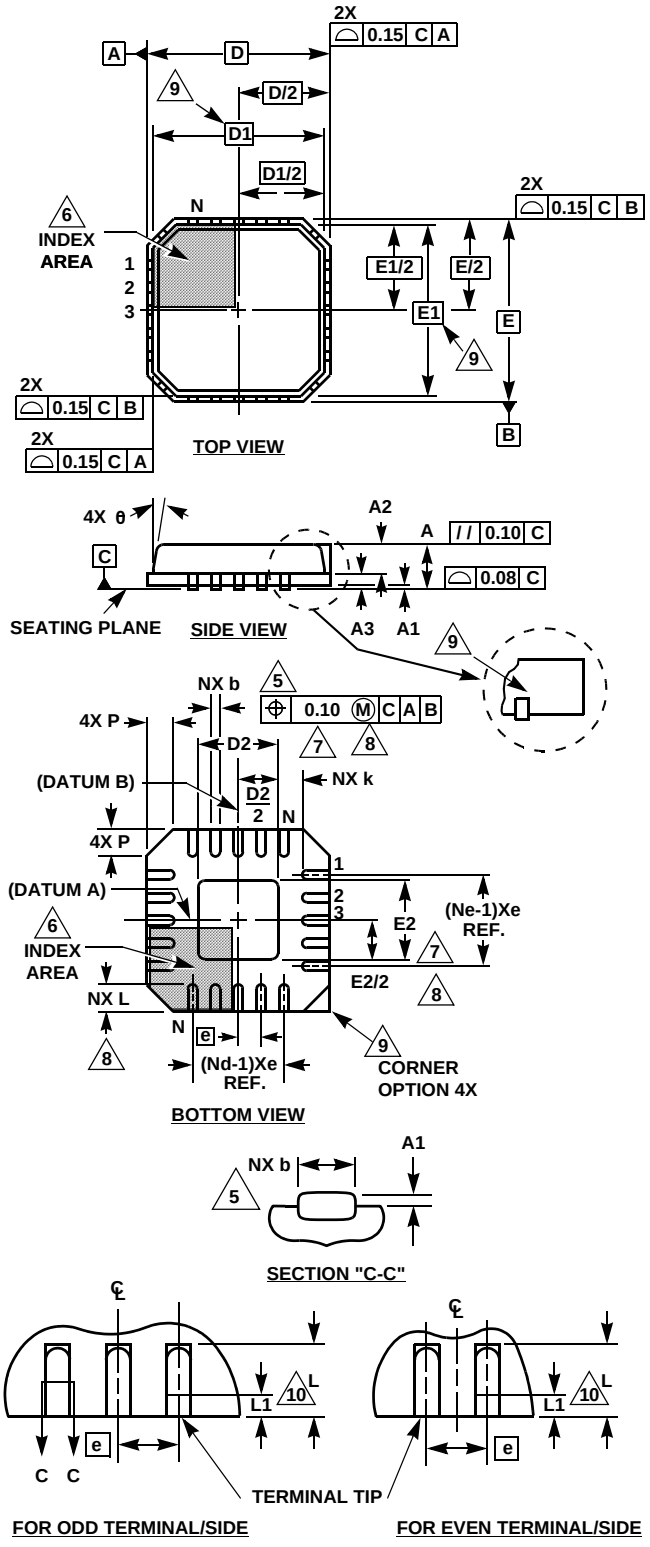
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Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L32.7x7

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VKKC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	TYP	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.38	5, 8
D		7.00 BSC		-
D1		6.75 BSC		9
D2	4.55	4.70	4.85	7, 8
E		7.00 BSC		-
E1		6.75 BSC		9
E2	4.55	4.70	4.85	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		32		2
Nd		8		3
Ne		8		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.