HAT3008R, HAT3008RJ

Silicon N / P Channel Power MOS FET
High Speed Power Switching

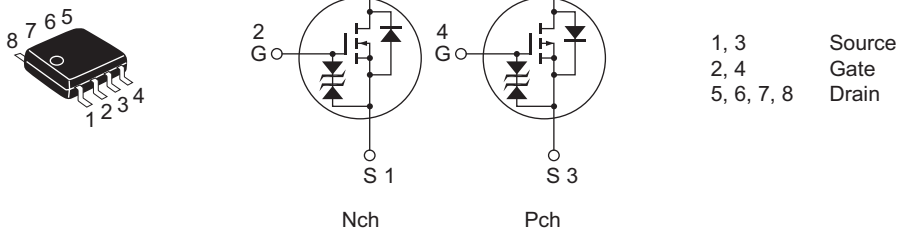
REJ03G1198-0400
(Previous: ADE-208-536B)
Rev.4.00
Sep 07, 2005

Features

- For Automotive Application (at Type Code “J”)
- Low on-resistance
- Capable of 4 V gate drive
- High density mounting

Outline

RENESAS Package code: PRSP0008DD-D
(Package name: SOP-8 <FP-8DAV>)



Absolute Maximum Ratings

(Ta = 25°C)

Item		Symbol	Value		Unit
			Nch	Pch	
Drain to source voltage		V_{DSS}	60	–60	V
Gate to source voltage		V_{GSS}	±20	±20	V
Drain current		I_D	5	–3.5	A
Drain peak current		$I_{D\ (pulse)}$ Note 1	40	–28	A
Body-drain diode reverse drain current		I_{DR}	5	–3.5	A
Avalanche current	HAT3008R	I_{AP} Note 4	—	—	—
	HAT3008RJ		5	–3.5	A
Avalanche energy	HAT3008R	E_{AR} Note 4	—	—	—
	HAT3008RJ		2.14	1.05	mJ
Channel dissipation		Pch Note 2	2	2	W
Channel dissipation		Pch Note 3	3	3	W
Channel temperature		Tch	150	150	°C
Storage temperature		Tstg	–55 to +150	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. 1 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), PW ≤ 10 s
3. 2 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), PW ≤ 10 s
4. Value at Tch = 25°C, Rg ≥ 50 Ω

Electrical Characteristics

N Channel

(Ta = 25°C)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage		$V_{(BR)\ DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage		$V_{(BR)\ GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	HAT3008R	I_{DSS}	—	—	1	µA	V_{DS} = 60 V, V_{GS} = 0
	HAT3008RJ	I_{DSS}	—	—	0.1	µA	
Zero gate voltage drain current	HAT3008R	I_{DSS}	—	—	—	µA	V_{DS} = 48 V, V_{GS} = 0 Ta = 125°C
	HAT3008RJ	I_{DSS}	—	—	10	µA	
Gate to source cutoff voltage		$V_{GS\ (off)}$	1.2	—	2.2	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance		$R_{DS\ (on)}$	—	0.043	0.058	Ω	I_D = 3 A, V_{GS} = 10 V Note 5
		$R_{DS\ (on)}$	—	0.056	0.084	Ω	I_D = 3 A, V_{GS} = 4 V Note 5
Forward transfer admittance		$\|y_{fs}\|$	6	9	—	S	I_D = 3 A, V_{DS} = 10 V Note 5
Input capacitance		Ciss	—	520	—	pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output capacitance		Coss	—	270	—	pF	
Reverse transfer capacitance		Crss	—	100	—	pF	
Turn-on delay time		$t_{d\ (on)}$	—	11	—	ns	V_{GS} = 10 V, I_D = 3 A V_{DD} ≅ 30 V
Rise time		t_r	—	40	—	ns	
Turn-off delay time		$t_{d\ (off)}$	—	110	—	ns	
Fall time		t_f	—	80	—	ns	
Body-drain diode forward voltage		V_{DF}	—	0.84	1.1	V	I_F = 5 A, V_{GS} = 0 Note 5
Body-drain diode reverse recovery time		t_{rr}	—	40	—	ns	I_F = 5 A, V_{GS} = 0 di_F/dt = 50 A/µs

Note: 5. Pulse test

P Channel

(Ta = 25°C)

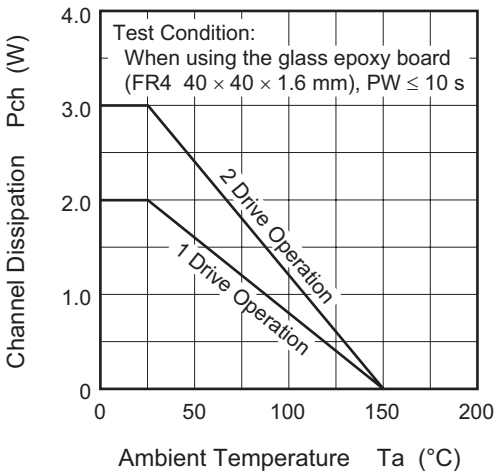
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage		$V_{(BR)\ DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage		$V_{(BR)\ GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	HAT3008R	I_{DSS}	—	—	–1	µA	V_{DS} = –60 V, V_{GS} = 0
	HAT3008RJ	I_{DSS}	—	—	–0.1	µA	
Zero gate voltage drain current	HAT3008R	I_{DSS}	—	—	—	µA	V_{DS} = –48 V, V_{GS} = 0
	HAT3008RJ	I_{DSS}	—	—	–10	µA	Ta = 125°C
Gate to source cutoff voltage		$V_{GS\ (off)}$	–1.2	—	–2.2	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance		$R_{DS\ (on)}$	—	0.12	0.15	Ω	I_D = –2 A, V_{GS} = –10 V Note 6
		$R_{DS\ (on)}$	—	0.16	0.23	Ω	I_D = –2 A, V_{GS} = –4 V Note 6
Forward transfer admittance		$\|y_{fs}\|$	3	4.5	—	S	I_D = –2 A, V_{DS} = –10 V Note 6
Input capacitance		Ciss	—	600	—	pF	V_{DS} = –10 V
Output capacitance		Coss	—	290	—	pF	V_{GS} = 0
Reverse transfer capacitance		Crss	—	75	—	pF	f = 1 MHz
Turn-on delay time		$t_{d\ (on)}$	—	11	—	ns	V_{GS} = –10 V, I_D = –2 A
Rise time		t_r	—	30	—	ns	V_{DD} ≅ –30 V
Turn-off delay time		$t_{d\ (off)}$	—	100	—	ns	
Fall time		t_f	—	55	—	ns	
Body-drain diode forward voltage		V_{DF}	—	–0.98	–1.28	V	I_F = –3.5 A, V_{GS} = 0 Note 6
Body-drain diode reverse recovery time		t_{rr}	—	70	—	ns	I_F = –3.5 A, V_{GS} = 0 di_F/dt = 50 A/µs

Note: 6. Pulse test

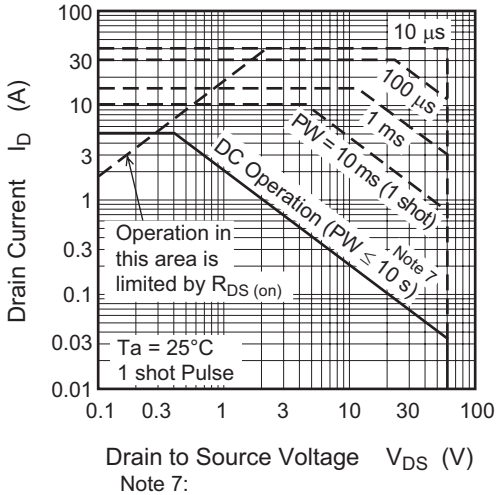
Main Characteristics

N Channel

Power vs. Temperature Derating

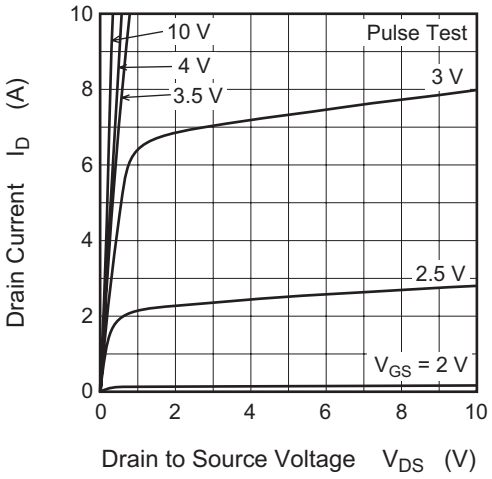


Maximum Safe Operation Area

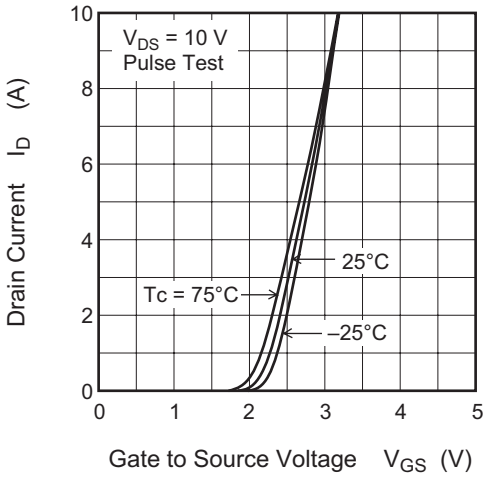


Note 7:
When using the glass epoxy board
(FR4 40 × 40 × 1.6 mm)

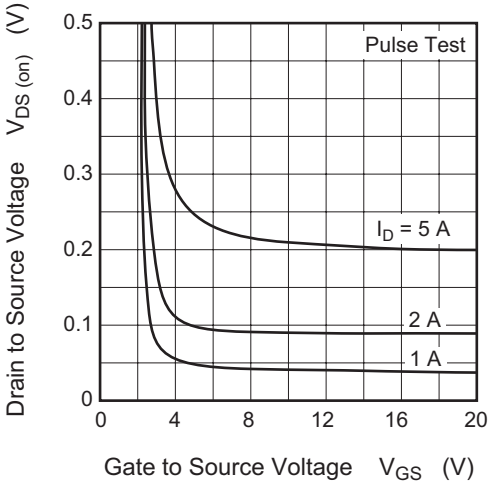
Typical Output Characteristics



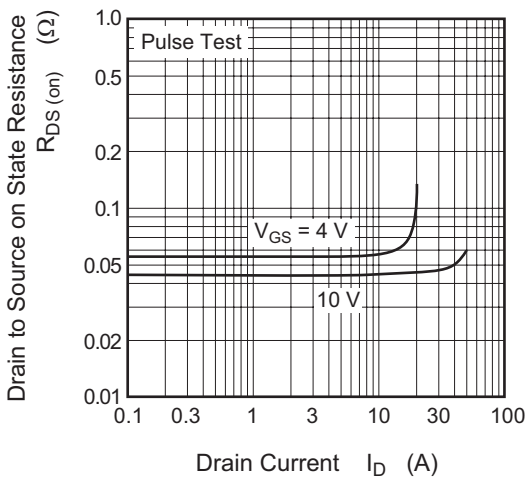
Typical Transfer Characteristics



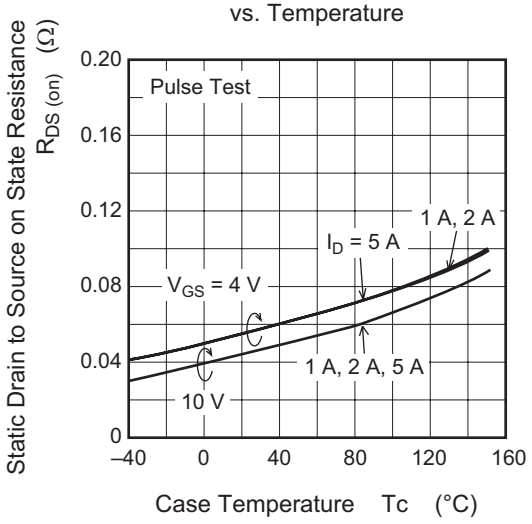
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



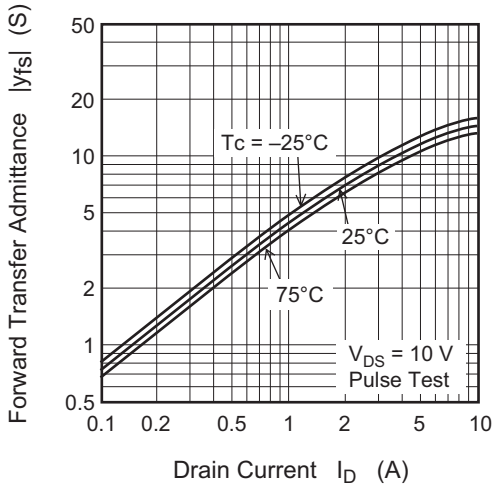
Static Drain to Source on State Resistance
vs. Drain Current



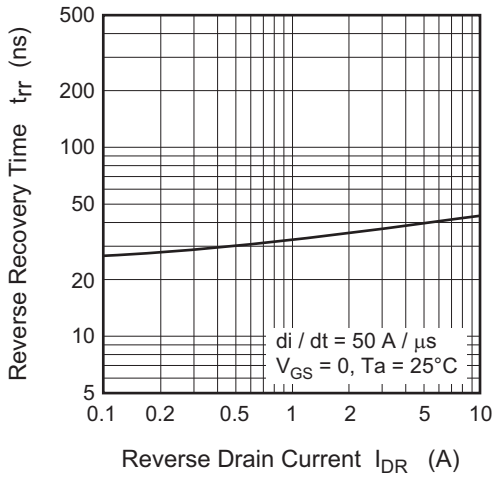
Static Drain to Source on State Resistance vs. Temperature



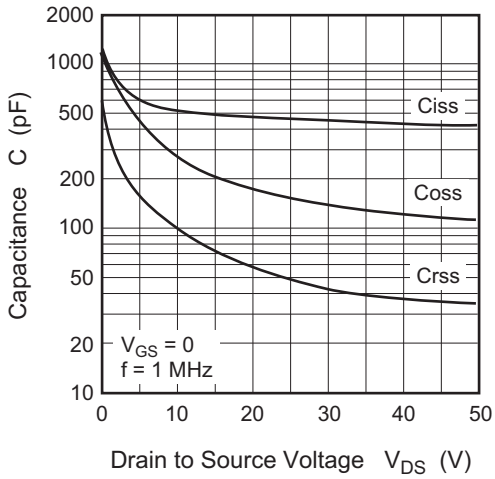
Forward Transfer Admittance vs. Drain Current



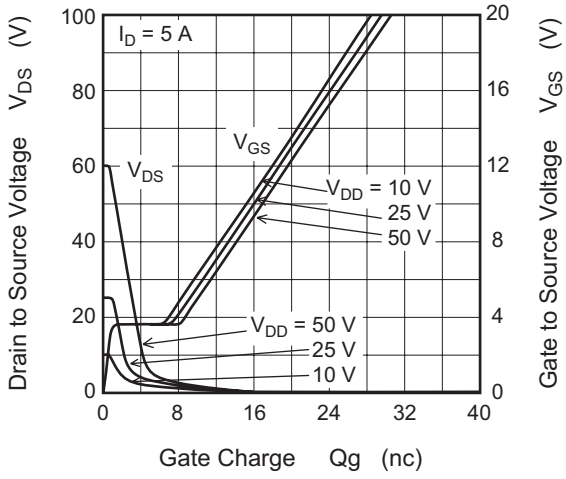
Body-Drain Diode Reverse Recovery Time



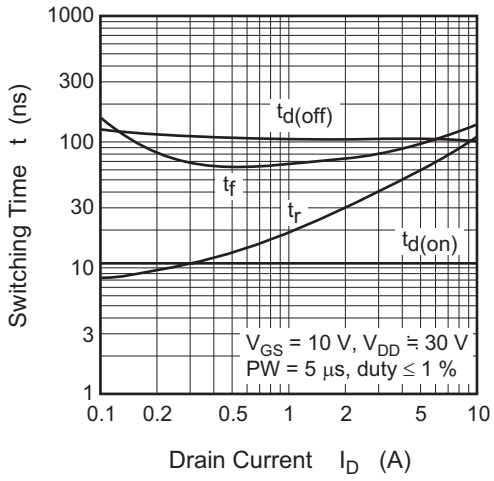
Typical Capacitance vs. Drain to Source Voltage



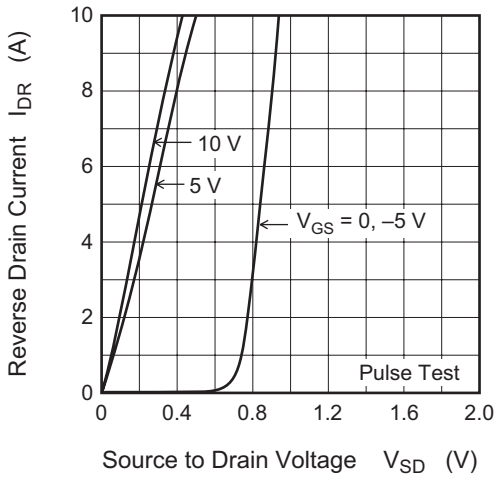
Dynamic Input Characteristics



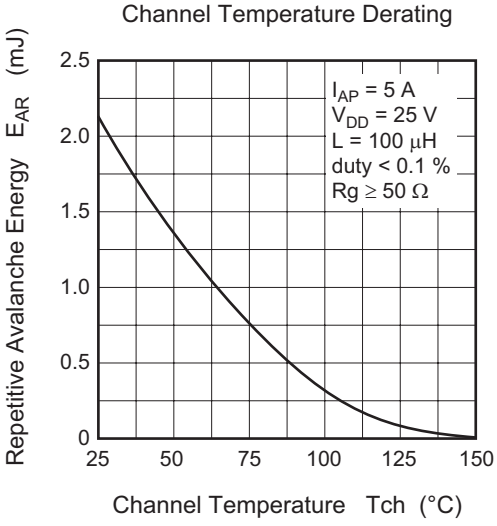
Switching Characteristics



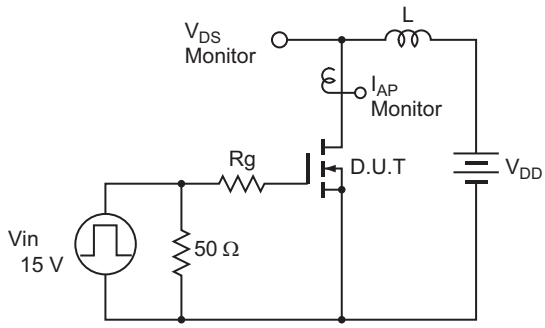
Reverse Drain Current vs.
Source to Drain Voltage



Maximum Avalanche Energy vs.
Channel Temperature Derating

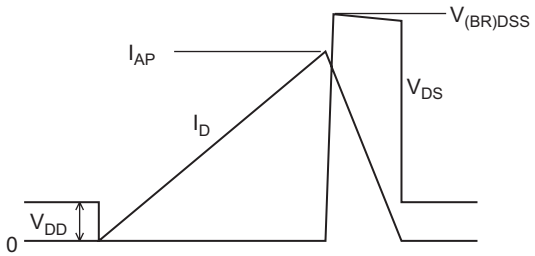


Avalanche Test Circuit

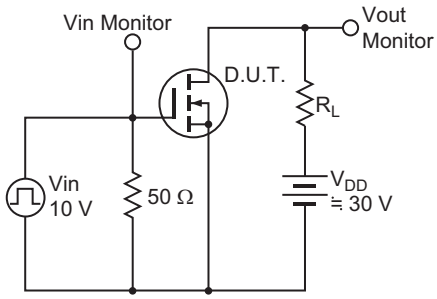


Avalanche Waveform

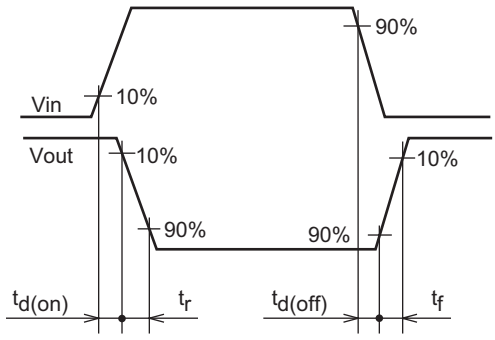
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

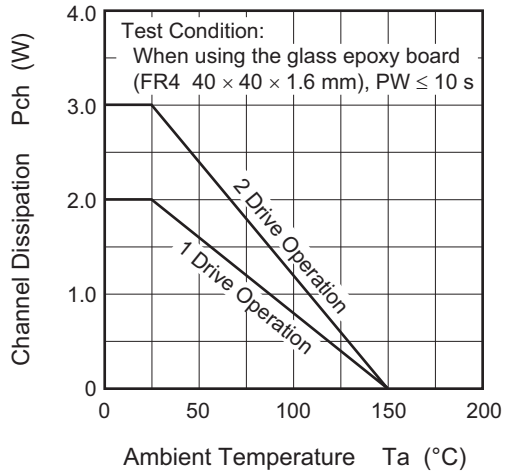


Switching Time Waveform

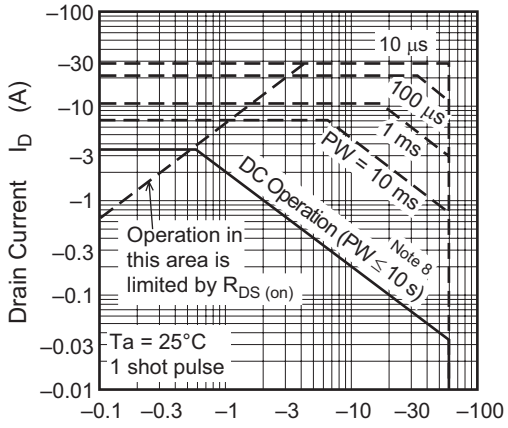


P Channel

Power vs. Temperature Derating

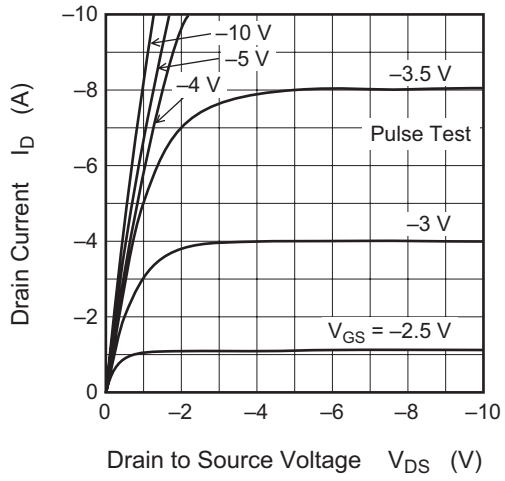


Maximum Safe Operation Area

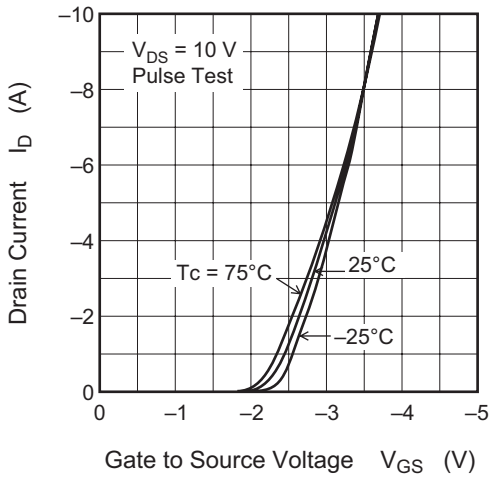


Note 8:
When using the glass epoxy board
(FR4 40 × 40 × 1.6 mm)

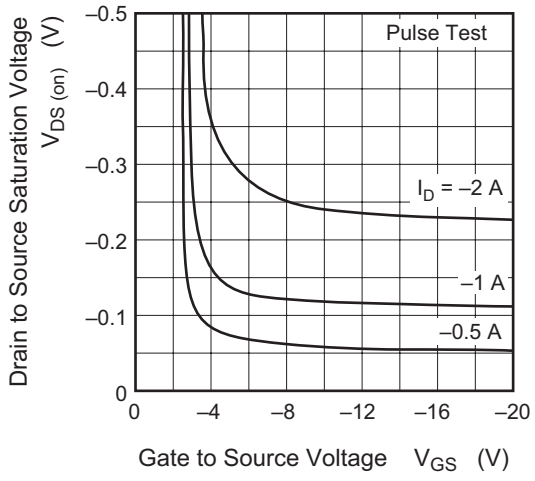
Typical Output Characteristics



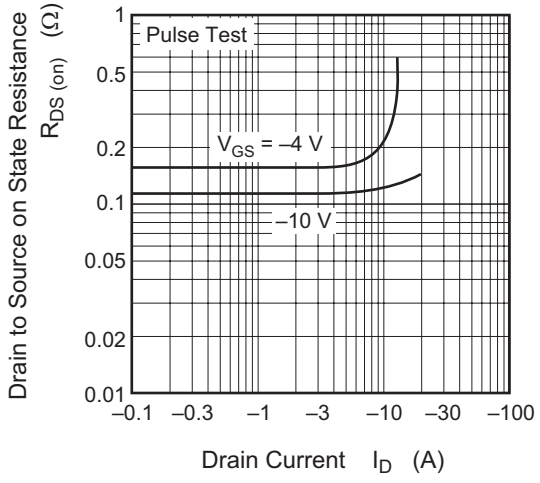
Typical Transfer Characteristics



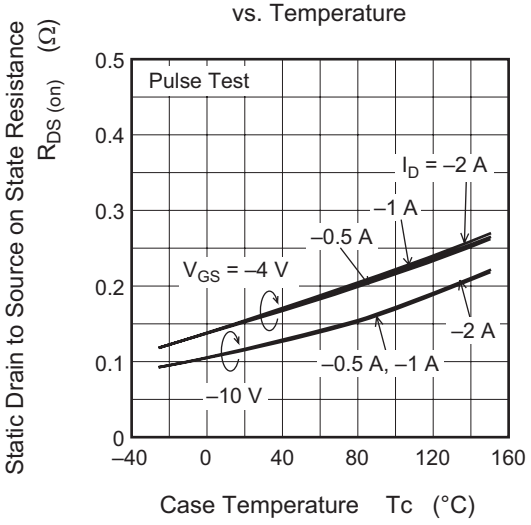
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



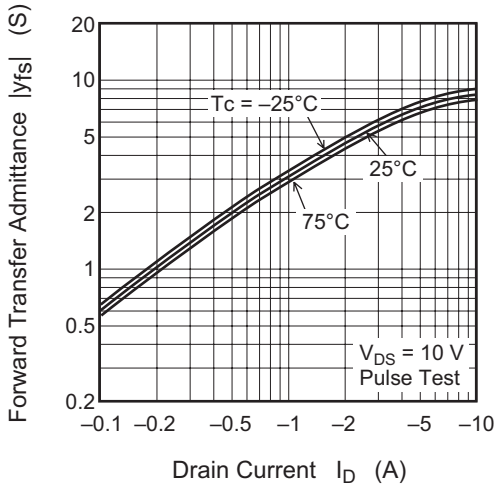
Static Drain to Source on State Resistance
vs. Drain Current



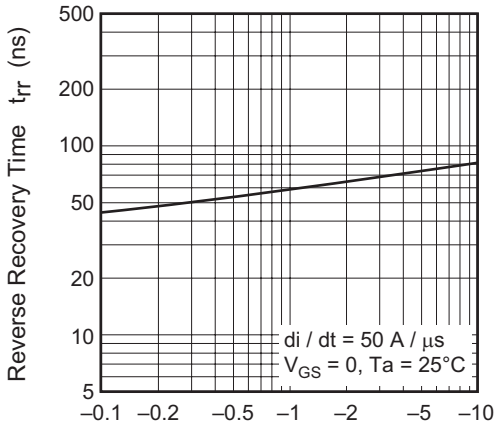
Static Drain to Source on State Resistance vs. Temperature



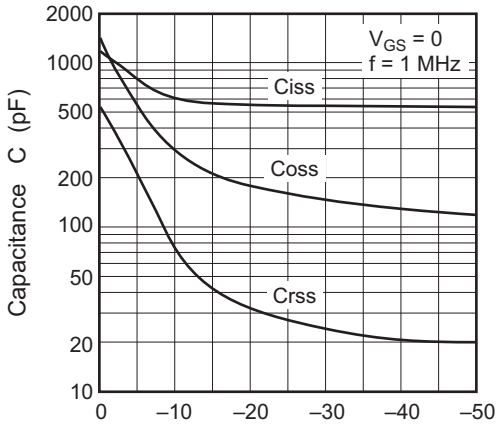
Forward Transfer Admittance vs. Drain Current



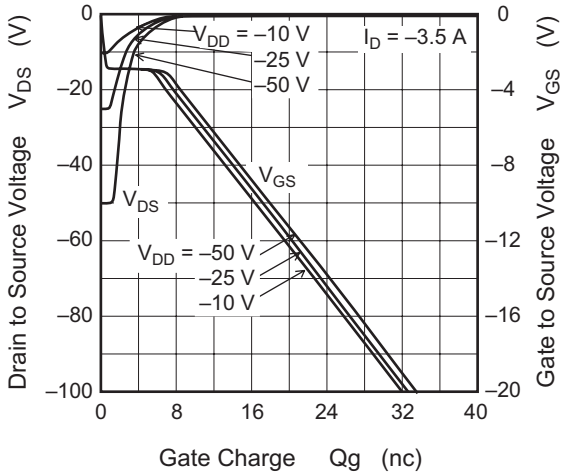
Body-Drain Diode Reverse Recovery Time



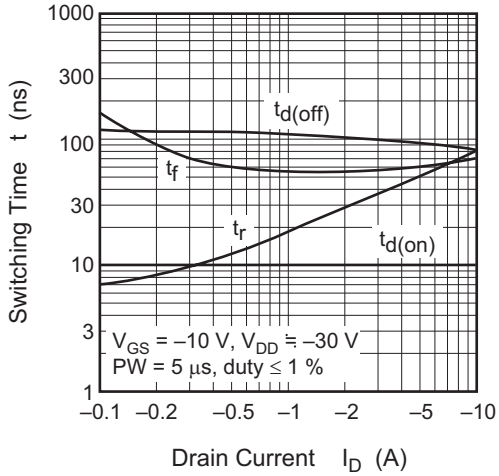
Typical Capacitance vs. Drain to Source Voltage



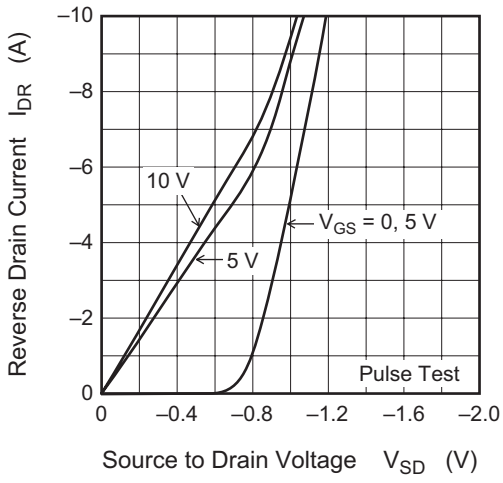
Dynamic Input Characteristics



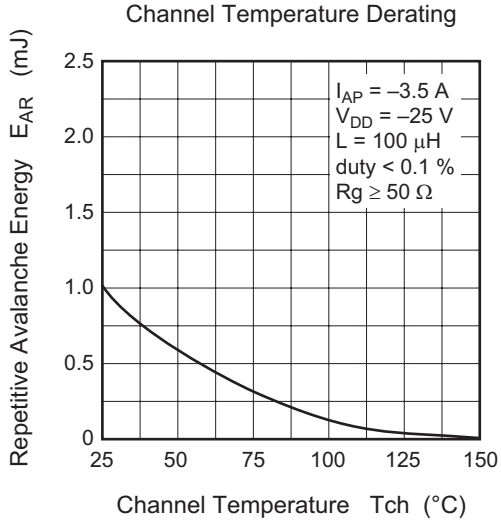
Switching Characteristics



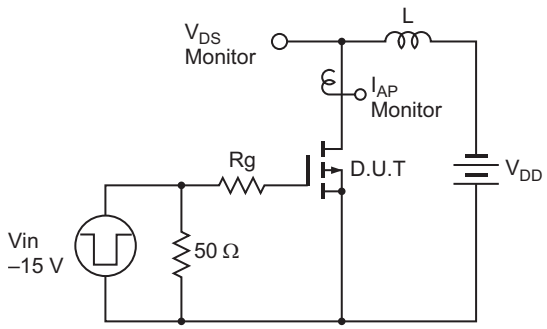
Reverse Drain Current vs. Source to Drain Voltage



Maximum Avalanche Energy vs. Channel Temperature Derating

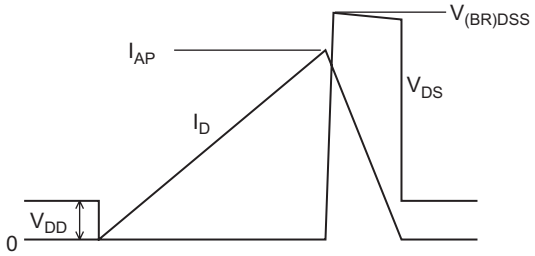


Avalanche Test Circuit

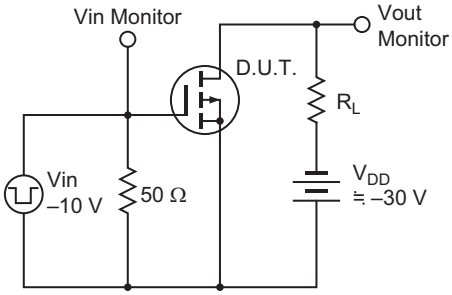


Avalanche Waveform

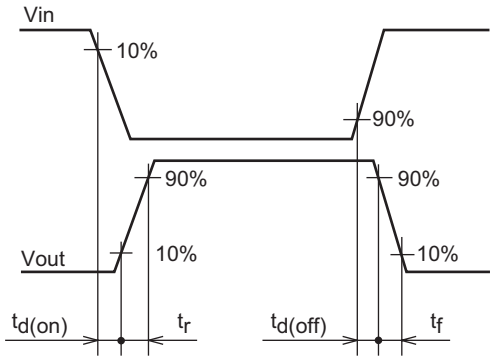
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

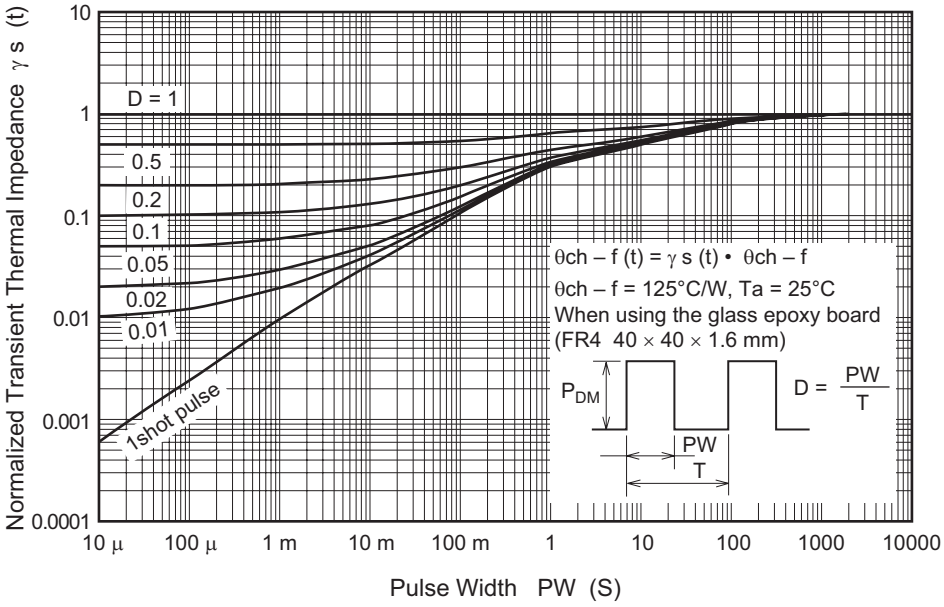


Switching Time Waveform

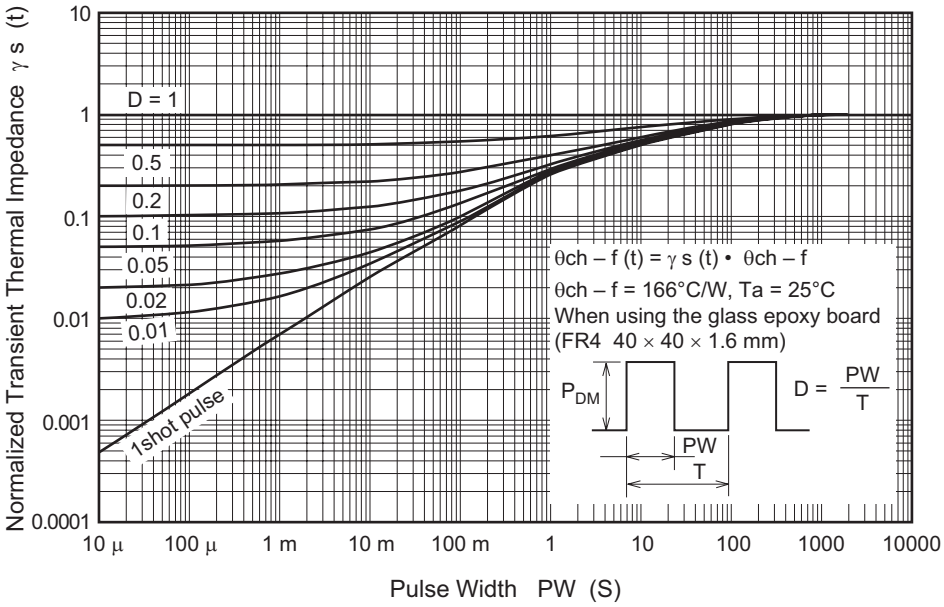


Common

Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)

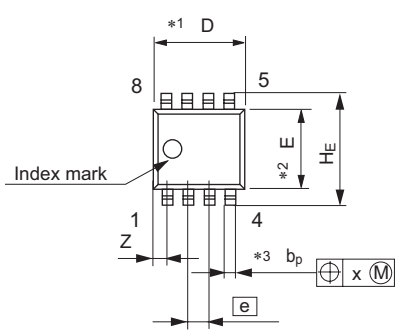


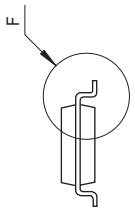
Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)

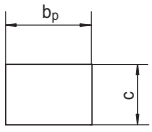


Package Dimensions

JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]
P-SOP8-3.95 × 4.9-1.27	PRSP0008DD-D	FP-8DAV	0.085g

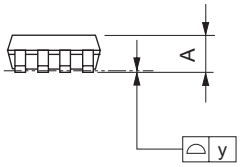


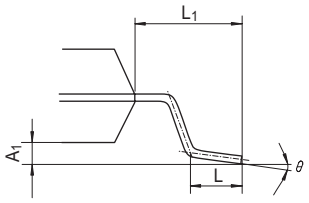




Terminal cross section
(Ni/Pd/Au plating)

NOTE)
1. DIMENSIONS "*1(Nom)" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.





Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.90	5.3
E	—	3.95	—
A_2	—	—	—
A_1	0.10	0.14	0.25
A	—	—	1.75
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.1
Z	—	—	0.75
L	0.40	0.60	1.27
L_1	—	1.08	—

Ordering Information

Part Name	Quantity	Shipping Container
HAT3008R-EL-E	2500 pcs	Taping
HAT3008RJ-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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Colophon .3.0