HA-5147/883

100MHz, Ultra Low Noise, Precision, High Slew Rate Operational Amplifier

June 1998

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **High Slew Rate . . . . . 28V/μs (Min)**
- **Wide Gain Bandwidth ($A_V \geq 10$) . . . . . 100MHz (Min)**
- **Low Noise (at 1kHz) . . . . . 4.5nV/$\sqrt{Hz}$ (Max)**
- **Low Offset Voltage . . . . . .100μV (Max)**
- **Low Offset Drift With Temperature . . . . 1.8μV/^{o}C (Max)**
- **High CMRR . . . . . .100dB (Min)**
- **High Voltage Gain . . . . . 700kV/V (Min)**

Applications

- **High Speed Signal Conditioners**
- **Wide Bandwidth Instrumentation Amplifiers**
- **Low Level Transducer Amplifiers**
- **Fast, Low Level Voltage Comparators**
- **Highest Quality Audio Preamplifiers**
- **Pulse/RF Amplifiers**

Description

The HA-5147/883 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Intersil DI technology and advanced processing techniques, this unique design unites low noise precision instrumentation performance with high speed wideband capability.

This amplifier's impressive list of features include low V_{OS}, wide gain-bandwidth, high open loop gain, and high CMRR. Additionally, this flexible device operates over a wide supply range while consuming only 120mW of power.

Using the HA-5147/883 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than ten.

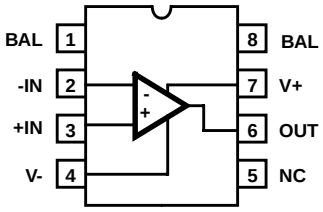
This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5147/883's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits.

Ordering Information

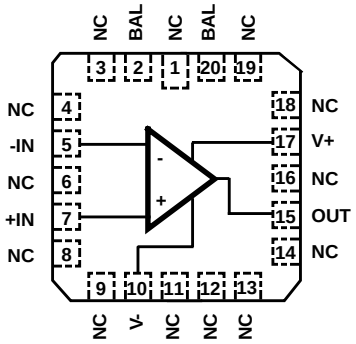
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HA4-5147/883	-55 to 125	20 Ld CLCC	J20.A
HA7-5147/883	-55 to 125	8 Ld CERDIP	F8.3A

Pinouts

HA-5147/883
(CERDIP)
TOP VIEW



HA-5147/883
(CLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
Differential Input Voltage (Note 1). 0.7V
Voltage at Either Input Terminal . . . . . V+ to V-
Input Current. 25mA
Output Current . . . . . Full Short Circuit Protection
ESD Rating. . . . . <2000V

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC
Supply Voltage . . . . . ±15V
$V_{INCM} \leq 1/2$ (V+ - V-)
$R_L \geq 600\Omega$

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	115	28
CLCC Package	65	15

Package Power Dissipation Limit at 75^oC for $T_J \leq 175^oC$
CERDIP Package 870mW
CLCC Package 1.54W
Package Power Dissipation Derating Factor Above 75^oC
CERDIP Package . . . . . $8.7mW/^oC$
CLCC Package . . . . . $15.4mW/^oC$
Maximum Junction Temperature (T_J) . . . . . 175^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: $V_{SUPPLY} = \pm15V$, $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 100k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMP. (^oC)	MIN	MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	25	-100	100	µV
			2, 3	125, -55	-300	300	µV
Input Bias Current	I_B	$V_{CM} = 0V$, $R_S = 10k\Omega, 50\Omega$ $\left(\frac{\lvert+I_B\rvert + \lvert-I_B\rvert}{2}\right)$	1	25	-	80	nA
			2, 3	125, -55	-	150	nA
Input Offset Current	I_{IO}	$V_{CM} = 0V$, $+R_S = 10k\Omega$, $-R_S = 10k\Omega$	1	25	-75	75	nA
			2, 3	125, -55	-135	135	nA
Common Mode Range	+CMR	V+ = +4.7V, V- = -25.3V	1	25	10.3	-	V
			2, 3	125, -55	10.3	-	V
	-CMR	V+ = +25.3V, V- = -4.7V	1	25	-	-10.3	V
			2, 3	125, -55	-	-10.3	V
Large Signal Voltage Gain	$+A_{VOL}$	$V_{OUT} = 0V$ and +10V, $R_L = 2k\Omega$	4	25	700	-	kV/V
			5, 6	125, -55	300	-	kV/V
	$-A_{VOL}$	$V_{OUT} = 0V$ and -10V, $R_L = 2k\Omega$	4	25	700	-	kV/V
			5, 6	125, -55	300	-	kV/V
Common Mode Rejection Ratio	+CMRR	$\Delta V_{CM} = +11V$	1	25	100	-	dB
		$\Delta V_{CM} = +10V$	2, 3	125, -55	100	-	dB
	-CMRR	$\Delta V_{CM} = -11V$	1	25	100	-	dB
		$\Delta V_{CM} = -10V$	2, 3	125, -55	100	-	dB

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Tested at: V_{SUPPLY} = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMP. (^oC)	MIN	MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	R_L = 2kΩ	4	25	11.5	-	V
			5, 6	125, -55	11.5	-	V
	$-V_{OUT1}$	R_L = 2kΩ	4	25	-	-11.5	V
			5, 6	125, -55	-	-11.5	V
	$+V_{OUT2}$	R_L = 600Ω	4	25	10	-	V
	$-V_{OUT2}$	R_L = 600Ω	4	25	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	25	16.5	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	25	-	-16.5	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	25	-	4	mA
			2, 3	125, -55	-	4	mA
	$-I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	25	-4	-	mA
			2, 3	125, -55	-4	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = +14V	1	25	86	-	dB
		ΔV_{SUP} = +13.5V	2, 3	125, -55	86	-	dB
	-PSRR	ΔV_{SUP} = +14V	1	25	86	-	dB
		ΔV_{SUP} = +13.5V	2, 3	125, -55	86	-	dB
Offset Voltage Adjustment	$+V_{IO}$Adj	Note 3	1	25	V_{IO}-1	-	mV
			2, 3	125, -55	V_{IO}-1	-	mV
	$-V_{IO}$Adj	Note 3	1	25	V_{IO}+1	-	mV
			2, 3	125, -55	V_{IO}+1	-	mV

NOTE:

3. Offset adjustment range is [V_{IO} (Measured) ±1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

TABLE 2. AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: V_{SUPPLY} = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +10V/V, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMP. (^oC)	MIN	MAX	UNITS
Slew Rate	+SR	V_{OUT} = -3V to +3V	7	25	28	-	V/µs
	-SR	V_{OUT} = +3V to -3V	7	25	28	-	V/µs
Rise and Fall Time	t_r	V_{OUT} = 0 to +200mV 10% ≤ t_r ≤ 90%	7	25	-	50	ns
	t_f	V_{OUT} = 0 to -200mV 10% ≤ t_f ≤ 90%	7	25	-	50	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	25	-	40	%
	-OS	V_{OUT} = 0 to -200mV	7	25	-	40	%

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Characterized at: V_{SUPPLY} = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_V = +10V/V, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMP. (^oC)	MIN	MAX	UNITS
Average Offset Voltage Drift	$V_{IO}TC$	V_{CM} = 0V	4	-55 to 125	-	1.8	$\mu V/^oC$
Differential Input Resistance	R_{IN}	V_{CM} = 0V	4	25	0.8	-	MΩ
Low Frequency Peak-to-Peak Noise	E_{NP-P}	0.1Hz to 10Hz	4	25	-	0.25	μV_{P-P}
Input Noise Voltage Density	E_N	R_S = 20Ω, f_O = 10Hz	4	25	-	10	$nV/\sqrt{Hz}$
		R_S = 20Ω, f_O = 100Hz	4	25	-	5.6	$nV/\sqrt{Hz}$
		R_S = 20Ω, f_O = 1kHz	4	25	-	4.5	$nV/\sqrt{Hz}$
Input Noise Current Density	I_N	R_S = 2MΩ, f_O = 10Hz	4	25	-	4.0	$pA/\sqrt{Hz}$
		R_S = 2MΩ, f_O = 100Hz	4	25	-	2.3	$pA/\sqrt{Hz}$
		R_S = 2MΩ, f_O = 1kHz	4	25	-	0.6	$pA/\sqrt{Hz}$
Gain Bandwidth Product	GBWP	V_O = 100mV, f_O = 10kHz	4	25	120	-	MHz
		V_O = 100mV, f_O = 1MHz	4	25	100	-	MHz
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	4, 5	25	445	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	4	-55 to 125	±10	-	V/V
Settling Time	t_S	To 0.1% for a 10V Step	4	25	-	600	µs
Output Resistance	R_{OUT}	Open Loop	4	25	-	100	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	4, 6	-55 to 125	-	120	mW

NOTES:

4. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
5. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
6. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on output.)

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 7), 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C and D Endpoints	1

NOTE:

7. PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:

104.3 x 65 x 19 mils
2650 x 1650 x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1.5kÅ

WORST CASE CURRENT DENSITY:

$3.6 \times 10^5 A/cm^2$ at 15mA
This device meets Glassivation Integrity Test Requirement per MIL-STD-883 Method 2021 and MIL-I-38535 Paragraph 30.5.5.4.

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

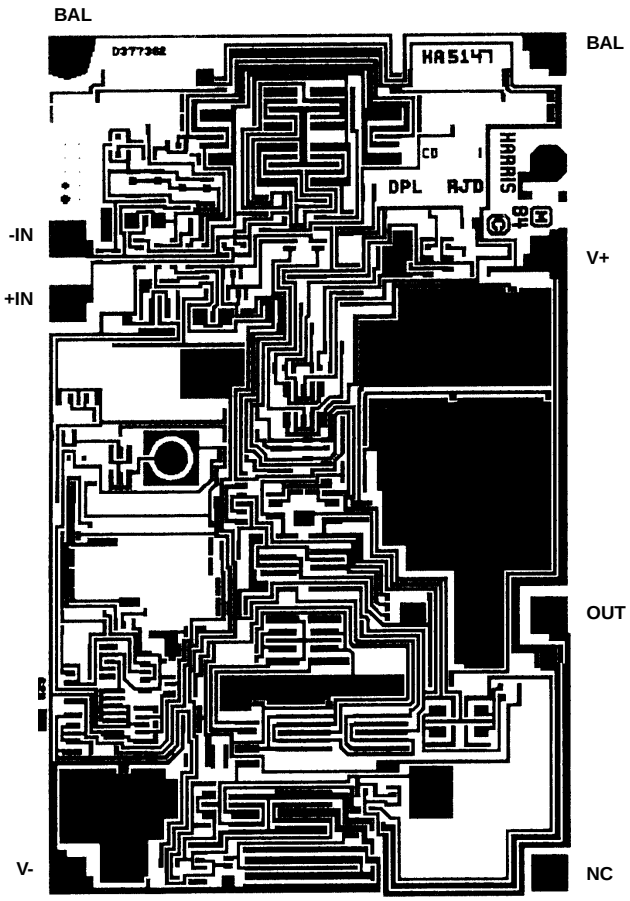
63

PROCESS:

Bipolar Dielectric Isolation

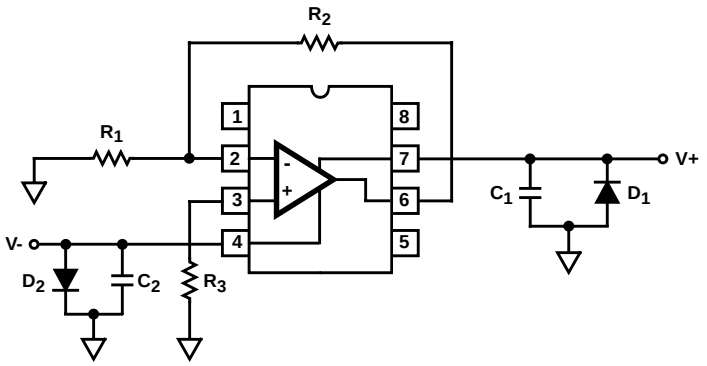
Metallization Mask Layout

HA-5147/883

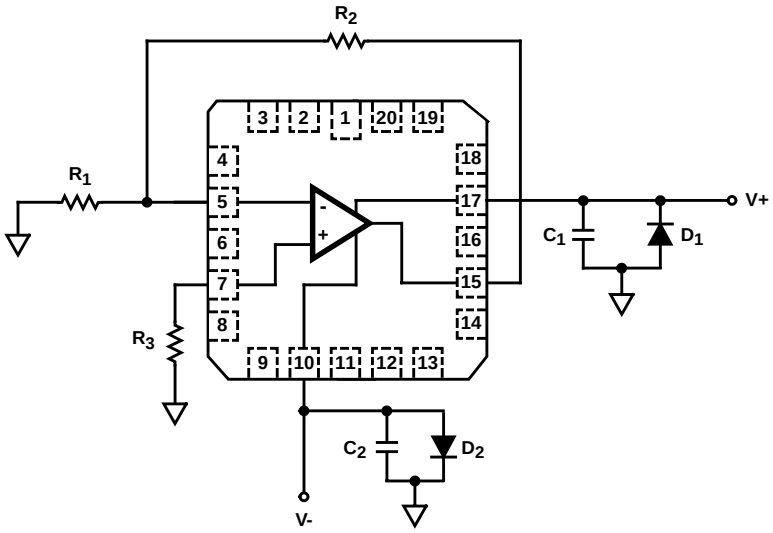


Burn-In Circuits

HA-5147/883 CERDIP



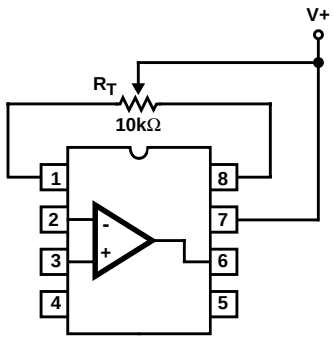
HA-5147/883 CLCC



NOTE:

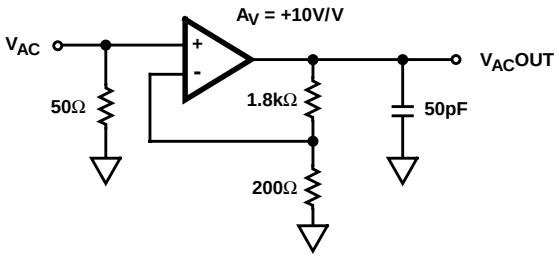
$R_1 = R_3 = 1k\Omega, \pm 5\%, {}^1/_4W$ (Min.)
$R_2 = 10k\Omega, \pm 5\%, {}^1/_4W$ (Min.)
$C_1 = C_2 = 0.01\mu F$/Socket or $0.1\mu F$/Row (Min.)
$D_1 = D_2$ = 1N4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

Typical Performance Information $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, Unless Otherwise Specified

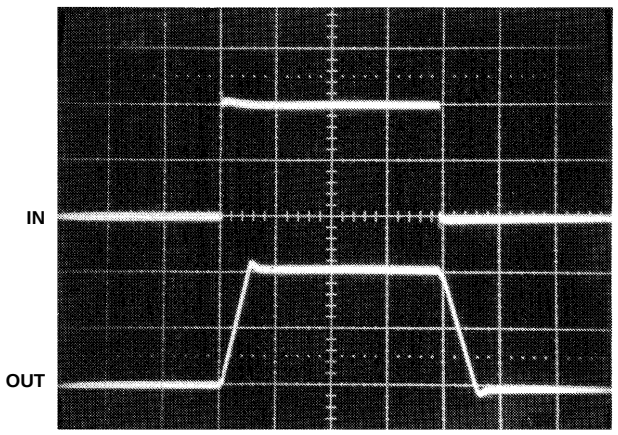


NOTE: Tested offset adjustment range is $|V_{OS} \pm 1mV|$ minimum referred to output. Typical range is ±4mV with $R_T = 10k\Omega$.

SUGGESTED OFFSET VOLTAGE ADJUSTMENT

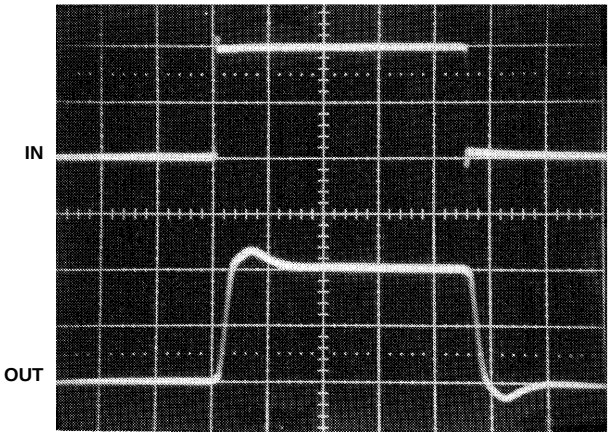


LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



Vertical Scale: Input = 0.5V/Div.
Output = 5V/Div.
Horizontal Scale: 500ns/Div.

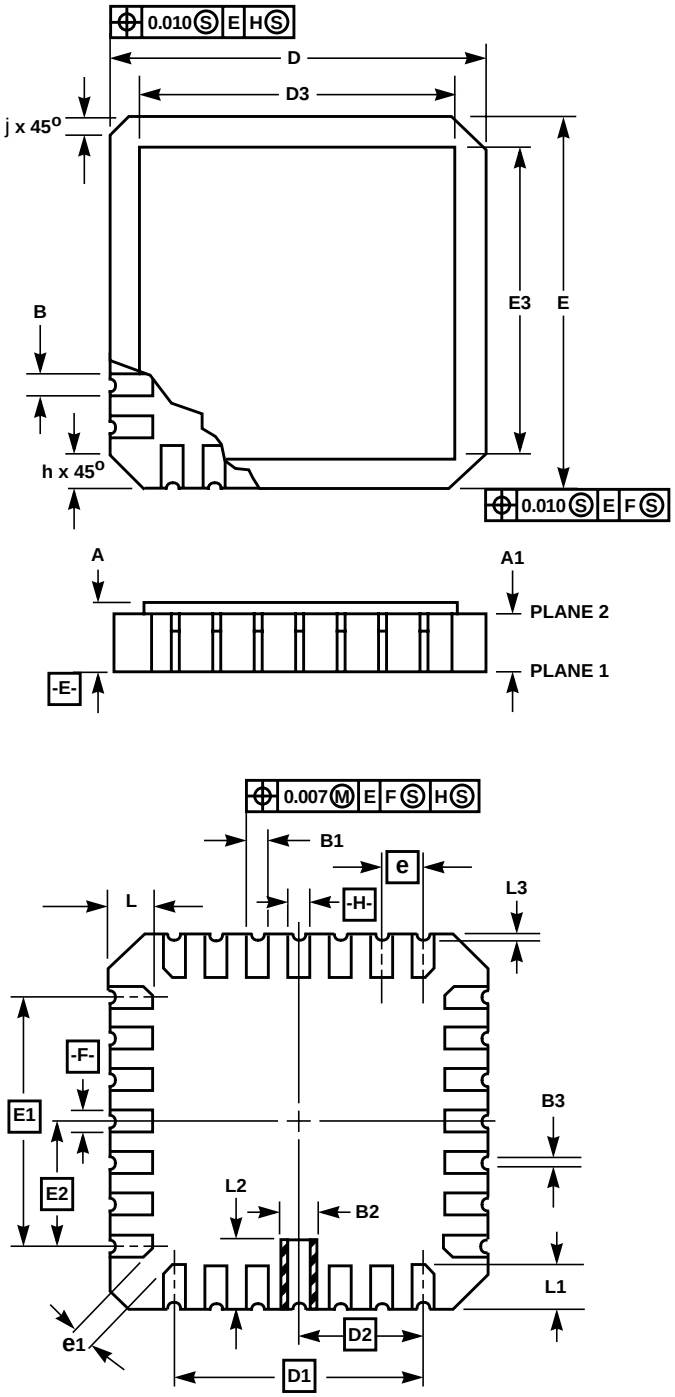
LARGE SIGNAL RESPONSE



Vertical Scale: Input = 10mV/Div.
Output = 100mV/Div.
Horizontal Scale: 100ns/Div.

SMALL SIGNAL RESPONSE

Ceramic Leadless Chip Carrier Packages (CLCC)



J20.A **MIL-STD-1835 CQCC1-N20 (C-2)**
20 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

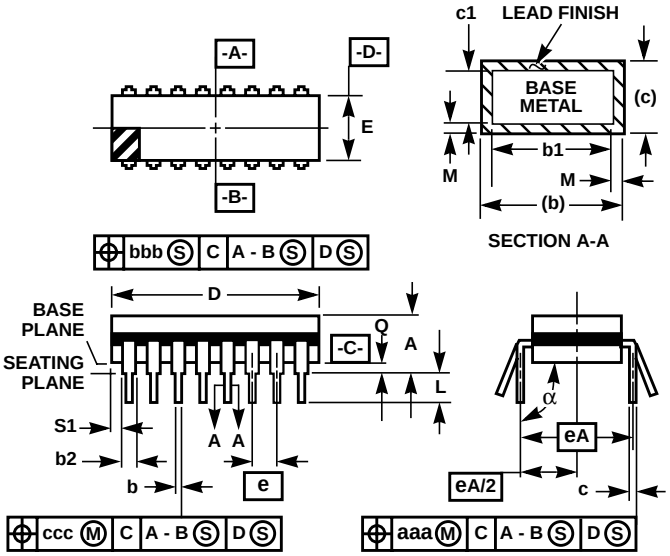
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

Rev. 0 5/18/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol “N” is the maximum number of terminals. Symbols “ND” and “NE” are the number of terminals along the sides of length “D” and “E”, respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer’s option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension “A” controls the overall package thickness. The maximum “A” dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH

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Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029