HA-5020

100MHz Current FeedbackVideo Amplifier With Disable

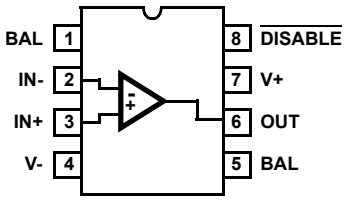
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The HA-5020 is a wide bandwidth, high slew rate amplifier optimized for video applications and gains between 1 and 10. Manufactured on Intersil's Reduced Feature Complementary Bipolar DI process, this amplifier uses current mode feedback to maintain higher bandwidth at a given gain than conventional voltage feedback amplifiers. Since it is a closed loop device, the HA-5020 offers better gain accuracy and lower distortion than open loop buffers.

The HA-5020 features low differential gain and phase and will drive two double terminated 75Ω coax cables to video levels with low distortion. Adding a gain flatness performance of 0.1dB makes this amplifier ideal for demanding video applications. The bandwidth and slew rate of the HA-5020 are relatively independent of closed loop gain. The 100MHz unity gain bandwidth only decreases to 60MHz at a gain of 10. The HA-5020 used in place of a conventional op amp will yield a significant improvement in the speed power product. To further reduce power, HA-5020 has a disable function which significantly reduces supply current, while forcing the output to a true high impedance state. This allows the outputs of multiple amplifiers to be wire-OR'd into multiplexer configurations. The device also includes output short circuit protection and output offset voltage adjustment.For multi channel versions of the HA-5020 see the HA5022 dual with disable, HA5023 dual, HA5013 triple and HA5024 quad with disable op amp data sheets.

Pinout

HA-5020
(PDIP, SOIC)
TOP VIEW



Features

- Wide Unity Gain Bandwidth 100MHz
- Slew Rate 800V/µs
- Output Current . . . . . ±30mA (Min)
- Drives 3.5V into 75Ω
- Differential Gain 0.03%
- Differential Phase . . . . . 0.03°
- Low Input Voltage Noise . . . . . 4.5nV/$\sqrt{Hz}$
- Low Supply Current . . . . . 10mA (Max)
- Wide Supply Range . . . . . ±5V to ±15V
- Output Enable/Disable
- High Performance Replacement for EL2020
- Pb-Free (RoHS Compliant)

Applications

- Unity Gain Video/Wideband Buffer
- Video Gain Block
- Video Distribution Amp/Coax Cable Driver
- Flash A/D Driver
- Waveform Generator Output Driver
- Current to Voltage Converter; D/A Output Buffer
- Radar Systems
- Imaging Systems

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (PB-free	PKG. DWG. #
HA3-5020-5Z (Note 2) **(No longer available, recommended replacement: HA9P5020-5Z, HA9P5020-5ZX96)**	HA3- 5020-5Z	0 to +75	8 Ld PDIP	E8.3
HA9P5020-5Z (Note 2)	50205Z	0 to +75	8 Ld SOIC	M8.15
HA9P5020-5ZX96 (Note 1)	50205Z	0 to +75	8 Ld SOIC (Tape and Reel)	M8.15

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (Note 3)

Voltage Between V+ and V- Terminals 36V
DC Input Voltage . . . . . $\pm V_{SUPPLY}$
Differential Input Voltage 10V
Output Current . . . . . Short Circuit Protected

Operating Conditions

Temperature Range . . . . . 0°C to +75°C

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package*	120	N/A
SOIC Package	165	N/A

Maximum Junction Temperature (Plastic Packages, Note 3) . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. Maximum power dissipation, including output load, must be designed to maintain junction temperature below +150°C for plastic packages.
4. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

$V_{SUPPLY} = \pm 15V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage (Notes 6, 17)		25	-	2	8	mV
		Full	-	-	10	mV
Average Input Offset Voltage Drift		Full	-	10	-	µV/°C
V_{IO} Common Mode Rejection Ratio (Note 17)	$V_{CM} = \pm 10V$	25	60	-	-	dB
		Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio (Note 17)	$\pm 4.5V \leq V_S \leq \pm 18V$	25	64	-	-	dB
		Full	60	-	-	dB
Non-Inverting Input (+IN) Current (Note 17)		25	-	3	8	µA
		Full	-	-	20	µA
+IN Common Mode Rejection	$V_{CM} = \pm 10V$	25	-	-	0.1	µA/V
		Full	-	-	0.5	µA/V
+IN Power Supply Rejection	$\pm 4.5V \leq V_S \leq \pm 18V$	25	-	-	0.06	µA/V
		Full	-	-	0.2	µA/V
Inverting Input (-IN) Current (Note 17)		25	-	12	20	µA
		Full	-	25	50	µA
-IN Common Mode Rejection	$V_{CM} = \pm 10V$	25	-	-	0.4	µA/V
		Full	-	-	0.5	µA/V
-IN Power Supply Rejection	$\pm 4.5V \leq V_S \leq \pm 18V$	25	-	-	0.2	µA/V
		Full	-	-	0.5	µA/V
TRANSFER CHARACTERISTICS						
Transimpedance (Notes 12, 17)		25	3500	-	-	V/mA
		Full	1000	-	-	V/mA
Open Loop DC Voltage Gain (Note 12)	$R_L = 400\Omega$, $V_{OUT} = \pm 10V$	25	70	-	-	dB
		Full	65	-	-	dB
Open Loop DC Voltage Gain	$R_L = 100\Omega$, $V_{OUT} = \pm 2.5V$	25	60	-	-	dB
		Full	55	-	-	dB

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Note 17)	$R_L = 150\Omega$	25 to 85	±12	±12.7	-	V
		-40 to 0	±11	±11.8	-	V
Output Current (Guaranteed by Output Voltage Test)		25	±30	±31.7	-	mA
		Full	±27.5	-	-	mA
POWER SUPPLY CHARACTERISTICS						
Quiescent Supply Current (Note 17)		Full	-	7.5	10	mA
Supply Current, Disabled (Note 17)	$\overline{DISABLE} = 0V$	Full	-	5	7.5	mA
$\overline{Disable}$ Pin Input Current	$\overline{DISABLE} = 0V$	Full	-	1.0	1.5	mA
Minimum Pin 8 Current to Disable (Note 7)		Full	350	-	-	µA
Maximum Pin 8 Current to Enable (Note 8)		Full	-	-	20	µA
AC CHARACTERISTICS ($A_V = +1$)						
Slew Rate (Note 9)		25	600	800	-	V/µs
		Full	500	700	-	V/µs
Full Power Bandwidth (Note 10) (Guaranteed by Slew Rate Test)		25	9.6	12.7	-	MHz
		Full	8.0	11.1	-	MHz
Rise Time (Note 11)		25	-	5	-	ns
Fall Time (Note 11)		25	-	5	-	ns
Propagation Delay (Notes 11, 17)		25	-	6	-	ns
-3dB Bandwidth (Note 17)	$V_{OUT} = 100mV$	25	-	100	-	MHz
Settling Time to 1%	10V Output Step	25	-	45	-	ns
Settling Time to 0.25%	10V Output Step	25	-	100	-	ns
AC CHARACTERISTICS ($A_V = +10$, $R_F = 383\Omega$)						
Slew Rate (Notes 9, 12)		25	900	1100	-	V/µs
		Full	700	-	-	V/µs
Full Power Bandwidth (Note 10) (Guaranteed by Slew Rate Test)		25	14.3	17.5	-	MHz
		Full	11.1	-	-	MHz
Rise Time (Note 11)		25	-	8	-	ns
Fall Time (Note 11)		25	-	8	-	ns
Propagation Delay (Notes 11, 17)		25	-	9	-	ns
-3dB Bandwidth	$V_{OUT} = 100mV$	25	-	60	-	MHz
Settling Time to 1%	10V Output Step	25	-	55	-	ns
Settling Time to 0.1%	10V Output Step	25	-	90	-	ns
INTERSIL VALUE ADDED SPECIFICATIONS						
Input Noise Voltage (Note 17)	f = 1kHz	25	-	4.5	-	$nV/\sqrt{Hz}$
+Input Noise Current (Note 17)	f = 1kHz	25	-	2.5	-	$pA/\sqrt{Hz}$
-Input Noise Current (Note 17)	f = 1kHz	25	-	25	-	$pA/\sqrt{Hz}$
Input Common Mode Range		Full	±10	±12	-	V
$-I_{BIAS}$ Adjust Range (Note 6)		Full	±25	±40	-	µA
Overshoot (Note 17)		25	-	7	-	%

Electrical Specifications V_{SUPPLY} = ±15V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, C_L ≤ 10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Output Current, Short Circuit (Note 17)	V_{IN} = ±10V, V_{OUT} = 0V	Full	±50	±65	-	mA
Output Current, Disabled (Note 17)	$\overline{DISABLE}$ = 0V, V_{OUT} = ±10V	Full	-	-	1	µA
Output Disable Time (Notes 13, 17)		25	-	10	-	µs
Output Enable Time (Notes 14, 17)		25	-	200	-	ns
Supply Voltage Range		25	±5	-	±15	V
Output Capacitance, Disabled (Note 15)	$\overline{DISABLE}$ = 0V	25	-	6	-	pF
VIDEO CHARACTERISTICS						
Differential Gain (Notes 16, 17)	R_L = 150Ω	25	-	0.03	-	%
Differential Phase (Notes 16, 17)	R_L = 150Ω	25	-	0.03	-	°
Gain Flatness	To 5MHz	25	-	0.1	-	dB

Electrical Specifications V+ = +5V, V- = -5V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, C_L ≤10pF, Unless Otherwise Specified. Parameters are not tested. The limits are guaranteed based on lab characterizations, and reflect lot-to-lot variation.

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage (Notes 6, 17)		25	-	2	8	mV
		Full	-	-	10	mV
Average Input Offset Voltage Drift		Full	-	10	-	µV/°C
V_{IO} Common Mode Rejection Ratio (Notes 17, 18)		25	50	-	-	dB
		Full	35	-	-	dB
V_{IO} Power Supply Rejection Ratio (Note 17)	±3.5V ≤ V_S ≤ ±6.5V	25	55	-	-	dB
		Full	50	-	-	dB
Non-Inverting Input (+IN) Current (Note 17)		25	-	3	8	µA
		Full	-	-	20	µA
+IN Common Mode Rejection (Note 18)		25	-	-	0.1	µA/V
		Full	-	-	0.5	µA/V
+IN Power Supply Rejection	±3.5V ≤ V_S ≤ ±6.5V	25	-	-	0.06	µA/V
		Full	-	-	0.2	µA/V
Inverting Input (-IN) Current (Note 17)		25	-	12	20	µA
		Full	-	25	50	µA
-IN Common Mode Rejection (Note 18)		25	-	-	0.4	µA/V
		Full	-	-	0.5	µA/V
-IN Power Supply Rejection	±3.5V ≤ V_S ≤ ±6.5V	25	-	-	0.2	µA/V
		Full	-	-	0.5	µA/V
TRANSFER CHARACTERISTICS						
Transimpedance (Notes 12, 17)		25	1000	-	-	V/mA
		Full	850	-	-	V/mA
Open Loop DC Voltage Gain	R_L = 400Ω, V_{OUT} = ±2.5V	25	65	-	-	dB
		Full	60	-	-	dB

Electrical Specifications $V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified. Parameters are not tested. The limits are guaranteed based on lab characterizations, and reflect lot-to-lot variation. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Open Loop DC Voltage Gain	$R_L = 100\Omega$, $V_{OUT} = \pm 2.5V$	25	50	-	-	dB
		Full	45	-	-	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Note 17)		25 to 85	±2.5	±3.0	-	V
		-40 to 0	±2.5	±3.0	-	V
Output Current (Guaranteed by Output Voltage Test)	$R_L = 100\Omega$	25	±16.6	±20	-	mA
		Full	±16.6	±20	-	mA
POWER SUPPLY CHARACTERISTICS						
Quiescent Supply Current (Note 17)		Full	-	7.5	10	mA
Supply Current, Disabled (Note 17)	$\overline{DISABLE} = 0V$	Full	-	5	7.5	mA
$\overline{Disable}$ Pin Input Current	$\overline{DISABLE} = 0V$	Full	-	1.0	1.5	mA
Minimum Pin 8 Current to Disable (Note 19)		Full	350	-	-	µA
Maximum Pin 8 Current to Enable (Note 8)		Full	-	-	20	µA
AC CHARACTERISTICS ($A_V = +1$)						
Slew Rate (Note 20)		25	215	400	-	V/µs
Full Power Bandwidth (Note 21)		25	22	28	-	MHz
Rise Time (Note 11)		25	-	6	-	ns
Fall Time (Note 11)		25	-	6	-	ns
Propagation Delay (Note 11)		25	-	6	-	ns
Overshoot		25	-	4.5	-	%
-3dB Bandwidth (Note 17)	$V_{OUT} = 100mV$	25	-	125	-	MHz
Settling Time to 1%	2V Output Step	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	25	-	75	-	ns
AC CHARACTERISTICS ($A_V = +2$, $R_F = 681\Omega$)						
Slew Rate (Note 20)		25	-	475	-	V/µs
Full Power Bandwidth (Note 21)		25	-	26	-	MHz
Rise Time (Note 11)		25	-	6	-	ns
Fall Time (Note 11)		25	-	6	-	ns
Propagation Delay (Note 11)		25	-	6	-	ns
Overshoot		25	-	12	-	%
-3dB Bandwidth (Note 17)	$V_{OUT} = 100mV$	25	-	95	-	MHz
Settling Time to 1%	2V Output Step	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	25	-	100	-	ns
AC CHARACTERISTICS ($A_V = +10$, $R_F = 383\Omega$)						
Slew Rate (Note 20)		25	350	475	-	V/µs
Full Power Bandwidth (Note 21)		25	28	38	-	MHz
Rise Time (Note 11)		25	-	8	-	ns
Fall Time (Note 11)		25	-	9	-	ns
Propagation Delay (Note 11)		25	-	9	-	ns
Overshoot		25	-	1.8	-	%

Electrical Specifications $V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified. Parameters are not tested. The limits are guaranteed based on lab characterizations, and reflect lot-to-lot variation. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
-3dB Bandwidth (Note 17)	V_{OUT} = 100mV	25	-	65	-	MHz
Settling Time to 1%	2V Output Step	25	-	75	-	ns
Settling Time to 0.25%	2V Output Step	25	-	130	-	ns
INTERSIL VALUE ADDED SPECIFICATIONS						
Input Noise Voltage (Note 17)	f = 1kHz	25	-	4.5	-	$nV/\sqrt{Hz}$
+Input Noise Current (Note 17)	f = 1kHz	25	-	2.5	-	$pA/\sqrt{Hz}$
-Input Noise Current (Note 17)	f = 1kHz	25	-	25	-	$pA/\sqrt{Hz}$
Input Common Mode Range		Full	±2.5V	–	-	V
Output Current, Short Circuit	V_{IN} = ±2.5V, V_{OUT} = 0V	Full	±40	±60	-	mA
Output Current, Disabled (Note 17)	$\overline{DISABLE}$ = 0V, V_{OUT} = ±2.5V, V_{IN} = 0V	Full	-	-	2	µA
Output Disable Time (Notes 17, 23)		25	-	40	-	µs
Output Enable Time (Notes 17, 21)		25	-	40	-	ns
Supply Voltage Range		25	±5	-	±15	V
Output Capacitance, Disabled (Note 22)	$\overline{DISABLE}$ = 0V	25	-	6	-	pF
VIDEO CHARACTERISTICS						
Differential Gain (Notes 16, 17)	$R_L = 150\Omega$	25	-	0.03	-	%
Differential Phase (Notes 16, 17)	$R_L = 150\Omega$	25	-	0.03	-	°
Gain Flatness	To 5MHz	25	-	0.1	-	dB

NOTES:

5. Suggested V_{OS} Adjust Circuit: The inverting input current ($-I_{BIAS}$) can be adjusted with an external 10kΩ pot between pins 1 and 5, wiper connected to V+. Since $-I_{BIAS}$ flows through the feedback resistor (R_F), the result is an adjustment in offset voltage. The amount of offset voltage adjustment is determined by the value of R_F ($\Delta V_{OS} = \Delta -I_{BIAS} * R_F$).
6. $R_L = 100\Omega$, $V_{IN} = 10V$. This is the minimum current which must be pulled out of the $\overline{Disable}$ pin in order to disable the output. The output is considered disabled when $-10mV \leq V_{OUT} \leq +10mV$.
7. $V_{IN} = 0V$. This is the maximum current that can be pulled out of the $\overline{Disable}$ pin with the HA-5020 remaining enabled. The HA-5020 is considered disabled when the supply current has decreased by at least 0.5mA.
8. V_{OUT} switches from -10V to +10V, or from +10V to -10V. Specification is from the 25% to 75% points.
9. $FPBW = \frac{Slew\ Rate}{2\pi V_{PEAK}}$; $V_{PEAK} = 10V$.
10. $R_L = 100\Omega$, $V_{OUT} = 1V$. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
11. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
12. V_{IN} = +10V, $\overline{Disable}$ = +15V to 0V. Measured from the 50% point of $\overline{Disable}$ to V_{OUT} = 0V.
13. V_{IN} = +10V, $\overline{Disable}$ = 0V to +15V. Measured from the 50% point of $\overline{Disable}$ to V_{OUT} = 10V.
14. V_{IN} = 0V, Force V_{OUT} from 0V to ±10V, $t_R = t_F$ = 50ns.
15. Measured with a VM700A video tester using a NTC-7 composite VITS.
16. See “Typical Performance Curves” on page 12 for more information.
17. V_{CM} = ±2.5V. At -40°C product is tested at V_{CM} = ±2.25V because short test duration does not allow self heating.
18. $R_L = 100\Omega$. $V_{IN} = 2.5V$. This is the minimum current which must be pulled out of the $\overline{Disable}$ pin in order to disable the output. The output is considered disabled when $-10mV \leq V_{OUT} \leq +10mV$.
19. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
20. $FPBW = \frac{Slew\ Rate}{2\pi V_{PEAK}}$; $V_{PEAK} = 2V$.
21. V_{IN} = 0V, Force V_{OUT} from 0V to ±2.5V, $t_R = t_F$ = 50ns.
22. V_{IN} = +2V, $\overline{Disable}$ = +5V to 0V. Measured from the 50% point of $\overline{Disable}$ to V_{OUT} = 0V.
23. V_{IN} = +2V, $\overline{Disable}$ = 0V to +5V. Measured from the 50% point of $\overline{Disable}$ to V_{OUT} = 2V.

Test Circuits and Waveforms

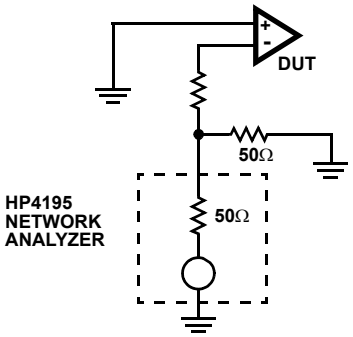


FIGURE 1. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

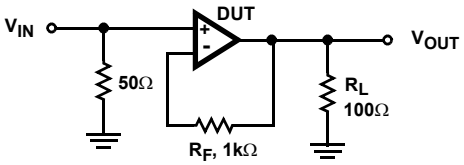


FIGURE 2. SMALL SIGNAL PULSE RESPONSE CIRCUIT

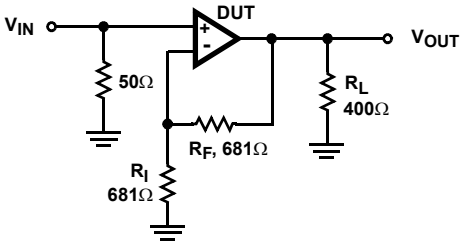
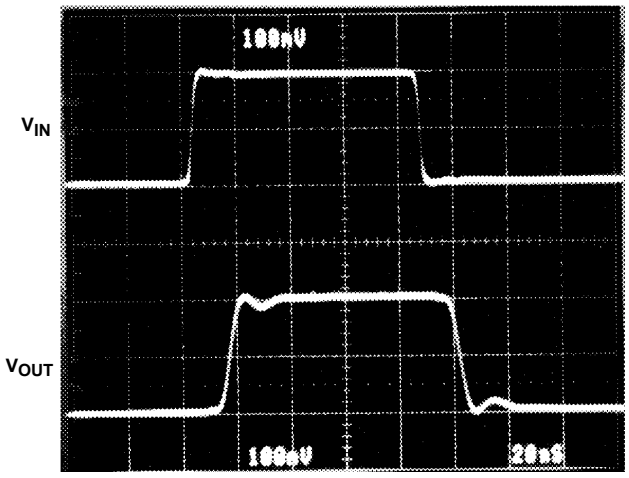
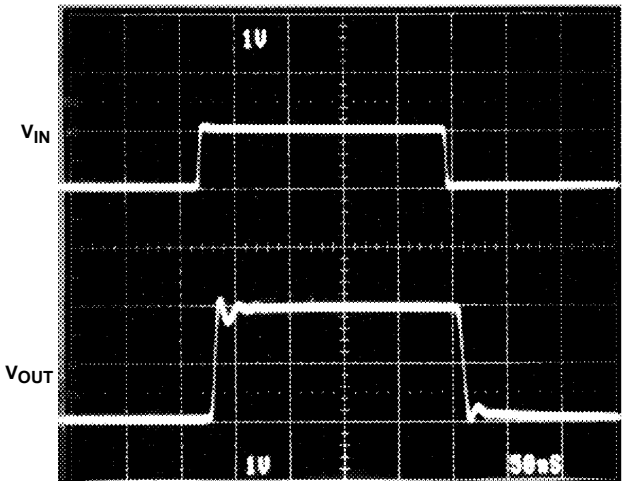


FIGURE 3. LARGE SIGNAL PULSE RESPONSE CIRCUIT



Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div.

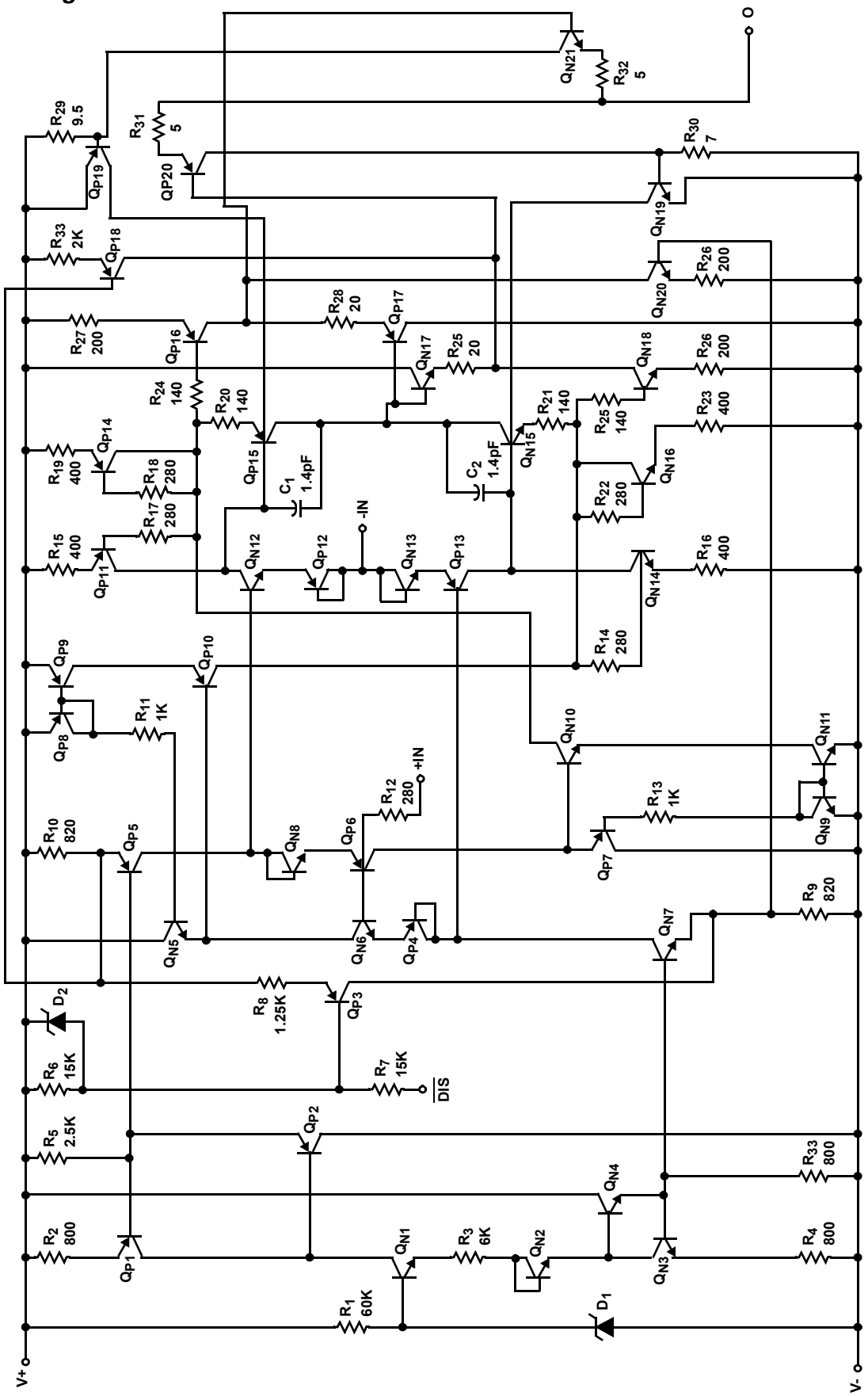
FIGURE 4. SMALL SIGNAL RESPONSE



Vertical Scale: V_{IN} = 1V/Div., V_{OUT} = 1V/Div.
Horizontal Scale: 50ns/Div.

FIGURE 5. LARGE SIGNAL RESPONSE

Schematic Diagram



Application Information

Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response illustrate the performance of the HA-5020 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HA-5020 design is optimized for a 1000Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those components connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value (10µF) tantalum or electrolytic capacitor in parallel with a small value (0.1µF) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to -IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 6.

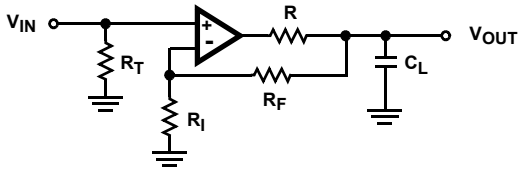


FIGURE 6. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resistor is highly dependent on the load, but 27Ω has been determined to be a good starting value.

Enable/Disable Function

When enabled the amplifier functions as a normal current feedback amplifier with all of the data in the electrical specifications table being valid and applicable. When disabled the amplifier output assumes a true high impedance state and the supply current is reduced significantly.

The circuit shown in Figure 7 is a simplified schematic of the enable/disable function. The large value resistors in series with the DISABLE pin makes it appear as a current source to the driver. When the driver pulls this pin low current flows out of the pin and into the driver. This current, which may be as large as 350µA when external circuit and process variables are at their extremes, is required to insure that point "A" achieves the proper potential to disable the output. The driver must have the compliance and capability of sinking all of this current.

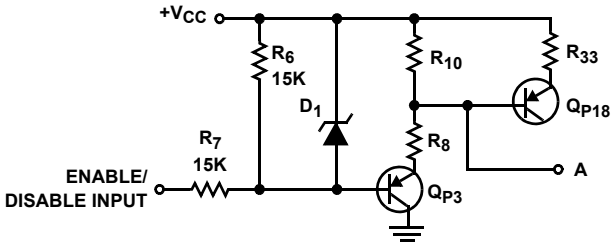


FIGURE 7. SIMPLIFIED SCHEMATIC OF ENABLE/DISABLE FUNCTION

When V_{CC} is +5V the DISABLE pin may be driven with a dedicated TTL gate. The maximum low level output voltage of the TTL gate, 0.4V, has enough compliance to insure that the amplifier will always be disabled even though D_1 will not turn on, and the TTL gate will sink enough current to keep point "A" at its proper voltage. When V_{CC} is greater than +5V the DISABLE pin should be driven with an open collector device that has a breakdown rating greater than V_{CC}.

Referring to Figure 7, it can be seen that R_6 will act as a pull-up resistor to $+V_{CC}$ if the DISABLE pin is left open. In those cases where the enable/disable function is not required on all circuits some circuits can be permanently enabled by letting the DISABLE pin float. If a driver is used to set the enable/disable level, be sure that the driver does not sink more than 20µA when the DISABLE pin is at a high level. TTL gates, especially CMOS versions, do not violate this criteria so it is permissible to control the enable/disable function with TTL.

Typical Applications

Two Channel Video Multiplexer

Referring to the amplifier U_{1A} in Figure 8, R_1 terminates the cable in its characteristic impedance of 75Ω, and R_4 back terminates the cable in its characteristic impedance. The amplifier is set up in a gain configuration of +2 to yield an overall network gain of +1 when driving a double terminated cable. The value of R_3 can be changed if a different network gain is desired. R_5 holds the disable pin at ground thus inhibiting the amplifier until the switch, S_1, is thrown to position 1. At position 1 the switch pulls the disable pin up to the plus supply rail thereby enabling the amplifier. Since all of the actual signal switching takes place within the amplifier, it's differential gain and phase parameters, which are 0.03% and 0.03° respectively, determine the circuit's performance. The other circuit, U_{1B}, operates in a similar manner.

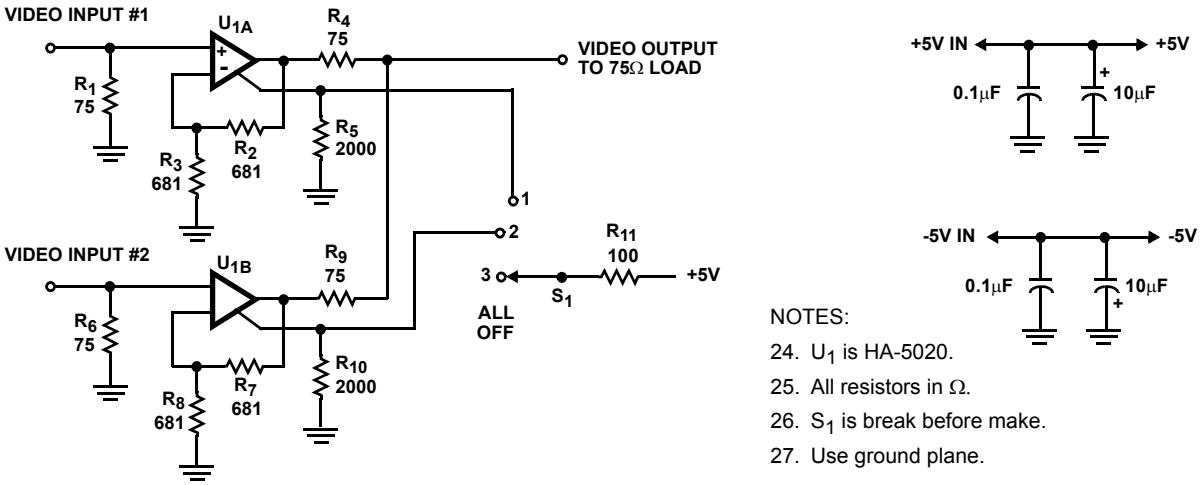
When the plus supply rail is 5V the disable pin can be driven by a dedicated TTL gate as discussed earlier. If a multiplexer IC or its equivalent is used to select channels its logic must be break before make. When these conditions are satisfied the HA-5020 is often used as a remote video multiplexer, and the multiplexer may be extended by adding more amplifier ICs.

Low Impedance Multiplexer

Two common problems surface when you try to multiplex multiple high speed signals into a low impedance source such as an A/D converter. The first problem is the low source impedance which tends to make amplifiers oscillate and causes gain errors. The second problem is the multiplexer which supplies no gain, introduces all kinds of distortion and limits the frequency response. Using op amps which have an enable/disable function, such as the HA-5020, eliminates the multiplexer problems because the external mux chip is not needed, and the HA-5020 can drive low impedance (large capacitance) loads if a series isolation resistor is used.

Referring to Figure 9, both inputs are terminated in their characteristic impedance; 75Ω is typical for video applications. Since the drivers usually are terminated in their characteristic impedance the input gain is 0.5, thus the amplifiers, U_2, are configured in a gain of +2 to set the circuit gain equal to one. Resistors R_2 and R_3 determine the amplifier gain, and if a different gain is desired R_2 should be changed according to the equation $G = (1 + R_3/R_2)$. R_3 sets the frequency response of the amplifier so you should refer to the manufacturers data sheet before changing its value. R_5, C_1 and D_1 are an asymmetrical charge/discharge time circuit which configures U_1 as a break before make switch to prevent both amplifiers from being active simultaneously. If this design is extended to more channels the drive logic must be designed to be break before make. R_4 is enclosed in the feedback loop of the amplifier so that the large open loop amplifier gain of U_2 will present the load with a small closed loop output impedance while keeping the amplifier stable for all values of load capacitance.

The circuit shown in Figure 9 was tested for the full range of capacitor values with no oscillations being observed; thus, problem one has been solved. The frequency and gain characteristics of the circuit are now those of the amplifier and independent of any multiplexing action; thus, problem two has been solved. The multiplexer transition time is approximately 15µs with the component values shown.



NOTES:

24. U_1 is HA-5020.
25. All resistors in Ω.
26. S_1 is break before make.
27. Use ground plane.

FIGURE 8. TWO CHANNEL HIGH IMPEDANCE MULTIPLEXER

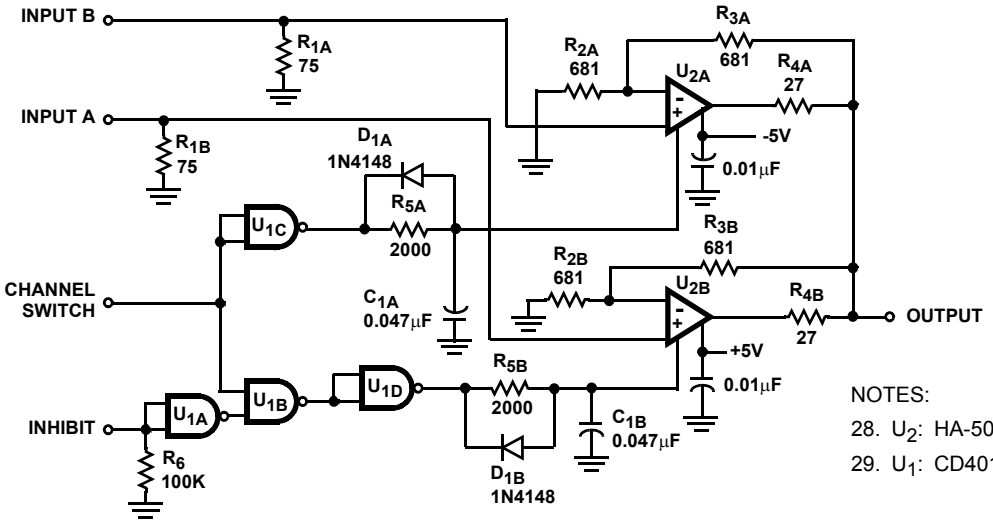


FIGURE 8. LOW IMPEDANCE MULTIPLEXER

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25°C$, unless otherwise specified

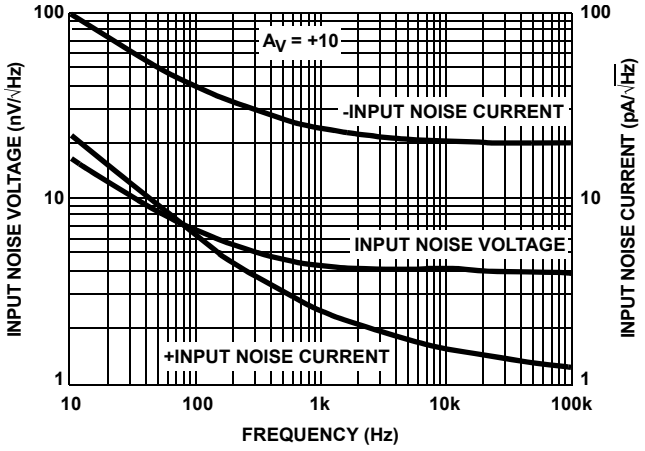


FIGURE 9. INPUT NOISE vs FREQUENCY (AVERAGE OF 18 UNITS FROM 3 LOTS)

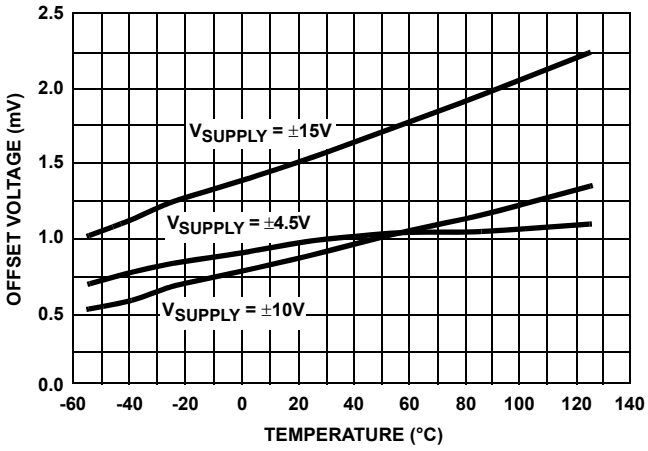


FIGURE 10. INPUT OFFSET VOLTAGE vs TEMPERATURE (ABSOLUTE VALUE AVERAGE OF 30 UNITS FROM 3 LOTS)

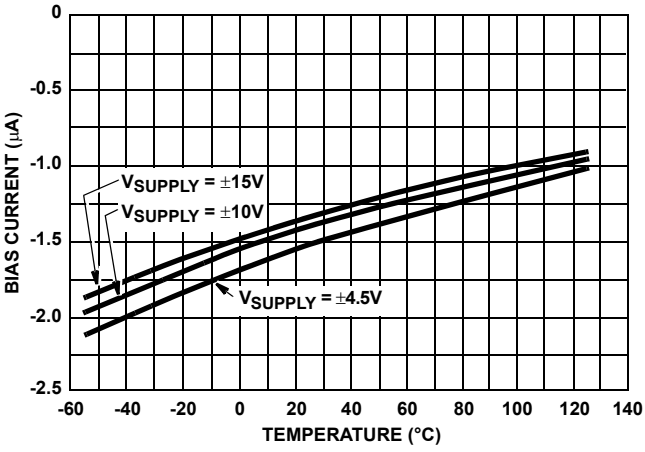


FIGURE 11. +INPUT BIAS CURRENT vs TEMPERATURE (AVERAGE OF 30 UNITS FROM 3 LOTS)

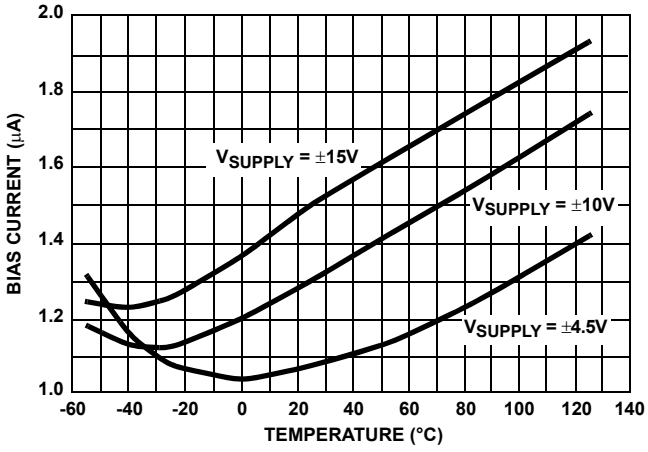


FIGURE 12. -INPUT BIAS CURRENT vs TEMPERATURE (ABSOLUTE VALUE AVERAGE OF 30 UNITS FROM 3 LOTS)

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25°C$, unless otherwise specified

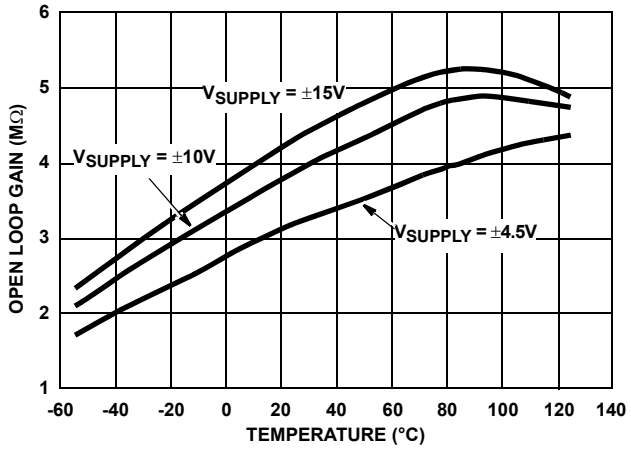


FIGURE 13. TRANSIMPEDANCE vs TEMPERATURE (AVERAGE OF 30 UNITS FROM 3 LOTS)

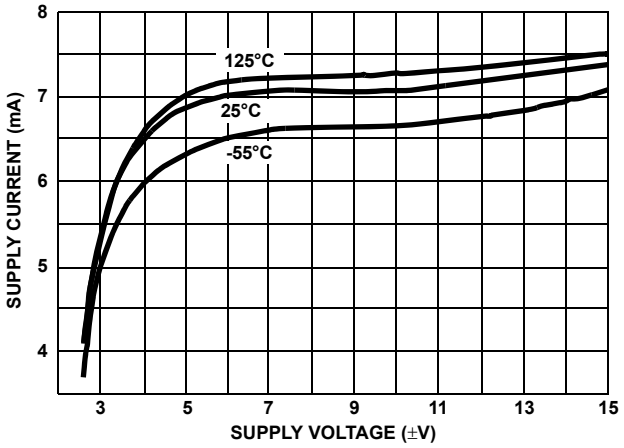


FIGURE 14. SUPPLY CURRENT vs SUPPLY VOLTAGE (AVERAGE OF 30 UNITS FROM 3 LOTS)

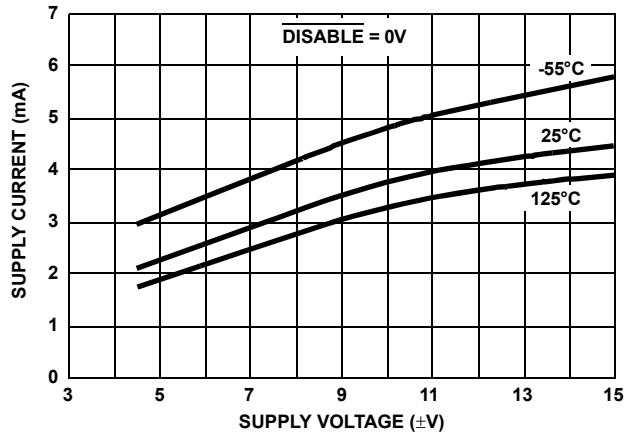


FIGURE 15. DISABLE SUPPLY CURRENT vs SUPPLY VOLTAGE (AVERAGE OF 30 UNITS FROM 3 LOTS)

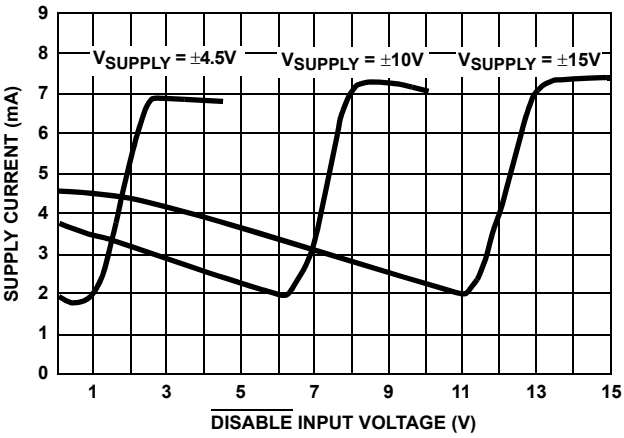


FIGURE 16. SUPPLY CURRENT vs $\overline{\text{DISABLE}}$ INPUT VOLTAGE

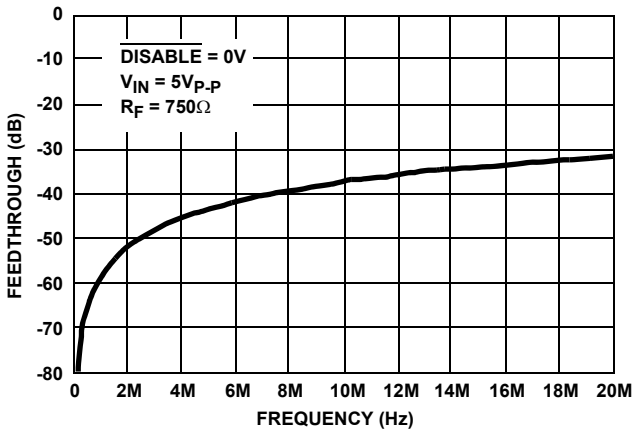


FIGURE 17. DISABLE MODE FEEDTHROUGH vs FREQUENCY

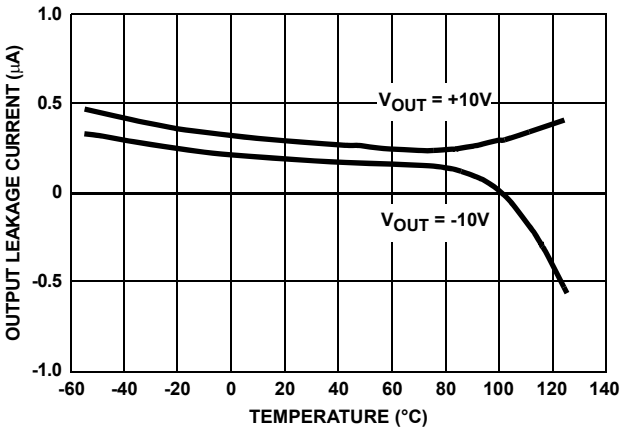


FIGURE 18. DISABLED OUTPUT LEAKAGE vs TEMPERATURE (AVERAGE OF 30 UNITS FROM 3 LOTS)

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25°C$, unless otherwise specified

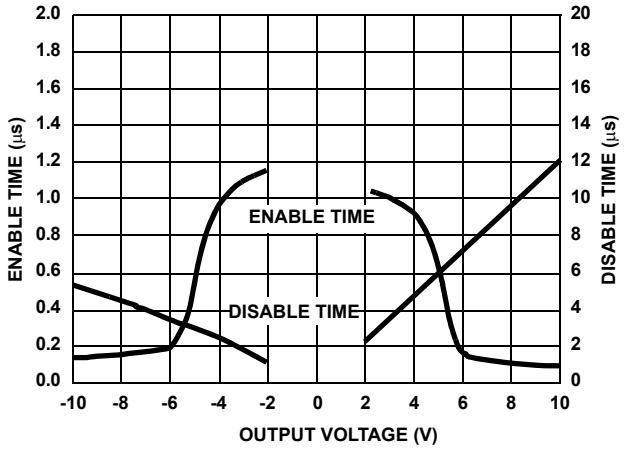


FIGURE 19. ENABLE/DISABLE TIME vs OUTPUT VOLTAGE (AVERAGE OF 9 UNITS FROM 3 LOTS)

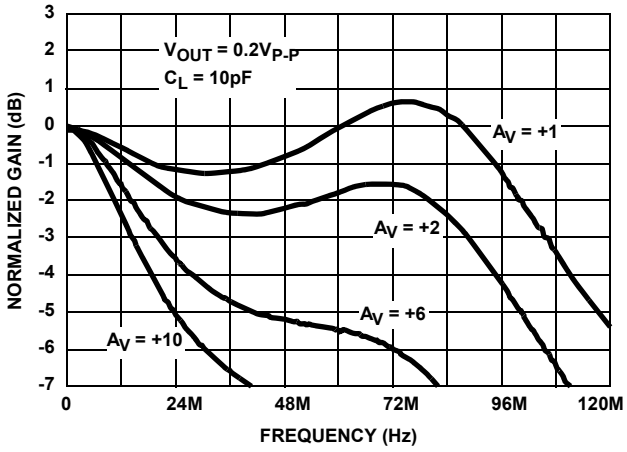


FIGURE 20. NON-INVERTING GAIN vs FREQUENCY

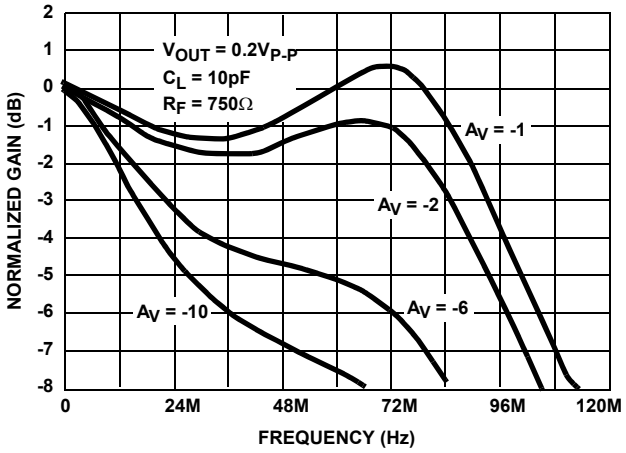


FIGURE 21. INVERTING FREQUENCY RESPONSE

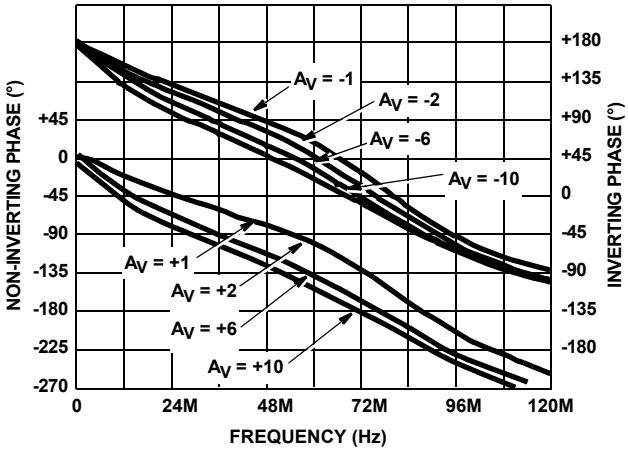


FIGURE 22. PHASE vs FREQUENCY

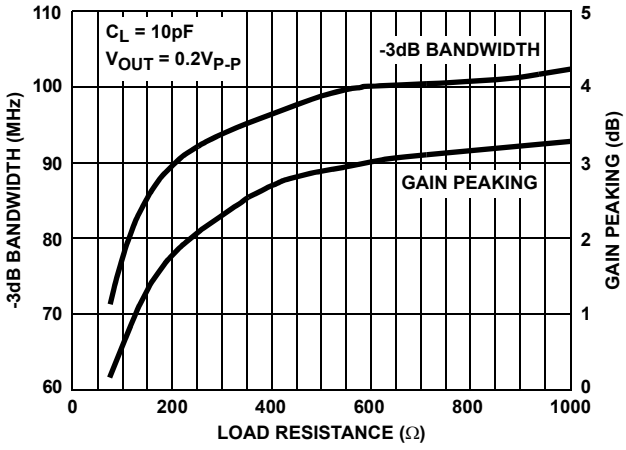


FIGURE 23. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

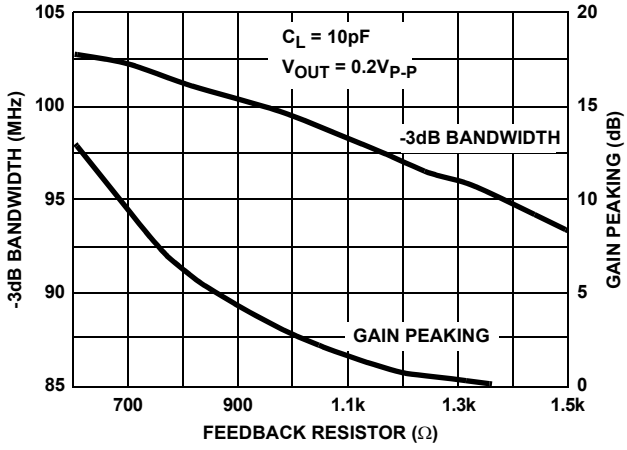


FIGURE 24. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25°C$, unless otherwise specified

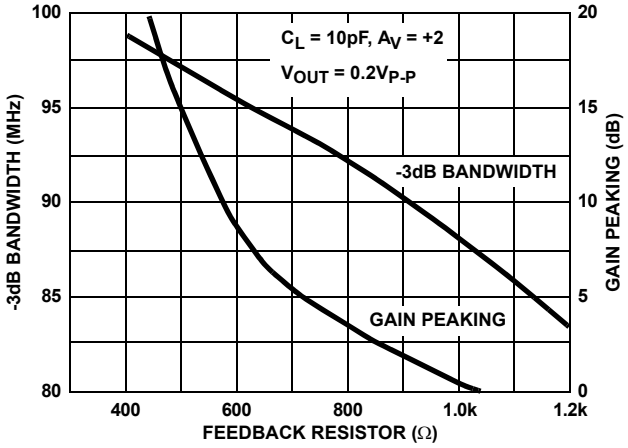


FIGURE 25. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

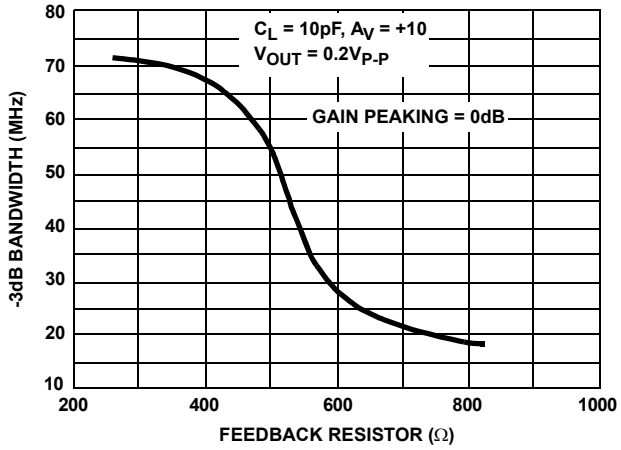


FIGURE 26. BANDWIDTH vs FEEDBACK RESISTANCE

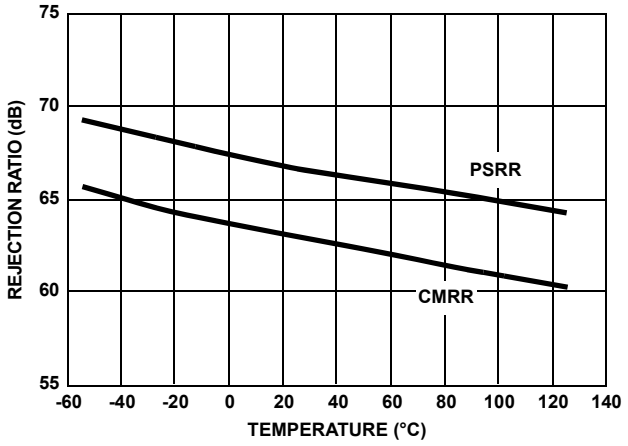


FIGURE 27. REJECTION RATIOS vs TEMPERATURE (AVERAGE OF 30 UNITS FROM 3 LOTS)

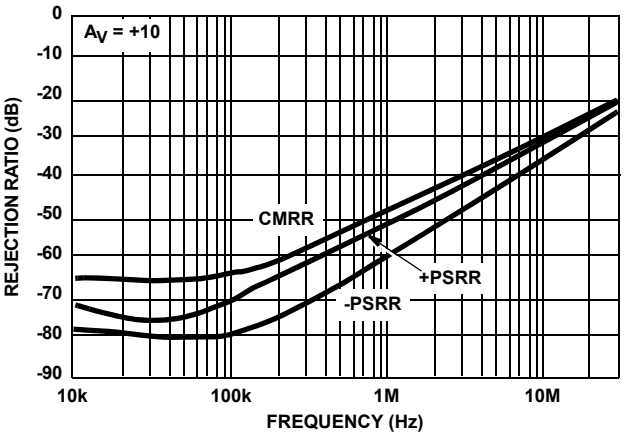


FIGURE 28. REJECTION RATIOS vs FREQUENCY

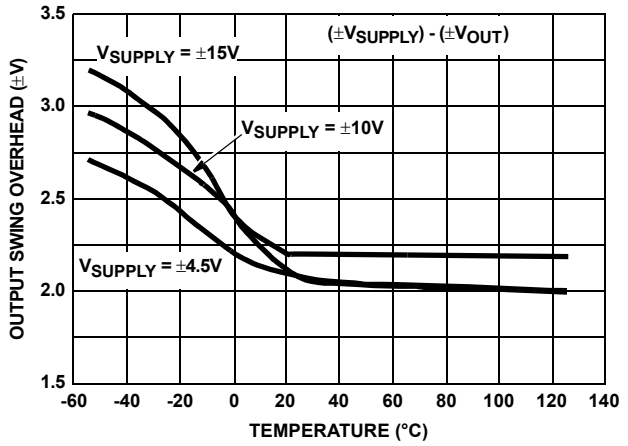


FIGURE 29. OUTPUT SWING OVERHEAD vs TEMPERATURE (AVERAGE OF 30 UNITS FROM 3 LOTS)

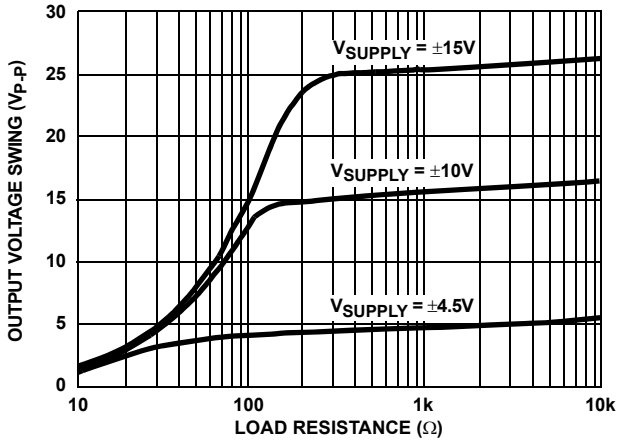


FIGURE 30. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25°C$, unless otherwise specified

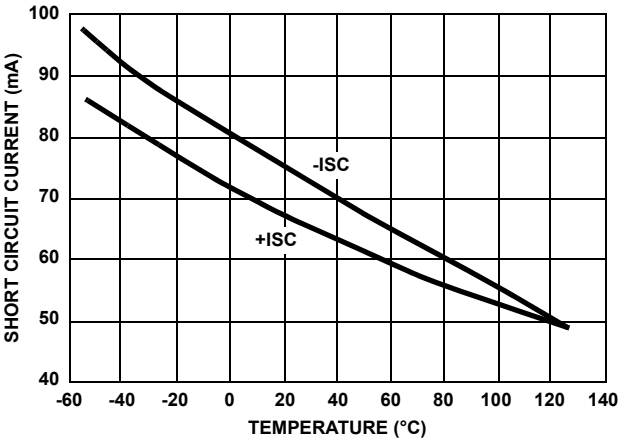


FIGURE 31. SHORT CIRCUIT CURRENT LIMIT vs TEMPERATURE

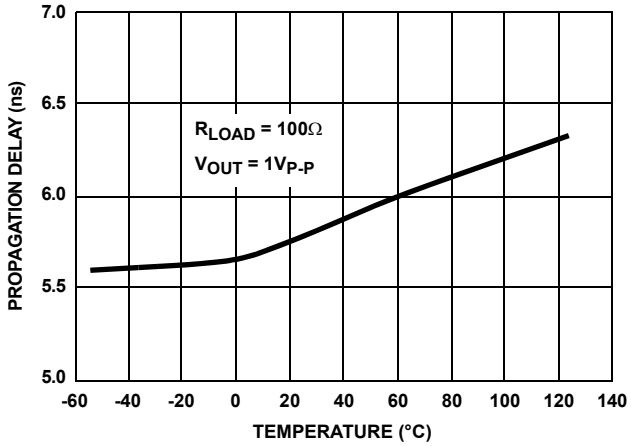


FIGURE 32. PROPAGATION DELAY vs TEMPERATURE (AVERAGE OF 18 UNITS FROM 3 LOTS)

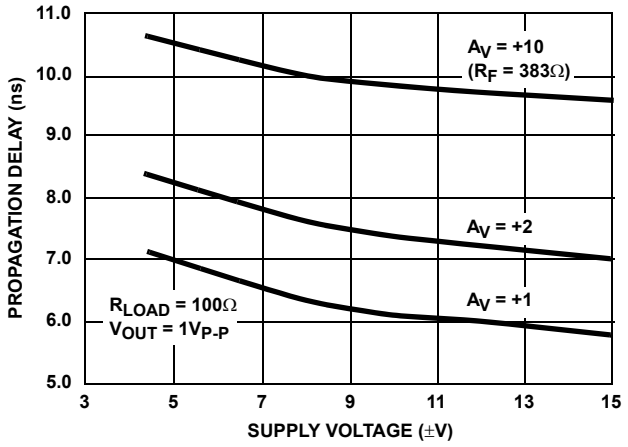


FIGURE 33. PROPAGATION DELAY vs SUPPLY VOLTAGE (AVERAGE OF 18 UNITS FROM 3 LOTS)

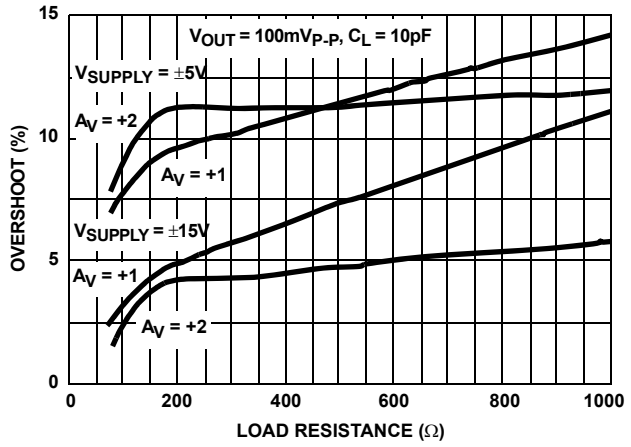


FIGURE 34. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

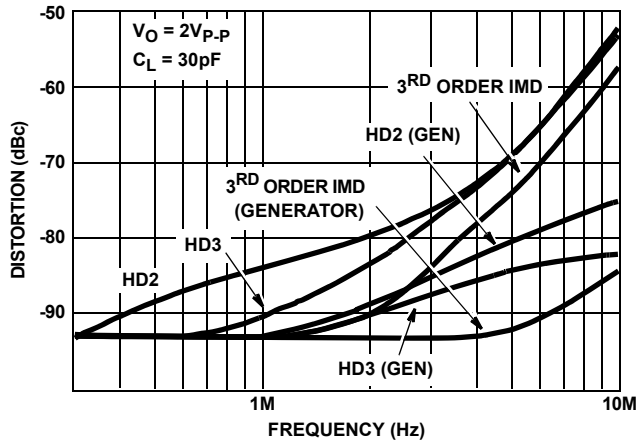


FIGURE 35. DISTORTION vs FREQUENCY

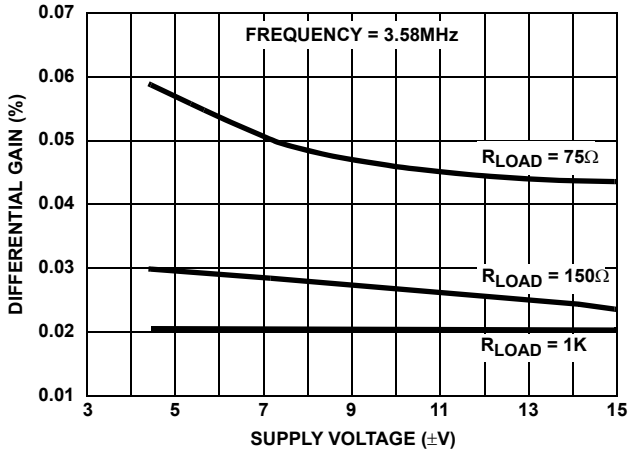


FIGURE 36. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE (AVERAGE OF 18 UNITS FROM 3 LOTS)

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25°C$, unless otherwise specified

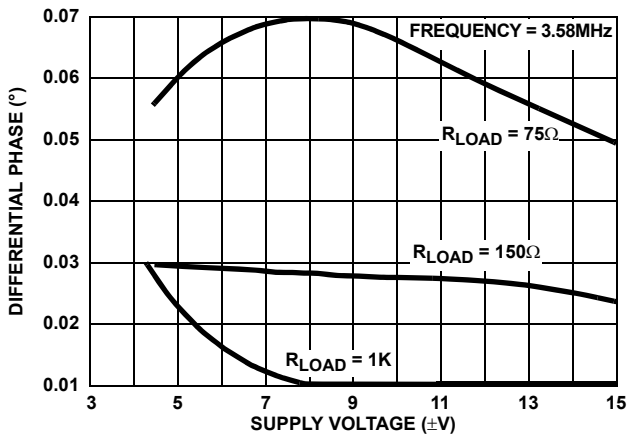


FIGURE 37. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE (AVERAGE OF 18 UNITS FROM 3 LOTS)

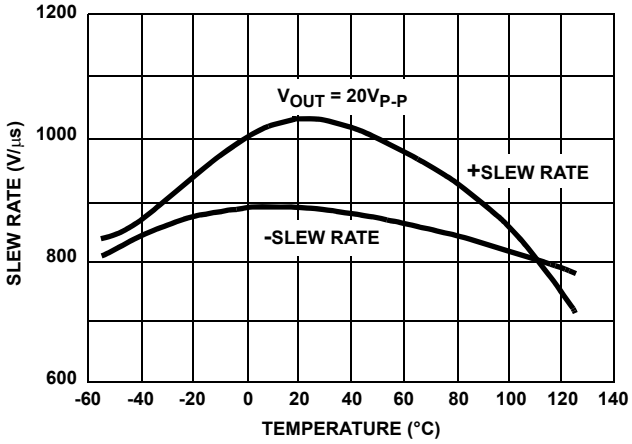


FIGURE 38. SLEW RATE vs TEMPERATURE (AVERAGE OF 30 UNITS FROM 3 LOTS)

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25°C$, Unless Otherwise Specified

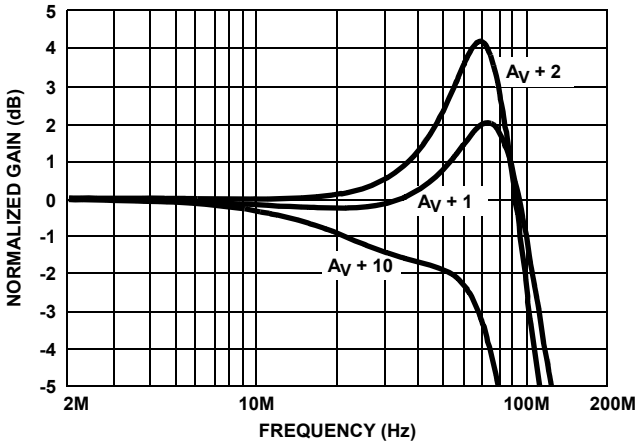


FIGURE 39. NON-INVERTING FREQUENCY RESPONSE

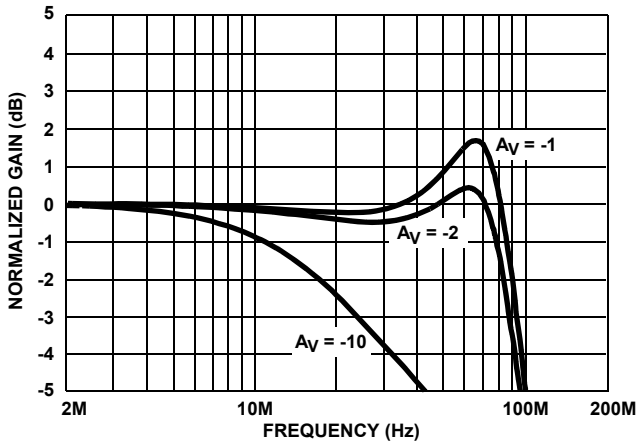


FIGURE 40. INVERTING FREQUENCY RESPONSE

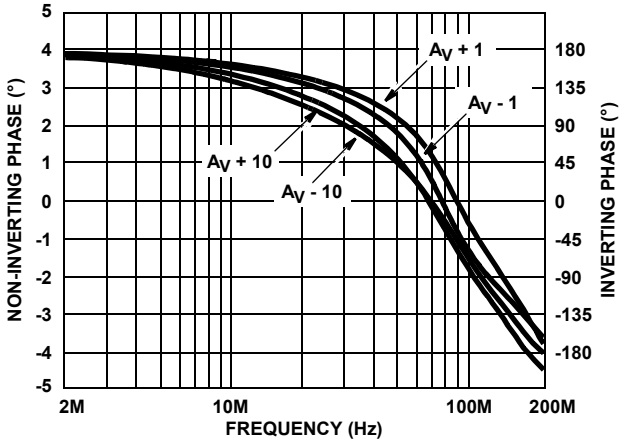


FIGURE 41. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

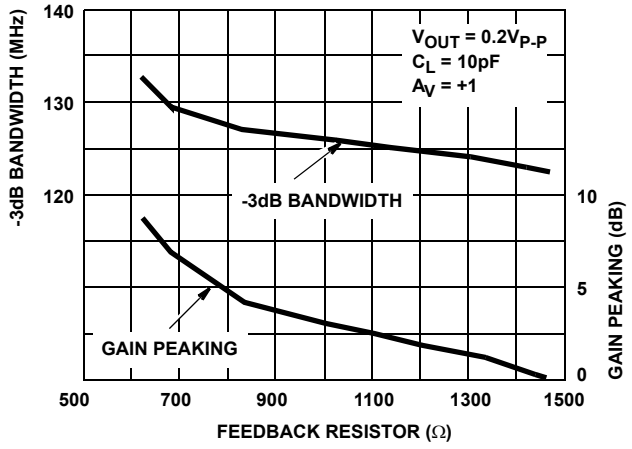


FIGURE 42. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

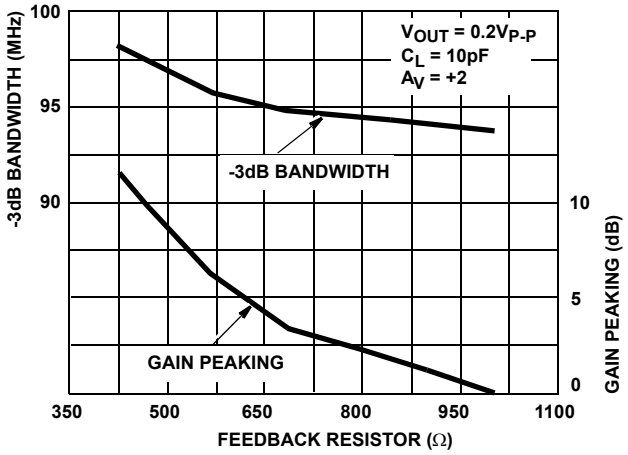


FIGURE 43. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

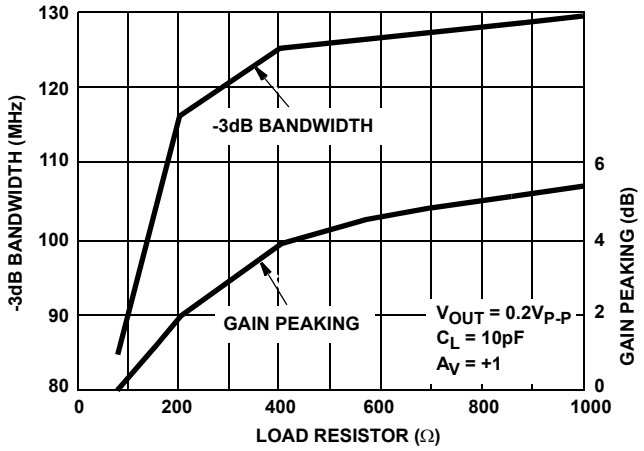


FIGURE 44. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

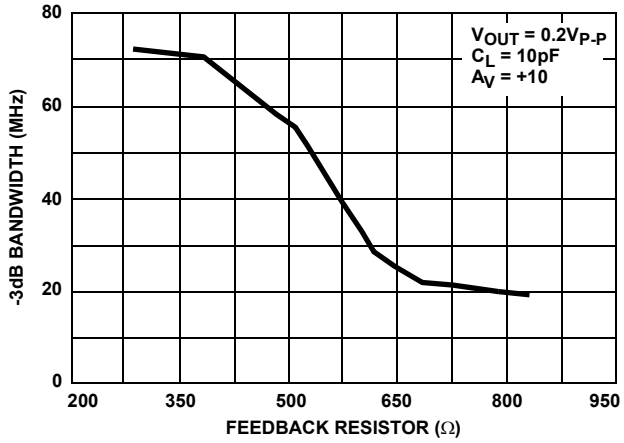


FIGURE 45. BANDWIDTH vs FEEDBACK RESISTANCE

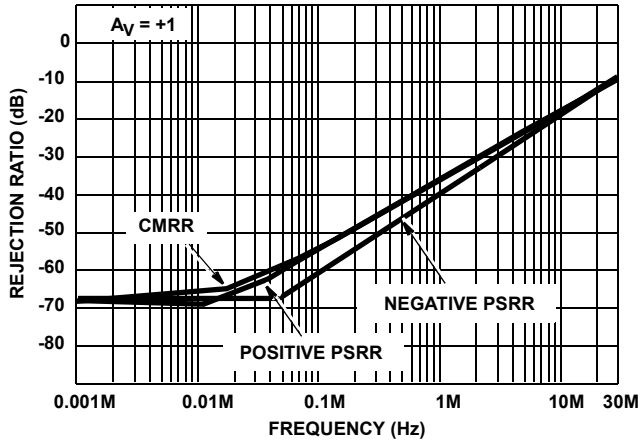


FIGURE 46. REJECTION RATIOS vs FREQUENCY

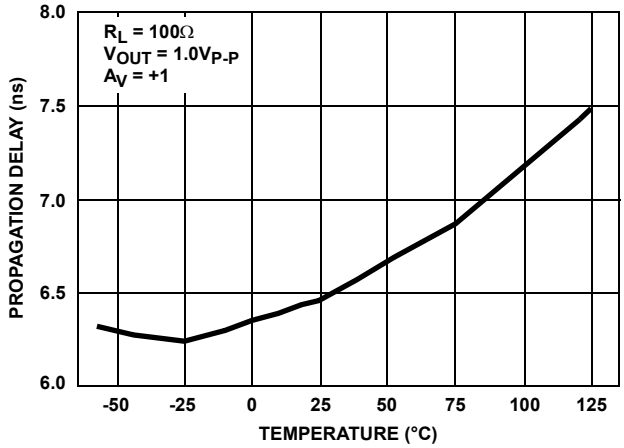


FIGURE 47. PROPAGATION DELAY vs TEMPERATURE

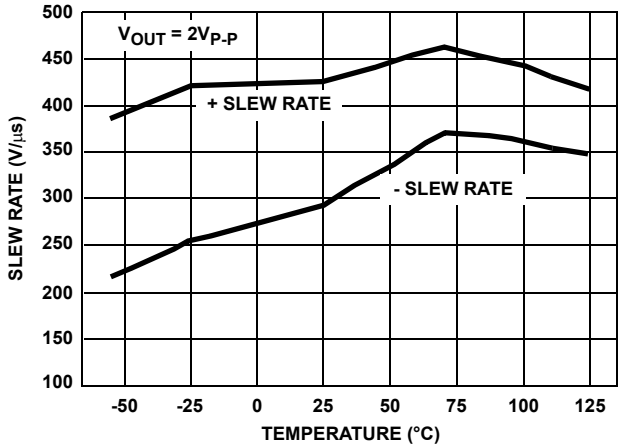


FIGURE 48. SLEW RATE vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

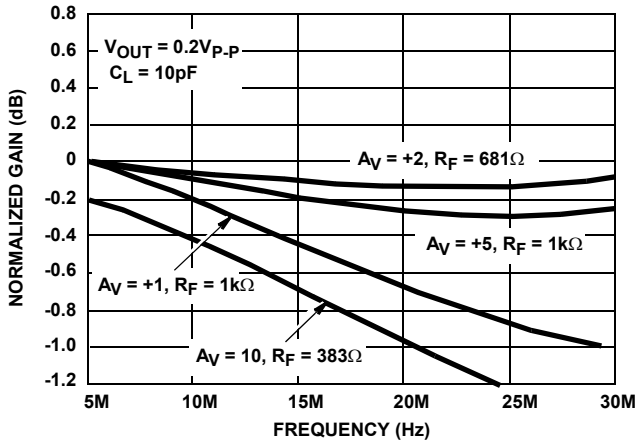


FIGURE 49. NON-INVERTING GAIN FLATNESS vs FREQUENCY

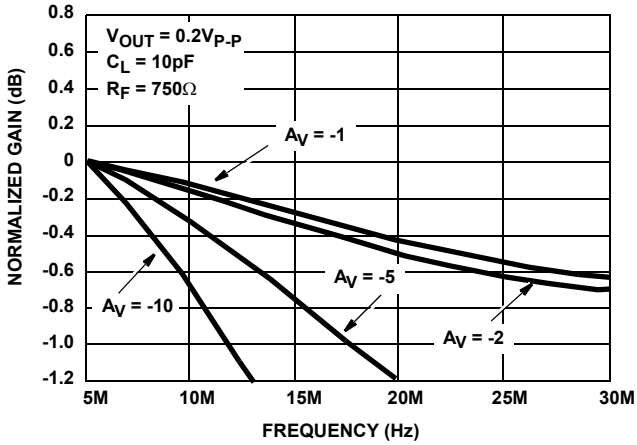


FIGURE 50. INVERTING GAIN FLATNESS vs FREQUENCY

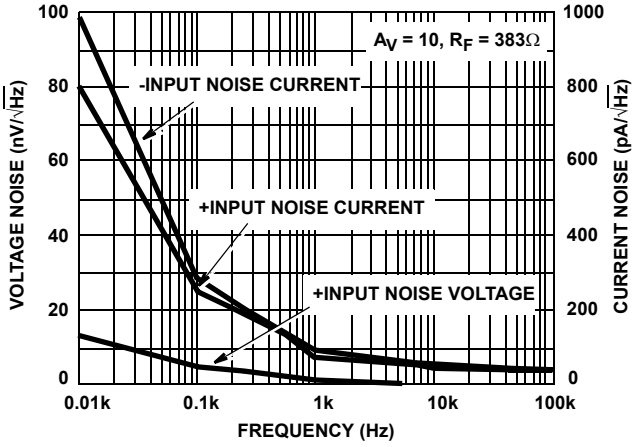


FIGURE 51. INPUT NOISE CHARACTERISTICS

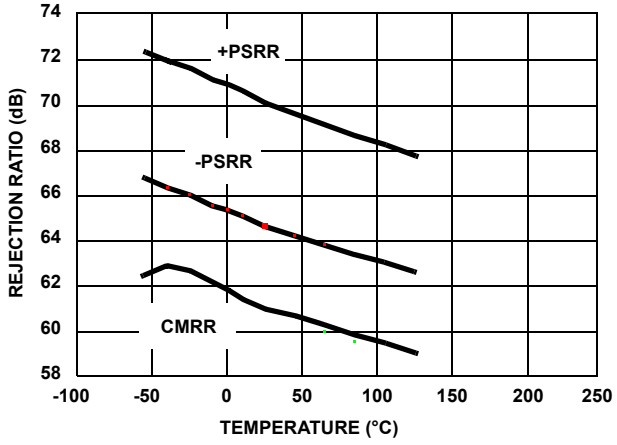


FIGURE 52. REJECTION RATIO vs TEMPERATURE

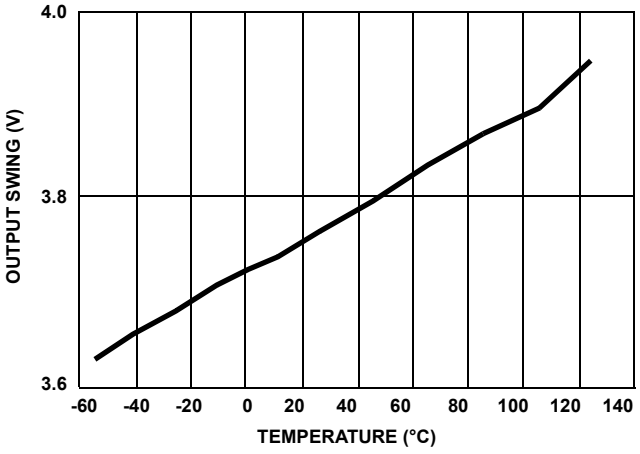


FIGURE 53. OUTPUT SWING vs TEMPERATURE

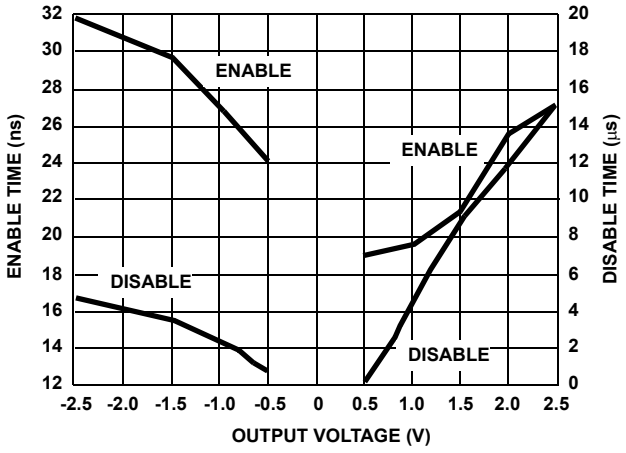


FIGURE 54. ENABLE/DISABLE TIME vs OUTPUT VOLTAGE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

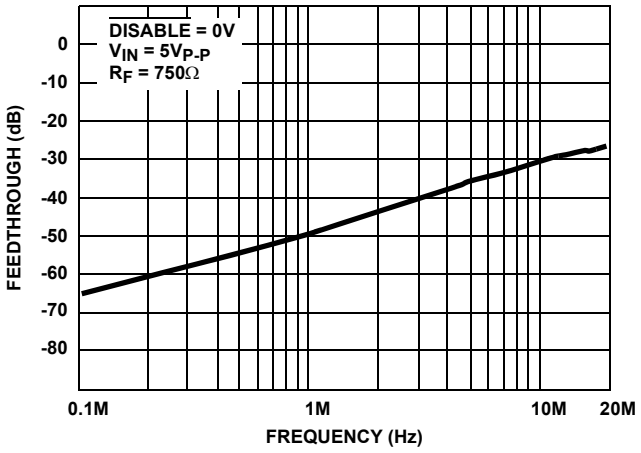


FIGURE 55. DISABLE FEEDTHROUGH vs FREQUENCY

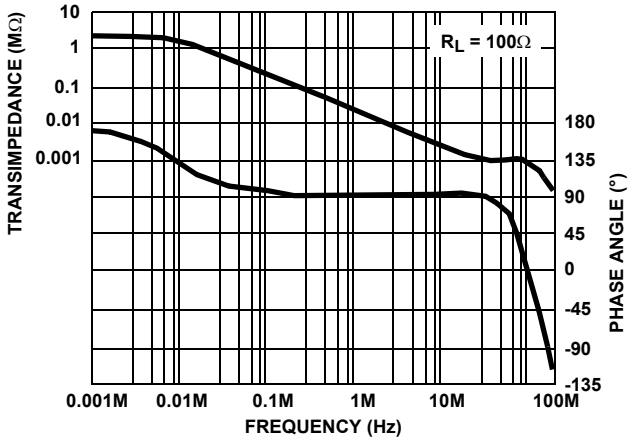


FIGURE 56. TRANSIMPEDANCE vs FREQUENCY

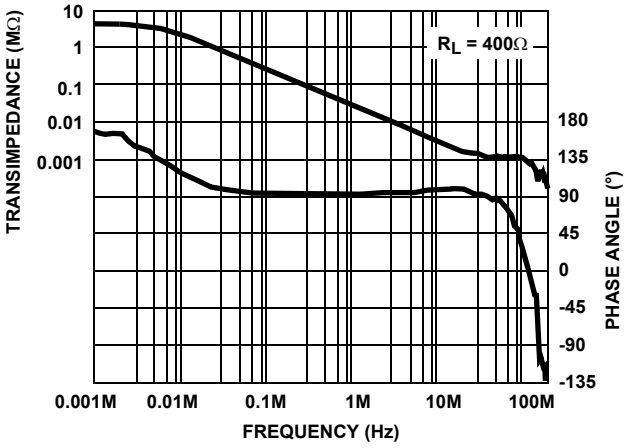


FIGURE 57. TRANSIMPEDENCE vs FREQUENCY

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 11, 2015	FN2845.13	Ordering Information table, page 2: HA3-5020-5Z - added: “(No longer available, recommended replacement: HA9P5020-5Z, HA9P5020-5ZX96)” Added Revision History and About Intersil.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Die Characteristics

DIE DIMENSIONS:

1640µm x 1520µm x 483µm

METALLIZATION:

Type: Aluminum, 1% Copper
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

PASSIVATION:

Type: Nitride over Silox
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1kÅ

TRANSISTOR COUNT:

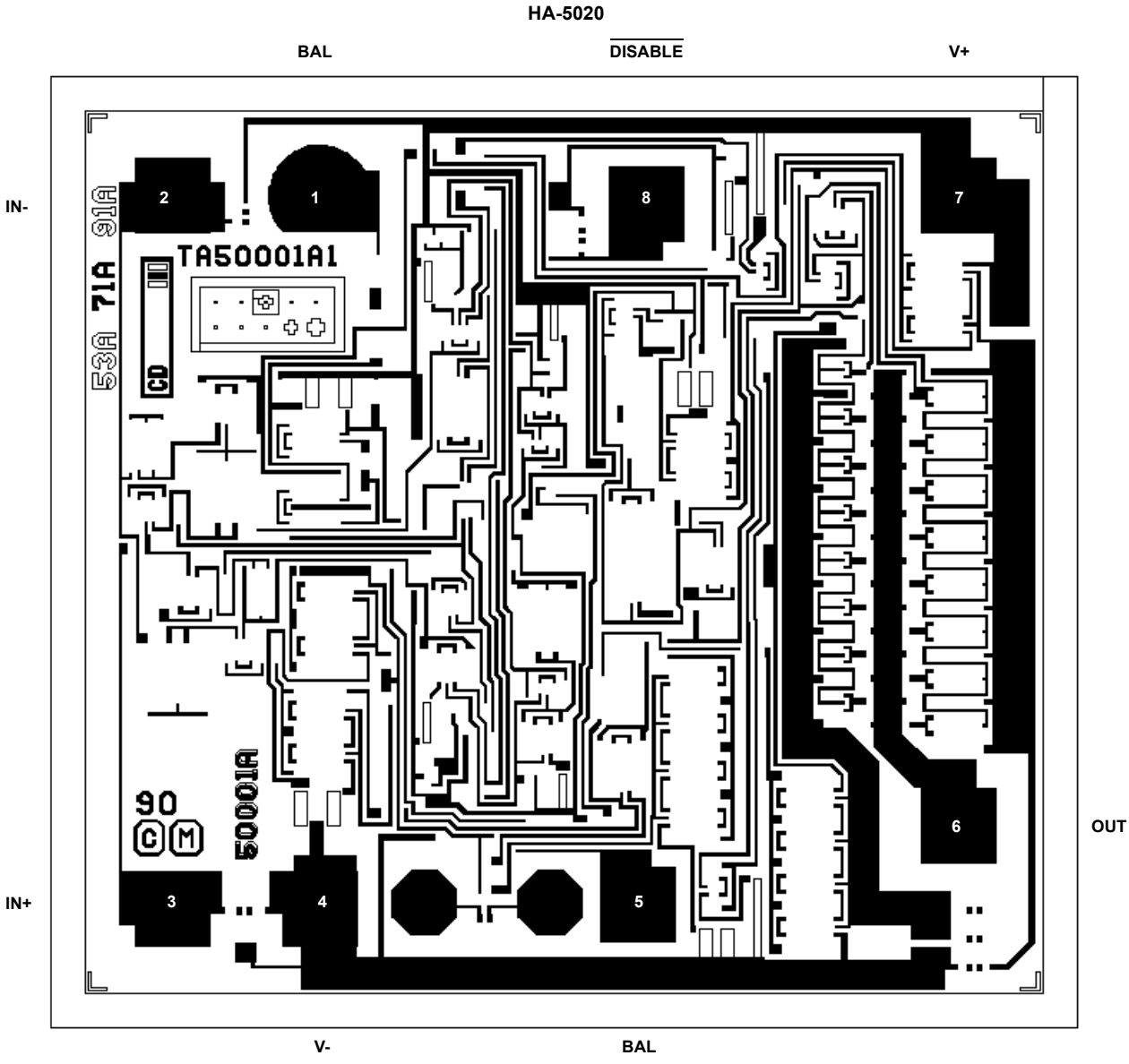
62

PROCESS:

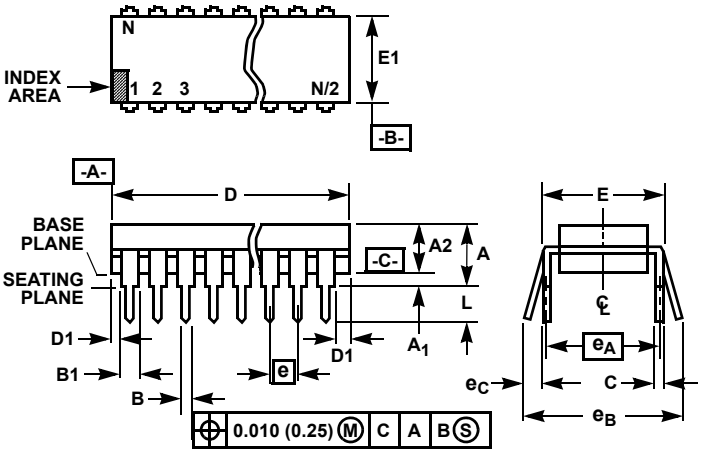
High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5020



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

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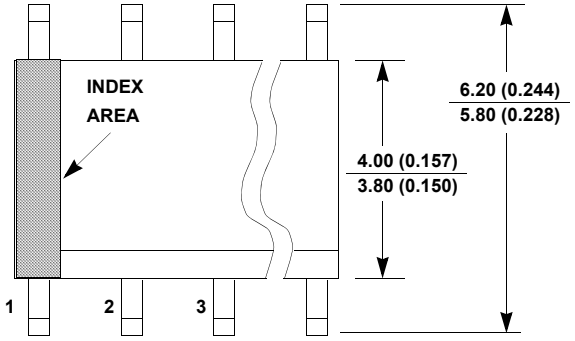
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

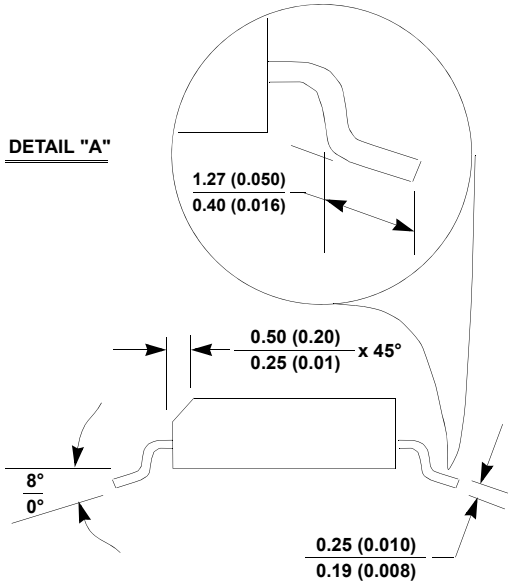
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

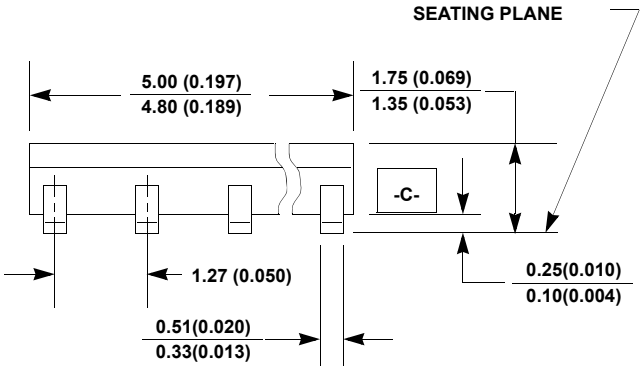
Rev 4, 1/12



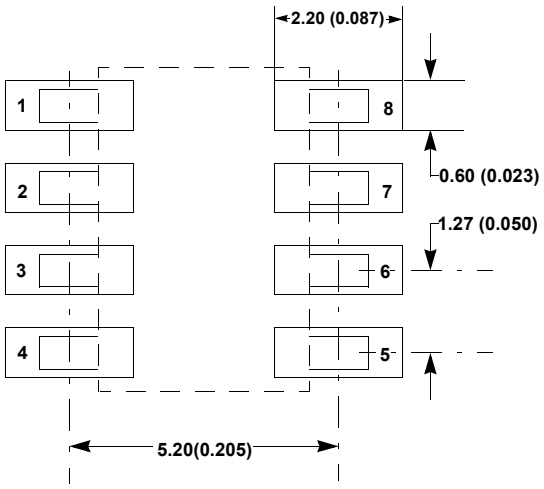
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.