Data Sheet | September 1998 | File Number 2898.3

40MHz, Fast Settling, Unity Gain Stable, Operational Amplifier

The HA-2541 is the first unity gain stable monolithic operational amplifier to achieve 40MHz unity gain bandwidth. A major addition to the Intersil series of high speed, wideband op amps, the HA-2541 is designed for video and pulse applications requiring stable amplifier response at low closed loop gains.

The uniqueness of the HA-2541 is that its slew rate and bandwidth characteristics are specified at unity gain. Historically, high slew rate, wide bandwidth and unity gain stability have been incompatible features for a monolithic operational amplifier. But features such as 250V/µs slew rate and 40MHz unity gain bandwidth clearly show that this is not the case for the HA-2541. These features, along with 90ns settling time to 0.1%, make this product an excellent choice for high speed data acquisition systems.

MIL-STD-883 product and data sheets are available upon request, Intersil AnswerFAX (407-724-7800) document #3698.

For further application suggestions on the HA-2541, please refer to Application Note AN550 (Using the HA-2541), and Application Note AN556 (Thermal Safe Operating Areas for High Current Operational Amplifiers), Intersil AnswerFAX (407-724-7800) document #9550 and 9556. Also see ‘Applications’ in this data sheet.

For a lower power version of this product, please see the HA-2841 data sheet.

Features

- Unity Gain Bandwidth 40MHz
- High Slew Rate 250V/µs
- Low Offset Voltage 0.8mV
- Fast Settling Time (0.1%) 90ns
- Power Bandwidth 4MHz
- Output Voltage Swing (Min) . . . . . ±10V
- Unity Gain Stability
- Monolithic Bipolar Dielectric Isolation Construction

Applications

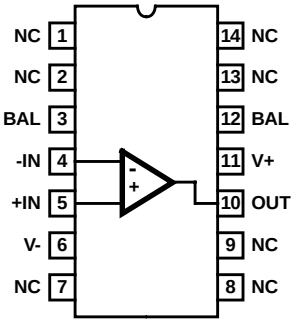
- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters
- High Speed A/D Input Buffer

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HA1-2541-5	0 to 75	14 Ld CERDIP	F14.3

Pinout

HA1-2541
(CERDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 321-724-7143 | Copyright © Intersil Corporation 1999

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Peak Output Current 50mA
Continuous Output Current . . . . . $28mA_{RMS}$

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	75	20

Maximum Junction Temperature (Note 1) . . . . . 175^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Operating Conditions

Temperature Range
HA-2541-5 . . . . . 0^oC to 75^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below 175^oC. By using Application Note AN556 on Safe Operating Area equations, along with the thermal resistances, proper load conditions can be determined. Heat sinking is recommended above 75^oC.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	HA-2541-5 0^oC TO 75^oC			UNITS
			MIN	TYP	MAX	
INPUT CHARACTERISTICS						
Offset Voltage		25	-	1	2	mV
		Full	-	-	6	mV
Average Offset Voltage Drift		Full	-	9	-	$\mu V/^oC$
Bias Current		25	-	11	35	µA
		Full	-	-	50	µA
Average Bias Current Drift		Full	-	85	-	$nA/^oC$
Offset Current		25	-	1	7	µA
		Full	-	-	9	µA
Input Resistance		25	-	100	-	kΩ
Input Capacitance		25	-	1	-	pF
Common Mode Range		Full	±10	±11	-	V
Input Noise Voltage	f = 1kHz, $R_g = 0\Omega$	25	-	10	-	$nV/\sqrt{Hz}$
Input Noise Current	f = 1kHz, $R_g = 0\Omega$	25	-	4	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	$V_O = \pm10V$	25	10	16	-	kV/V
		Full	5	-	-	kV/V
Common Mode Rejection Ratio	$V_{CM} = \pm10V$	Full	70	90	-	dB
Minimum Stable Gain		25	1	-	-	V/V
Unity Gain Bandwidth	$V_O = 90mV$	25	-	40	-	MHz
OUTPUT CHARACTERISTICS						
Output Voltage Swing	$R_L = 1k\Omega$	Full	±10	±11	-	V
Output Current	$R_L = 1k\Omega$	25	±10	±15	-	mA
Output Resistance		25	-	2	-	Ω
Full Power Bandwidth (Note 3)	$V_P = 10V$	25	3	4	-	MHz
Differential Gain	Note 4	25	-	0.1	-	%
Differential Phase	Note 4	25	-	0.2	-	Degrees
Harmonic Distortion	Note 6	25	-	<0.01	-	%

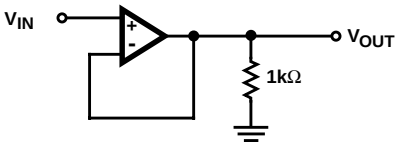
Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^oC)	HA-2541-5 0^oC TO 75^oC			UNITS
			MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 5)						
Rise Time		25	-	4	-	ns
Overshoot		25	-	40	-	%
Slew Rate		25	200	250	-	V/µs
Settling Time	10V Step To 0.1%	25	-	90	-	ns
	10V Step To 0.01%	25	-	175	-	ns
POWER REQUIREMENTS						
Supply Current		25	-	29	-	mA
		Full	-	-	40	mA
Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$	Full	70	78	-	dB

NOTES:

3. Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
4. Differential Gain and Phase are measured with a 1V differential voltage at 5MHz.
5. Refer to Test Circuits section of this data sheet.
6. f = 10kHz; $A_V = 5$; $V_O = 14V_{P-P}$.

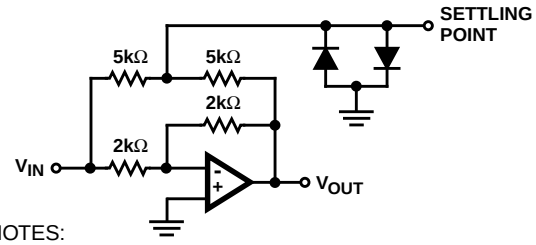
Test Circuits and Waveforms



NOTES:

7. $V_S = \pm15V$.
8. $A_V = +1$.
9. $C_L \leq 10pF$.

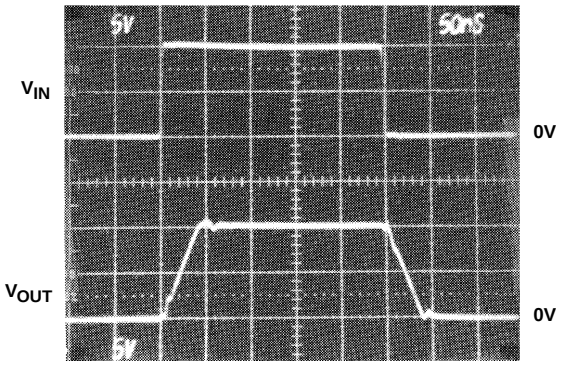
FIGURE 1. TRANSIENT RESPONSE TEST CIRCUIT



NOTES:

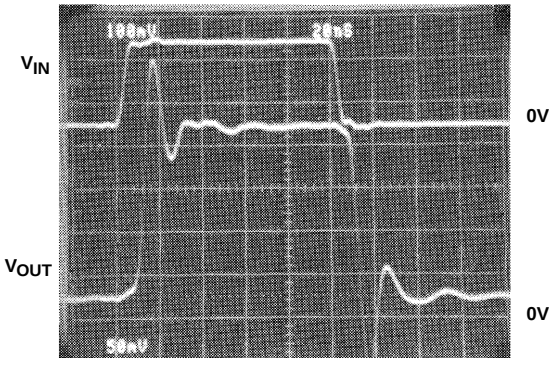
10. $A_V = -1$.
11. Feedback and summing resistor ratios should be 0.1% matched.
12. HP5082-2810 clipping diodes recommended.
13. Tektronix P6201 FET probe used at settling point.

FIGURE 2. SETTLING TIME TEST CIRCUIT



Vertical Scale: 5V/Div.
Horizontal Scale: 50ns/Div.

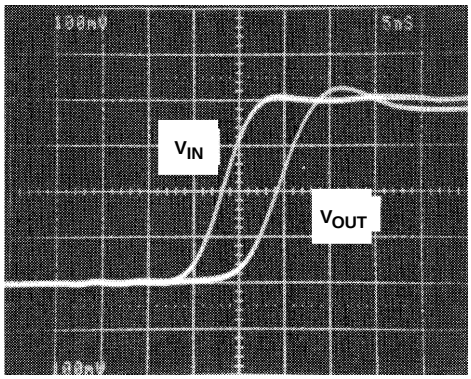
LARGE SIGNAL RESPONSE



Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 50mV/Div.
Horizontal Scale: 20ns/Div.

SMALL SIGNAL RESPONSE

Test Circuits and Waveforms (Continued)



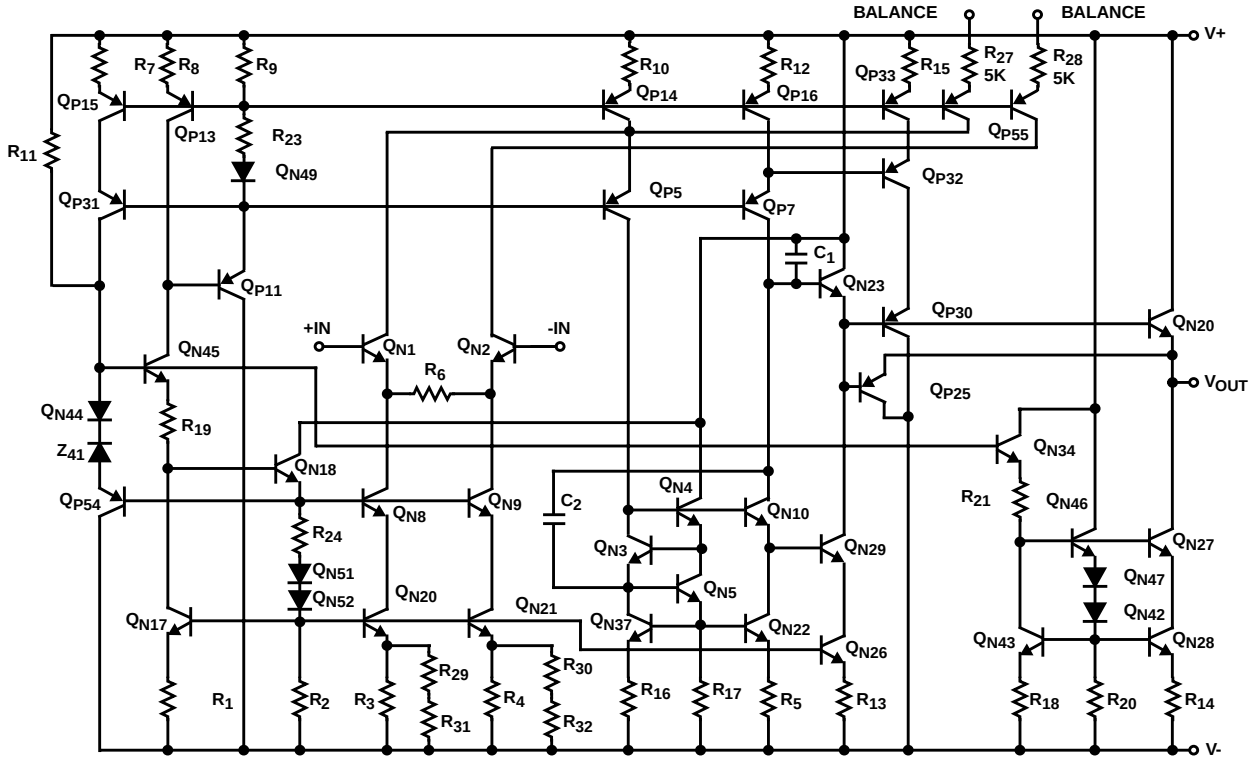
Vertical Scale: 100mV/Div.
Horizontal Scale: 5ns/Div.

PROPAGATION DELAY

NOTES:

14. $V_S = \pm 15V$, $R_L = 1k\Omega$.
15. $T_A = 25^oC$.
16. Propagation delay variance is negligible over full temperature range.

Schematic Diagram



Typical Applications (Also see Application Note AN550)

Application 1

High power amplifiers and buffers are in use in a wide variety of applications. Many times the “high power” capability is needed to drive large capacitive loads as well as low value resistive loads. In both cases the final driver stage is usually a power transistor of some type, but because of their inherently low gain, several stages of pre-drivers are often required. The HA-2541, with its 10mA output rating, is powerful enough to drive a power transistor without additional stages of current amplification. This capability is well demonstrated with the high power buffer circuit in Figure 3.

The HA-2541 acts as the pre-driver to the output power transistor. Together, they form a unity gain buffer with the ability to drive three 50Ω coaxial cables in parallel, each with a capacitance of 2000pF. The total combined load is 16.6Ω and 6000pF capacitance.

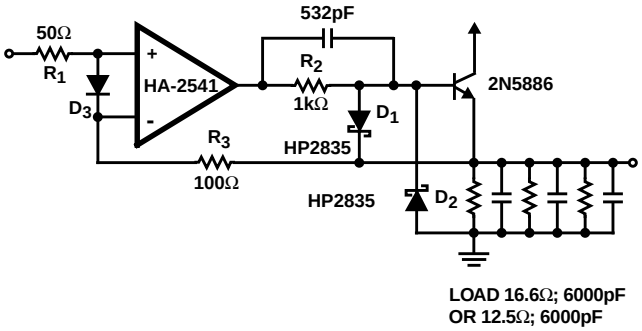


FIGURE 3. DRIVING POWER TRANSISTORS TO GAIN ADDITIONAL CURRENT BOOSTING

Application 2

VIDEO

One of the primary uses of the HA-2541 is in the area of video applications. These applications include signal construction, synchronization addition and removal, as well as signal modification. A wide bandwidth device such as the HA-2541 is well suited for use in this class of amplifier. This, however, is a more involved group of applications than ordinary amplifier applications since video signals contain precise DC levels which must be retained.

The addition of a clamping circuit restores DC levels at the output of an amplifier stage. The circuit shown in Figure 4 utilizes the HA-5320 sample and hold amplifier as the DC clamp. Also shown is a 3.57MHz trap in series, which will block the color burst portion of the video signal and allow the DC level to be amplified and restored.

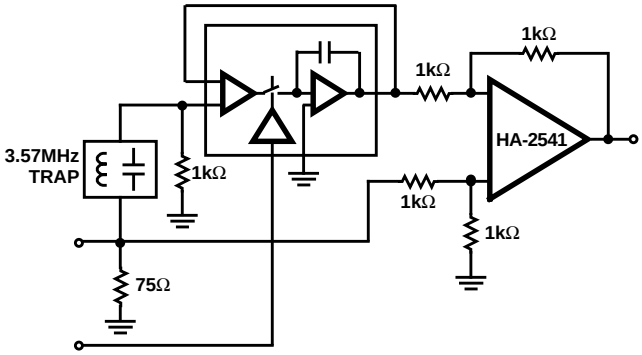
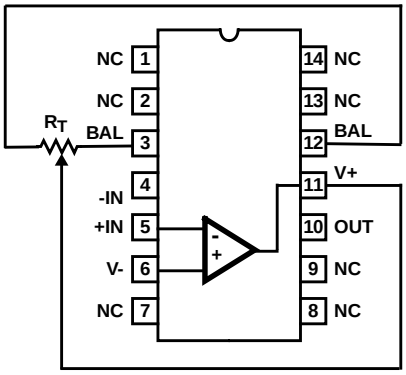


FIGURE 4. VIDEO DC RESTORER

Suggested Offset Voltage Adjustment



NOTE: Tested Offset Adjustment Range is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is ±15mV for R_T = 5kΩ.

Typical Performance Curves

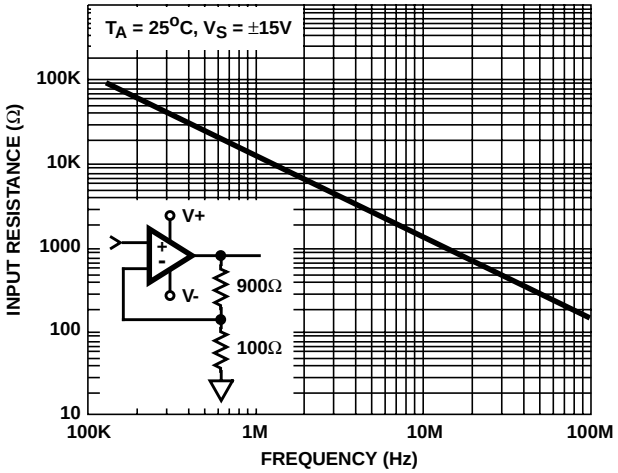


FIGURE 5. INPUT RESISTANCE vs FREQUENCY

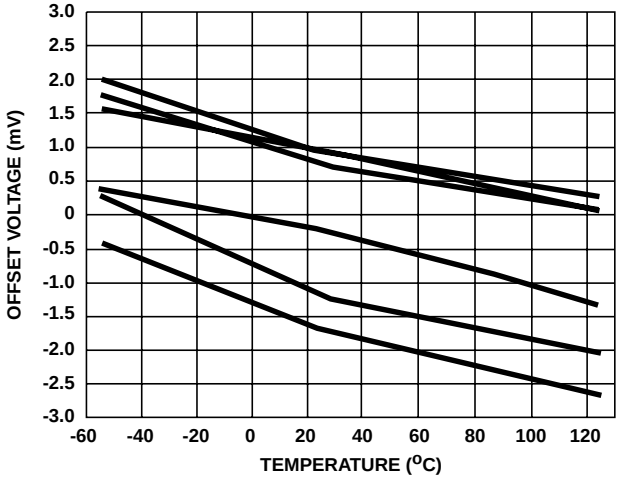


FIGURE 6. OFFSET VOLTAGE vs TEMPERATURE (6 REPRESENTATIVE UNITS)

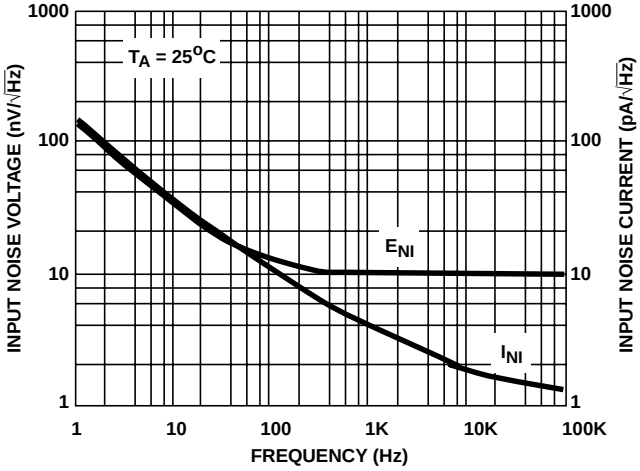


FIGURE 7. NOISE DENSITY vs FREQUENCY

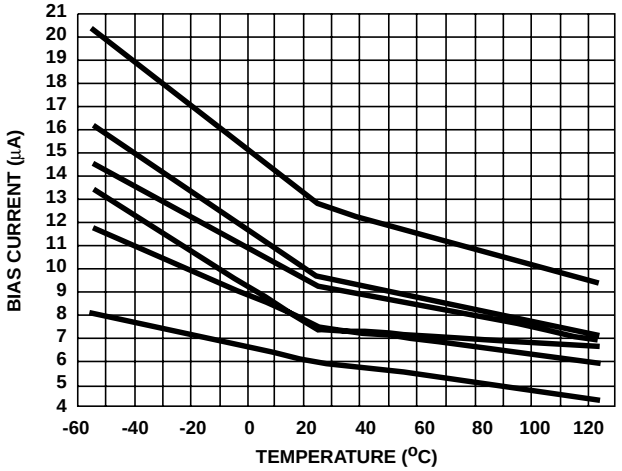


FIGURE 8. BIAS CURRENT vs TEMPERATURE (6 REPRESENTATIVE UNITS)

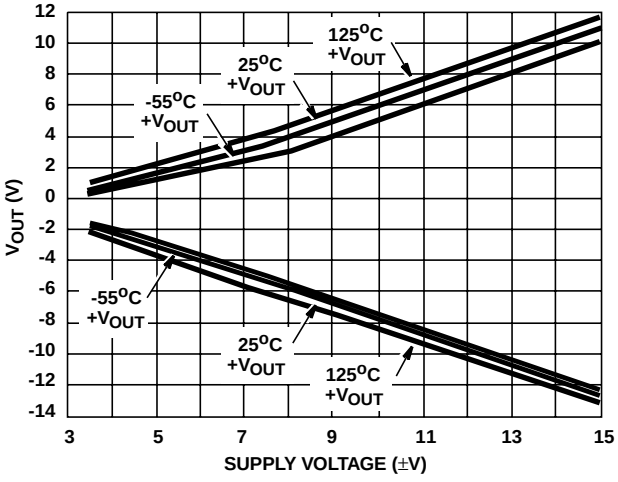


FIGURE 9. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

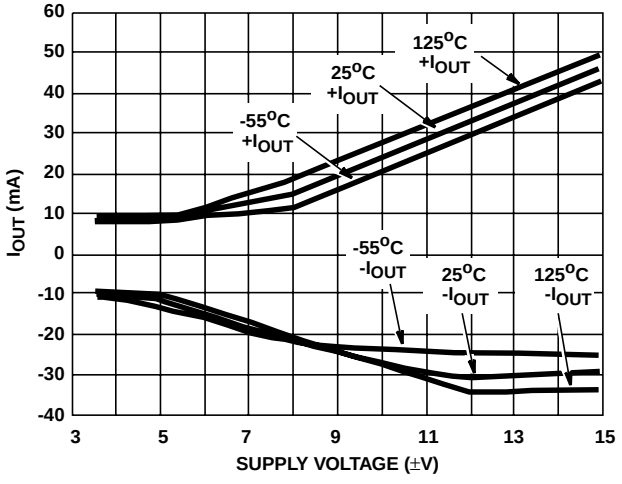


FIGURE 10. OUTPUT CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

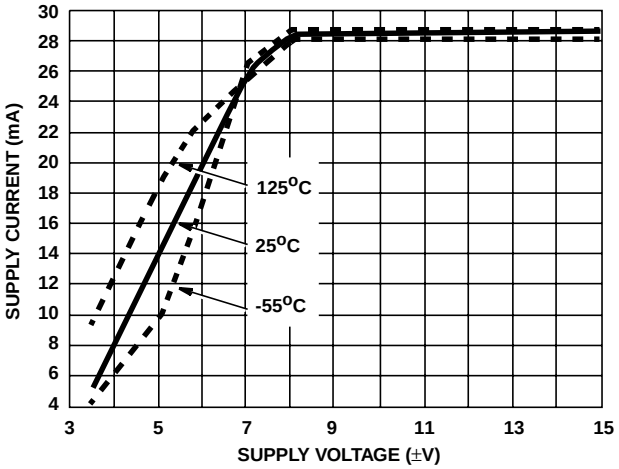


FIGURE 11. SUPPLY CURRENT vs SUPPLY VOLTAGE

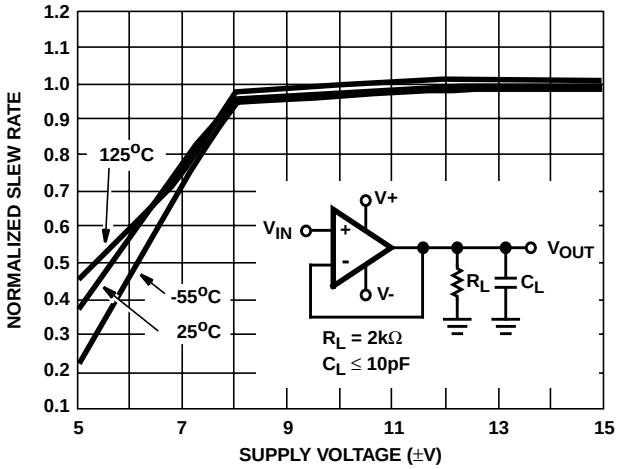


FIGURE 12. SLEW RATE vs SUPPLY VOLTAGE (NORMALIZED WITH V_S = ±15V AT 25°C)

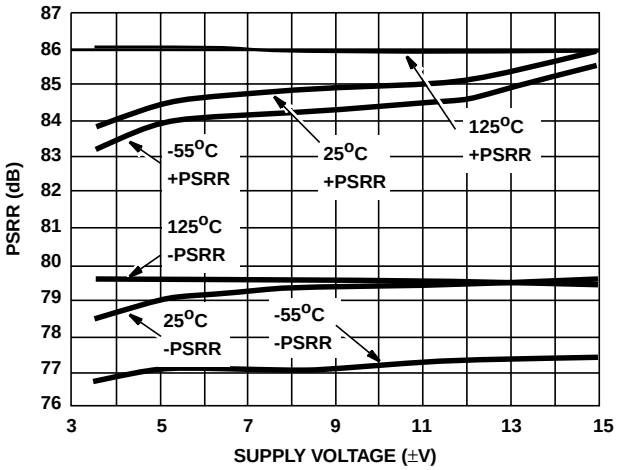


FIGURE 13. PSRR vs SUPPLY VOLTAGE (AVERAGE OF 3 LOTS)

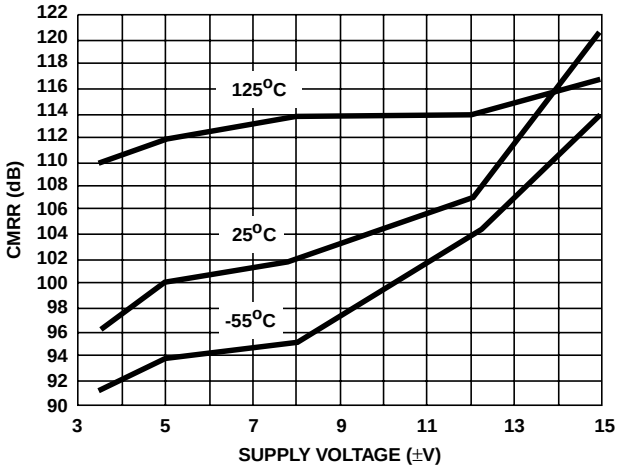


FIGURE 14. CMRR vs SUPPLY VOLTAGE (AVERAGE OF 3 LOTS)

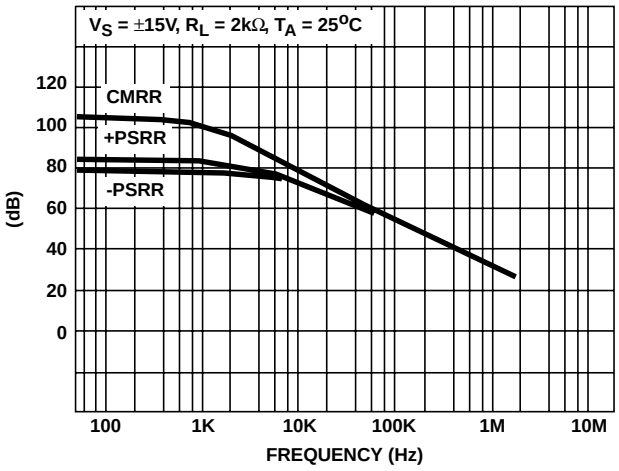


FIGURE 15. REJECTION RATIOS vs FREQUENCY

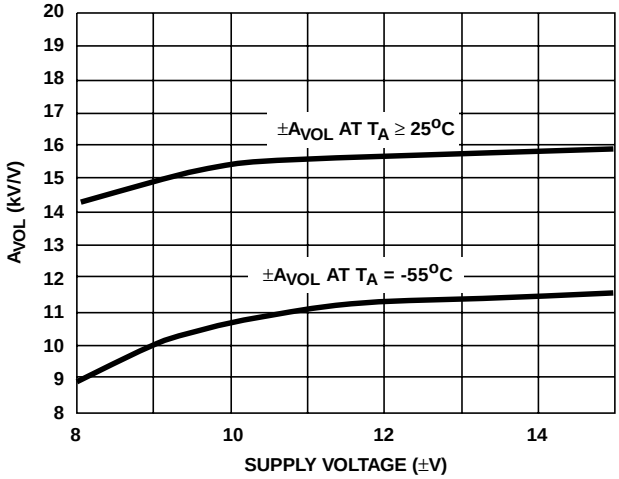


FIGURE 16. OPEN LOOP GAIN vs SUPPLY VOLTAGE (AVERAGE OF 3 LOTS)

Typical Performance Curves (Continued)

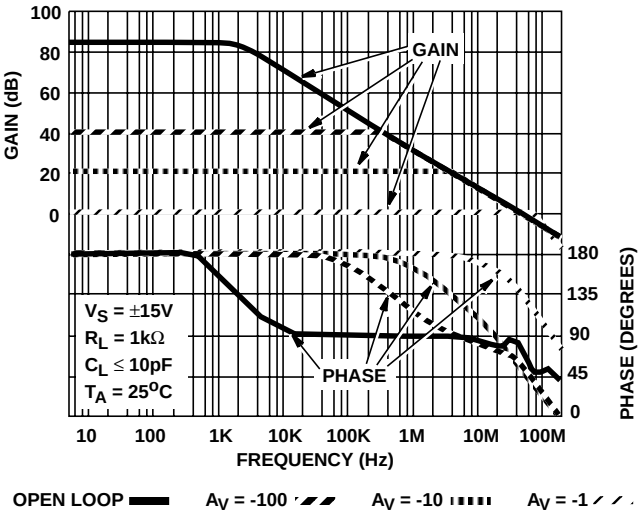


FIGURE 17. GAIN AND PHASE FREQUENCY RESPONSE

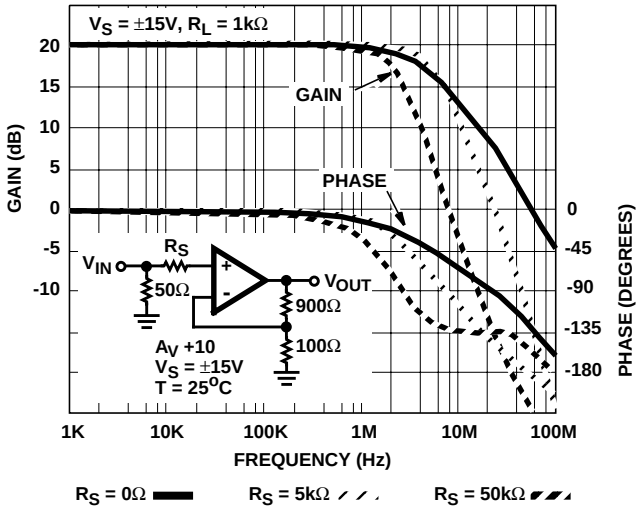


FIGURE 18. SMALL SIGNAL BANDWIDTH vs SOURCE RESISTANCE

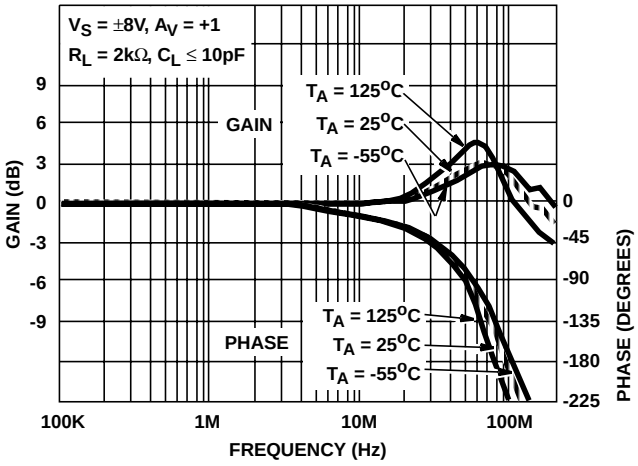


FIGURE 19. CLOSED LOOP FREQUENCY RESPONSE

Die Characteristics

DIE DIMENSIONS:

80 mils x 90 mils x 19 mils
2020µm x 2280µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride(Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

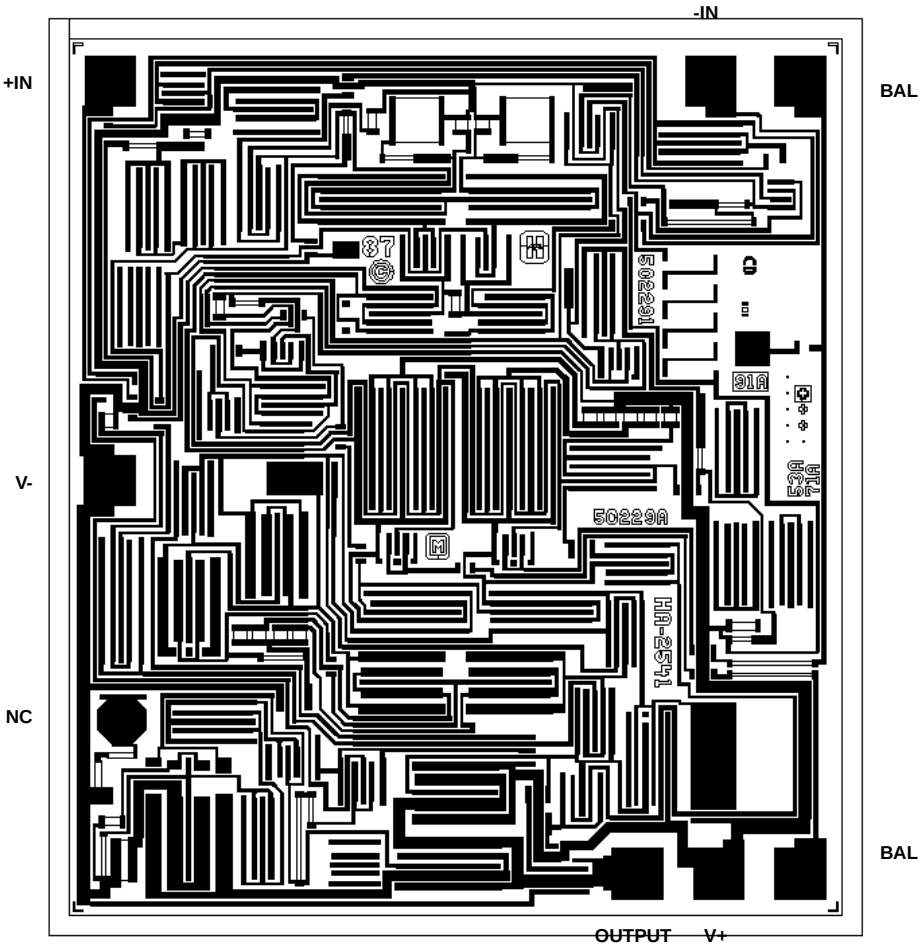
41

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2541



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**