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H8/3714 Series

HD6433712
HD6433713
HD6433714, HD6473714

Hardware Manual

Preface

The H8/300L Series of single-chip microcomputers has the high-speed H8/300L CPU at its core, with many necessary peripheral functions on-chip. The H8/300L CPU instruction set is compatible with the H8/300 CPU, and is ideal for realtime control.

The H8/3714 Series has a system-on-a-chip architecture that includes such peripheral functions as a vacuum fluorescent display controller/driver, five timers, a 14-bit PWM, a two-channel serial communication interface, and an A/D converter. It also has high-voltage pins capable of directly driving a vacuum fluorescent display, making it ideal for use in systems employing this type of display.

This manual describes the hardware of the H8/3714 Series. For details on the instruction set, refer to the H8/300L Series Programming Manual.

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Section 1 Overview

1.1 Overview

The H8/300L Series is a series of single-chip microcontrollers (MCU: microcomputer unit) built around the high-speed H8/300L CPU and equipped with peripheral system functions on-chip.

Within the H8/300L Series, the H8/3714 Series microcontrollers are equipped with high-voltage pins. On-chip peripheral functions include a vacuum fluorescent display (VFD) controller/driver, timers, a 14-bit pulse width modulator (digital-to-analog converter), two serial communication interface channels, and an analog-to-digital converter. Together, these functions make the H8/3714 Series ideally suited for embedded control of systems requiring a vacuum fluorescent display. On-chip memory is 16 kbytes of ROM and 384 bytes of RAM in the H8/3712, 24 kbytes of ROM and 384 bytes of RAM in the H8/3713, or 32 kbytes of ROM and 512 bytes of RAM in the H8/3714, providing a choice for systems of different sizes. The ZTAT™* versions of the H8/3714 come with user-programmable PROM.

Table 1 summarizes the features of the H8/3714 Series.

Note: * ZTAT (zero turn-around time) is a trademark of Hitachi, Ltd.

Table 1-1 Features

Item	Description
CPU	General-register architecture
	• General registers: Sixteen 8-bit registers (can be used as eight 16-bit registers)
	Operating speed
	• Max. operating speed: 4.19 MHz
	• Add/subtract: 0.5 µs (operating at ϕ = 4 MHz)
	• Multiply/divide: 3.5 µs (operating at ϕ = 4 MHz)
	• Can run on 32 kHz subclock
	Instruction set compatible with H8/300 CPU
	• Instruction length of 2 bytes or 4 bytes
	• Basic arithmetic operations between registers
	• MOV instruction for data transfer between memory and registers
	Instruction features
	• Multiply (8 bits $\times$ 8 bits)
	• Divide (16 bits $\div$ 8 bits)
	• Bit accumulator
	• Register-indirect designation of bit position
Memory	• H8/3714: 32 kbyte ROM, 512 byte RAM
	• H8/3713: 24 kbyte ROM, 384 byte RAM
	• H8/3712: 16 kbyte ROM, 384 byte RAM

Table 1-1 Features (cont)

Item	Description
Timers	• Timer A: 8-bit interval timer Count-up timer with selection of eight internal clock signals divided from the system clock (ϕ)* and four clock signals divided from the subclock (ϕ_{SUB}) • Timer B: 8-bit reload timer Count-up timer with selection of seven internal clock signals or event input from pin $P1_0/\overline{IRQ_0}$ • Timer C: 8-bit reload timer Count-up/count-down timer with selection of seven internal clock signals or event input from pin $P1_1/\overline{IRQ_1}$ • Timer D: 8-bit event counter Up-counter for counting input from pin $P1_6/\overline{EVENT}$ • Timer E: 8-bit reloadable timer Count-up timer with selection of eight internal clock signals. Square-wave (50% duty cycle) output with a fixed frequency or variable frequency controlled by timer E overflow can be selected by pin $P1_5/\overline{IRQ_5}$/TMOE settings. Note: * ϕ indicates a clock frequency that is divided in half from the original oscillator frequency
14-bit PWM	• Pulse-division PWM designed for less ripple • Can be used as a 14-bit D/A converter by connecting to an external low-pass filter
VFD driver/controller	• Up to 24 segment pins and up to 16 digit pins (of which 8 are for both uses) • Brightness adjustable in 8 steps (dimmer function) • Digit and segment pins can be switched to use as general-purpose high-voltage pins • Key scan interval can be enabled or disabled • Interrupt can be requested when key scan interval starts
Serial communication interface	• 2-channel synchronous SCI1 and SCI2 • Choice of 8-bit or 16-bit data transfer (SCI1) • Automatic transfer of 32-byte data (SCI2) • Overrun error detection possible • Interrupt can be requested when transfer is complete

Table 1-1 Features (cont)

Item	Description
A/D converter	• Successive approximations using a resistance ladder • Resolution: 8 bits • 8-channel analog input port • Conversion time: 31/ϕ or 62/ϕ per channel • Interrupt can be requested at completion of A/D conversion
I/O ports	• High-voltage I/O pins: 32 • High-voltage input pin: 1 • Standard-voltage I/O pins: 12 • Standard-voltage input pins: 9
Interrupts	• Four external interrupt pins: $\overline{IRQ_5}$, $\overline{IRQ_4}$, $\overline{IRQ_1}$, $\overline{IRQ_0}$ • Ten internal interrupt sources
Low power operation modes	• Sleep mode • Standby mode • Watch mode • Subactive mode
Other	• Built-in pulse generators for system clock and subclock • Timer A can run on the subclock for use as a time base

Product lineup

Product Code			
Mask ROM Version	**ZTAT™ Version**	**Package**	**ROM/RAM Size**
HD6433714H	HD6473714H	64 pin GFP (FP-64A)	ROM: 32 kbytes RAM: 512 bytes
HD6433714P	HD6473714P	64 pin SDIP (DP-64S)	
HD6433713H	—	64 pin QFP (FP-64A)	ROM: 24 kbytes RAM: 384 bytes
HD6433713P	—	64 pin SDIP (DP-64S)	
HD6433712H	—	64 pin QFP (FP-64A)	ROM: 16 kbytes RAM: 384 bytes
HD6433712P	—	64 pin SDIP (DP-64S)	

1.2 Internal Block Diagram

Figure 1-1 is an internal block diagram of the H8/3714 Series.

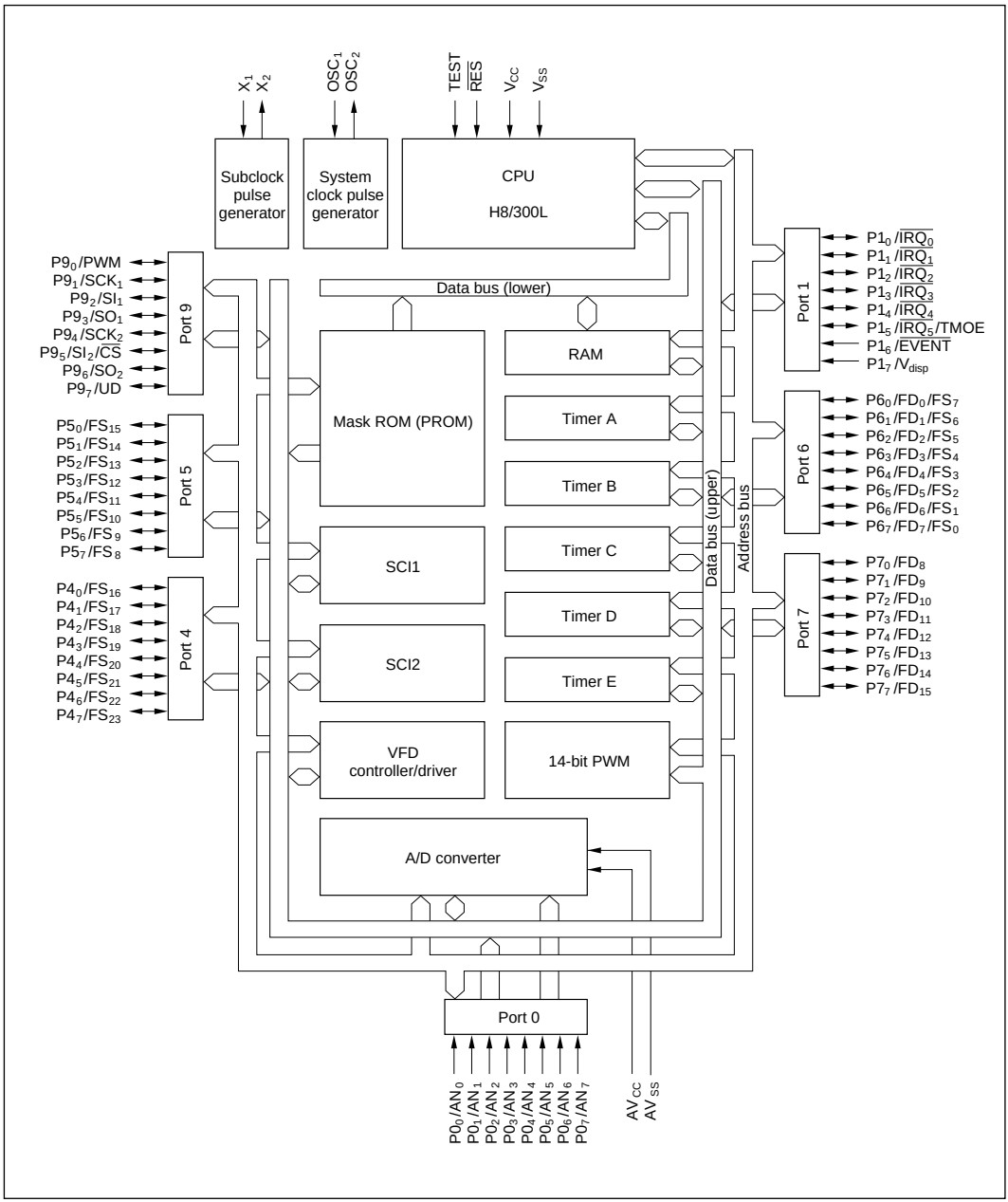


Figure 1-1 Block Diagram

1.3 Pin Arrangement and Functions

1.3.1 Pin Arrangement

The pin arrangements for the H8/3714 Series are shown in figure 1-2 (FP-64A) and figure 1-3 (DP-64S).

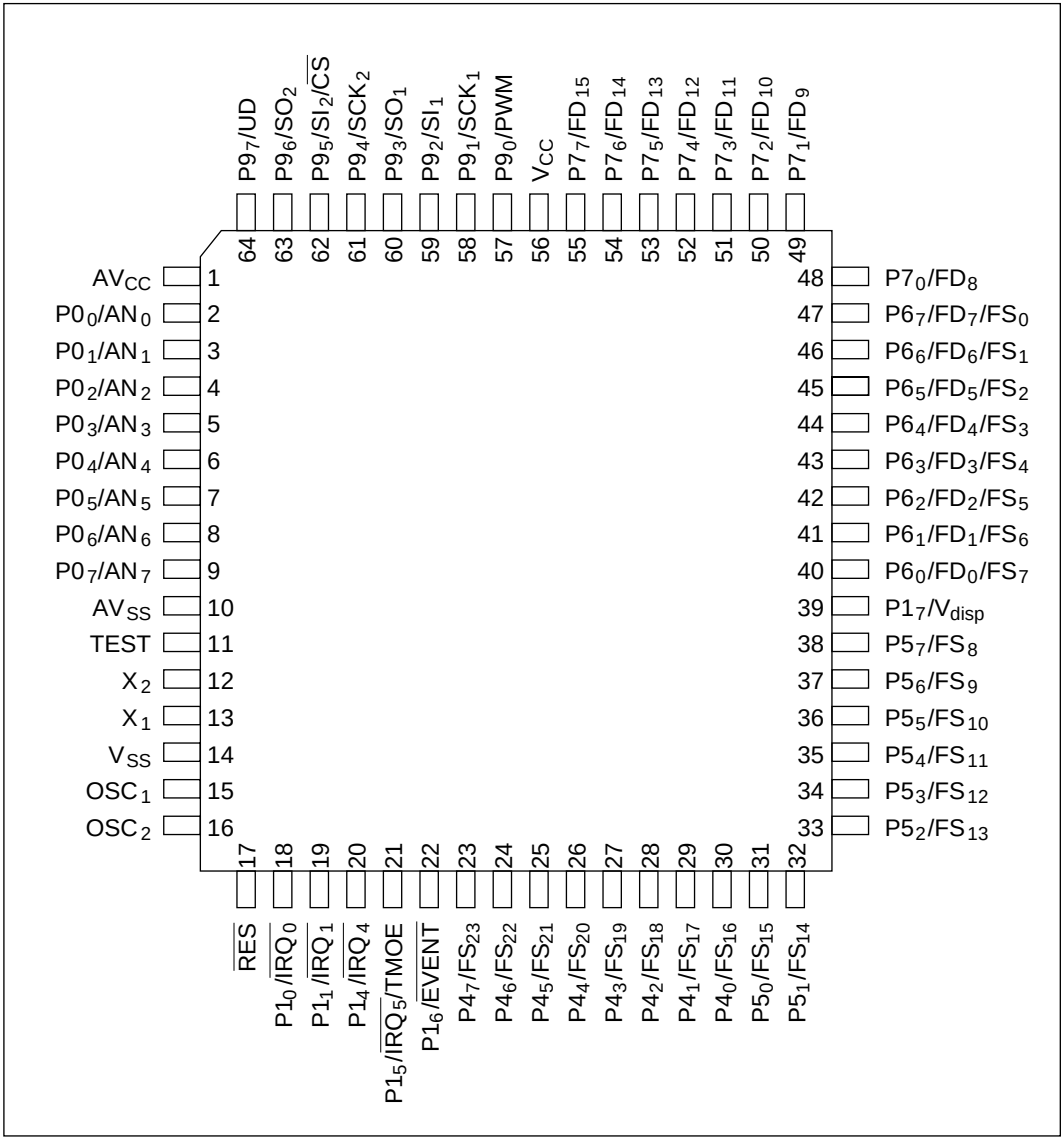


Figure 1-2 Pin Arrangement (FP-64A: Top View)

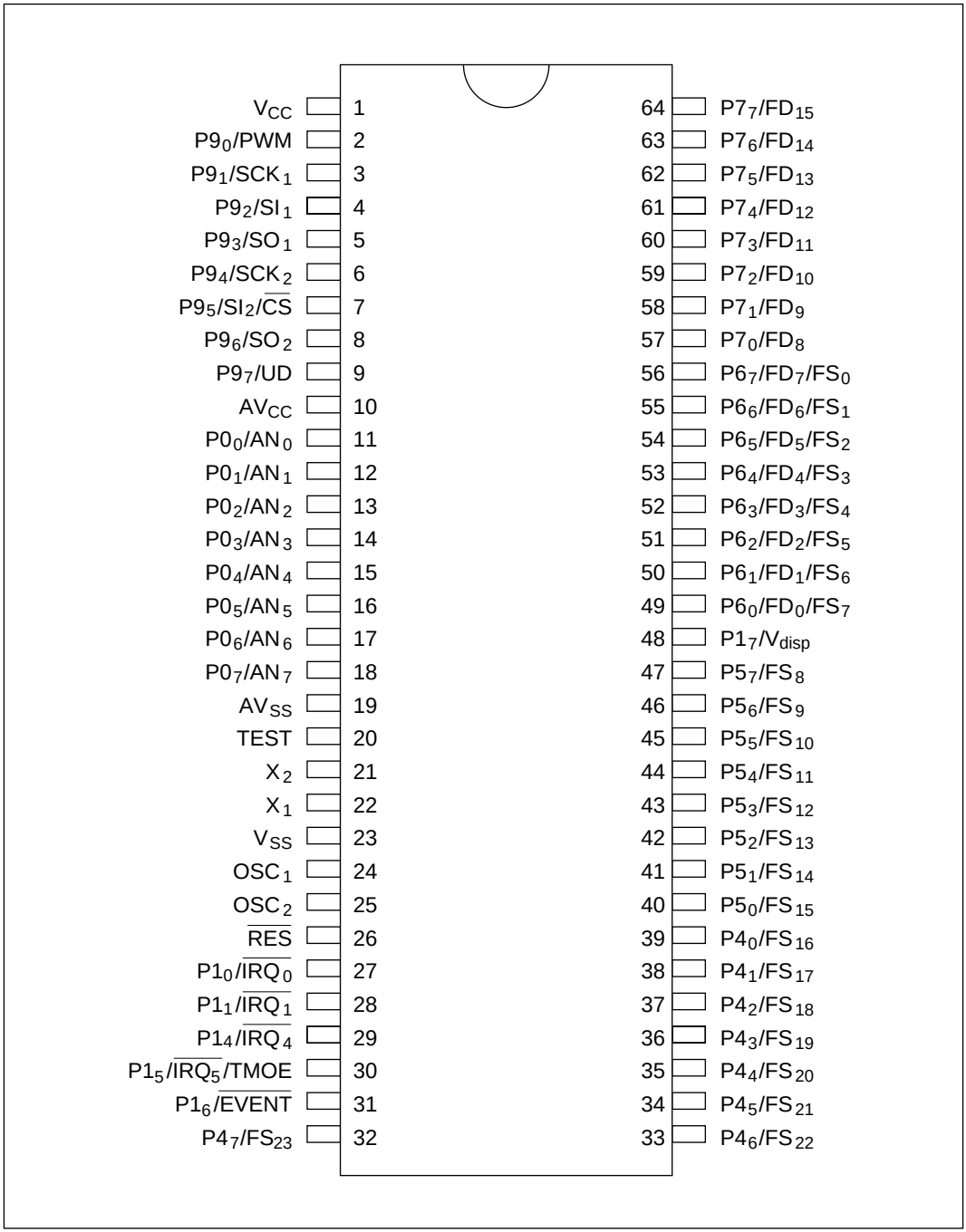


Figure 1-3 Pin Arrangement (DP-64S: Top View)

1.3.2 Pin Functions

1. List of pin functions

Table 1-2 lists the pin functions of the LSI.

Table 1-2 List of Pin Functions

Pin No.			
FP-64A	**DP-64S**	**Name and Function**	**PROM Mode**
6	15	$P0_4/AN_4$ (standard input port/analog input channel)	NC
7	16	$P0_5/AN_5$ (standard input port/analog input channel)	NC
8	17	$P0_6/AN_6$ (standard input port/analog input channel)	NC
9	18	$P0_7/AN_7$ (standard input port/analog input channel)	NC
10	19	AV_{SS} (reference voltage for A/D converter)	V_{SS}
11	20	TEST (test pin)	V_{CC}
12	21	X_2 (subclock oscillator connection)	NC
13	22	X_1 (subclock oscillator connection)	V_{CC}
14	23	V_{SS} (ground)	V_{SS}
15	24	OSC_1 (system clock oscillator connection)	V_{SS}
16	25	OSC_2 (system clock oscillator connection)	NC
17	26	$\overline{RES}$ (reset input)	V_{PP}
18	27	$P1_0/\overline{IRQ_0}$ (standard I/O port/external interrupt or timer B event input)	NC
19	28	$P1_1/\overline{IRQ_1}$ (standard I/O port/external interrupt or timer C event input)	NC
20	29	$P1_4/\overline{IRQ_4}$ (standard I/O port/external interrupt)	NC
21	30	$P1_5/\overline{IRQ_5}$/TMOE (standard I/O port/external interrupt/warning tone output)	NC
22	31	$P1_6/\overline{EVENT}$ (standard input port/timer D event input)	EA_9
23	32	$P4_7/FS_{23}$ (high-voltage I/O port/VFD segment output)	NC
24	33	$P4_6/FS_{22}$ (high-voltage I/O port/VFD segment output)	NC
25	34	$P4_5/FS_{21}$ (high-voltage I/O port/VFD segment output)	NC
26	35	$P4_4/FS_{20}$ (high-voltage I/O port/VFD segment output)	NC
27	36	$P4_3/FS_{19}$ (high-voltage I/O port/VFD segment output)	V_{CC}
28	37	$P4_2/FS_{18}$ (high-voltage I/O port/VFD segment output)	V_{CC}
29	38	$P4_1/FS_{17}$ (high-voltage I/O port/VFD segment output)	V_{SS}

Table 1-2 List of Pin Functions (cont)

Pin No.			
FP-64A	**DP-64S**	**Name and Function**	**PROM Mode**
30	39	$P4_0/FS_{16}$ (high-voltage I/O port/VFD segment output)	V_{SS}
31	40	$P5_0/FS_{15}$ (high-voltage I/O port/VFD segment output)	EA_0
32	41	$P5_1/FS_{14}$ (high-voltage I/O port/VFD segment output)	EA_1
33	42	$P5_2/FS_{13}$ (high-voltage I/O port/VFD segment output)	EA_2
34	43	$P5_3/FS_{12}$ (high-voltage I/O port/VFD segment output)	EA_3
35	44	$P5_4/FS_{11}$ (high-voltage I/O port/VFD segment output)	EA_4
36	45	$P5_5/FS_{10}$ (high-voltage I/O port/VFD segment output)	EA_5
37	46	$P5_6/FS_9$ (high-voltage I/O port/VFD segment output)	EA_6
38	47	$P5_7/FS_8$ (high-voltage I/O port/VFD segment output)	EA_7
39	48	$P1_7/V_{disp}$ (high-voltage input port/VFD power source)	V_{CC}
40	49	$P6_0/FD_0/FS_7$ (high-voltage I/O port/VFD digit-segment output)	NC
41	50	$P6_1/FD_1/FS_6$ (high-voltage I/O port/VFD digit-segment output)	NC
42	51	$P6_2/FD_2/FS_5$ (high-voltage I/O port/VFD digit-segment output)	NC
43	52	$P6_3/FD_3/FS_4$ (high-voltage I/O port/VFD digit-segment output)	NC
44	53	$P6_4/FD_4/FS_3$ (high-voltage I/O port/VFD digit-segment output)	NC
45	54	$P6_5/FD_5/FS_2$ (high-voltage I/O port/VFD digit-segment output)	NC
46	55	$P6_6/FD_6/FS_1$ (high-voltage I/O port/VFD digit-segment output)	NC
47	56	$P6_7/FD_7/FS_0$ (high-voltage I/O port/VFD digit-segment output)	NC
48	57	$P7_0/FD_8$ (high-voltage I/O port/VFD digit output)	EA_8
49	58	$P7_1/FD_9$ (high-voltage I/O port/VFD digit output)	$\overline{OE}$
50	59	$P7_2/FD_{10}$ (high-voltage I/O port/VFD digit output)	EA_{10}

Table 1-2 List of Pin Functions (cont)

Pin No.			
FP-64A	**DP-64S**	**Name and Function**	**PROM Mode**
51	60	$P7_3/FD_{11}$ (high-voltage I/O port/VFD digit output)	EA_{11}
52	61	$P7_4/FD_{12}$ (high-voltage I/O port/VFD digit output)	EA_{12}
53	62	$P7_5/FD_{13}$ (high-voltage I/O port/VFD digit output)	EA_{13}
54	63	$P7_6/FD_{14}$ (high-voltage I/O port/VFD digit output)	EA_{14}
55	64	$P7_7/FD_{15}$ (high-voltage I/O port/VFD digit output)	$\overline{CE}$
56	1	V_{CC} (system power source)	V_{CC}
57	2	$P9_0$/PWM (standard I/O port/PWM output)	EO_0
58	3	$P9_1/SCK_1$ (standard I/O port/clock output)	EO_1
59	4	$P9_2/SI_1$ (standard I/O port/data input)	EO_2
60	5	$P9_3/SO_1$ (standard I/O port/data output)	EO_3
61	6	$P9_4/SCK_2$ (standard I/O port/clock I/O)	EO_4
62	7	$P9_5/SI_2/\overline{CS}$ (standard I/O port/data input/chip select output)	EO_5
63	8	$P9_6/SO_2$ (standard I/O port/data output)	EO_6
64	9	$P9_7$/UD (standard I/O port/timer C up-down control)	EO_7
1	10	AV_{CC} (reference power source for A/D converter)	V_{CC}
2	11	PO_0/AN_0 (standard input port/analog input channel)	NC
3	12	PO_1/AN_1 (standard input port/analog input channel)	NC
4	13	PO_2/AN_2 (standard input port/analog input channel)	NC
5	14	PO_3/AN_3 (standard input port/analog input channel)	NC

Notes: 1. NC pins should be left unconnected.
2. Details on PROM mode are given in 4.2, PROM Mode.

Table 1-3 explains the functions of each pin in more detail.

Table 1-3 Pin Functions

Type	Symbol	Pin No. FP-64A	Pin No. DP-64S	I/O	Name and Functions
Power supply pins	V_{CC}	56	1	Input	**Power source:** Connects to a power supply (+5 V) All V_{CC} pins should be connected to the system power supply (+5 V).
	V_{SS}	14	23	Input	**Ground:** Connects to a power supply (0 V). All V_{SS} pins should be connected to the system power supply (0 V).
	AV_{CC}	1	10	Input	**Analog power supply:** This is the reference power supply pin for the A/D converter. When the A/D converter is not used, connect this pin to the system power supply (+5 V).
	AV_{SS}	10	19	Input	**Analog ground:** This is the A/D converter ground pin. It should be connected to the system power supply (0 V).
	V_{disp}	39	48	Input	**VFD power supply:** This pin should be connected to a VFD driver power supply.
Clock pins	OSC_1	15	24	Input	This pin connects to a crystal or ceramic oscillator, or can be used to input an external clock. See section 6, Clock Pulse Generators, for a typical connection diagram.
	OSC_2	16	25	Output	This pin connects to a crystal or ceramic oscillator.
	X_1	13	22	Input	This pin connects to a 32.768 kHz crystal oscillator. For a typical connection diagram, see section 6, Clock Pulse Generators.
	X_2	12	21	Output	This pin connects to a 32.768 kHz crystal oscillator.

Table 1-3 Pin Functions (cont)

Type	Symbol	Pin No. FP-64A	Pin No. DP-64S	I/O	Name and Functions
System control	$\overline{RES}$	17	26	Input	**Reset:** When this pin goes to low level, the chip is reset.
	TEST	11	20	Input	**Test:** This pin is not for use in application systems. It should be connected to V_{SS}.
Interrupt pins	$\overline{IRQ_0}$	18	27	Input	**External interrupt request 0:** This is an input pin for external interrupts for which there is a choice between rising and falling edge sensing. It can be used to exit low-power mode. This pin can be used as the event input pin for timer B. A noise cancel function is also provided.
	$\overline{IRQ_1}$	19	28	Input	**External interrupt request 1:** This is an input pin for external interrupts for which there is a choice between rising and falling edge sensing. It can be used to exit low-power mode. This pin can be used as the event input pin for timer C.
	$\overline{IRQ_4}$	20	29	Input	**External interrupt request 4:** This is an input pin for external interrupts for which there is a choice between rising and falling edge sensing.
	$\overline{IRQ_5}$	21	30	Input	**External interrupt request 5:** This is an input pin for external interrupts that are detected at the falling edge.

Table 1-3 Pin Functions (cont)

Type	Symbol	Pin No. FP-64A	Pin No. DP-64S	I/O	Name and Functions
Timer pins	$\overline{IRQ_0}$	18	27	Input	**Timer B event counter input:** This is an event input pin for input to the timer B counter.
	$\overline{IRQ_1}$	19	28	Input	**Timer C event counter input:** This is an event input pin for input to the timer C counter.
	UD	64	9	Input	**Timer C up/down select:** This pin selects whether the timer C counter is used for up- or down-counting. At high level it selects down-counting, and at low level up-counting. Input to this pin is valid only when bit TMC6 in timer mode register C (TMC) is set to 1.
	$\overline{EVENT}$	22	31	Input	**Timer D event counter input:** This is an event input pin for input to the timer D counter.
	TMOE	21	30	Output	**Timer E output:** This is an output pin for waveforms generated by the timer E output circuit.
14-bit PWM pin	PWM	57	2	Output	**14-bit PWM output:** This is an output pin for waveforms generated by the 14-bit PWM.
Serial communication interface (SCI) pins	SO_1 SO_2	60 63	5 8	Output	**Serial transmit data output (channels 1 and 2):** These are SCI data output pins.
	SI_1 SI_2	59 62	4 7	Input	**Serial receive data input (channels 1 and 2):** These are SCI data input pins.
	SCK_1 SCK_2	58 61	3 6	I/O	**Serial clock I/O (channels 1 and 2):** These are SCI clock I/O pins.
	$\overline{CS}$	62	7	Output	**Chip select output:** When SCI2 is in transmit mode and the serial clock is an internal clock, this pin goes low. This function is valid when bit SI2 in port mode register 2 (PMR2) is 1 and the CS bit in PMR3 is 1.

Table 1-3 Pin Functions (cont)

Type	Symbol	Pin No. FP-64A	Pin No. DP-64S	I/O	Name and Functions
I/O ports	$P0_7$ to $P0_0$	9 to 2	18 to 11	Input	**Port 0:** This is an 8-bit input port.
	$P1_7$	39	48	Input	**Port 1 (bit 7):** This is a 1-bit high-voltage input pin.
	$P1_6$	22	31	Input	**Port 1 (bit 6):** This is a 1-bit input pin.
	$P1_5$, $P1_4$, $P1_1$, $P1_0$	21 to 18	30 to 27	I/O	**Port 1:** This is a 4-bit group of I/O pins. Input or output can be designated for each bit by means of port control register 1 (PCR1).
	$P4_7$ to $P4_0$	23 to 30	32 to 39	I/O	**Port 4:** This is an 8-bit high-voltage I/O port.
	$P5_7$ to $P5_0$	38 to 31	47 to 40	I/O	**Port 5:** This is an 8-bit high-voltage I/O port.
	$P6_7$ to $P6_0$	47 to 40	56 to 49	I/O	**Port 6:** This is an 8-bit high-voltage I/O port.
	$P7_7$ to $P7_0$	55 to 48	64 to 57	I/O	**Port 7:** This is an 8-bit high-voltage I/O port.
	$P9_7$ to $P9_0$	64 to 57	9 to 2	I/O	**Port 9:** This is an 8-bit I/O port. Input or output can be designated for each bit by means of PCR9.
A/D converter	AN_7 to AN_0	9 to 2	18 to 11	Input	**Analog input channels 7 to 0:** These are analog data input channels to the A/D converter.
VFD controller/ driver	FD_{15} to FD_0	55 to 40	64 to 49	Output	**VFD digit output:** These are digit output pins from the VFD controller/driver.
	FS_{23} to FS_8 FS_7 to FS_0	23 to 38 40 to 47	32 to 47 49 to 56	I/O	**VFD segment output:** These are segment output pins from the VFD controller/driver. When a key scan interval is set during display operations, these pins can be used by the CPU during this interval as general-purpose I/O ports.

Section 2 CPU

2.1 Overview

The H8/300L CPU has sixteen 8-bit general registers, which can also be paired as eight 16-bit registers. Its concise, optimized instruction set is designed for high-speed operation.

2.1.1 Features

The main features of the H8/300L CPU are listed below.

- General-register architecture
  - — Sixteen 8-bit general registers, also usable as eight 16-bit general registers
- Instruction set with 55 basic instructions, including:
  - — Multiply and divide instructions
  - — Powerful bit-manipulation instructions
- Eight addressing modes

— Register direct	Rn
— Register indirect	@Rn
— Register indirect with displacement	@(d:16, Rn)
— Register indirect with post-increment or pre-decrement	@Rn+ or @–Rn
— Absolute address	@aa:8 or @aa:16
— Immediate	#xx:8 or #xx:16
— Program-counter relative	@(d:8, PC)
— Memory indirect	@@aa:8

- 64-kbyte address space
- High-speed operation
  - — All frequently used instructions are executed in two to four states
  - — High-speed arithmetic and logic operations
  - — 8- or 16-bit register-register add or subtract: 0.5 µs*
  - — 8 × 8-bit multiply: 3.5 µs*
  - — 16 ÷ 8-bit divide: 3.5 µs*
- Low-power operation modes
  - — SLEEP instruction for transfer to low-power operation

Note: * These values are at ϕ = 4 MHz.

2.1.2 Address Space

The H8/300L CPU supports an address space of up to 64 kbytes for storing program code and data.

The memory map varies with the ROM size. Figure 2-1 gives memory map.

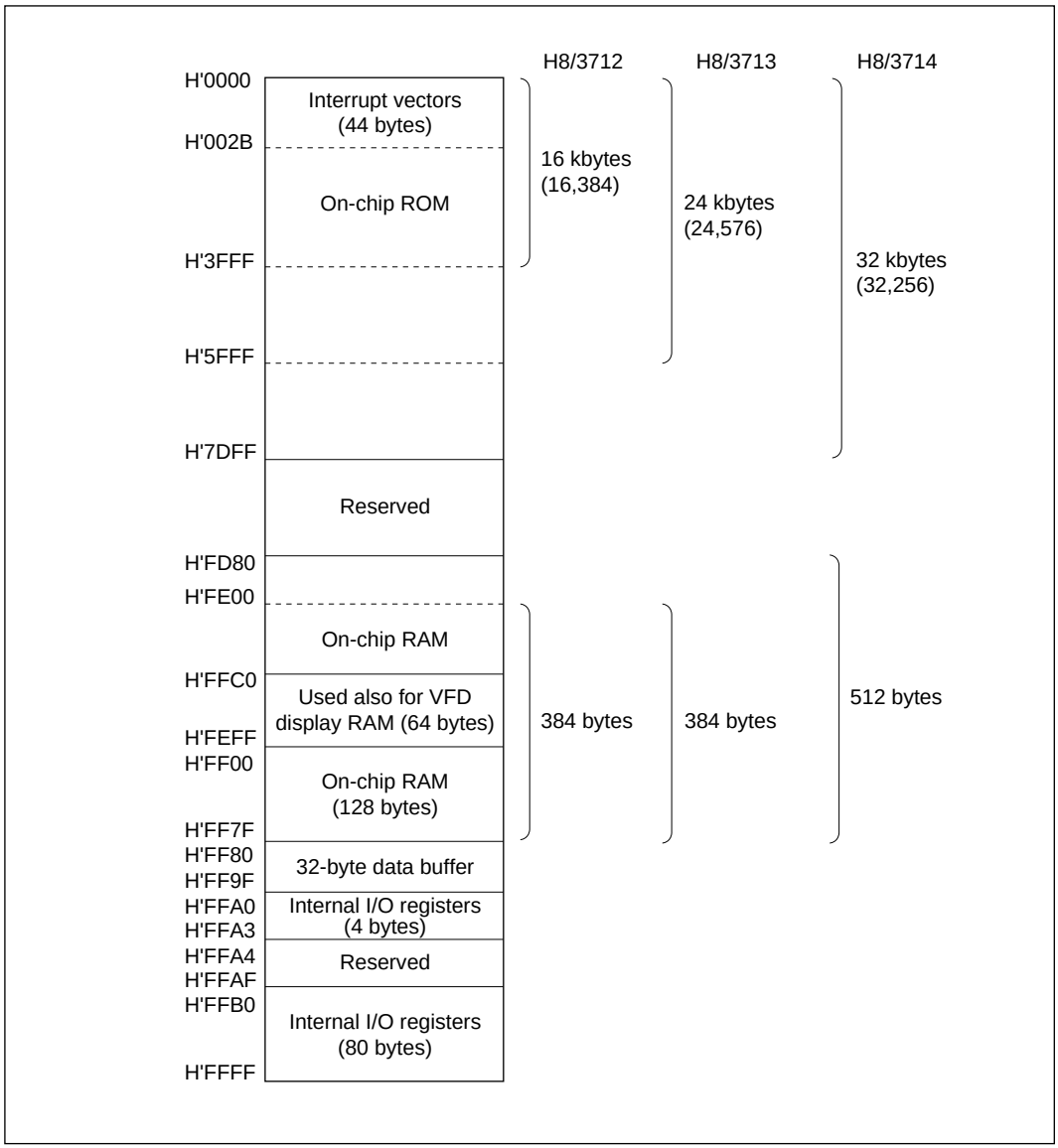


Figure 2-1 Memory Map

2.1.3 Register Configuration

Figure 2-2 shows the register structure of the H8/300L CPU. There are two groups of registers: the general registers and control registers.

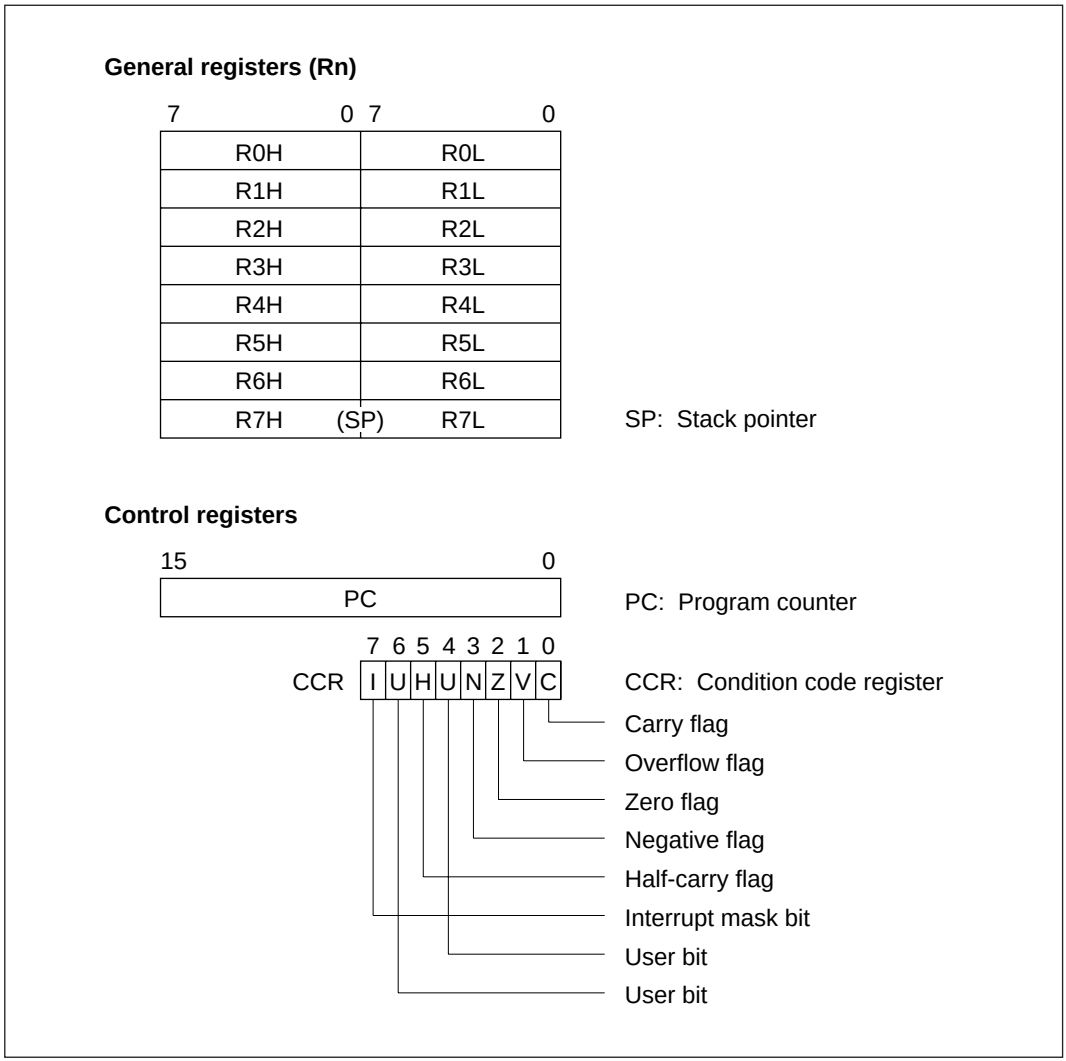


Figure 2-2 CPU Registers

2.2 Register Descriptions

2.2.1 General Registers

All the general registers can be used as both data registers and address registers.

When used as data registers, they can be accessed as 16-bit registers (R0 to R7), or the high bytes (R0H to R7H) and low bytes (R0L to R7L) can be accessed separately as 8-bit registers.

When used as address registers, the general registers are accessed as 16-bit registers (R0 to R7).

R7 also functions as the stack pointer (SP), used implicitly by hardware in exception processing and subroutine calls. When it functions as the stack pointer, as indicated in figure 2-3, SP (R7) points to the top of the stack.

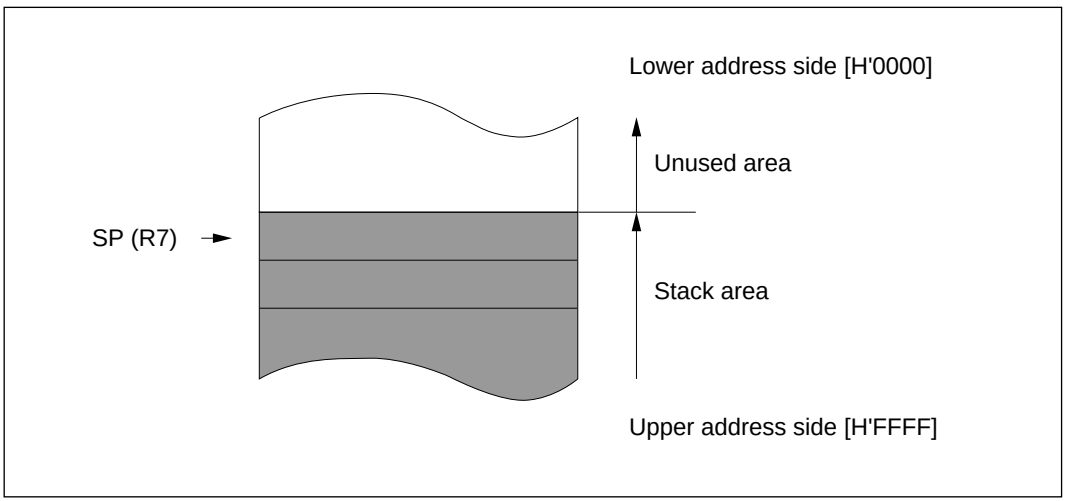


Figure 2-3 Stack Pointer

2.2.2 Control Registers

The CPU control registers include a 16-bit program counter (PC) and an 8-bit condition code register (CCR).

1. **Program Counter (PC):** This 16-bit register indicates the address of the next instruction the CPU will execute. All instructions are fetched 16 bits (1 word) at a time, so the least significant bit of the PC is ignored (always regarded as 0).

2. **Condition Code Register (CCR):** This 8-bit register contains internal status information, including the interrupt mask bit (I) and half-carry (H), negative (N), zero (Z), overflow (V), and carry (C) flags.

Bit 7—Interrupt Mask Bit (I): When this bit is set to 1, interrupts are masked. This bit is set to 1 automatically at the start of exception handling. The interrupt mask bit may be read and written by software. For further details, see 3.2.2, Interrupts.

Bit 6—User Bit (U): Can be written and read by software (using the LDC, STC, ANDC, ORC, and XORC instructions).

Bit 5—Half-Carry Flag (H): When the ADD.B, ADDX.B, SUB.B, SUBX.B, CMP.B, or NEG.B instruction is executed, this flag is set to 1 if there is a carry or borrow at bit 3, and is cleared to 0 otherwise.

The H flag is used implicitly by the DAA and DAS instructions.

When the ADD.W, SUB.W, or CMP.W instruction is executed, the H flag is set to 1 if there is a carry or borrow at bit 11, and is cleared to 0 otherwise.

Bit 4—User Bit (U): Can be written and read by software (using the LDC, STC, ANDC, ORC, and XORC instructions).

Bit 3—Negative Flag (N): Indicates the most significant bit (sign bit) of the result of an instruction.

Bit 2—Zero Flag (Z): Set to 1 to indicate zero data, and cleared to 0 to indicate non-zero data.

Bit 1—Overflow Flag (V): Set to 1 when an arithmetic overflow occurs, and cleared to 0 at other times.

Bit 0—Carry Flag (C): Set to 1 when a carry occurs, and cleared to 0 otherwise. Used by:

- Add instructions, to indicate a carry
- Subtract instructions, to indicate a borrow
- Shift and rotate instructions, to store the value shifted out of the end bit

The carry flag is also used as a bit accumulator by bit manipulation instructions.

Some instructions leave some or all of the flag bits unchanged. The LDC, STC, ANDC, ORC, and XORC instructions enable the CPU to load and store the CCR, and to set or clear selected bits by logic operations. The N, Z, V, and C flags are used as branching conditions for conditional branching (Bcc) instructions.

Refer to the *H8/300L Series Programming Manual* for the action of each instruction on the flag bits.

2.2.3 Initial Register Values

When the CPU is reset, the program counter (PC) is initialized to the value stored at address H'0000 in the vector table, and the I bit in the CCR is set to 1. The other CCR bits and the general registers are not initialized. In particular, the stack pointer (R7) is not initialized. To prevent program crashes the stack pointer should be initialized by software, by the first instruction executed after a reset.

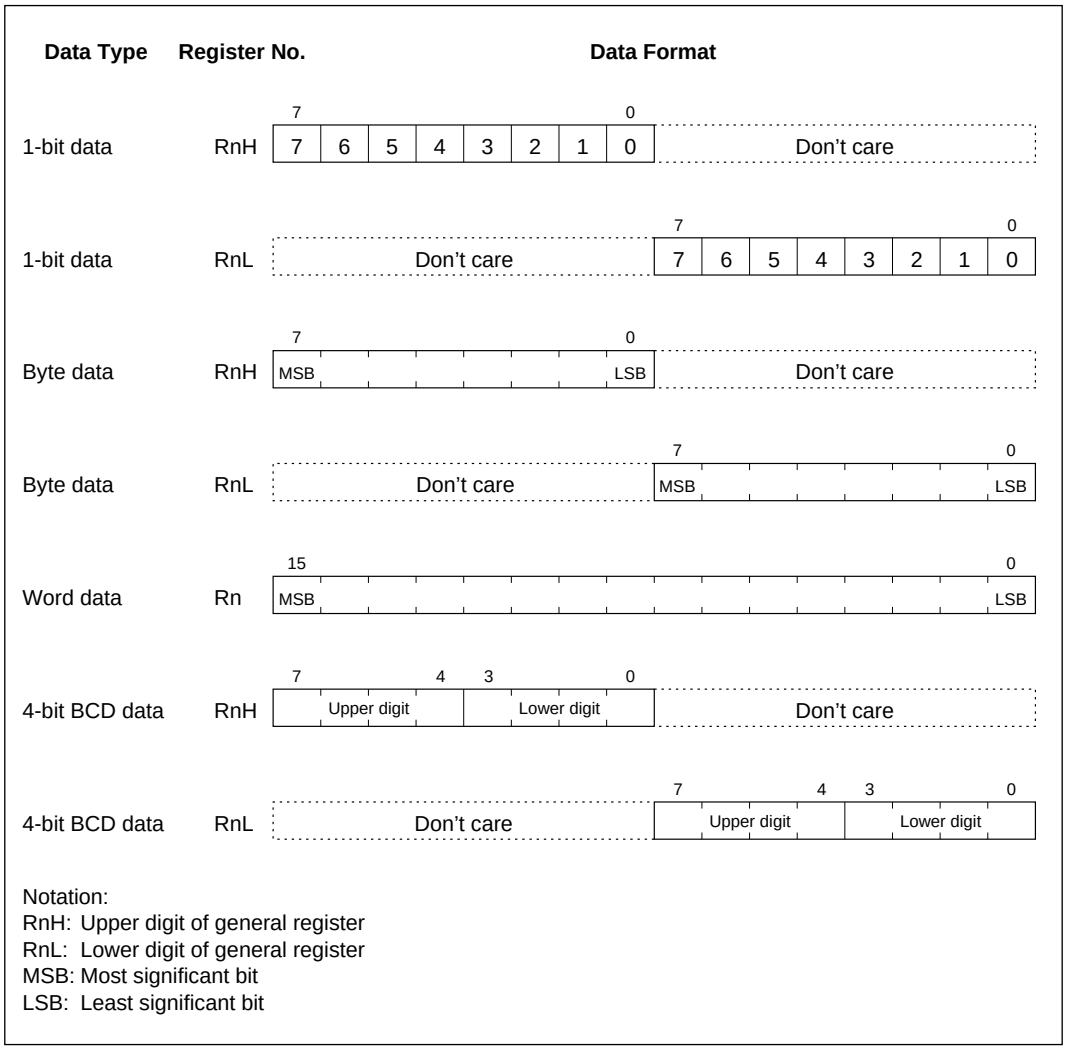
2.3 Data Formats

The H8/300L CPU can process 1-bit data, 4-bit (BCD) data, 8-bit (byte) data, and 16-bit (word) data.

- Bit manipulation instructions operate on 1-bit data specified as bit n in a byte operand (n = 0, 1, 2, ..., 7).
- All arithmetic and logic instructions except ADDS and SUBS can operate on byte data.
- The MOV.W, ADD.W, SUB.W, CMP.W, ADDS, SUBS, MULXU (8 bits × 8 bits), and DIVXU (16 bits ÷ 8 bits) instructions operate on word data.
- The DAA and DAS instructions perform decimal arithmetic adjustments on byte data in packed BCD form. Each nibble of the byte is treated as a decimal digit.

2.3.1 Data Formats in General Registers

Data of all the sizes above can be stored in general registers as shown in figure 2-4.



Notation:
RnH: Upper digit of general register
RnL: Lower digit of general register
MSB: Most significant bit
LSB: Least significant bit

Figure 2-4 Register Data Formats

2.3.2 Memory Data Formats

Figure 2-5 indicates the data formats in memory. For access by the H8/300L CPU, word data stored in memory must always begin at an even address. In word access the least significant bit of the address is regarded as 0. If an odd address is specified, the access is performed at the preceding even address. This rule affects the MOV.W instruction, and also applies to instruction fetching.

Word access is possible to the ROM and RAM areas. For details, see 2.8.1, Notes on Data Access.

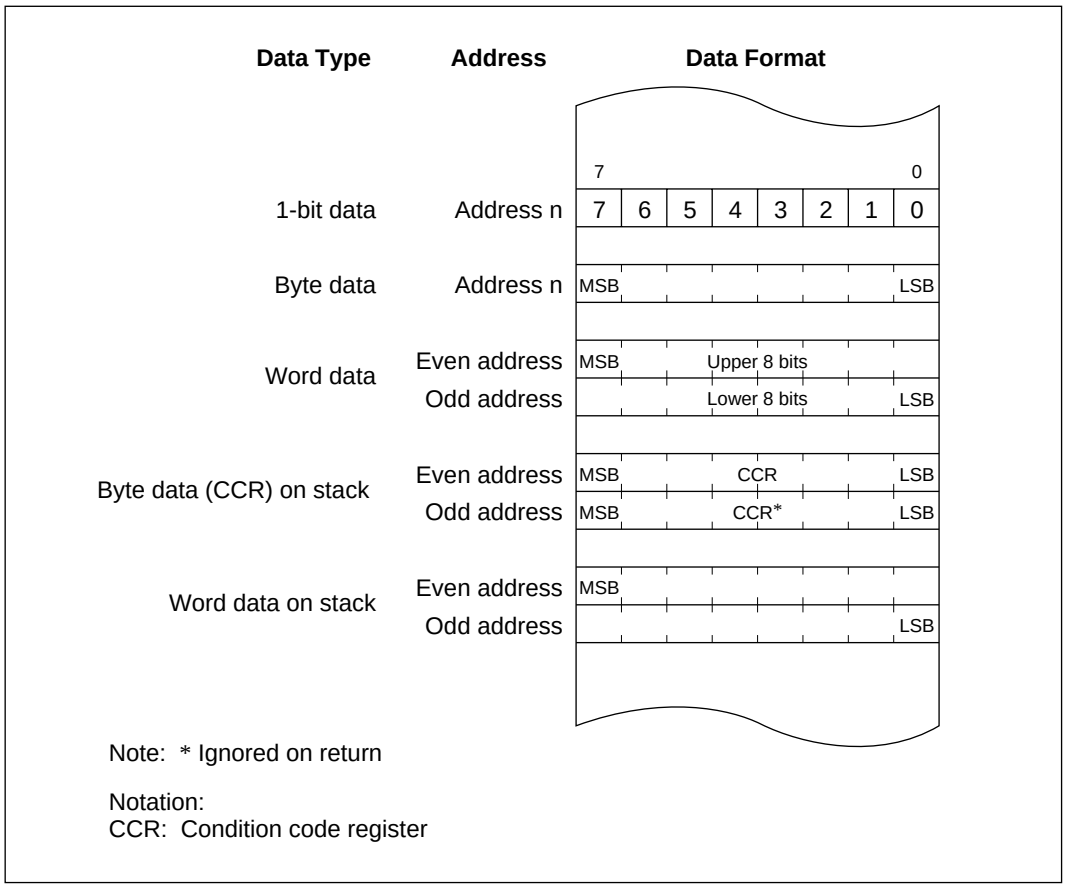


Figure 2-5 Memory Data Formats

When the stack is accessed using R7 as an address register, word access should always be performed. For further details, see 3.2.10, Notes on Stack Area Use. When the CCR is pushed on the stack, two identical copies of the CCR are pushed to make a complete word. When they are restored, the lower byte is ignored.

2.4 Addressing Modes

2.4.1 Addressing Modes

The H8/300L CPU supports the eight addressing modes listed in table 2-1. Each instruction uses a subset of these addressing modes.

Table 2-1 Addressing Modes

No.	Address Modes	Symbol
1	Register direct	Rn
2	Register indirect	@Rn
3	Register indirect with displacement	@(d:16, Rn)
4	Register indirect with post-increment Register indirect with pre-decrement	@Rn+ @–Rn
5	Absolute address	@aa:8 or @aa:16
6	Immediate	#xx:8 or #xx:16
7	Program-counter relative	@(d:8, PC)
8	Memory indirect	@@aa:8

1. **Register Direct—Rn:** The register field of the instruction specifies an 8- or 16-bit general register containing the operand.

   Only the MOV.W, ADD.W, SUB.W, CMP.W, ADDS, SUBS, MULXU (8 bits × 8 bits), and DIVXU (16 bits ÷ 8 bits) instructions have 16-bit operands.

2. **Register Indirect—@Rn:** The register field of the instruction specifies a 16-bit general register containing the address of the operand.

3. **Register Indirect with Displacement—@(d:16, Rn):** The instruction has a second word (bytes 3 and 4) containing a displacement which is added to the contents of the specified general register to obtain the operand address.

   This mode is used only in MOV instructions. For the MOV.W instruction, the resulting address must be even.

4. **Register Indirect with Post-Increment or Pre-Decrement—@Rn+ or @–Rn:**

   - Register indirect with post-increment—@Rn+

     The @Rn+ mode is used with MOV instructions that load registers from memory.

     The register field of the instruction specifies a 16-bit general register containing the address of the operand. After the operand is accessed, the register is incremented by 1 for MOV.B or 2 for MOV.W. For MOV.W, the original contents of the 16-bit general register must be even.

   - Register indirect with pre-decrement—@–Rn

     The @–Rn mode is used with MOV instructions that store register contents to memory.

     The register field of the instruction specifies a 16-bit general register which is decremented by 1 or 2 to obtain the address of the operand in memory. The register retains the decremented value. The size of the decrement is 1 for MOV.B or 2 for MOV.W. For MOV.W, the original contents of the register must be even.

5. **Absolute Address—@aa:8 or @aa:16:** The instruction specifies the absolute address of the operand in memory.

   The absolute address may be 8 bits long (@aa:8) or 16 bits long (@aa:16). The MOV.B and bit manipulation instructions can use 8-bit absolute addresses. The MOV.B, MOV.W, JMP, and JSR instructions can use 16-bit absolute addresses.

   For an 8-bit absolute address, the upper 8 bits are assumed to be 1 (H'FF). The address range is H'FF00 to H'FFFF (65280 to 65535).

6. **Immediate—#xx:8 or #xx:16:** The instruction contains an 8-bit operand (#xx:8) in its second byte, or a 16-bit operand (#xx:16) in its third and fourth bytes. Only MOV.W instructions can contain 16-bit immediate values.

   The ADDS and SUBS instructions implicitly contain the value 1 or 2 as immediate data. Some bit manipulation instructions contain 3-bit immediate data in the second or fourth byte of the instruction, specifying a bit number.

7. **Program-Counter Relative—@(d:8, PC):** This mode is used in the Bcc and BSR instructions. An 8-bit displacement in byte 2 of the instruction code is sign-extended to 16 bits and added to the program counter contents to generate a branch destination address. The possible branching range is –126 to +128 bytes (–63 to +64 words) from the current address. The displacement should be an even number.

8. **Memory Indirect—@@aa:8:** This mode can be used by the JMP and JSR instructions. The second byte of the instruction code specifies an 8-bit absolute address. The word located at this address contains the branch destination address.

   The upper 8 bits of the absolute address are assumed to be 0 (H'00), so the address range is from H'0000 to H'00FF (0 to 255). Note that with the H8/3714 Series, addresses H'0000 to H'002B (0 to 43) are located in the vector table.

   If an odd address is specified as a branch destination or as the operand address of a MOV.W instruction, the least significant bit is regarded as 0, causing word access to be performed at the address preceding the specified address. See 2.3.2, Memory Data Formats, for further information.

2.4.2 Effective Address Calculation

Table 2-2 shows how effective addresses are calculated in each of the addressing modes.

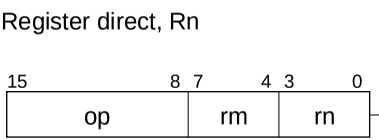
Arithmetic and logic instructions use register direct addressing (1). The ADD.B, ADDX, SUBX, CMP.B, AND, OR, and XOR instructions can also use immediate addressing (6).

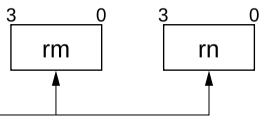
Data transfer instructions can use all addressing modes except program-counter relative (7) and memory indirect (8).

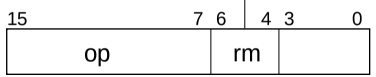
Bit manipulation instructions use register direct (1), register indirect (2), or absolute addressing (5) to specify a byte operand, and 3-bit immediate addressing (6) to specify a bit position in that byte. The BSET, BCLR, BNOT, and BTST instructions can also use register direct addressing (1) to specify the bit position.

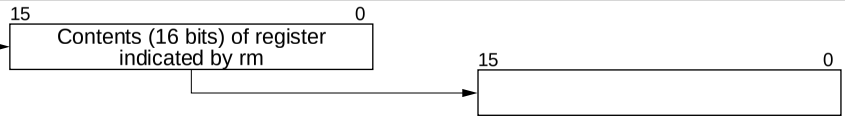
Table 2-2 Effective Address Calculation

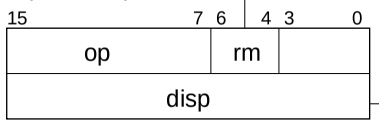
No.	Addressing Mode and Instruction Format	Effective Address Calculation Method	Effective Address (EA)
1	Register direct, Rn		Operand is contents indicated by rm/rn.
2	Register indirect, @Rn	Contents (16 bits) of register indicated by rm	
3	Register indirect with displacement, @(d:16, Rn)	Contents (16 bits) of register indicated by rm + disp	
4	Register indirect with post-increment, @Rn+	Contents (16 bits) of register indicated by rm + 1 or 2	
	Register indirect with pre-decrement, @–Rn	Contents (16 bits) of register indicated by rm − 1 or 2	

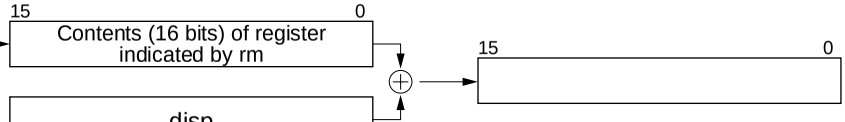


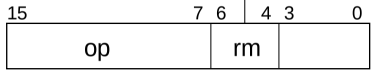


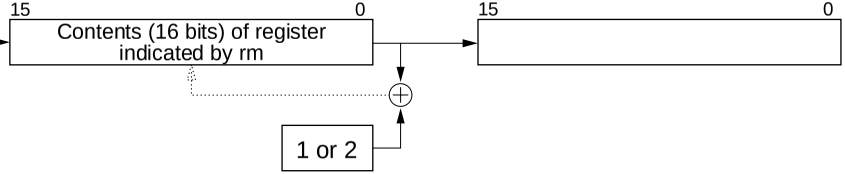


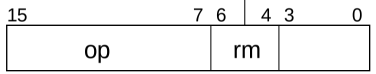


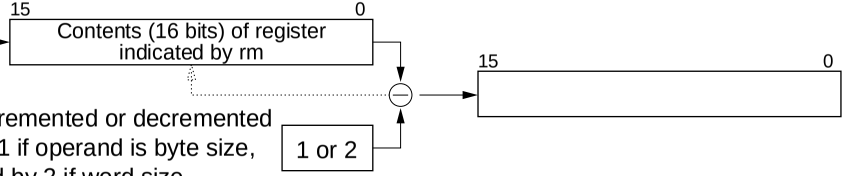












Incremented or decremented by 1 if operand is byte size, and by 2 if word size.

Table 2-2 Effective Address Calculation (cont)

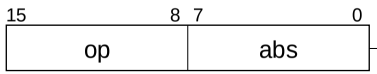
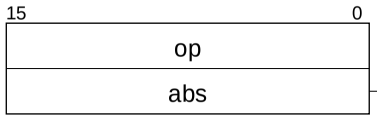
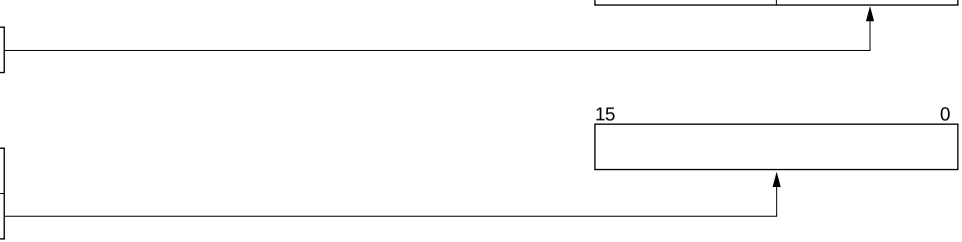
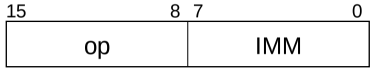
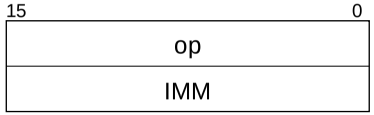
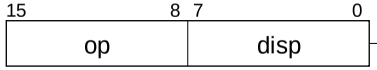
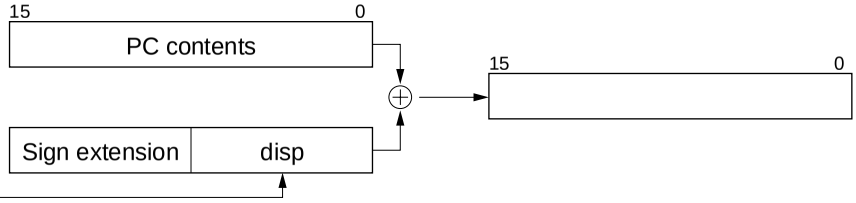
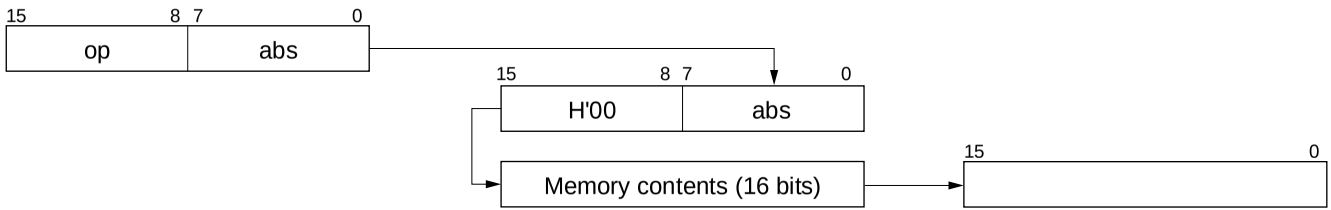
No.	Addressing Mode and Instruction Format	Effective Address Calculation Method	Effective Address (EA)
5	Absolute address @aa:8  @aa:16  	 	
6	Immediate #xx:8  #xx:16  		Operand is 1- or 2-byte immediate data.
7	Program-counter relative @(d:8, PC)  	 	

Table 2-2 Effective Address Calculation (cont)

No.	Addressing Mode and Instruction Format	Effective Address Calculation Method	Effective Address (EA)
8	Memory indirect, @@aa:8		

Notation:
rm, rn: Register field
op: Operation field
disp: Displacement
IMM: Immediate data
abs: Absolute address

2.5 Instruction Set

The H8/300L CPU can use a total of 55 instructions, which are grouped by function in table 2-3.

Table 2-3 Instruction Set

Function	Instructions	Types
Data transfer	MOV, PUSH*1, POP*1	1
Arithmetic operations	ADD, SUB, ADDX, SUBX, INC, DEC, ADDS, SUBS, DAA, DAS, MULXU, DIVXU, CMP, NEG	14
Logic operations	AND, OR, XOR, NOT	4
Shift	SHAL, SHAR, SHLL, SHLR, ROTL, ROTR, ROTXL, ROTXR	8
Bit manipulation	BSET, BCLR, BNOT, BTST, BAND, BIAND, BOR, BIOR, BXOR, BIXOR, BLD, BILD, BST, BIST	14
Branch	Bcc*2, JMP, BSR, JSR, RTS	5
System control	RTE, SLEEP, LDC, STC, ANDC, ORC, XORC, NOP	8
Block data transfer	EEPMOV	1
		Total: 55

Notes: 1. PUSH Rn is equivalent to MOV.W Rn, @–SP.
POP Rn is equivalent to MOV.W @SP+, Rn.
2. Bcc is the generic designation of a conditional branch instruction.

The following sections give a concise summary of the instructions in each category, and indicate the bit patterns of their object code. The notation used is defined next.

Notation	
Rd	General register (destination)
Rs	General register (source)
Rn	General register
(EAd) <EAd>	Destination operand
(EAs) <EAs>	Source operand
CCR	Condition code register
N	N (negative) flag of CCR
Z	Z (zero) flag of CCR
V	V (overflow) flag of CCR
C	C (carry) flag of CCR
PC	Program counter
SP	Stack pointer
#IMM	Immediate data
disp	Displacement
+	Addition
–	Subtraction
×	Multiplication
÷	Division
∧	AND logical
∨	OR logical
⊕	Exclusive OR logical
→	Move
~	Inverse logic (logical complement)
:3	3-bit length
:8	8-bit length
:16	16-bit length
( ) < >	Contents of operand effective address

2.5.1 Data Transfer Instructions

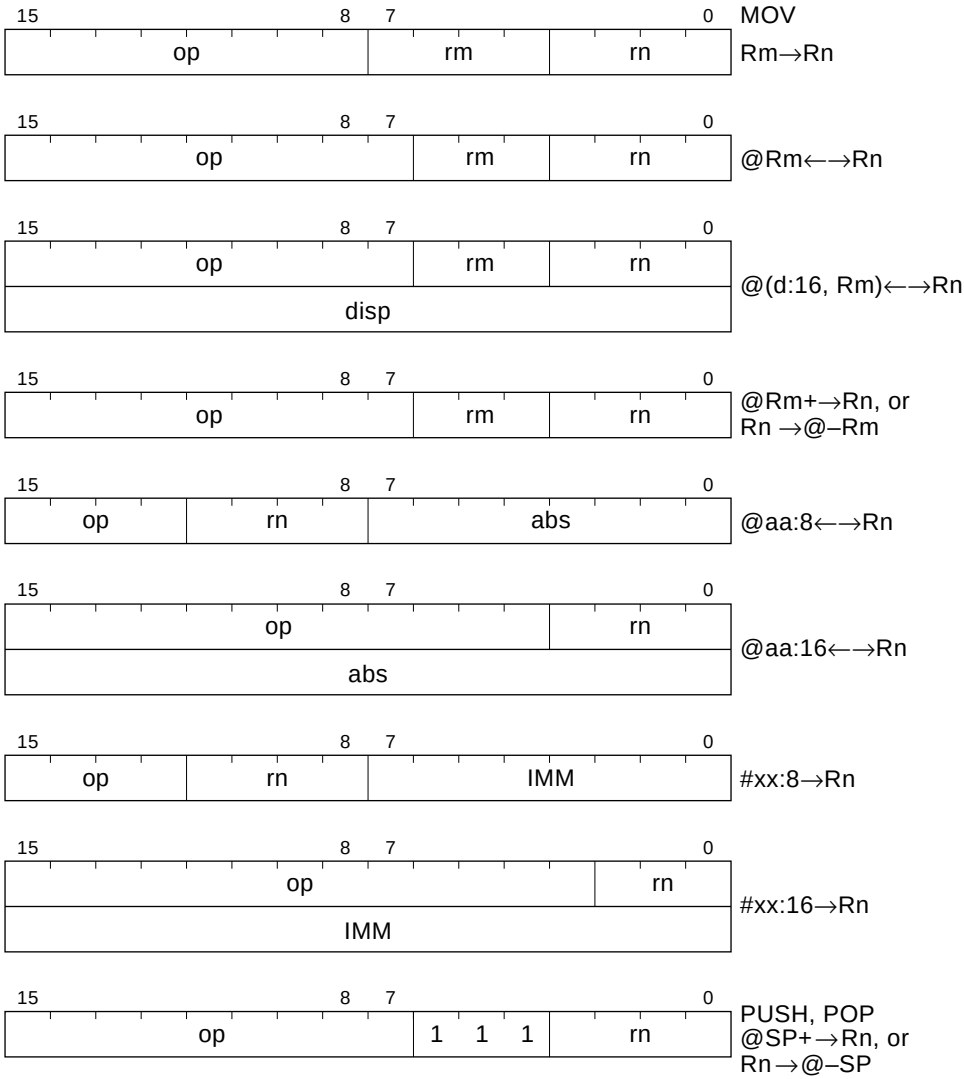
Table 2-4 describes the data transfer instructions. Figure 2-6 shows their object code formats.

Table 2-4 Data Transfer Instructions

Instruction	Size*	Function
MOV	B/W	(EAs) → Rd, Rs → (EAd) Moves data between two general registers or between a general register and memory, or moves immediate data to a general register. The Rn, @Rn, @(d:16, Rn), @aa:16, #xx:8 or #xx:16, @–Rn, and @Rn+ addressing modes are available for byte or word data. The @aa:8 addressing mode is available for byte data only. The @–R7 and @R7+ modes require word operands. Do not specify byte size for these two modes.
PUSH	W	Rn → @–SP Pushes a 16-bit general register onto the stack. Equivalent to MOV.W Rn, @–SP.
POP	W	@SP+ → Rn Pops a 16-bit general register from the stack. Equivalent to MOV.W @SP+, Rn.

Notes: * Size: Operand size
B: Byte
W: Word

Certain precautions are required in data access. See 2.8.1, Notes on Data Access, for details.



Notation:
op: Operation field
rm, rn: Register field
disp: Displacement
abs: Absolute address
IMM: Immediate data

Figure 2-6 Data Transfer Instruction Codes

2.5.2 Arithmetic Operations

Table 2-5 describes the arithmetic instructions. See figure 3-6 in section 3.5.4, Shift Operations for their object codes.

Table 2-5 Arithmetic Instructions

Instruction	Size*	Function
ADD SUB	B/W	Rd ± Rs → Rd, Rd + #IMM → Rd Performs addition or subtraction on data in two general registers, or addition on immediate data and data in a general register. Immediate data cannot be subtracted from data in a general register. Word data can be added or subtracted only when both words are in general registers.
ADDX SUBX	B	Rd ± Rs ± C → Rd, Rd ± #IMM ± C → Rd Performs addition or subtraction with carry or borrow on byte data in two general registers, or addition or subtraction on immediate data and data in a general register.
INC DEC	B	Rd ± 1 → Rd Increments or decrements a general register.
ADDS SUBS	W	Rd ± 1 → Rd, Rd ± 2 → Rd Adds or subtracts immediate data to or from data in a general register. The immediate data must be 1 or 2.
DAA DAS	B	Rd decimal adjust → Rd Decimal-adjusts (adjusts to packed BCD) an addition or subtraction result in a general register by referring to the CCR.
MULXU	B	Rd × Rs → Rd Performs 8-bit × 8-bit unsigned multiplication on data in two general registers, providing a 16-bit result.
DIVXU	B	Rd ÷ Rs → Rd Performs 16-bit ÷ 8-bit unsigned division on data in two general registers, providing an 8-bit quotient and 8-bit remainder.
CMP	B/W	Rd – Rs, Rd – #IMM Compares data in a general register with data in another general register or with immediate data, and sets the CCR according to the result. Word data can be compared only between two general registers.
NEG	B	0 – Rd → Rd Obtains the two's complement (arithmetic complement) of data in a general register.

Notes: * Size: Operand size
B: Byte
W: Word

2.5.3 Logic Operations

Table 2-6 describes the four instructions that perform logic operations.

Table 2-6 Logic Operation Instructions

Instruction	Size*	Function
AND	B	Rd ∧ Rs → Rd, Rd ∧ #IMM → Rd Performs a logical AND operation on a general register and another general register or immediate data.
OR	B	Rd ∨ Rs → Rd, Rd ∨ #IMM → Rd Performs a logical OR operation on a general register and another general register or immediate data.
XOR	B	Rd ⊕ Rs → Rd, Rd ⊕ #IMM → Rd Performs a logical exclusive OR operation on a general register and another general register or immediate data.
NOT	B	~ Rd → Rd Obtains the one's complement (logical complement) of general register contents.

Notes: * Size: Operand size
B: Byte

2.5.4 Shift Operations

Table 2-7 describes the eight shift instructions.

Table 2-7 Shift Instructions

Instruction	Size*	Function
SHAL SHAR	B	Rd shift → Rd Performs an arithmetic shift operation on general register contents.
SHLL SHLR	B	Rd shift → Rd Performs a logical shift operation on general register contents.
ROTL ROTR	B	Rd rotate → Rd Rotates general register contents.
ROTXL ROTXR	B	Rd rotate through carry → Rd Rotates general register contents through the C (carry) bit.

Notes: * Size: Operand size
B: Byte

Figure 2-7 shows the instruction code format of arithmetic, logic, and shift instructions.

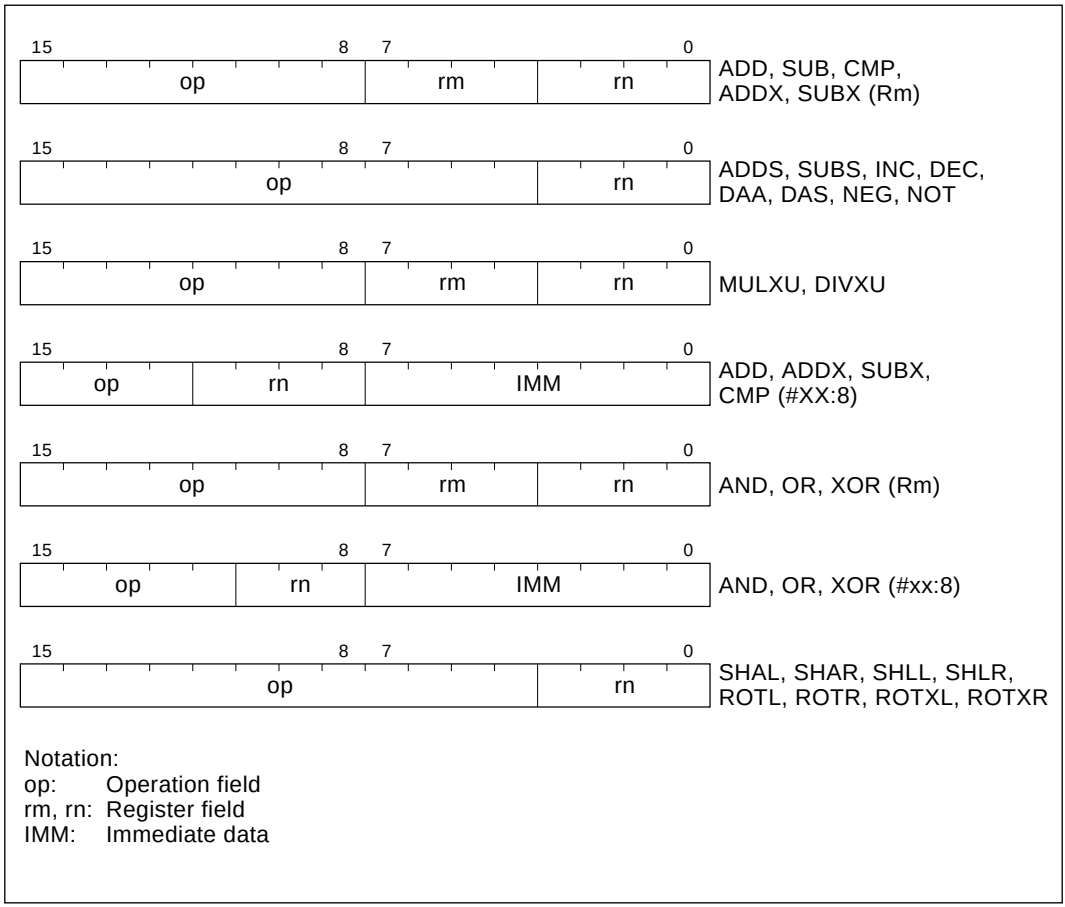


Figure 2-7 Arithmetic, Logic, and Shift Instruction Codes

2.5.5 Bit Manipulations

Table 2-8 describes the bit-manipulation instructions. Figure 2-8 shows their object code formats.

Table 2-8 Bit-Manipulation Instructions

Instruction	Size*	Function
BSET	B	1 → (<bit-No.> of <EAd>) Sets a specified bit in a general register or memory to 1. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BCLR	B	0 → (<bit-No.> of <EAd>) Clears a specified bit in a general register or memory to 0. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BNOT	B	~ (<bit-No.> of <EAd>) → (<bit-No.> of <EAd>) Inverts a specified bit in a general register or memory. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BTST	B	~ (<bit-No.> of <EAd>) → Z Tests a specified bit in a general register or memory and sets or clears the zero flag accordingly. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BAND	B	C ∧ (<bit-No.> of <EAd>) → C ANDs the carry flag with a specified bit in a general register or memory and stores the result in the carry flag.
BIAND	B	C ∧ [~ (<bit-No.> of <EAd>)] → C ANDs the carry flag with the inverse of a specified bit in a general register or memory and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BOR	B	C ∨ (<bit-No.> of <EAd>) → C ORs the carry flag with a specified bit in a general register or memory and stores the result in the carry flag.
BIOR	B	C ∨ [~ (<bit-No.> of <EAd>)] → C ORs the carry flag with the inverse of a specified bit in a general register or memory and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.

Notes: * Size: Operand size
B: Byte

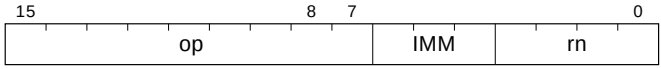
Table 2-8 Bit-Manipulation Instructions (cont)

Instruction	Size*	Function
BXOR	B	C ⊕ (<bit-No.> of <EAd>) → C
		XORs the carry flag with a specified bit in a general register or memory and stores the result in the carry flag.
BIXOR	B	C ⊕ ~ [(<bit-No.> of <EAd>)] → C
		XORs the carry flag with the inverse of a specified bit in a general register or memory and stores the result in the carry flag.
		The bit number is specified by 3-bit immediate data.
BLD	B	(<bit-No.> of <EAd>) → C
		Copies a specified bit in a general register or memory to the carry flag.
BILD	B	~ (<bit-No.> of <EAd>) → C
		Copies the inverse of a specified bit in a general register or memory to the carry flag.
		The bit number is specified by 3-bit immediate data.
BST	B	C → (<bit-No.> of <EAd>)
		Copies the carry flag to a specified bit in a general register or memory.
BIST	B	~ C → (<bit-No.> of <EAd>)
		Copies the inverse of the carry flag to a specified bit in a general register or memory.
		The bit number is specified by 3-bit immediate data.

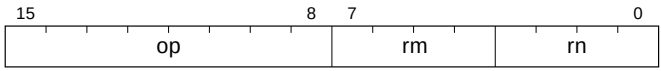
Notes: * Size: Operand size
B: Byte

Certain precautions are required in bit manipulation. See 2.8.2, Notes on Bit Manipulation, for details.

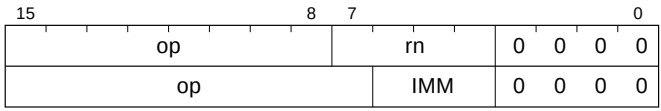
BSET, BCLR, BNOT, BTST



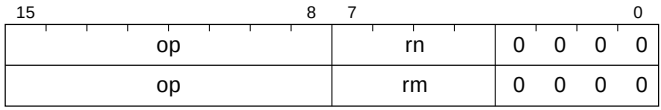
Operand: register direct (Rn)
Bit No.: immediate (#xx:3)



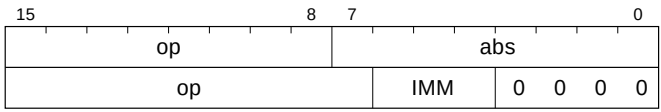
Operand: register direct (Rn)
Bit No.: register direct (Rm)



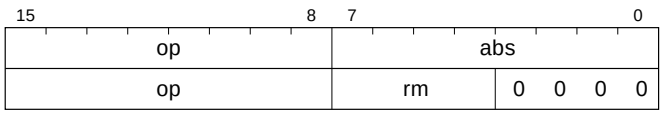
Operand: register indirect (@Rn)
Bit No.: immediate (#xx:3)



Operand: register indirect (@Rn)
Bit No.: register direct (Rm)

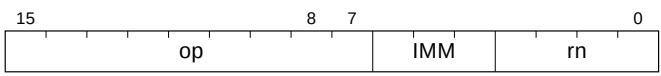


Operand: absolute (@aa:8)
Bit No.: immediate (#xx:3)

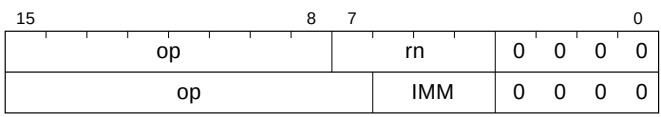


Operand: absolute (@aa:8)
Bit No.: register direct (Rm)

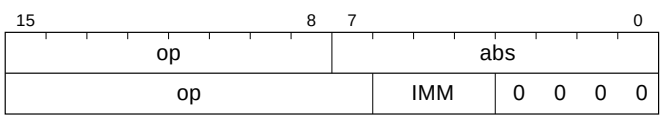
BAND, BOR, BXOR, BLD, BST



Operand: register direct (Rn)
Bit No.: immediate (#xx:3)



Operand: register indirect (@Rn)
Bit No.: immediate (#xx:3)

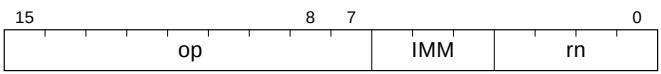


Operand: absolute (@aa:8)
Bit No.: immediate (#xx:3)

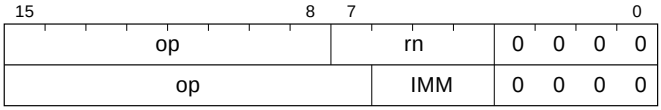
Notation:
op: Operation field
rm, rn: Register field
abs: Absolute address
IMM: Immediate data

Figure 2-8 Bit Manipulation Instruction Codes

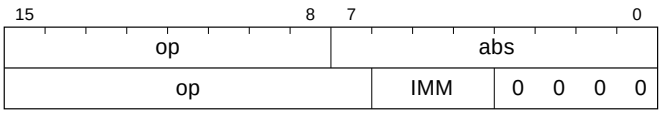
BIAND, BIOR, BIXOR, BILD, BIST



Operand: register direct (Rn)
Bit No.: immediate (#xx:3)



Operand: register indirect (@Rn)
Bit No.: immediate (#xx:3)



Operand: absolute (@aa:8)
Bit No.: immediate (#xx:3)

Notation:
op: Operation field
rm, rn: Register field
abs: Absolute address
IMM: Immediate data

Figure 2-8 Bit Manipulation Instruction Codes (cont)

2.5.6 Branching Instructions

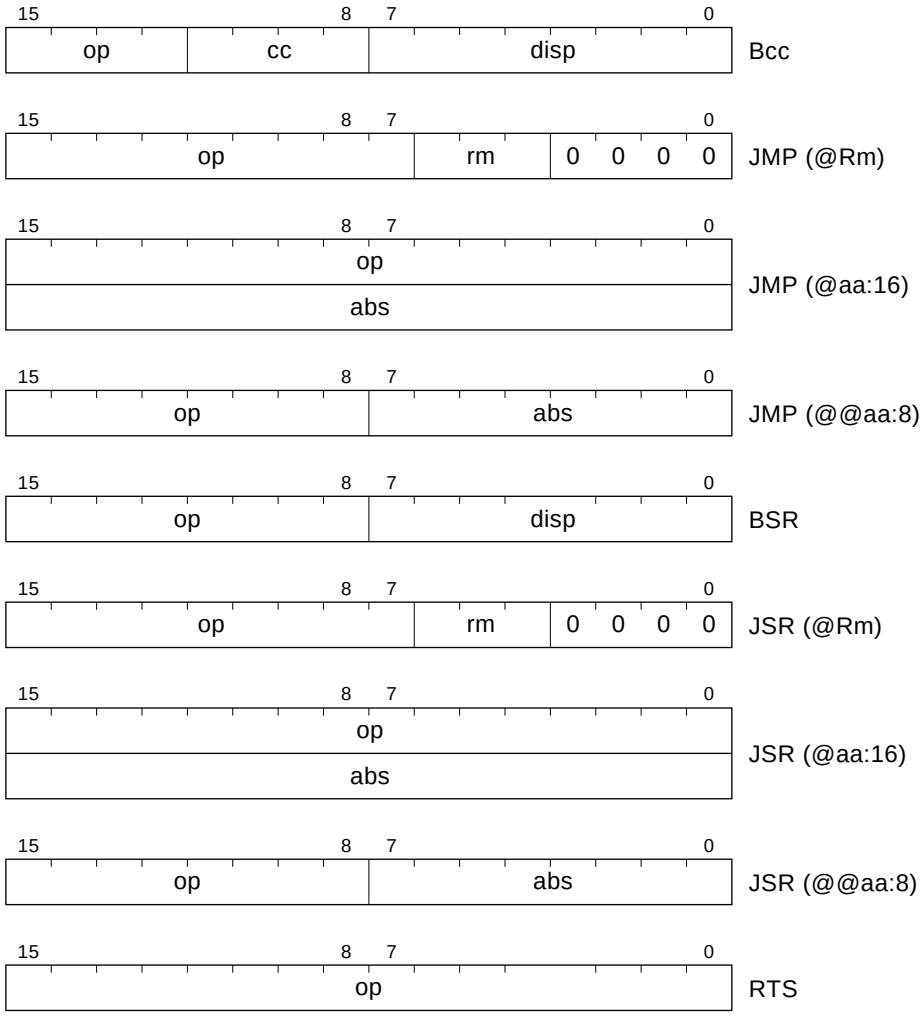
Table 2-9 describes the branching instructions.

Table 2-9 Branching Instructions

Instruction	Size	Function
Bcc	—	Branches to the designated address if condition cc is true. The branching conditions are given below.

Mnemonic	Description	Condition
BRA (BT)	Always (true)	Always
BRN (BF)	Never (false)	Never
BHI	High	$C \vee Z = 0$
BLS	Low or same	$C \vee Z = 1$
BCC (BHS)	Carry clear (high or same)	$C = 0$
BCS (BLO)	Carry set (low)	$C = 1$
BNE	Not equal	$Z = 0$
BEQ	Equal	$Z = 1$
BVC	Overflow clear	$V = 0$
BVS	Overflow set	$V = 1$
BPL	Plus	$N = 0$
BMI	Minus	$N = 1$
BGE	Greater or equal	$N \oplus V = 0$
BLT	Less than	$N \oplus V = 1$
BGT	Greater than	$Z \vee (N \oplus V) = 0$
BLE	Less or equal	$Z \vee (N \oplus V) = 1$

JMP	—	Branches unconditionally to a specified address.
JSR	—	Branches to a subroutine at a specified address.
BSR	—	Branches to a subroutine at a specified displacement from the current address.
RTS	—	Returns from a subroutine.



Notation:
op: Operation field
cc: Condition field
rm: Register field
disp: Displacement
abs: Absolute address

Figure 2-9 Branching Instruction Codes

2.5.7 System Control Instructions

Table 2-10 describes the system control instructions. Figure 2-10 shows their object code formats.

Table 2-10 System Control Instructions

Instruction	Size*	Function
RTE	—	Returns from an exception-handling routine.
SLEEP	—	Causes a transition from active mode to a power-down mode (sleep mode, standby mode, or watch mode), or from subactive mode to watch mode, or from subactive mode via watch mode to active mode. For details, see 3.3, System Modes.
LDC	B	Rs → CCR, #IMM → CCR Moves immediate data or general register contents to the condition code register.
STC	B	CCR → Rd Copies the condition code register to a specified general register.
ANDC	B	CCR ∧ #IMM → CCR Logically ANDs the condition code register with immediate data.
ORC	B	CCR ∨ #IMM → CCR Logically ORs the condition code register with immediate data.
XORC	B	CCR ⊕ #IMM → CCR Logically exclusive-ORs the condition code register with immediate data.
NOP	—	PC + 2 → PC Only increments the program counter.

Notes: * Size: Operand size
B: Byte

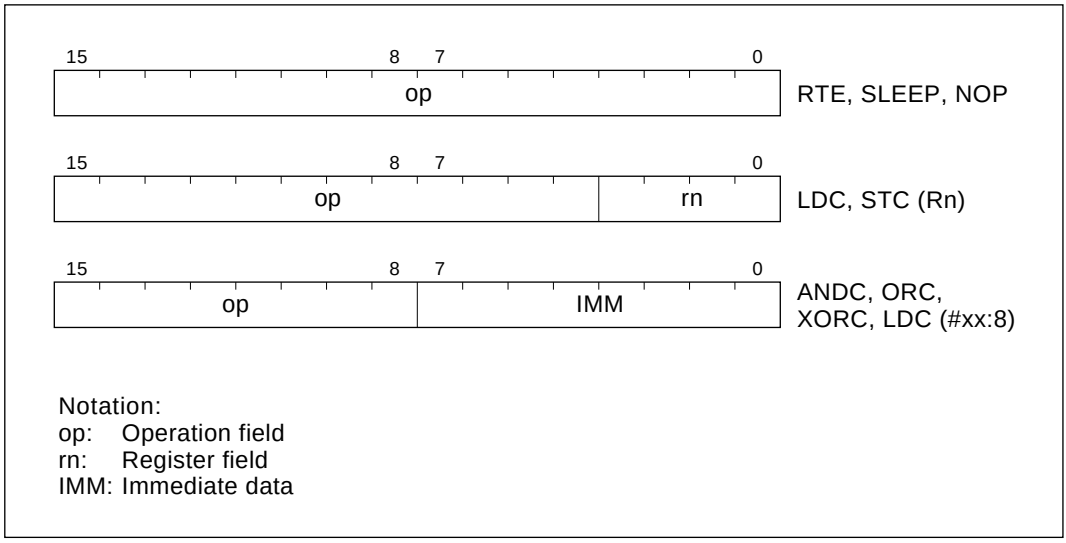


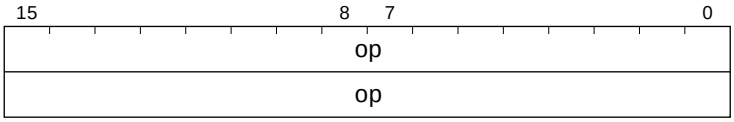
Figure 2-10 System Control Instruction Codes

2.5.8 Block Data Transfer Instruction

Table 2-11 describes the block data transfer instruction. Figure 2-11 shows its object code format.

Table 2-11 Block Data Transfer Instruction

Instruction	Size	Function
EEPMOV	—	If R4L ≠ 0 then repeat @R5+ → @R6+ R4L – 1 → R4L until R4L = 0 else next; Moves a data block according to parameters set in general registers R4L, R5, and R6. R4L: Size of block (bytes) R5: Starting source address R6: Starting destination address Execution of the next instruction starts as soon as the block transfer is completed.

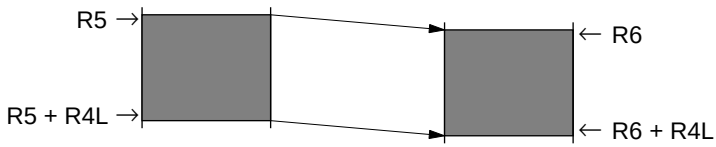


Notation:
op: Operation field

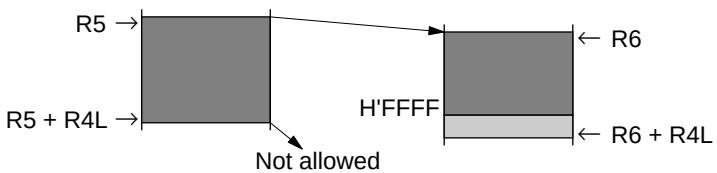
Figure 2-11 Block Data Transfer Instruction Code

Notes on EEPMOV Instruction

1. The EEPMOV instruction is a block data transfer instruction. It moves the number of bytes specified by R4L from the address specified by R5 to the address specified by R6.



2. When setting R4L and R6, make sure that the final destination address (R6 + R4L) does not exceed H'FFFF. The value in R6 must not change from H'FFFF to H'0000 during execution of the instruction.



2.6 CPU States

2.6.1 Overview

There are three CPU states: program execution state, program halt state, and exception-handling state. Program execution state includes active mode and subactive mode. In program halt state there are sleep mode, standby mode, and watch mode. These states are shown in figure 2-12. Figure 2-13 shows the state transitions.

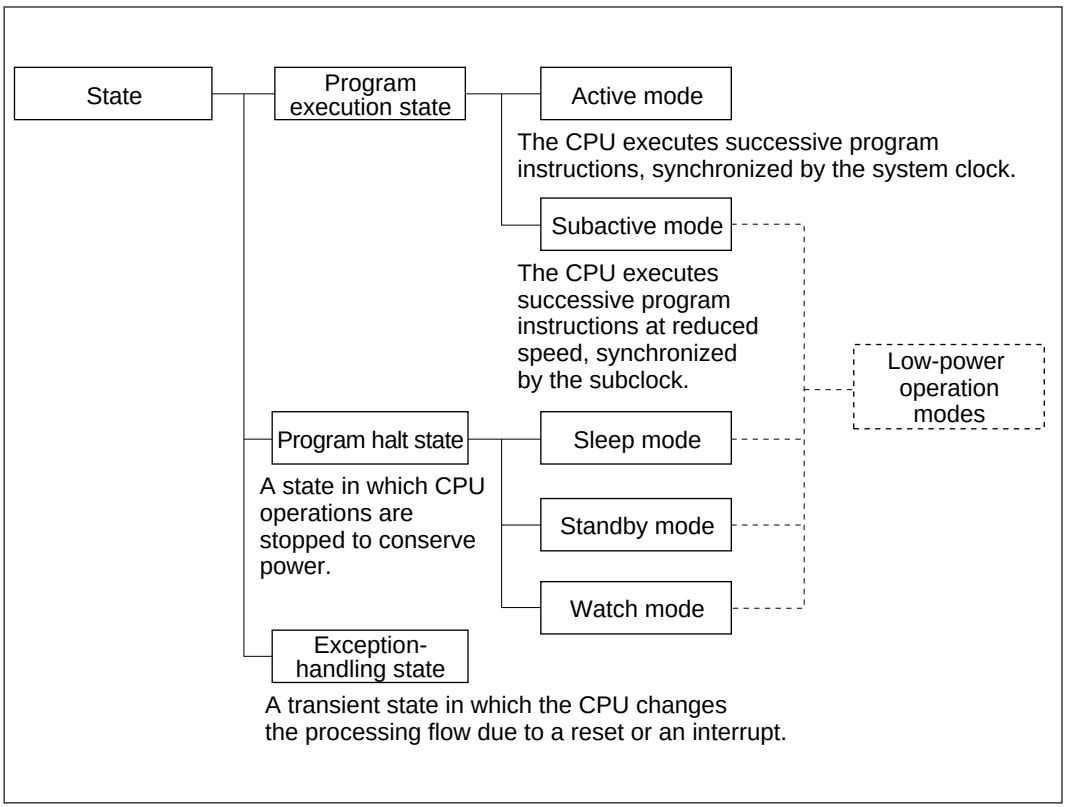


Figure 2-12 CPU Operation States

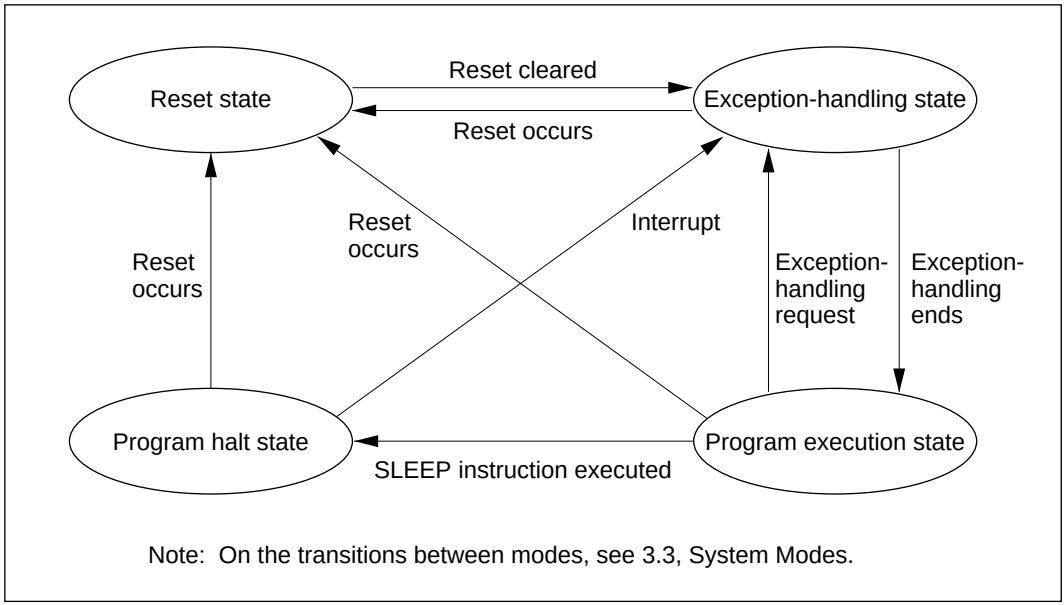


Figure 2-13 State Transitions

2.6.2 Program Execution State

In the program execution state the CPU executes program instructions in sequence.

There are two modes in this state, active mode and subactive mode. Operation is synchronized with the system clock in active mode, and with a subclock in subactive mode. For details on these modes, see 3.3, System Modes.

2.6.3 Program Halt State

In the program halt state there are three modes: sleep mode, standby mode, and watch mode. For details on these modes, see 3.3, System Modes.

2.6.4 Exception-Handling State

The exception-handling state is a transient state occurring when exception handling is started by a reset or interrupt, and the CPU changes its normal processing flow. In exception handling caused by an interrupt, SP (R7) is referenced and the PC and CCR values are saved on the stack.

For details on interrupt handling, see 3.2.2, Interrupts.

2.7 Basic Operation Timing

CPU operation is synchronized by a clock (ϕ_i). ϕ_i is either the system clock (ϕ) generated by the system clock oscillator circuit, or the subclock (ϕ_{SUB}) generated by the subclock oscillator circuit. ϕ_i denotes ϕ in active mode and ϕ_{SUB} in subactive mode. For details, see section 6, Clock Pulse Generators. The period from the rising edge of ϕ_i to the next rising edge is called one state. A memory cycle or bus cycle consists of two states; access to on-chip memory and to on-chip peripheral modules always takes place in two states.

2.7.1 Access to On-Chip Memory (RAM, ROM)

Two-state access is employed for on-chip memory. The data bus width is 16 bits, allowing access in byte or word size. Figure 2-14 shows the on-chip memory access cycle.

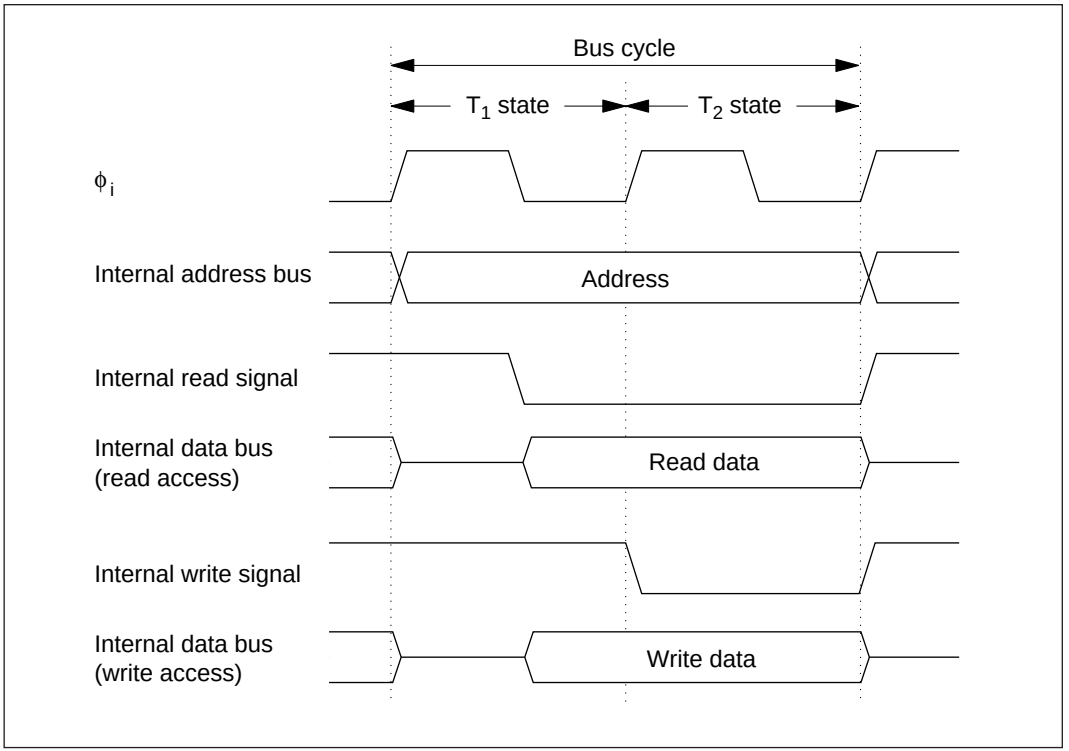


Figure 2-14 On-Chip Memory Access Cycle

2.7.2 Access to On-Chip Peripheral Modules

On-chip peripheral modules are accessed in two states. The data bus width is 8 bits, so access is made in byte size only. This means that two instructions must be used for a word size data access. Figure 2-15 shows the on-chip peripheral module access cycle.

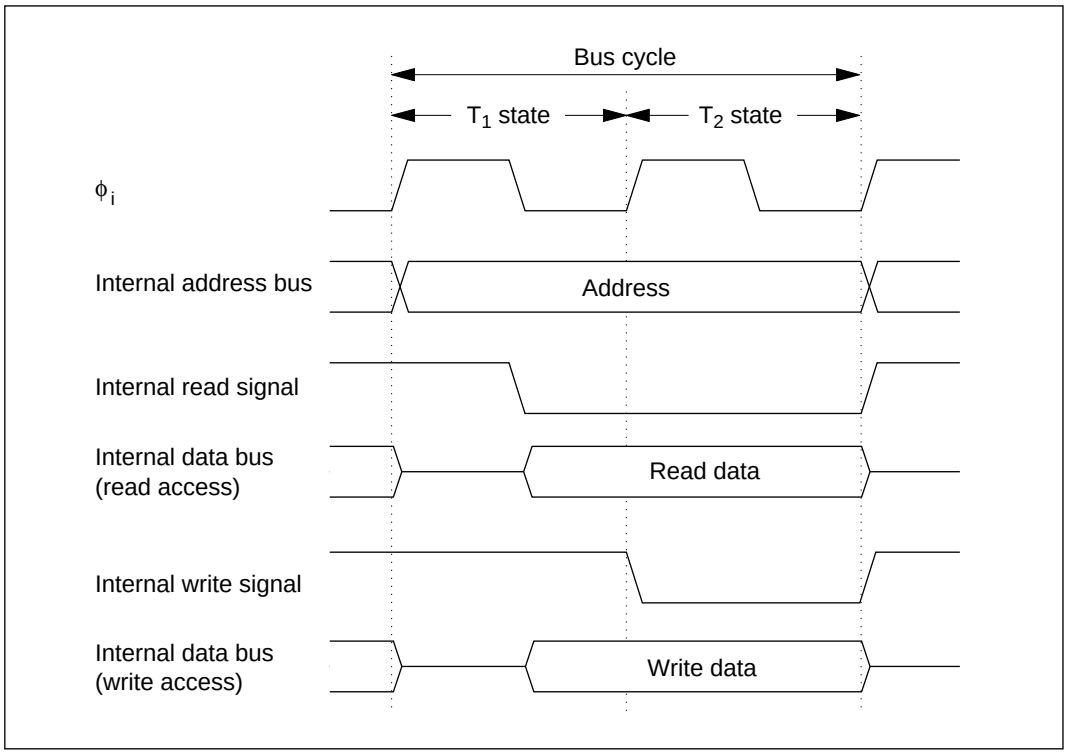


Figure 2-15 On-Chip Peripheral Module Access Cycle

2.8 Application Notes

The following points are to be observed in using the H8/300L CPU.

2.8.1 Notes on Data Access

1. The address space of the H8/300L CPU includes some empty areas in addition to the RAM, registers, and ROM areas available to the user. If these empty areas are mistakenly accessed by an application program, the following results will occur.

   Transfer from CPU to empty area:

   The transferred data will be lost. This action may also cause the CPU to misoperate.

   Transfer from empty area to CPU:

   Unpredictiable data is transferred.

2. Internal data transfer to or from on-chip modules other than ROM and RAM areas makes use of an 8-bit data width. If word access is attempted to these areas, the following results will occur.

   Word access from CPU to I/O register area:

   Upper byte: Will be written to I/O register.

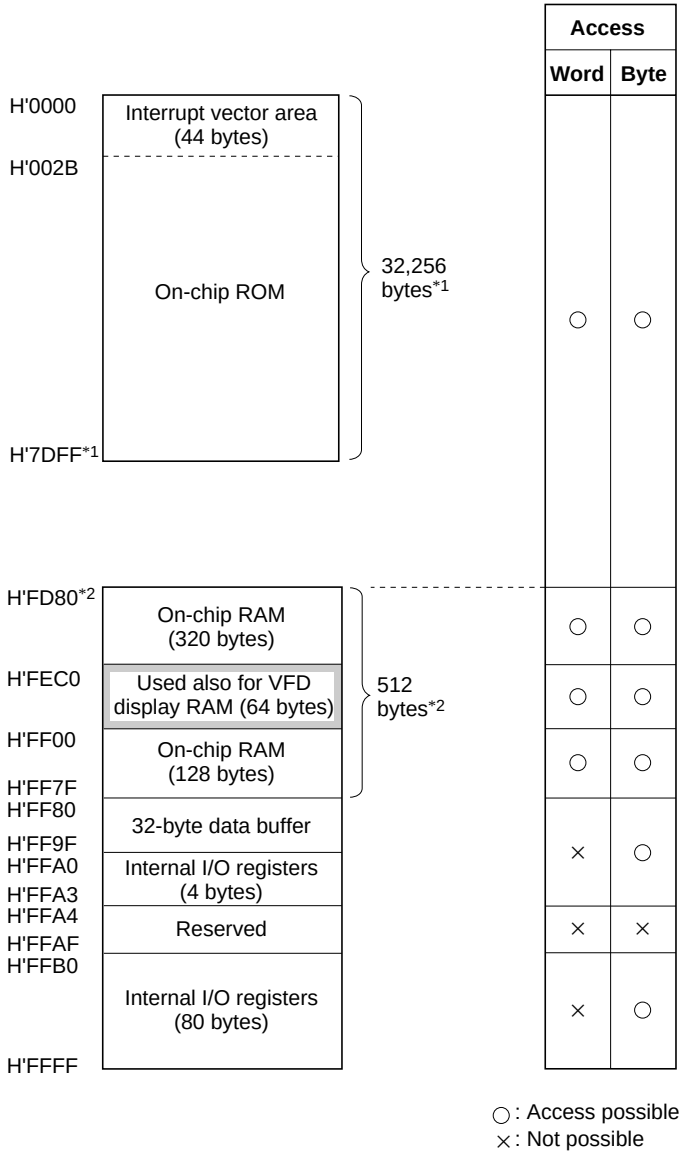
   Lower byte: Transferred data will be lost.

   Word access from I/O register to CPU:

   Upper byte: Will be written to upper part of CPU register.

   Lower byte: Data written to lower part of CPU register cannot be guaranteed.

   Byte size instructions should therefore be used when transferring data to or from I/O registers outside the on-chip ROM and RAM areas. Figure 2-16 shows the data size in which access can be made with on-chip peripheral modules.



Notes: The above example is a description of the H8/3714.

1. The H8/3713 has 24,576 bytes of on-chip ROM, and its ending address is H'5FFF. The H8/3712 has 16,384 bytes of on-chip ROM, and its ending address is H'3FFF.
2. The H8/3713 and H8/3712 each have 384 bytes of on-chip RAM, and their ending address is H'FE00.

Figure 2-16 Data Size for Access to and from On-Chip Peripheral Modules

2.8.2 Notes on Bit Manipulation

The H8/300L CPU executes bit manipulation instructions by a read-modify-write operation on 8-bit data. When bit manipulation instructions are executed in the cases illustrated below, care must be taken since the operation may affect other bits besides those being manipulated.

1. Bit manipulation in two registers assigned to the same address (when the source and destination are different)

Example 1: Timer load register and timer counter

In this example, a bit manipulation instruction is executed in the timer load register and timer counter of a reloadable timer. Since the timer load register and timer counter share the same address, the operations take place as follows.

a. Read: The timer counter value at the time is read.

b. Modify: The CPU modifies (sets or resets) the bit designated with the instruction. (Other bits remain the same.)

c. Write: The modified data is written to the timer load register.

The timer counter is counting based on the system clock (ϕ), so the value read is not necessarily the same as the value in the timer load register. As a result, bits other than the intended bit in the timer load register may be modified to the timer counter value.

Figure 2-17 shows the reloadable timer configuration.

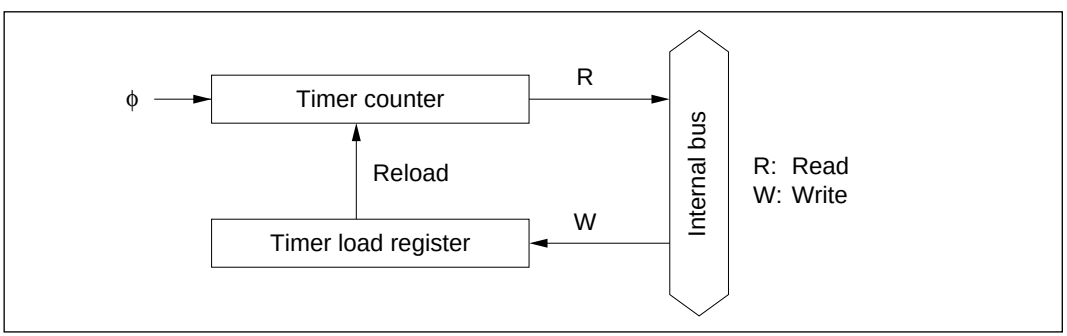


Figure 2-17 Reloadable Timer Configuration

Example 2: Port data register (pin input and data register)

When a bit manipulation instruction is executed designating a port data register, it may cause changes in pin I/O states or data register contents other than the intended bit.

As noted above, the H8/300L CPU executes bit manipulation instructions by a read-modify-write operation on 8-bit data. Since the same address is used for the I/O port data register and reading of pin input, a bit manipulation instruction designating a port functions as follows.

① High-voltage pin: pin other than the modified bit

- When set as an input pin (data register = 0)

  First the CPU reads the pin input level (read), then it sets or resets the designated bit (modify; other bits remain the same), and writes that value to the data register (write). If the input level is high (read data = 1), a value of 1 is written to the data register, changing the input pin to an output pin (high-level output). If the input level is low, no change occurs.

- When set as an output pin (data register = 1, high-level output)

  If the output level is higher than the input high level (V_{IH}), there is no change.

  If the output level is lower than the input low level (V_{IL}), a value of 0 is written to the data register, so that the PMOS buffer transistor is turned off resulting in pull-down (low level) or high-impedance state.

  If the output level is pulled down by the load to an intermediate level, the resulting state is indeterminate.

② Standard-voltage pin: pin other than the modified bit

- When set as an input pin

  The CPU reads the pin input level and writes that value to the data register, which may or may not result in a change to the data register contents.

- When set as an output pin

  The data register is read, so no change occurs.

2. Bit manipulation in registers containing write-only bits

Example: PWM data registers, etc.
(Note that read and write characteristics can differ from bit to bit.)

Write-only bits cannot be read. Write-only bits other than the intended bit are set to 1.

Table 2-12 lists the registers that share the same address, while table 2-13 lists the registers that contain write-only bits.

Table 2-12 Registers Assigned to the Same Address

Register Name	Abbreviation	Address
Timer load register B/timer counter B	TLB/TCB	H'FFC3
Timer load register C/timer counter C	TLC/TCC	H'FFC5
Timer load register E/timer counter E	TLE/TCE	H'FFC9
Port data register 1*	PDR1	H'FFD1
Port data register 4*	PDR4	H'FFD4
Port data register 5*	PDR5	H'FFD5
Port data register 6*	PDR6	H'FFD6
Port data register 7*	PDR7	H'FFD7
Port data register 9*	PDR9	H'FFD9

Note: * These port data registers are used also for pin input.

Table 2-13 Registers with Write-Only Bits

Register Name	Abbreviation	Address
Serial mode register 1	SMR1	H'FFB0
PWM control register	PWCR	H'FFCC
PWM data register U	PWDRU	H'FFCD
PWM data register L	PWDRL	H'FFCE
Port control register 1	PCR1	H'FFE1
Port control register 9	PCR9	H'FFE9
Port mode register 0	PMR0	H'FFEF
Timer mode register D*1	TMD	H'FFC6
System control register 2*2	SYSCR2	H'FFF1

Notes: 1. Only bit CRL (bit 7) is write-only.
2. Bit DTON (bit 3) is a write-only bit only in subactive mode. In active mode it cannot be read or written.

Section 3 System Control

3.1 Overview

This section explains the reset state, exception handling, and system modes.

3.2 Exception Handling

Exception handling includes processing of reset exceptions and of interrupts. Table 3-1 summarizes the exception sources and their priorities. Reset exception handling has the highest priority.

Table 3-1 Types of Exception Handling and Priorities

Priority	Exception Source	Timing for Start of Exception Handling
High ↑ Low	Reset	Reset exception handling starts as soon as $\overline{\text{RES}}$ pin changes from low to high.
	Interrupt	When interrupt request is made, interrupt exception handling starts after execution of present instruction is completed.

3.2.1 Reset

When the $\overline{\text{RES}}$ pin goes low, all processing stops and the chip enters the reset state. The internal state of the CPU and the registers of on-chip peripheral modules are initialized. The I bit of the condition code register (CCR) is set, masking all interrupts.

As soon as the $\overline{\text{RES}}$ pin goes from low to high, reset exception handling starts. The contents of the reset vector address (H'0000 to H'0001) are read and loaded into the program counter (PC). Then program execution starts from the address indicated in PC. Figure 3-1 shows the reset sequence.

Notes: 1. To make sure a reset is carried out properly, when power is turned on the $\overline{\text{RES}}$ pin should be kept low for at least 20 ms after the rise of the power supply.

2. When resetting during operation, keep the $\overline{\text{RES}}$ pin low for at least 10 system clock cycles.

3. After a reset, if an interrupt were to be accepted before the stack pointer (SP: R7) was initialized, PC and CCR would not be pushed onto the stack correctly, resulting in program runaway. To prevent this, immediately after reset exception handling all interrupts are masked. Programs should be coded to initialize the stack pointer before clearing the interrupt mask. An even-numbered address must be set in SP. It is recommended that programs start with an instruction initializing SP (e.g., MOV.W #xx:16, SP).

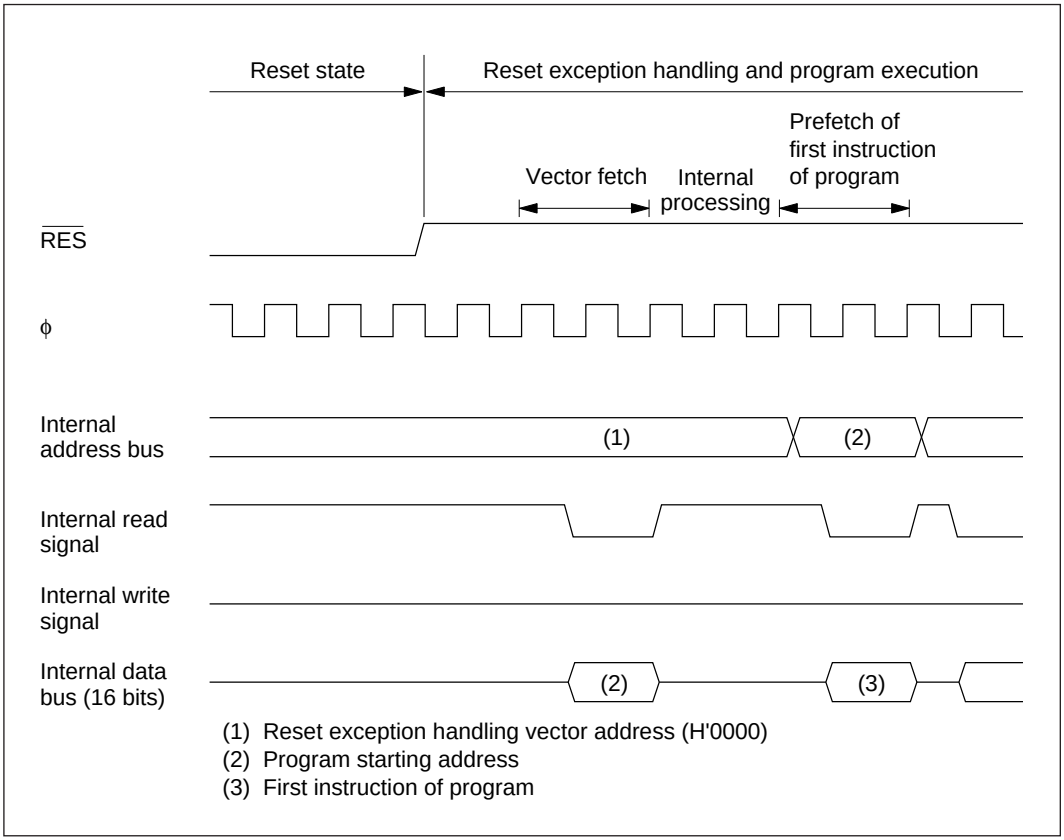


Figure 3-1 Reset Sequence

3.2.2 Interrupts

The interrupt sources include external interrupts (IRQ_5, IRQ_4, IRQ_1, IRQ_0), and internal interrupts requested from on-chip peripheral modules. Table 3-2 shows the interrupt sources, their priorities, and their vector addresses. When more than one interrupt is requested, the interrupt with the highest priority is processed.

The interrupts have the following features.

- Both internal interrupts and external interrupts (IRQ_5, IRQ_4, IRQ_1, IRQ_0), can be masked by the I bit of CCR. When this bit is set to 1, interrupt request flags are set but interrupts are not accepted.
- External interrupt pins $\overline{IRQ_4}$, $\overline{IRQ_1}$, and $\overline{IRQ_0}$ can be set independently for rising-edge or falling-edge sensing. For external interrupt pin $\overline{IRQ_5}$, the falling edge is sensed.

Table 3-2 Interrupt Sources

Priority	Interrupt	Origin of Interrupt	Vector Starting Address
High	Reset	External pin	H'0000
↑	(Reserved)*1	—	H'0002
			H'0004
			H'0006
	IRQ_0	External pin	H'0008
	IRQ_1		H'000A
	(Reserved)*1		H'000C
	(Reserved)*1		H'000E
	IRQ_4		H'0010
	IRQ_5		H'0012
	Key scan	VFD	H'0014
	Timer A overflow	Timer A	H'0016
	Timer B overflow	Timer B	H'0018
	Timer C overflow	Timer C	H'001A
	Timer D overflow	Timer D	H'001C
	Timer E overflow	Timer E	H'001E
	Direct transfer	Standby timer activator*2	H'0020
	(Reserved)*1	—	H'0022
			H'0024
	SCI1 transfer complete, error	Serial communication interface 1	H'0026
	SCI2 transfer complete, error	Serial communication interface 2	H'0028
Low	A/D conversion end	A/D converter	H'002A

Notes: 1. Vector addresses indicated as “Reserved” cannot be used.
2. This circuit is triggered by a SLEEP instruction and generates an interrupt after a certain time.

3.2.3 Interrupt Control Registers

Table 3-3 lists the registers that are used to control interrupts.

Table 3-3 Interrupt Control Registers

Register Name	Abbreviation	R/W	Initial Value	Address
Port mode register 1	PMR1	R/W	H'0C	H'FFEB
IRQ edge select register	IEGR	R/W	H'EC	H'FFF2
Interrupt enable register 1	IENR1	R/W	H'C0	H'FFF3
Interrupt enable register 2	IENR2	R/W	H'00	H'FFF4
Interrupt enable register 3	IENR3	R/W	H'3C	H'FFF5
Interrupt request register 1	IRR1	R/W*	H'C0	H'FFF6
Interrupt request register 2	IRR2	R/W*	H'00	H'FFF7
Interrupt request register 3	IRR3	R/W*	H'3C	H'FFF8

Note: * Write is enabled only for writing of 0 to clear flag.

1. Port mode register 1 (PMR1)

Bit	7	6	5	4	3	2	1	0
	NOISE CANCEL	EVENT	IRQC5	IRQC4	—	—	IRQC1	IRQC0
Initial value	0	0	0	0	1	1	0	0
Read/Write	R/W	R/W	R/W	R/W	—	—	R/W	R/W

PMR1 is an 8-bit read/write register that designates whether pins in port 1 are used for general-purpose I/O or for external interrupt input. It is also used to turn the noise canceller function of pin $\overline{IRQ_0}$ on or off.

Note: Before switching a pin function by modifying bit IRQ5, IRQ4, IRQ1, or IRQ0 in PMR1, first clear the interrupt enable flag to disable the interrupt. After the pin function has been switched, issue any instruction, then clear the interrupt request flag to 0.

Program example:

```
        .
        .
MOV. B R0L, @IENR1  ..... Disable interrupt
MOV. B R0L, @PMR1   ..... Change pin function
NOP                 ..... Issue any instruction
MOV. B R0L, @IRR1   ..... Clear interrupt request flag
MOV. B R1L, @IENR1  ..... Enable interrupt
        .
        .
```

Bit 7: Noise cancel (NOISE CANCEL)

This bit enables or disables the noise canceller function of pin $\overline{IRQ_0}$.

Bit 7 NOISE CANCEL	Description	
0	Disables the noise canceller function of pin $\overline{IRQ_0}$.	(initial value)
1	Enables the noise canceller function of pin $\overline{IRQ_0}$. Input is sampled at intervals of 256 states. If two consecutive values do not match, the input is regarded as noise.	

Bit 6: $P1_6/\overline{EVENT}$ pin function switch (EVENT)

Bit 6 EVENT	Description	
0	$P1_6/\overline{EVENT}$ pin functions as $P1_6$ pin.	(initial value)
1	$P1_6/\overline{EVENT}$ pin functions as $\overline{EVENT}$ pin.	

Bit 5: $P1_5/\overline{IRQ_5}$/TMOE pin function switch (IRQC5)

Bit 5 IRQC5	Description	
0	$P1_5/\overline{IRQ_5}$/TMOE pin functions as $P1_5$/TMOE pin.*	(initial value)
1	$P1_5/\overline{IRQ_5}$/TMOE pin functions as $\overline{IRQ_5}$ pin.	

Note: * For the TMOE usage of this pin, see 7.3.2, Port Mode Register 4 .

Bit 4: $P1_4/\overline{IRQ_4}$ pin function switch (IRQC4)

Bit 4 IRQC4	Description	
0	$P1_4/\overline{IRQ_4}$ pin functions as $P1_4$ pin.	(initial value)
1	$P1_4/\overline{IRQ_4}$ pin functions as $\overline{IRQ_4}$ pin.	

Bits 3 and 2: Reserved bits

Bits 3 and 2 are reserved; they always read 1, and cannot be modified.

Bit 1: $P1_1/\overline{IRQ_1}$ pin function switch (IRQC1)

Bit 1 IRQC1	Description	
0	$P1_1/\overline{IRQ_1}$ pin functions as $P1_1$ pin.	(initial value)
1	$P1_1/\overline{IRQ_1}$ pin functions as $\overline{IRQ_1}$ pin.	

Bit 0: $P1_0/\overline{IRQ_0}$ pin function switch (IRQC0)

Bit 0 IRQC0	Description	
0	$P1_0/\overline{IRQ_0}$ pin functions as $P1_0$ pin.	(initial value)
1	$P1_0/\overline{IRQ_0}$ pin functions as $\overline{IRQ_0}$ pin.	

2. IRQ edge select register (IEGR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	IEG4	—	—	IEG1	IEG0
Initial value	1	1	1	0	1	1	0	0
Read/Write	—	—	—	R/W	—	—	R/W	R/W

IEGR is an 8-bit read/write register, used to designate rising edge sensing or falling edge sensing for pins $\overline{IRQ_0}$, $\overline{IRQ_1}$, and $\overline{IRQ_4}$.

Bits 7 to 5: Reserved bits

Bits 7 to 5 are reserved; they always read 1, and cannot be modified.

Bit 4: $\overline{IRQ_4}$ pin input edge select (IEG4)

Bit 4 IEG4	Description	
0	Falling edge of $\overline{IRQ_4}$ pin input is detected.	(initial value)
1	Rising edge of $\overline{IRQ_4}$ pin input is detected.	

Bits 3 and 2: Reserved bits

Bits 3 and 2 are reserved; they always read 1, and cannot be modified.

Bit 1: $\overline{IRQ_1}$ pin input edge select (IEG1)

Bit 1 IEG1	Description	
0	Falling edge of $\overline{IRQ_1}$ pin input is detected.	(initial value)
1	Rising edge of $\overline{IRQ_1}$ pin input is detected.	

Bit 0: $\overline{IRQ_0}$ pin input edge select (IEG0)

Bit 0 IEG0	Description	
0	Falling edge of $\overline{IRQ_0}$ pin input is detected.	(initial value)
1	Rising edge of $\overline{IRQ_0}$ pin input is detected.	

3. Interrupt enable register 1 (IENR1)

Bit	7	6	5	4	3	2	1	0
	—	—	IEN5	IEN4	—	—	IEN1	IEN0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

IENR1 is an 8-bit read/write register that enables or disables external interrupts.

Bits 7 and 6: Reserved bits

Bits 7 and 6 are reserved; they always read 1, and cannot be modified.

Bits 5 and 4: IRQ_5 and IRQ_4 interrupt enable (IEN5 and IEN4)

Bits 5 and 4 IEN5, IEN4	Description	
0	Disables interrupt requests by IRRI5 and IRRI4.	(initial value)
1	Enables interrupt requests by IRRI5 and IRRI4.	

Bits 3 and 2: Reserved bits

Bits 3 and 2 are reserved, but they can be written and read.

Bits 1 and 0: IRQ_1 and IRQ_0 interrupt enable (IEN1 and IEN0)

Bits 1 and 0 IEN1, IEN0	Description	
0	Disables interrupt requests by IRRI1 and IRRI0.	(initial value)
1	Enables interrupt requests by IRRI1 and IRRI0.	

4. Interrupt enable register 2 (IENR2)

Bit	7	6	5	4	3	2	1	0
	—	—	IENDT	IENTE	IENTD	IENTC	IENTB	IENTA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IENR2 is an 8-bit read/write register that enables or disables direct transfer interrupts and timer A to E overflow interrupts.

Bits 7 and 6: Reserved bits

Bits 7 and 6 are reserved, but they can be written and read.

Bit 5: Direct transfer interrupt enable (IENDT)

Bit 5 IENDT	**Description**	
0	Disables direct transfer interrupt requests by IRRDT.	(initial value)
1	Enables interrupt requests by IRRDT.	

Bits 4 to 0: Timer E to A interrupt enable (IENTE to IENTA)

Bits 4 to 0 IENTE to IENTA	**Description**	
0	Disables interrupt requests by IRRTE to IRRTA.	(initial value)
1	Enables interrupt requests by IRRTE to IRRTA.	

5. Interrupt enable register 3 (IENR3)

Bit	7	6	5	4	3	2	1	0
	IENAD	IENKS	—	—	—	—	IENS2	IENS1
Initial value	0	0	1	1	1	1	0	0
Read/Write	R/W	R/W	—	—	—	—	R/W	R/W

IENR3 is an 8-bit read/write register that enables or disables A/D converter, key scan, and serial communication interface 1 and 2 interrupts.

Bit 7: A/D converter interrupt enable (IENAD)

Bit 7 IENAD	Description	
0	Disables interrupt requests by IRRAD.	(initial value)
1	Enables interrupt requests by IRRAD.	

Bit 6: Key scan interrupt enable (IENKS)

Bit 6 IENKS	Description	
0	Disables interrupt requests by IRRKS.	(initial value)
1	Enables interrupt requests by IRRKS.	

Bits 5 to 2: Reserved bits

Bits 5 to 2 are reserved; they always read 1, and cannot be modified.

Bits 1 and 0: Serial communication interface 2 and 1 interrupt enable (IENS2 and IENS1)

Bits 1 and 0 IENS2, IENS1	Description	
0	Disables interrupt requests by IRRS2 and IRRS1.	(initial value)
1	Enables interrupt requests by IRRS2 and IRRS1.	

6. Interrupt request register 1 (IRR1)

Bit	7	6	5	4	3	2	1	0
	—	—	IRRI5	IRRI4	—	—	IRRI1	IRRI0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	R/W*	R/W*	—	—	R/W*	R/W*

Note: * Only 0 can be written, to clear the flag.

IRR1 is an 8-bit read/write register with flags that are set to 1 when an external interrupt is requested.

Bits 7 and 6: Reserved bits

Bits 7 and 6 are reserved; they always read 1, and cannot be modified.

Bits 5 and 4: IRQ_5 and IRQ_4 interrupt request (IRRI5 and IRRI4)

Bits 5 and 4 IRRI5, IRRI4	Description
0	No interrupt request from the corresponding pin ($\overline{IRQ_5}$ or $\overline{IRQ_4}$). (initial value)
1	**Setting condition:** Set when the corresponding pin ($\overline{IRQ_5}$ or $\overline{IRQ_4}$) is designated for interrupt input in PMR1 and the designated edge is input. **Clearing method:** Cleared when software writes 0 in the flag. (The flag is not automatically cleared when an interrupt is accepted.)

Bits 3 and 2: Reserved bits

Bits 3 and 2 are reserved; they always read 0, and cannot be modified.

Bits 1 and 0: IRQ_1 and IRQ_0 interrupt request (IRRI1 and IRRI0)

Bits 1 and 0 IRRI1, IRRI0	Description
0	No interrupt request from the corresponding pin ($\overline{IRQ_1}$ or $\overline{IRQ_0}$). (initial value)
1	**Setting condition:** Set when the corresponding pin ($\overline{IRQ_1}$ or $\overline{IRQ_0}$) is designated for interrupt input in PMR1 and the designated edge is input. **Clearing method:** Cleared when software writes 0 in the flag. (The flag is not automatically cleared when an interrupt is accepted.)

7. Interrupt request register 2 (IRR2)

Bit	7	6	5	4	3	2	1	0
	—	—	IRRDT	IRRTE	IRRTD	IRRTC	IRRTB	IRRTA
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Note: * Only 0 can be written, to clear the flag.

IRR2 is an 8-bit read/write register with flags that are set to 1 when a direct transfer interrupt or timer A to E overflow interrupt is requested.

Bits 7 and 6: Reserved bits

Bits 7 and 6 are reserved; they always read 0, and only 0 may be written.

Bit 5: Direct transfer interrupt request (IRRDT)

Bits 5 IRRDT	Description
0	No direct transfer interrupt request. (initial value)
1	**Setting conditions:** In subactive mode, when the system control register 2 (SYSCR2) DTON bit = 1, the system control register 1 (SYSCR1) LSON bit = 0, and the interrupt enable register 2 (IENR2) IENDT bit = 1, execution of a SLEEP instruction results in direct transfer to active mode via watch mode. During this process a direct transfer interrupt is requested and the IRRDT flag is set to 1. **Clearing method:** Cleared when software writes 0 in the flag. (The flag is not automatically cleared when an interrupt is accepted.)

Bits 4 to 0: Timer E to A interrupt request (IRRTE to IRRTA)

Bits 4 to 0 IRRTE to IRRTA	Description
0	No overflow interrupt request from the corresponding timer (E to A). (initial value)
1	**Setting conditions:** When a timer E to A overflow interrupt is requested, the corresponding flag (IRRTE to IRRTA) is set to 1. **Clearing method:** Cleared when software writes 0 in the flag. (The flag is not automatically cleared when an interrupt is accepted.)

8. Interrupt request register 3 (IRR3)

Bit	7	6	5	4	3	2	1	0
	IRRAD	IRRKS	—	—	—	—	IRRS2	IRRS1
Initial value	0	0	1	1	1	1	0	0
Read/Write	R/W*	R/W*	—	—	—	—	R/W*	R/W*

Note: * Only 0 can be written, to clear the flag.

Bit 7: A/D conversion complete interrupt request (IRRAD)

Bit 7 IRRAD	Description
0	No A/D converter interrupt request. (initial value)
1	**Setting conditions:** When the A/D converter completes A/D conversion, an interrupt is requested and the IRRAD flag is set to 1. **Clearing method:** Cleared when software writes 0 in the flag. (The flag is not automatically cleared when an interrupt is accepted.)

Bit 6: Key scan interrupt request (IRRKS)

Bit 6 IRRKS	Description
0	No key scan interrupt request. (initial value)
1	**Setting conditions:** When the VFD controller/driver requests a key scan interrupt, the IRRKS flag is set to 1. **Clearing method:** Cleared when software writes 0 in the flag. (The flag is not automatically cleared when an interrupt is accepted.)

Bits 5 to 2: Reserved bits

Bits 5 to 2 are reserved; they always read 1, and cannot be modified.

Bits 1 and 0: Serial communication interface 2 and 1 interrupt request (IRRS2, IRRS1)

Bits 1, 0 IRRS2, IRRS1	Description
0	No transfer complete or error interrupt request by the corresponding serial communication interface. (initial value)
1	**Setting conditions:** When an interrupt is requested due to transfer complete or error on serial communication interface 2 or 1, the corresponding flag (IRRS2 or IRRS1) is set to 1. **Clearing method:** Cleared when software writes 0 in the flag. (The flag is not automatically cleared when an interrupt is accepted.)

3.2.4 External Interrupts

There are four external interrupts, IRQ_5, IRQ_4, IRQ_1, and IRQ_0. These interrupts are requested by means of input signals at pins $\overline{IRQ_5}$, $\overline{IRQ_4}$, $\overline{IRQ_1}$, and $\overline{IRQ_0}$.

Interrupts IRQ_4, IRQ_1, and IRQ_0 are detected by either rising edge sensing or falling edge sensing, depending on the settings of bits IEG4, IEG1, and IEG0 in the IRQ edge select register (IEGR). IRQ_5 is detected by falling edge sensing only. In order to enable external interrupt input, it is first necessary to set the corresponding bit in port mode register 1 (PMR1) to 1.

When the designated edge is input at pins $\overline{IRQ_5}$, $\overline{IRQ_4}$, $\overline{IRQ_1}$, and $\overline{IRQ_0}$, the corresponding flag in interrupt request register 1 (IRR1) is set to 1. After the interrupt is accepted, the flag that was set is not automatically cleared, so the interrupt handling routine must be programmed to clear the flag to 0. A given interrupt request can be disabled by clearing its interrupt enable bit to 0.

Interrupts IRQ_5, IRQ_4, IRQ_1, and IRQ_0 are enabled by setting bits IEN5, IEN4, IEN1, and IEN0 to 1 in interrupt enable register 1. All interrupts can be masked by setting the I bit in CCR to 1.

When an IRQ_5, IRQ_4, IRQ_1, or IRQ_0 interrupt request is accepted, the I bit is set to 1. The order of priority is from IRQ_0 (high) to IRQ_5 (low). For details see table 3-2.

A noise canceller function can be selected for IRQ_0 interrupts, in which case a noise cancellation circuit samples the IRQ_0 input every 256 states. If two consecutive sampling results do not match, noise is assumed and the request is not accepted.

3.2.5 Internal Interrupts

There are ten internal interrupts that can be requested by the on-chip peripheral modules. These interrupts can be masked (held pending) by setting the I bit in CCR to 1. When an internal interrupt request is accepted and the interrupt exception handling sequence is executed, the I bit is set to 1. For the order of priority of interrupts from on-chip peripheral modules, see table 3-2.

3.2.6 Interrupt Operations

Interrupts are controlled by an interrupt controller. Figure 3-2 shows a block diagram of the interrupt controller, while figure 3-3 shows the flow up to interrupt acceptance.

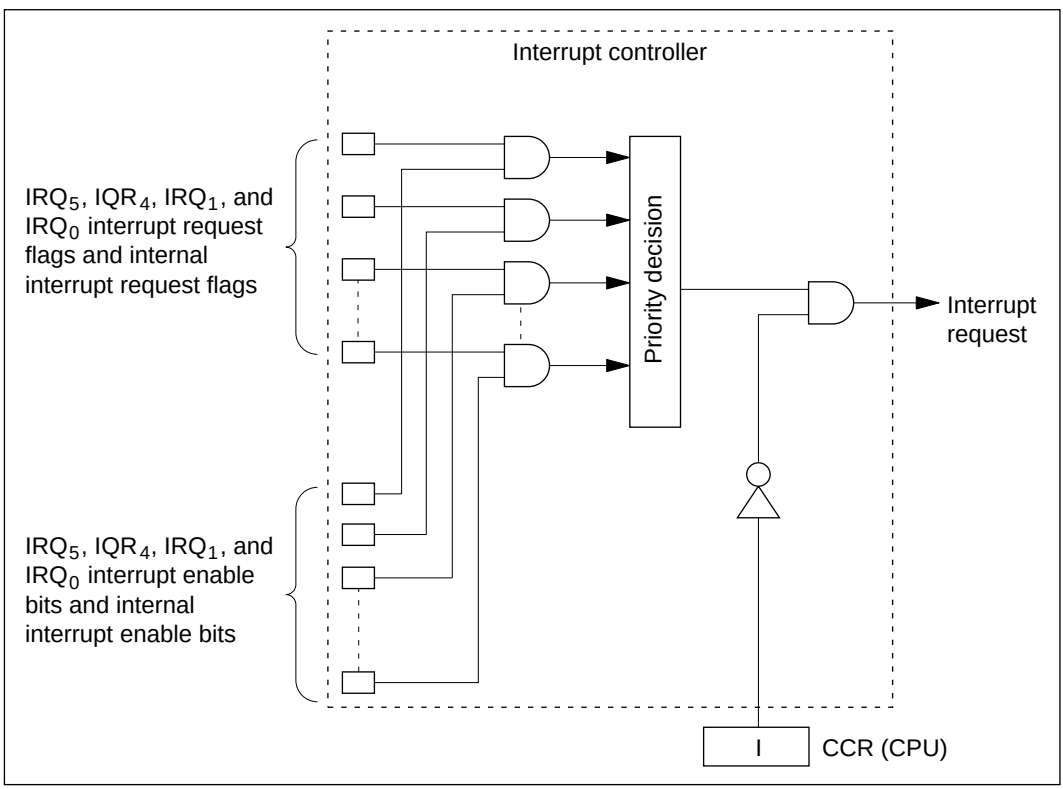


Figure 3-2 Block Diagram of Interrupt Controller

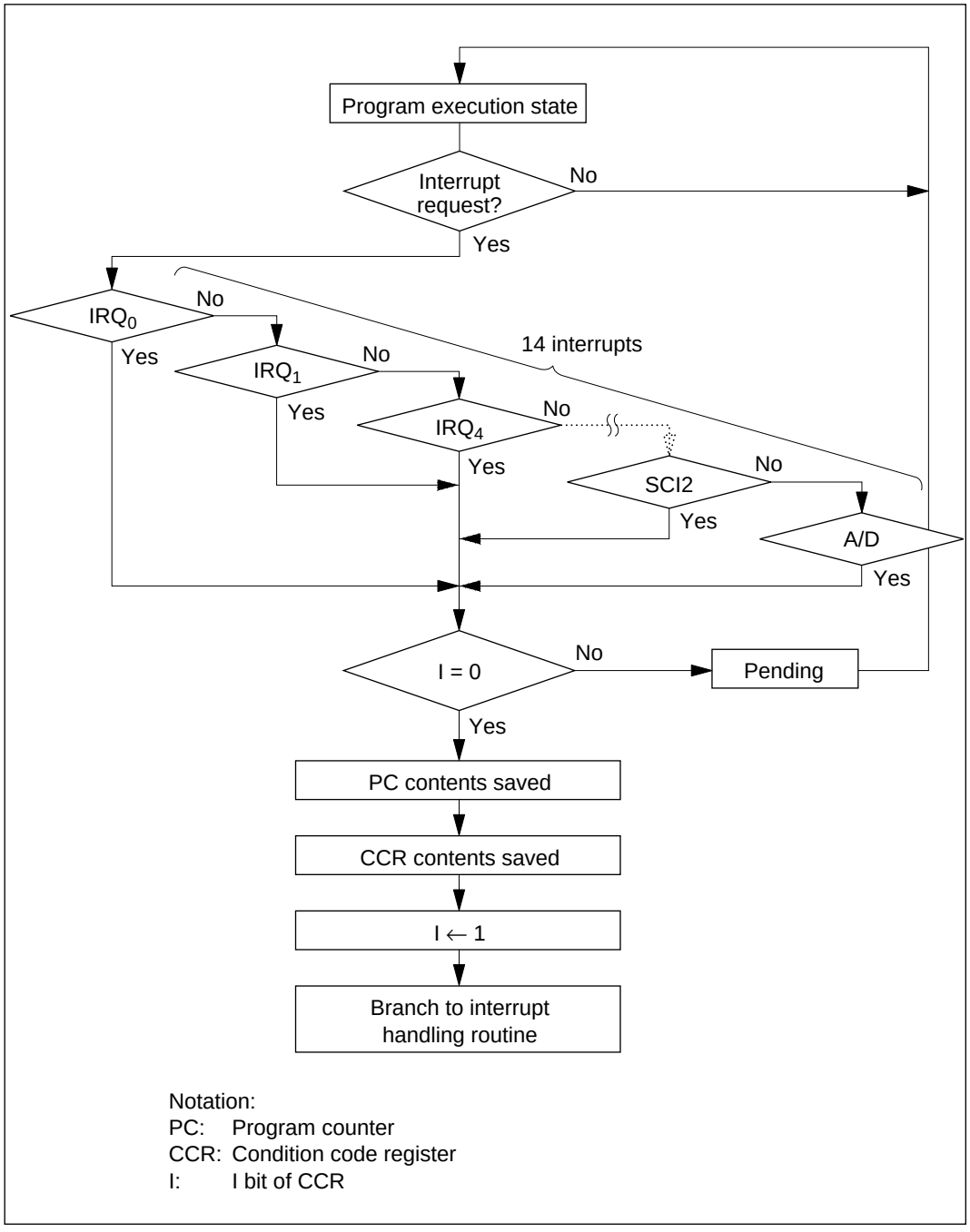


Figure 3-3 Flow Up to Interrupt Acceptance

The following operations take place when an interrupt occurs.

1. When an interrupt is requested by external interrupt pin input or by a peripheral module, an interrupt request signal is sent to the interrupt controller.

2. When the interrupt controller receives an interrupt request signal, it sets the interrupt request flag.

3. From among the interrupts for which the corresponding interrupt enable bit is also set to 1, the interrupt controller selects the interrupt request with the highest priority and holds the others pending. (See table 3-2.)

4. The interrupt controller checks the I bit of CCR. If the I bit is 0, the selected interrupt request is accepted; if the I bit is 1, the interrupt request is held pending.

5. If the interrupt is accepted, after processing of the current instruction is completed, both PC and CCR are pushed onto the stack. The state of the stack at this time is shown in figure 3-4. The PC value pushed onto the stack is the address of the first instruction to be executed upon return from interrupt handling.

6. The I bit of CCR is set to 1, masking all further interrupts.

7. A vector address is generated for the accepted interrupt, and the contents of that address are read and loaded into PC. Program execution then resumes from the address indicated in PC.

Note: No interrupt detection takes place immediately after completion of ORC, ANDC, XORC, or LDC instructions.

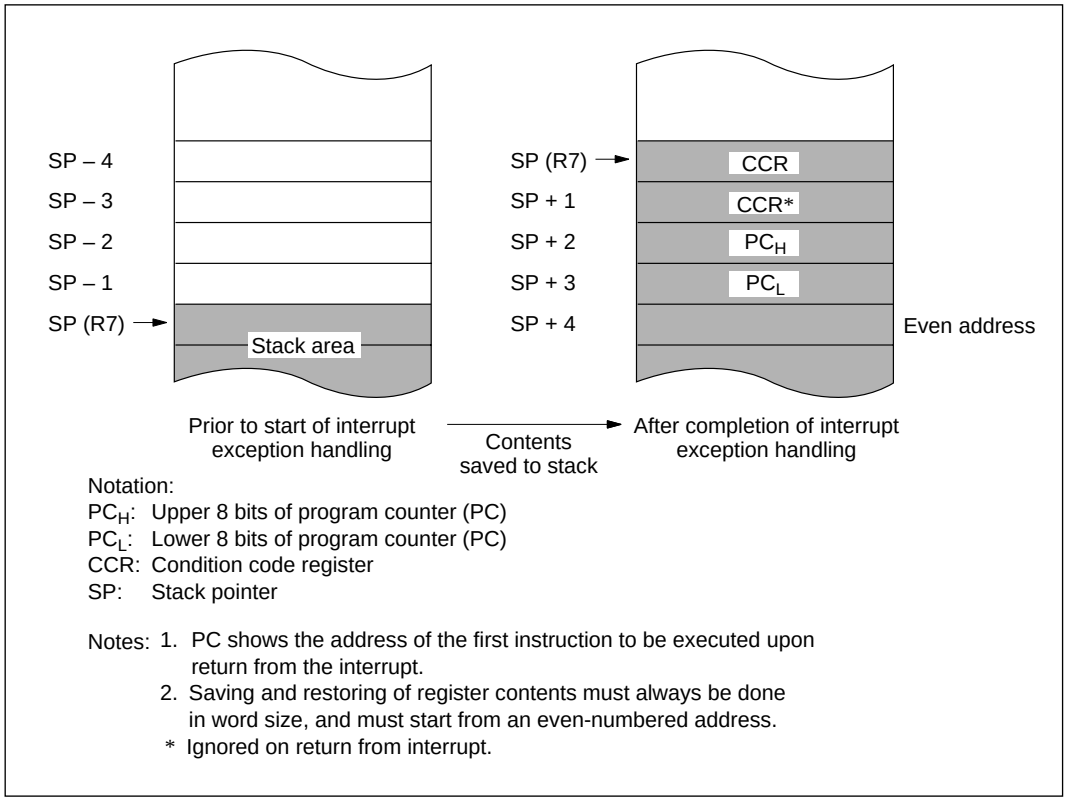


Figure 3-4 Stack State after Completion of Interrupt Exception Handling

Figure 3-5 shows a typical interrupt sequence.

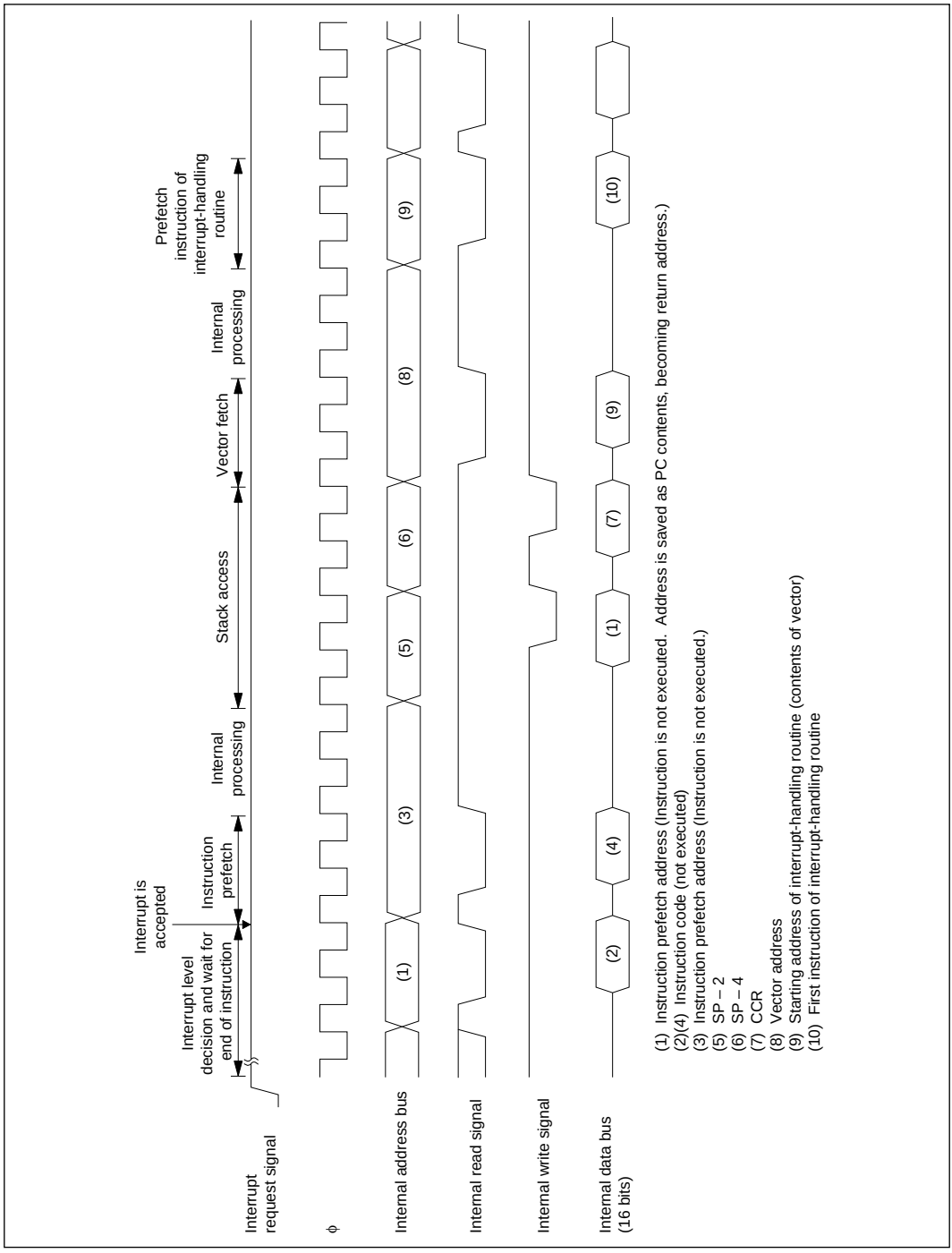


Figure 3-5 Interrupt Sequence

3.2.7 Return from an Interrupt

After completion of interrupt handling, the handler routine ends by executing an RTE instruction, to resume the original program from the point the interrupt. When RTE is executed, the values saved on the stack are restored to CCR and PC as shown in figure 3-6. Instruction execution resumes from the address indicated in PC.

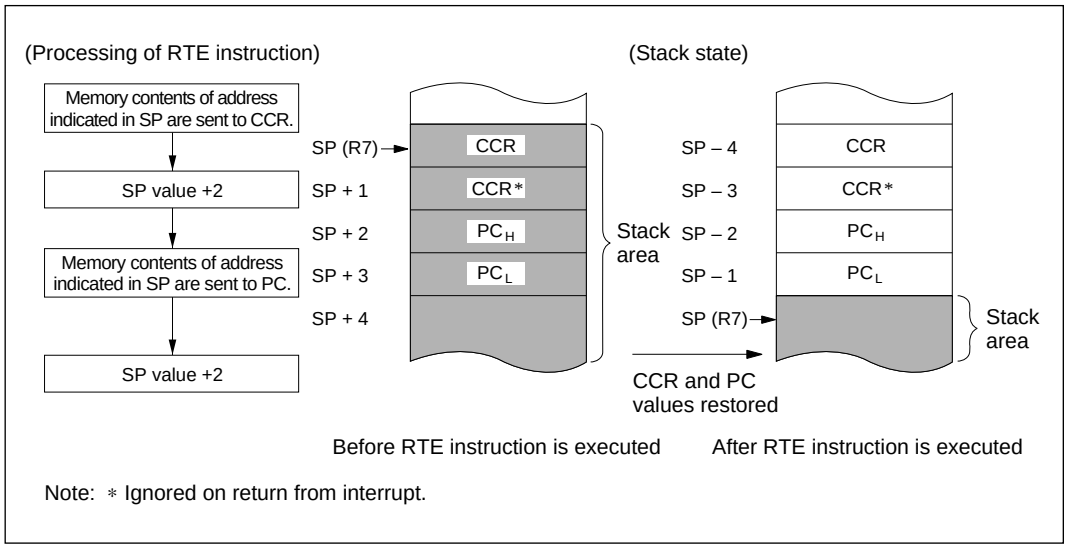


Figure 3-6 Stack State When RTE Instruction is Executed

3.2.8 Interrupt Response Time

Table 3-4 shows the number of wait states after an interrupt request flag is set and until the first instruction of the interrupt handler is executed.

Table 3-4 Interrupt Wait States

No.	Item	States
1	Waiting time for completion of current instruction*	1 to 13
2	Saving of PC and CCR to stack	4
3	Vector fetch	2
4	Instruction fetch	4
5	Internal processing	4
	Total	15 to 27

Note: * Not including EEPMOV instruction.

3.2.9 Valid Interrupts in Each Mode

Table 3-5 shows the valid interrupts in each mode. For details of the modes, see 3.3, System Modes.

Table 3-5 Valid Interrupts in Each Mode

	Mode				
Interrupt	**Active**	**Sleep**	**Standby**	**Watch**	**Subactive**
IRQ_0	❍	❍	❍	❍	❍
IRQ_1	❍	❍	❍	×	×
IRQ_4	❍	×	×	×	×
IRQ_5	❍	×	×	×	×
Key scan	❍	×	×	×	×
Timer A overflow	❍	❍	×	❍	❍
Timer B overflow	❍	×	×	×	×
Timer C overflow	❍	×	×	×	×
Timer D overflow	❍	×	×	×	×
Timer E overflow	❍	×	×	×	×
Direct transfer	×	×	×	×	Δ
SCI1 transfer complete or error	❍	×	×	×	×
SCI2 transfer complete or error	❍	×	×	×	×
A/D conversion end	❍	×	×	×	×

Note: The above table does not include interrupts occurring during a mode transition.

Notation:

❍: When an interrupt request flag is set, interrupt exception handling is started if the I bit = 0 in CCR and the interrupt enable bit = 1 for that interrupt. In sleep mode, standby mode, and watch mode, a mode transition takes place before interrupt exception handling starts.

Δ: When a SLEEP instruction is executed while the DTON bit = 1 and the LSON bit = 0, first a transition is made to watch mode and the interrupt request flag is set in synchronization with the subclock. When the interrupt request flag is set, if the interrupt enable flag = 1 for that interrupt and the I bit = 0 in CCR, a transition is made to active mode and interrupt exception handling starts.

×: The interrupt request flag is not set, and no mode transition occurs.

3.2.10 Notes on Stack Area Use

When word data is accessed in the H8/300L Series, the least significant bit of the address is regarded as 0. Access to the stack always takes place in word size, so the stack pointer (SP: R7) should never indicate an odd address. Use PUSH Rn (MOV.W Rn, @–SP) or POP Rn (MOV.W @SP+, Rn) to save or restore register values.

Setting an odd address in SP may cause a program to crash. An example is shown in figure 3-7.

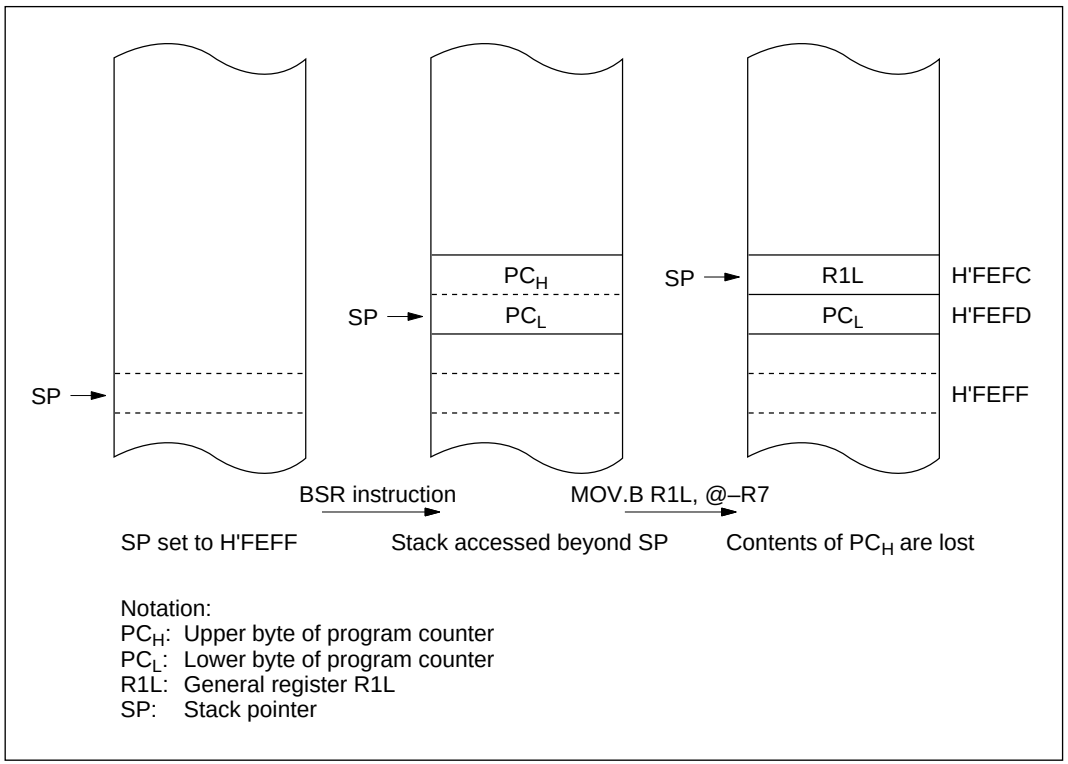


Figure 3-7 CPU Operation When Odd Address is Set in SP

Word access is also performed when the condition code register (CCR) is saved and restored by the interrupt exception-handling sequence and RTE instruction. When CCR is saved, the CCR value is saved in both the upper and lower bytes of the word data. When CCR is restored, it is loaded with the value at the even address. The value at the odd address is ignored.

3.3 System Modes

The H8/300L CPU is equipped with power-down modes for minimizing power dissipation. These and the other system modes are described below. There are five modes altogether, as follows.

- Active mode
- Sleep mode
- Standby mode
- Watch mode
- Subactive mode

} Low-power operation modes

Figure 3-8 shows the transitions among these modes.

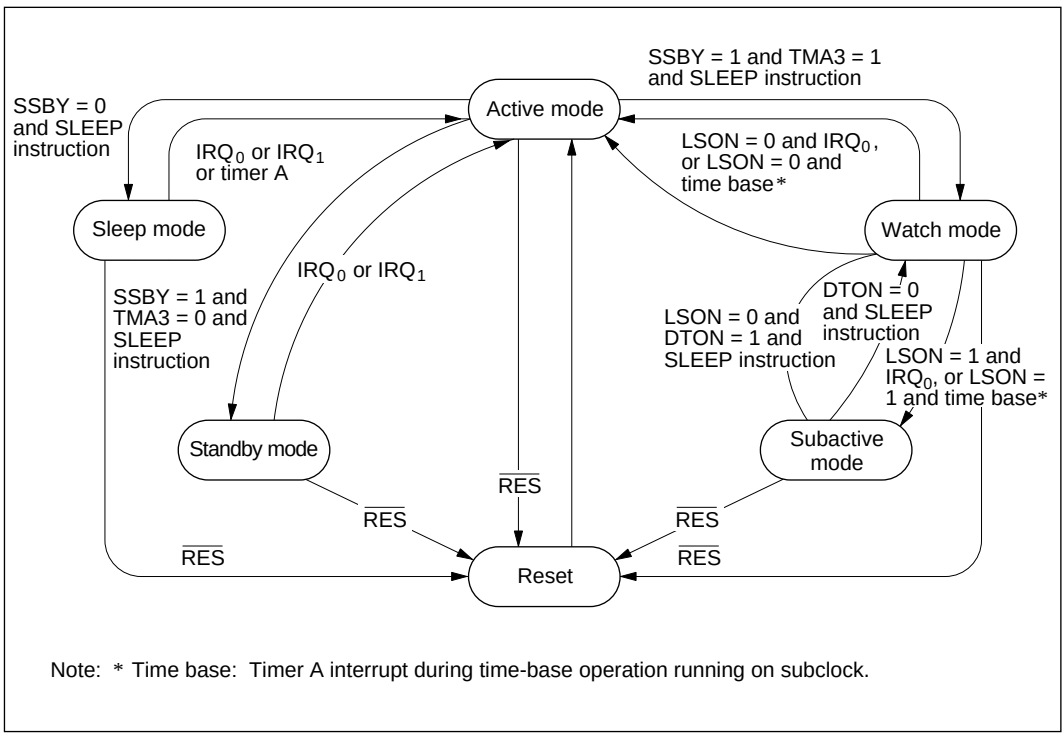


Figure 3-8 System Mode Transition Diagram

3.3.1 Active Mode

In active mode, the CPU executes instructions in synchronization with the system clock.

3.3.2 Low-Power Operation Mode

The H8/300L CPU supports four low-power operation modes: sleep mode, standby mode, watch mode, and subactive mode. These modes are described below.

Sleep mode: Sleep mode is entered by executing a SLEEP instruction while the SSBY bit in system control register 1 (SYSCR1) is cleared to 0. As soon as the SLEEP instruction has been executed, the CPU and on-chip peripheral modules halt operation, except for timer A. The contents of the internal registers of the CPU and on-chip peripheral modules, as well as the RAM contents, are retained.

Standby mode: Standby mode is entered by executing a SLEEP instruction while the SSBY bit in system control register 1 (SYSCR1) is set to 1 and timer mode register A (TMA) bit TMA3 = 0. In this mode, the CPU, system clock, and on-chip peripheral modules halt all operations. Output from the on-chip peripheral modules is reset; but as long as a minimum required voltage is applied, the contents of the internal registers of the CPU and on-chip peripheral modules, as well as the RAM contents, are retained. Standard I/O ports go to the high-impedance state. In high-voltage ports, the PMOS buffer transistors are switched off.

Watch mode: Watch mode is entered by executing a SLEEP instruction while the SSBY bit in system control register 1 (SYSCR1) is set to 1 and timer mode register A (TMA) bit TMA3 = 1. In this mode, the CPU, system clock, and on-chip peripheral modules halt, except for timer A. Output from the on-chip peripheral modules is reset; but as long as a minimum required voltage is applied, the contents of the internal registers of the CPU and on-chip peripheral modules, as well as the RAM contents, are retained. Standard I/O ports go to the high-impedance state. In high-voltage ports, the PMOS buffer transistors are switched off.

Subactive mode: Subactive mode is entered when a time base or IRQ_0 interrupt request is accepted in watch mode while the LSON bit in system control register 1 (SYSCR1) is set to 1. In this mode the CPU operates in synchronization with the subclock. On-chip peripheral modules halt operation, except for the time-base function of timer A. Output from the on-chip peripheral modules is reset; but as long as a minimum required voltage is applied, the contents of the internal registers of the on-chip peripheral modules are retained. Standard I/O ports go to the high-impedance state. In high-voltage ports, the PMOS buffer transistors are switched off.

Table 3-6 shows the internal states in each mode.

Table 3-6 Internal States in Operation Modes

Function		Active	Sleep	Standby	Watch	Subactive
System clock		Functions	Functions	Halted	Halted	Halted
Subclock		Functions	Functions	Functions	Functions	Functions
CPU operation	Instructions	Functions	Halted	Halted	Halted	Functions
	RAM	Functions	Retained	Retained	Retained	Functions
	Registers	Functions	Retained	Retained	Retained	Functions
	I/O	Functions	Retained	Retained*1	Retained*1	Functions*1, *2
Peripheral module interrupts	IRQ_0	Functions	Functions	Functions	Functions	Functions
	IRQ_1	Functions	Functions	Functions	Retained	Retained
	IRQ_4, IRQ_5	Functions	Retained	Retained	Retained	Retained
	Timer A	Functions	Functions	Retained	Functions*3	Functions*3
	Timer B	Functions	Retained	Retained	Retained	Retained
	Timer C	Functions	Retained	Retained	Retained	Retained
	Timer D	Functions	Retained	Retained	Retained	Retained
	Timer E	Functions	Retained	Retained	Retained	Retained
	SCI1, SCI2	Functions	Retained	Retained	Retained	Retained
	VFD	Functions	Retained (output is reset)	Retained (output is reset)	Retained (output is reset)	Retained (output is reset)
	PWM	Functions	Retained (output is reset)	Retained (output is reset)	Retained (output is reset)	Retained (output is reset)
	A/D	Functions	Retained	Retained	Retained	Retained

Notes: 1. Register contents are retained; output goes to high-impedance state.
2. Input (read) functions.
3. Functions when the time base function is selected.

1. Sleep mode

Operation in sleep mode is described below.

- Transition to sleep mode

  The system goes from active mode to sleep mode when a SLEEP instruction is executed while the SSBY bit in system control register 1 (SYSCR1) is cleared to 0. In this mode CPU operation is halted but the register, RAM, and port contents are retained. The clock pulse generator operates, as do external interrupts (IRQ_1 and IRQ_0) and timer A.

- Clearing sleep mode

  Sleep mode is cleared by an interrupt (IRQ_1, IRQ_0, or timer A) or by input at the $\overline{RES}$ pin.

  — Clearing by interrupt (IRQ_1, IRQ_0, or timer A)

  When an IRQ_1, IRQ_0, or timer A interrupt is requested, sleep mode is cleared and interrupt exception handling starts. Sleep mode is not cleared if the I bit in the condition code register (CCR) is set to 1 or the particular interrupt is disabled in the interrupt enable register.

  Before transition to sleep mode, other interrupts should be disabled.

  — Clearing by $\overline{RES}$ input

  When the $\overline{RES}$ pin goes low, the CPU goes into the reset state and sleep mode is cleared.

2. Standby mode

Operation in standby mode is described below.

- Transition to standby mode

  The system goes from active mode to standby mode when a SLEEP instruction is executed while the SSBY bit in system control register 1 (SYSCR1) is set to 1 and bit TMA3 in timer mode register A (TMA) is cleared to 0. In standby mode the clock pulse generator stops, so the CPU and on-chip peripheral modules stop functioning. As long as a minimum required voltage is applied, the CPU register contents and data in the on-chip RAM will be retained. Standard I/O ports go to the high-impedance state. In high-voltage ports, the PMOS buffer transistors are switched off.

- Clearing standby mode

  Standby mode is cleared by an external interrupt (IRQ_1, IRQ_0) or by input at the $\overline{RES}$ pin.

  — Clearing by interrupt (IRQ_1, IRQ_0)

  When an IRQ_1 or IRQ_0 interrupt signal is input, the clock pulse generator starts. After the time set in bits STS2 to STS0 in system control register 1 (SYSCR1) has elapsed, a stable clock signal is supplied to the entire chip, standby mode is cleared, and interrupt exception handling starts. Before the transition to standby mode, other interrupts should be disabled. Standby mode is not cleared if the I bit in the condition code register (CCR) is set to 1 or the particular interrupt is disabled in the interrupt enable register.

  — Clearing by $\overline{RES}$ input

  When the $\overline{RES}$ pin goes low, the clock pulse generator starts and standby mode is cleared. After the pulse generator output has stabilized, if the $\overline{RES}$ pin is driven high, the CPU starts reset exception handling.

  Since clock signals are supplied to the entire chip as soon as the clock pulse generator starts functioning, the $\overline{RES}$ pin should be kept at the low level until the pulse generator output stabilizes.

3. Watch mode

Operation in watch mode is described below.

- Transition to watch mode

  From active mode, watch mode is entered when a SLEEP instruction is executed while the SSBY bit in system control register 1 (SYSCR1) is set to 1 and bit TMA3 in timer mode register A (TMA) is set to 1. From subactive mode, watch mode is entered when a SLEEP instruction is executed while the DTON bit in system control register 2 (SYSCR2) is cleared to 0.

  In watch mode, operation of the system clock pulse generator and of on-chip peripheral modules is halted, except for the time-base function of timer A. Output from the on-chip peripheral modules is reset; but as long as a minimum required voltage is applied, the contents of the internal registers of the CPU and on-chip peripheral modules, and the on-chip RAM contents, are retained.

- Clearing watch mode

  Watch mode is cleared by a time-base interrupt from timer A, by an IRQ_0 interrupt, or by input at the $\overline{RES}$ pin.

  — Clearing by timer A time-base interrupt or IRQ_0 interrupt

  When timer A overflows or an IRQ_0 interrupt signal is input, if the LSON bit in system control register 1 (SYSCR1) is cleared to 0, the clock pulse generator starts. After the time set in bits STS2 to STS0 in system control register 1 (SYSCR1) has elapsed, a stable clock signal is supplied to the entire chip, watch mode is cleared, and interrupt exception handling starts. If LSON = 1, the system goes to subactive mode.

  In watch mode, the subclock (ϕ_{SUB}) is prescaled to generate a clock signal which is supplied to timer A. Timer A operates as a time base.

  Before the transition to watch mode, other external interrupts should be disabled. Watch mode is not cleared if the I bit in the condition code register (CCR) is set to 1 or the particular interrupt is disabled in the interrupt enable register.

  — Clearing by $\overline{RES}$ input

  When the $\overline{RES}$ pin goes low, the clock pulse generator starts and watch mode is cleared. After the pulse generator output has stabilized, if the $\overline{RES}$ pin is driven high, the CPU starts reset exception handling.

  Since clock signals are supplied to the entire chip as soon as the clock pulse generator starts functioning, the $\overline{RES}$ pin should be kept at the low level until the pulse generator output stabilizes.

4. Subactive mode

   Operation in subactive mode is described below.

- Transition to subactive mode

  Subactive mode is entered from watch mode if the LSON bit in system control register 1 (SYSCR1) is set to 1 at the time of a timer A time-base interrupt or IRQ_0 interrupt request.

  In subactive mode, the CPU operates in synchronization with the subclock (ϕ_{SUB}). The on-chip peripheral modules halt operation, except for the time base function of timer A. Output from the on-chip peripheral modules is reset; but as long as a minimum required voltage is applied, the contents of the internal registers of the on-chip peripheral modules are retained. Standard I/O ports go to the high-impedance state. In high-voltage ports, the PMOS buffer transistors are switched off.

- Clearing subactive mode

  Subactive mode is cleared by a SLEEP instruction or by input at the $\overline{\text{RES}}$ pin.

  — Clearing by SLEEP instruction

  When a SLEEP instruction is executed in subactive mode, subactive mode is cleared. If the DTON bit of system control register 2 (SYSCR2) is cleared to 0 when the SLEEP instruction is executed, the system goes to watch mode. If DTON = 1 and LSON = 0, a direct transfer interrupt is requested and the clock pulse generator starts. After the time set in bits STS2 to STS0 in system control register 1 (SYSCR1) has elapsed, a stable clock signal is supplied to the entire chip, and the system goes to active mode.

  Before the transition to active mode, other interrupts should be disabled. The direct transfer from subactive mode to active mode does not take place if the I bit in the condition code register (CCR) is set to 1 or the direct transfer interrupt is disabled in the interrupt enable register.

  — Clearing by $\overline{\text{RES}}$ input

  When the $\overline{\text{RES}}$ pin goes low, the clock pulse generator starts and subactive mode is cleared. After the pulse generator output has stabilized, if the $\overline{\text{RES}}$ pin is driven high, the CPU starts reset exception handling.

  Since clock signals are supplied to the entire chip as soon as the clock pulse generator starts functioning, the $\overline{\text{RES}}$ pin should be kept at the low level until the pulse generator output stabilizes.

3.3.3 Application Notes

1. In order to ensure sufficient time for the clock pulse generator to reach stable operation after clearing of standby mode or watch mode, or after a direct transfer from subactive to active mode, bits STS2 to STS0 in system control register 1 (SYSCR1) should be set as follows.

- When a ceramic oscillator is used

  Set bits STS2 to STS0 for a waiting time of at least 10 ms (see figure 3-9). For details, see 3.4.1, System Control Register 1 (SYSCR1).

- When an external clock is used

  Any values may be set. Normally the minimum time (STS2 = STS1 = STS0 = 0) should be set.

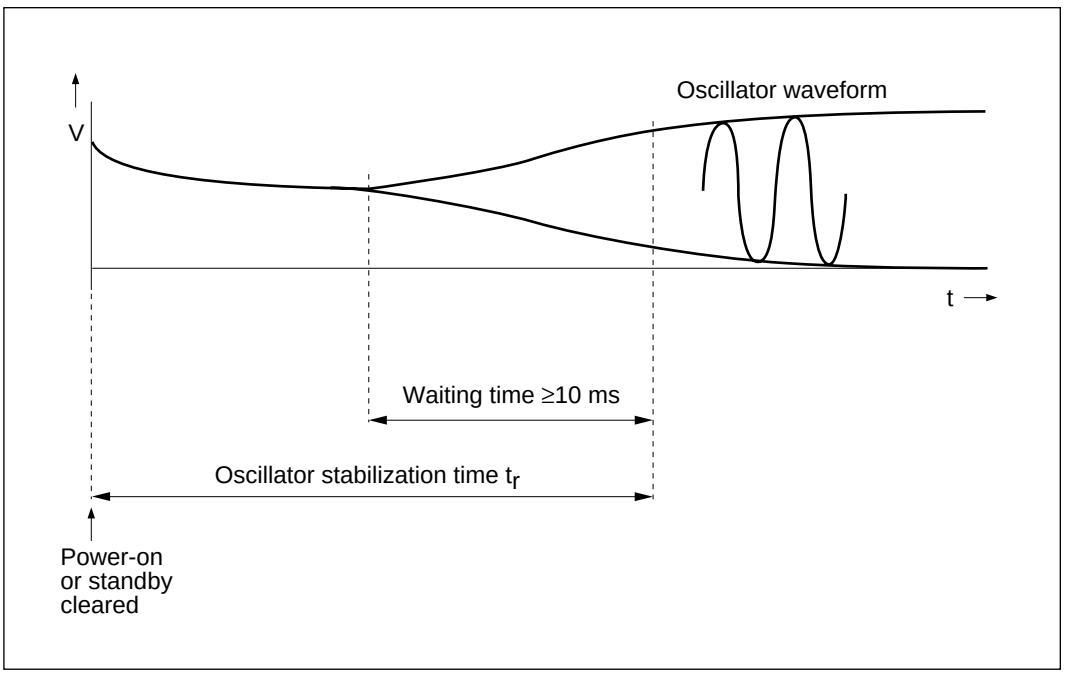


Figure 3-9 Waiting Time

2. To make a transition from subactive mode to active mode, the LSON bit in SYSCR1 should be cleared to 0 and the DTON bit in system control register 2 (SYSCR2) should be set to 1. Direct transfer is not possible when the LSON bit = 1.

3.4 System Control Registers

Table 3-7 shows how the system control registers (SYSCR1 and SYSCR2) are configured. These two registers are used to control the power-down modes.

Table 3-7 Register Configuration

Name	Abbreviation	R/W	Initial Value	Address
System control register 1	SYSCR1	R/W	H'00	H'FFF0
System control register 2	SYSCR2	R/W	H'F4	H'FFF1

3.4.1 System Control Register 1 (SYSCR1)

Bit	7	6	5	4	3	2	1	0
	SSBY	STS2	STS1	STS0	LSON	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W*	R/W	R/W	R/W	R/W	R/W	—	—

Note: * Write is enabled only in active mode.

SYSCR1 is an 8-bit read/write register for control of power-down modes.

Bit 7: Standby (SSBY)

This bit designates transition to standby mode.

When standby mode is cleared by an external interrupt and the system goes to active mode, this bit remains set to 1. It must be cleared by writing a 0. Writing is possible only in active mode.

Bit 7 SSBY	Explanation
0	When a SLEEP instruction is executed, a transition is made to sleep mode. (initial value)
1	When a SLEEP instruction is executed, a transition is made to standby mode or watch mode.

Bits 6 to 4: Standby timer select 2 to 0 (STS2 to STS0)

When a mode in which the system clock is stopped (standby, watch, or subactive mode) is cleared, the system waits for stable clock operation for a time set in these bits. The designation should be made according to the clock frequency so that the waiting time is at least 10 ms.

Bit 6 STS2	Bit 5 STS1	Bit 4 STS0	Explanation	
0	0	0	Wait time = 8,192 states.	(initial value)
0	0	1	Wait time = 16,384 states.	
0	1	0	Wait time = 32,768 states.	
0	1	1	Wait time = 65,536 states.	
1	*	*	Wait time = 131,072 states.	

Note: * Don't care.

Bit 3: Low speed on flag (LSON)

This bit chooses the system clock (ϕ) or subclock (ϕ_{SUB}) as the CPU operating clock when watch mode is cleared. Since this relates to the transitions between operation modes, this bit functions in combination with other control bits and interrupt input.

Bit 3 LSON	Explanation	
0	The CPU operates on the system clock (ϕ).	(initial value)
1	The CPU operates on the subclock (ϕ_{SUB}).	

Bit 2: Reserved bit

This bit is reserved, but it can be written and read.

Bits 1 and 0: Reserved bits

These bits are reserved; they always read 0, and cannot be modified.

3.4.2 System Control Register 2 (SYSCR2)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	DTON	—	—	—
Initial value	1	1	1	1	0	1	0	0
Read/Write	—	—	—	—	W*	—	R/W	R/W

Note: * Write is enabled only in subactive mode.

SYSCR2 is an 8-bit read/write register for control of direct transfer from subactive mode to active mode.

Bits 7 to 4: Reserved bits

These bits are reserved; they always read 1, and cannot be modified.

Bit 3: Direct transfer on flag (DTON)

This bit designates whether a transition is made to active mode or to watch mode when a SLEEP instruction is executed in subactive mode. When transfer to active mode is designated, the transition takes place via watch mode to allow time for the clock pulse generator to stabilize.

Bit 3 DTON	Explanation
0	When a SLEEP instruction is executed in subactive mode, a transition is made to watch mode. (initial value)
1	When a SLEEP instruction is executed in subactive mode while the LSON bit in system control register 1 (SYSCR1) is cleared to 0, a direct transfer interrupt is requested, and the system goes to active mode via watch mode.

Bit 2: Reserved bit

This bit is reserved; it always reads 1, and cannot be modified.

Bits 1 and 0: Reserved bits

These bits are reserved, but they can be written and read.

Section 4 ROM

4.1 Overview

The H8/3714 has 32 kbytes of on-chip mask ROM. The H8/3713 has 24 kbytes, and the H8/3712 has 16 kbytes. The ROM is connected to the CPU by a 16-bit data bus, allowing high-speed two-state access for both byte data and word data. The ZTAT™ version of the H8/3714 has a 32-kbyte PROM.

4.1.1 Block Diagram

Figure 4-1 gives a block diagram of the on-chip ROM.

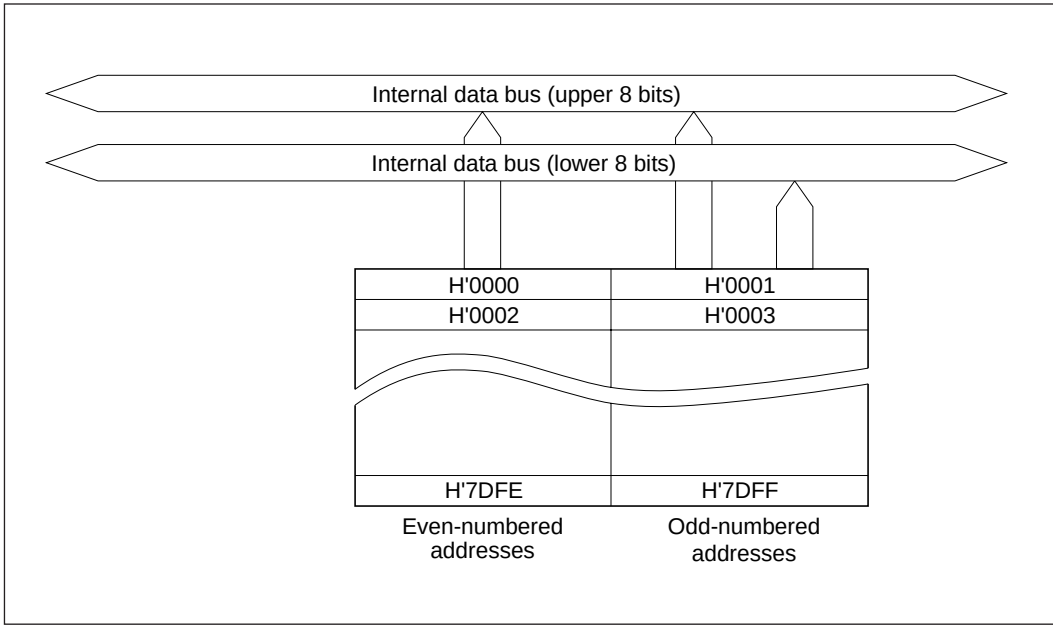


Figure 4-1 ROM Block Diagram (H8/3714)

4.2 PROM Mode

4.2.1 Selection of PROM Mode

If the on-chip ROM is a PROM, setting the chip to PROM mode stops operation as a microcontroller and allows the PROM to be programmed in the same way as the HN27C256H. Table 4-1 shows how to select PROM mode.

Table 4-1 Selection of PROM Mode

Pin Name	Setting
Test pin TEST	High level
Mode pin MD_0 ($P4_0/FS_{16}$)	Low level
Mode pin MD_1 ($P4_1/FS_{17}$)	
Mode pin MD_2 ($P1_7/V_{disp}$)	High level

4.2.2 Socket Adapter Pin Arrangement and Memory Map

A standard PROM programmer can be used to program the PROM. A socket adapter is required for conversion to 28 pins, as listed in table 4-2.

Figure 4-2 shows the pin-to-pin wiring of the socket adapter. Figure 4-3 shows a memory map.

Table 4-2 Socket Adapter

Package	Socket Adapter
64-pin (FP-64A)	HS3714ESH01H
64-pin (DP-64S)	HS3714ESS01H

H8/3714			EPROM Socket	
FP-64A	**DP-64S**	**Pin**	**Pin**	**HN27C256H**
17	26	$\overline{RES}$	V_{PP}	1
57	2	$P9_0$	EO_0	11
58	3	$P9_1$	EO_1	12
59	4	$P9_2$	EO_2	13
60	5	$P9_3$	EO_3	15
61	6	$P9_4$	EO_4	16
62	7	$P9_5$	EO_5	17
63	8	$P9_6$	EO_6	18
64	9	$P9_7$	EO_7	19
31	40	$P5_0$	EA_0	10
32	41	$P5_1$	EA_1	9
33	42	$P5_2$	EA_2	8
34	43	$P5_3$	EA_3	7
35	44	$P5_4$	EA_4	6
36	45	$P5_5$	EA_5	5
37	46	$P5_6$	EA_6	4
38	47	$P5_7$	EA_7	3
48	57	$P7_0$	EA_8	25
22	31	$P1_6$	EA_9	24
50	59	$P7_2$	EA_{10}	21
51	60	$P7_3$	EA_{11}	23
52	61	$P7_4$	EA_{12}	2
53	62	$P7_5$	EA_{13}	26
54	63	$P7_6$	EA_{14}	27
55	64	$P7_7$	$\overline{CE}$	20
49	58	$P7_1$	$\overline{OE}$	22
27	36	$P4_3$	V_{CC}	28
28	37	$P4_2$		
39	48	$P1_7$		
29	38	$P4_1$	V_{SS}	14
30	39	$P4_0$		
56, 1	1, 10	V_{CC}, AV_{CC}	V_{CC}	28
14, 10	23, 19	V_{SS}, AV_{SS}	V_{SS}	14
11	20, 22	TEST, X1	V_{CC}	28
15	24	OSC_1	V_{SS}	14

Note: Pins not indicated above should be left open.

Figure 4-2 Socket Adapter Pin Correspondence

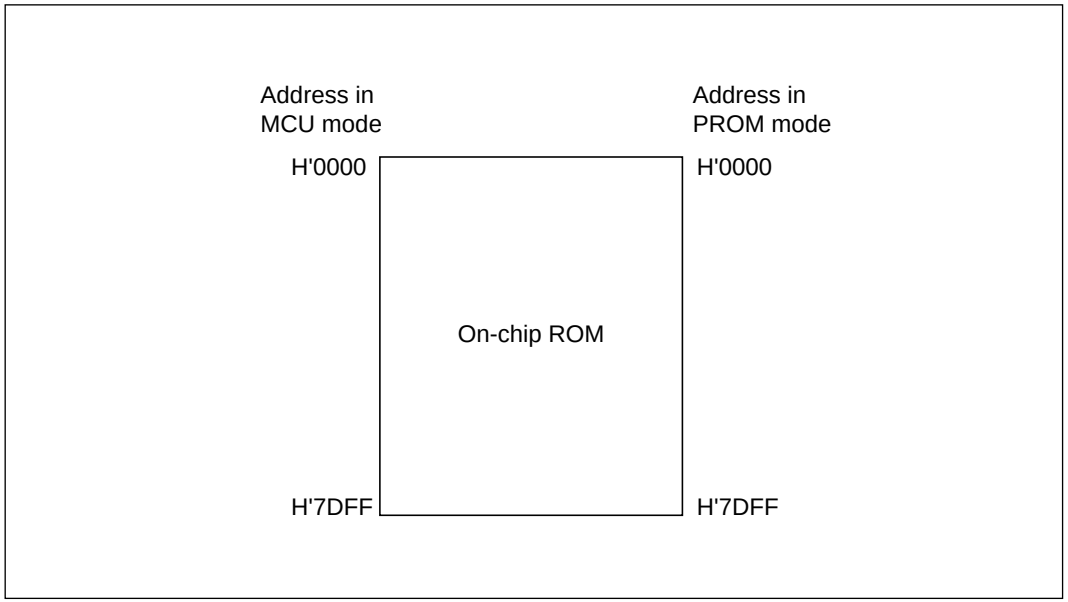


Figure 4-3 Memory Map in PROM Mode

4.3 Programming

The write, verify, and other modes are selected as shown in table 4-3 in PROM mode.

Table 4-3 Mode Selection in PROM Mode

	Pin					
Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	EO_7 to EO_0	EA_{14} to EA_0
Write	L	H	V_{PP}	V_{CC}	Data input	Address input
Verify	H	L	V_{PP}	V_{CC}	Data output	Address input
Programming disabled	H	H	V_{PP}	V_{CC}	High impedance	Address input

Notation:
L: Low level
H: High level
V_{PP}: V_{PP} level
V_{CC}: V_{CC} level

The specifications for writing and reading the on-chip PROM are identical to those for the standard HN27C256H EPROM.

4.3.1 Writing and Verifying

An efficient, high-speed programming method is provided for writing and verifying the PROM data. This method achieves high speed without voltage stress on the device and without lowering the reliability of written data. H'FF data is written in unused address areas.

The basic flow of this high-speed programming method is shown in figure 4-4. Table 4-4 and table 4-5 give the electrical characteristics in programming mode. Figure 4-5 shows a timing diagram.

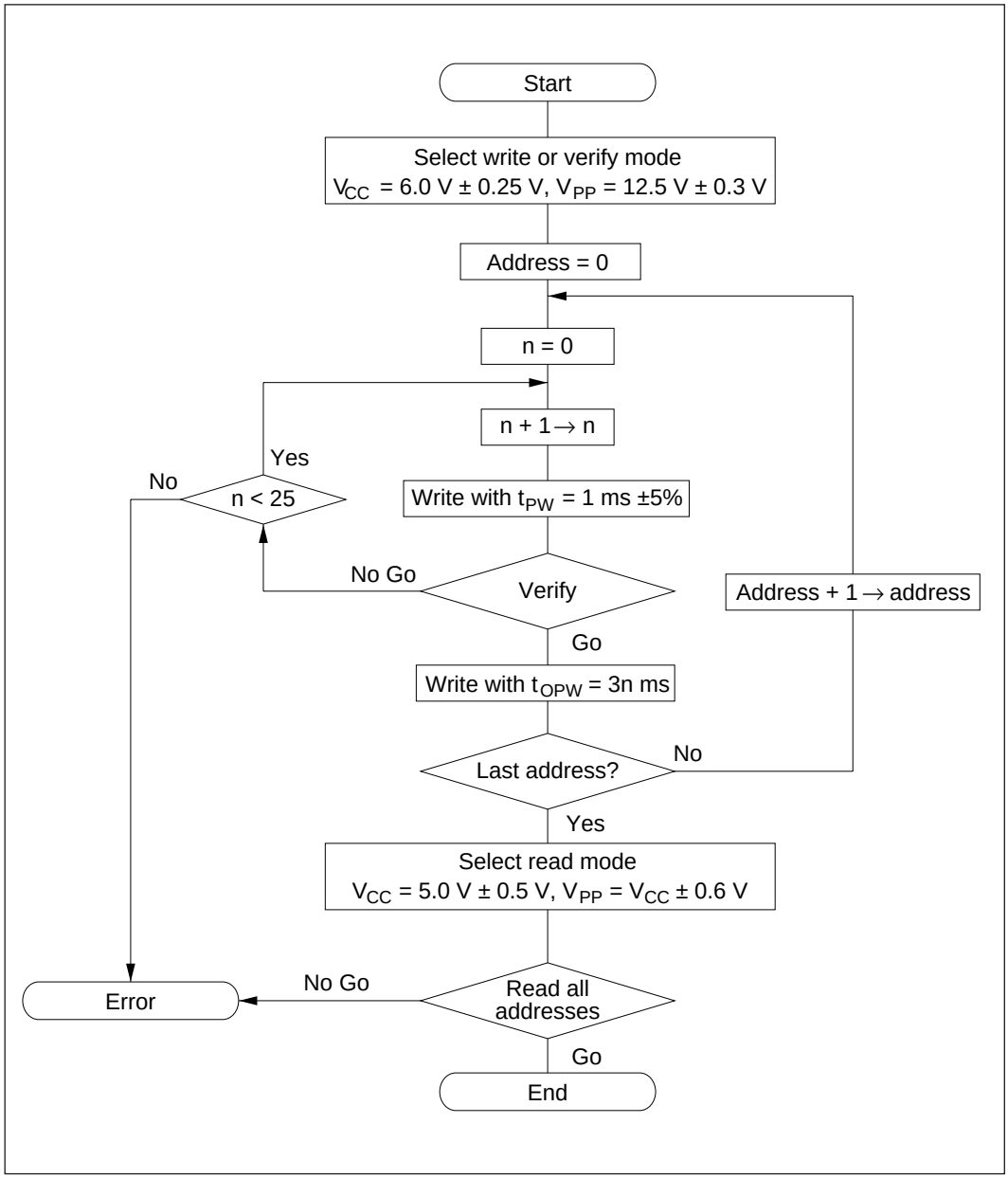


Figure 4-4 High-Speed Programming Flow Chart

Table 4-4 DC Characteristics (preliminary)

(Conditions: V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ±0.3 V, V_{SS} = 0.0 V, T_a = 25°C ±5°C)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input high-level voltage	EA_{14} to EA_0, $\overline{OE}$, $\overline{CE}$	V_{IH}	2.4	—	V_{CC} + 0.3	V	
Input low-level voltage	EA_{14} to EA_0, $\overline{OE}$, $\overline{CE}$	V_{IL}	–0.3	—	0.8	V	
Output high-level voltage	EO_7 to EO_0	V_{OH}	2.4	—	—	V	I_{OH} = –200 µA
Output low-level voltage	EO_7 to EO_0	V_{OL}	—	—	0.45	V	I_{OL} = 1.6 mA
Input leakage current	EO_7 to EO_0, EA_{14} to EA_0, $\overline{OE}$, $\overline{CE}$	$\|I_{LI}\|$	—	—	2	µA	V_{IN} = 5.25 V/0.5 V
V_{CC} current		I_{CC}	—	—	40	mA	
V_{PP} current		I_{PP}	—	—	40	mA	

Table 4-5 AC Characteristics

(Conditions: V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ±0.3 V, V_{SS} = 0.0 V, T_a = 25°C ±5°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2	—	—	µs	Figure 4-5*
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
Data output disable time	t_{DF}	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
Programming pulse width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{CE}$ pulse width for overwrite programming	t_{OPW}	2.85	—	78.75	ms	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
Data output delay time	t_{OE}	0	—	500	ns	

Notes: * Input pulse level: 0.8 to 2.2 V
Input rise time/fall time ≤ 20 ns
Timing reference levels Input: 1.0 V, 2.0 V
Output: 0.8 V, 2.0 V

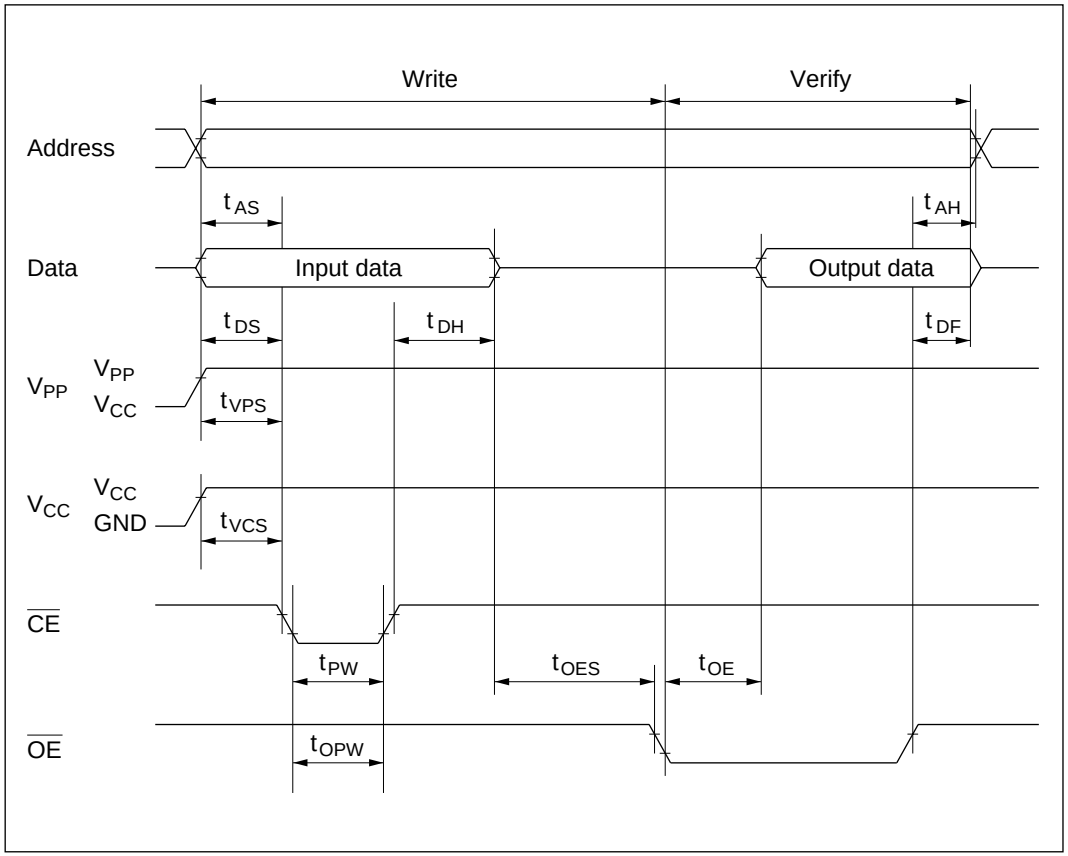


Figure 4-5 PROM Write/Verify Timing

4.3.2 Programming Precautions

1. Use the specified programming voltage and timing.

   The programming voltage in PROM mode (V_{PP}) is 12.5 V. Use of a higher voltage can permanently damage the chip. Be especially careful with respect to PROM programmer overshoot.

   Setting the PROM programmer to Hitachi specifications for the HN27C256H or to Intel specifications will result in a correct V_{PP} of 12.5 V.

2. Make sure the index marks on the PROM programmer socket, socket adapter, and chip are properly aligned. If they are not, the chip may be destroyed by excessive current flow. Before programming, be sure the chip is properly mounted in the PROM programmer.

3. Avoid touching the socket adapter or chip during programming, since this may cause contact faults and write errors.

4. Some commercially available EPROM programmers execute a device test before writing, reading, or verifying. The device test is a leakage test of the EPROM pins or ZTAT microcontroller pins. (A ZTAT microcontroller is a microcontroller with on-chip EPROM.) The function of this test is to check whether the device is correctly inserted in the socket, by confirming that leakage current flow is above a certain minimum level.

   In devices like the H8/3714 in which the on-chip EPROM is assigned to high-voltage pins (PMOS open-drain pins), no leakage current flows in the sink direction. That may cause the device test to fail and prevent writing, reading, or verifying. If this occurs, switch the device test off.

   Note that in some EPROM programmers, the device test cannot be switched off.

4.3.3 Reliability of Written Data

An effective way to assure the data holding characteristics of the programmed chips is to bake them at 150˚C, then screen them for data errors. This procedure quickly eliminates chips with PROM memory cells prone to early data retention failure.

Figure 4-8 shows a flow chart of this screening procedure.

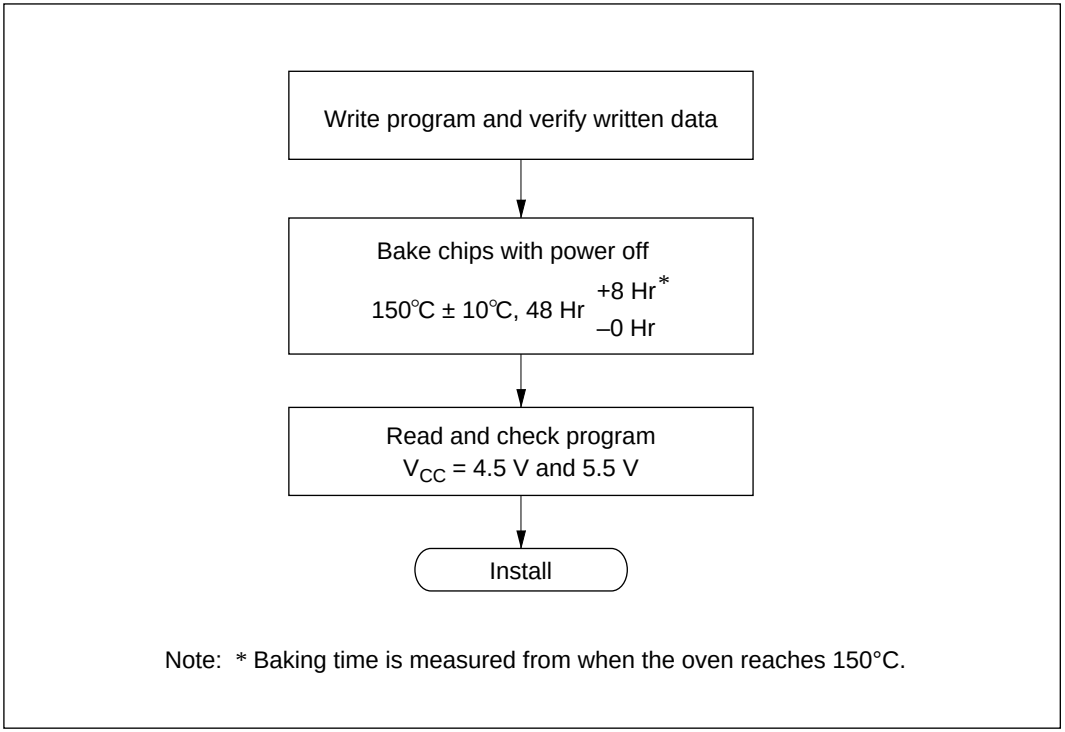


Figure 4-6 Recommended Screening Procedure

If write errors occur repeatedly while the same PROM programmer is being used, stop programming and check for problems in the PROM programmer and socket adapter, etc.

Please notify your Hitachi representative of any problems occurring during programming or in screening after high-temperature baking.

Section 5 RAM

5.1 Overview

The H8/3714 has 512 bytes of high-speed static RAM on-chip. The H8/3713 and the H8/3712 each has 384 bytes. The RAM is connected to the CPU by a 16-bit data bus, allowing high-speed two-state access for both byte data and word data.

5.1.1 Block Diagram

Figure 5-1 shows a block diagram of the on-chip RAM.

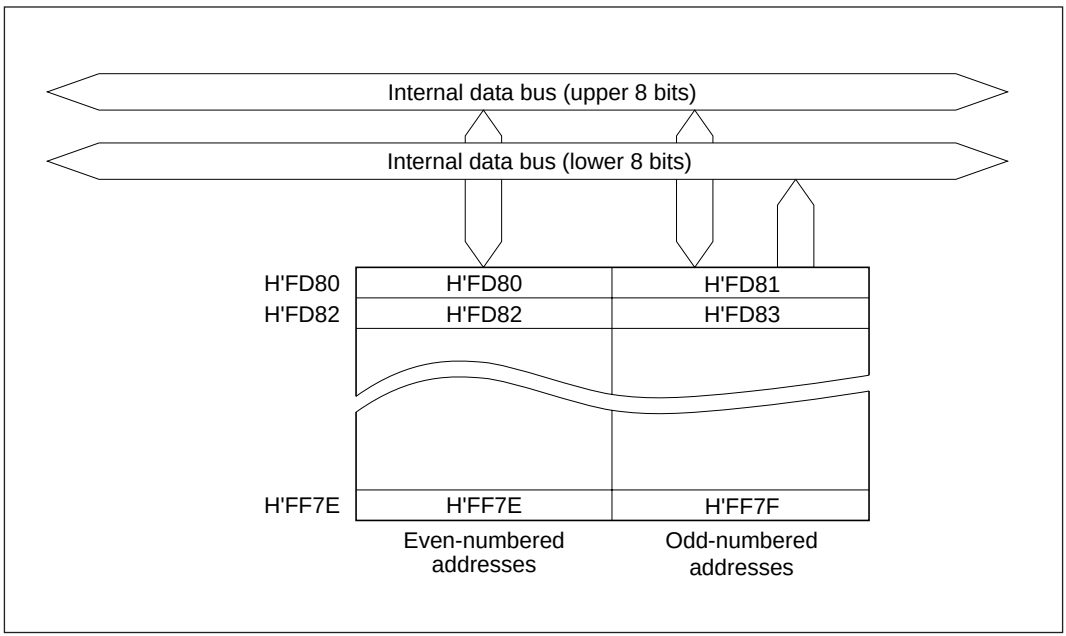


Figure 5-1 RAM Block Diagram (H8/3714)

5.1.2 Display RAM Area

In the H8/3714, H8/3713 and H8/3712, RAM addresses H'FEC0 to H'FEFF are also used as a display RAM for the VFD controller/driver. If the VFD controller/driver is not used, this area is available as an ordinary RAM.

Section 6 Clock Pulse Generators

6.1 Overview

Clock oscillator circuitry (CPG: Clock Pulse Generator) is provided on-chip, including both a system clock pulse generator and a subclock pulse generator. The system clock pulse generator consists of a system clock oscillator, system clock divider, and a clock divider (prescaler S) for the on-chip peripheral modules. The subclock pulse generator consists of a subclock oscillator circuit, subclock divider, and a further subclock divider (prescaler W) for time-base use.

6.1.1 Block Diagram

Figure 6-1 shows a block diagram of the clock pulse generators.

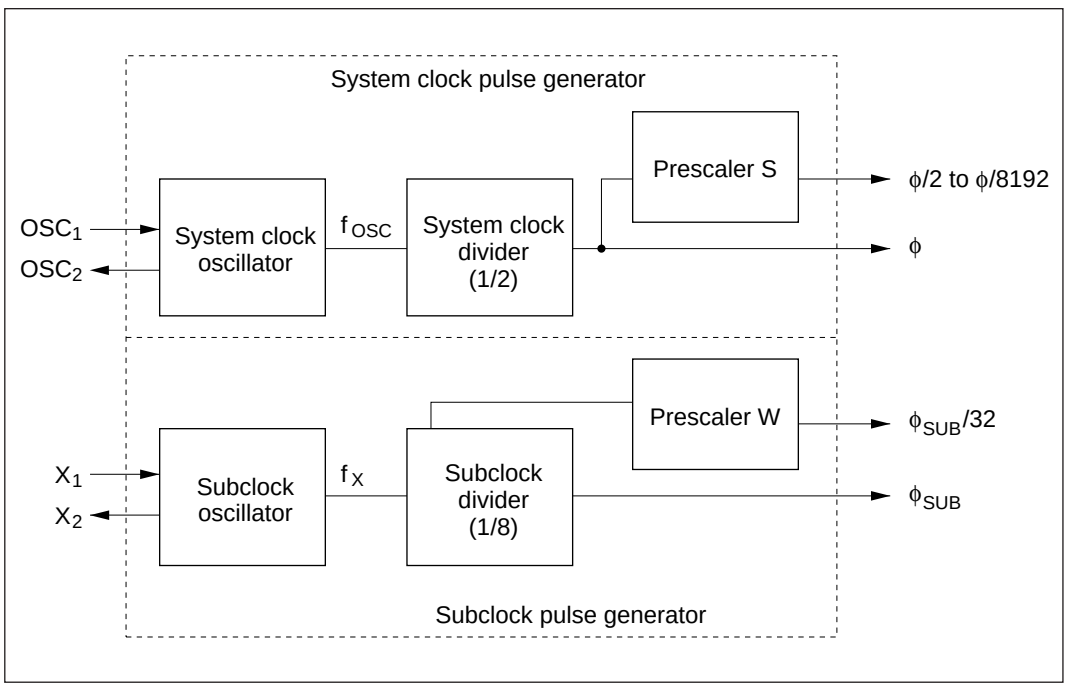


Figure 6-1 Block Diagram of Clock Pulse Generators

6.2 System Clock Generator

Clock pulses can be supplied to the system clock divider either by connecting a crystal or ceramic oscillator, or by providing external clock input.

1. Connecting a crystal oscillator

- Circuit configuration

  Figure 6-2 shows a typical method of connecting a crystal oscillator.

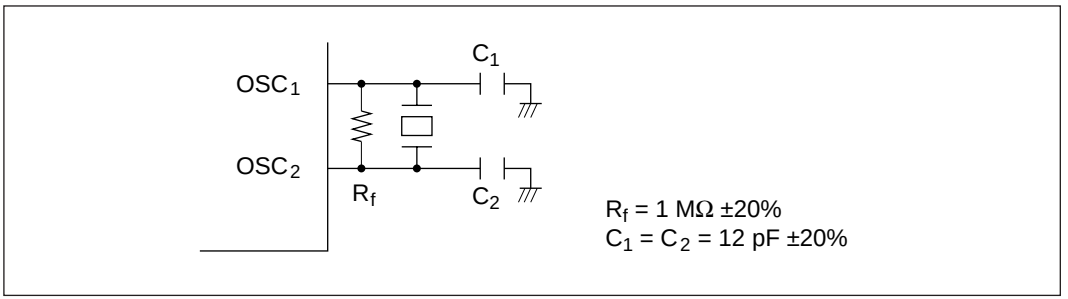


Figure 6-2 Typical Connection to Crystal Oscillator

- Crystal oscillator

  Figure 6-3 shows the equivalent circuit of the crystal oscillator. An oscillator having the characteristics given in table 6-1 should be used.

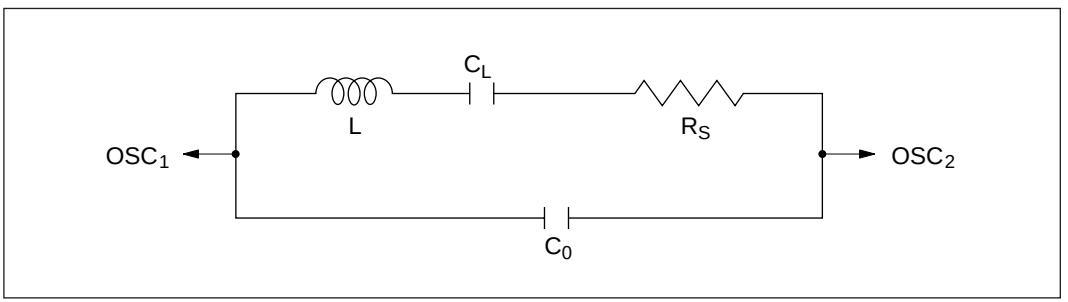


Figure 6-3 Equivalent Circuit of Crystal Oscillator

Table 6-1 Crystal Oscillator Parameters

	Frequency (MHz)		
	2	**4**	**8**
R_S max (Ω)	500	100	50
C_0 max (pF)	7	7	7

2. Connecting a ceramic oscillator

- Circuit configuration

Figure 6-4 shows a typical method of connecting a ceramic oscillator.

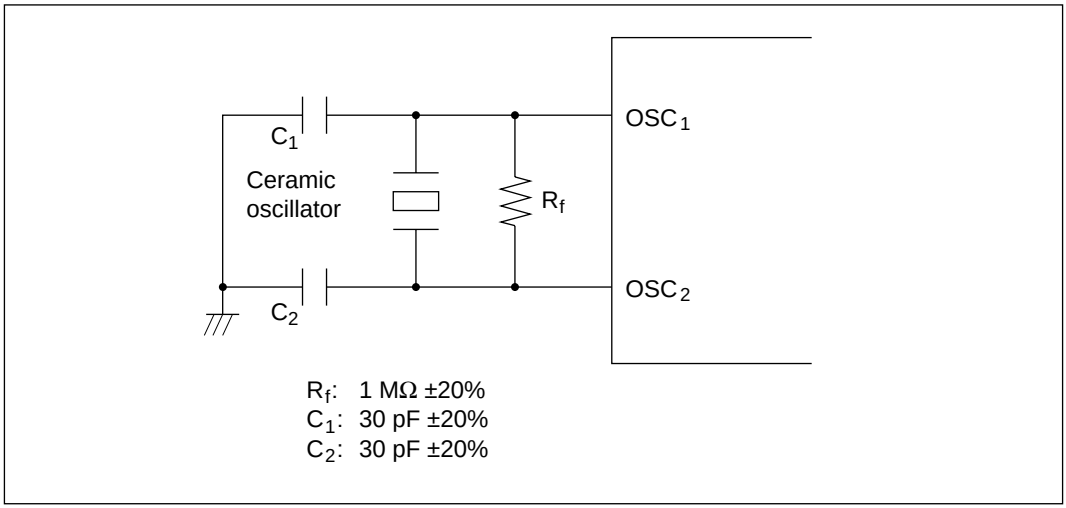


Figure 6-4 Typical Connection to Ceramic Oscillator

3. Notes on board design

When generating clock pulses by connecting a crystal or ceramic oscillator, pay careful attention to the following points.

Avoid running signal lines close to the oscillator circuit, since the oscillator may be adversely affected by induction currents. (See figure 6-5.)

The board should be designed so that the oscillator and load capacitors are located as close as possible to pins OSC_1 and OSC_2.

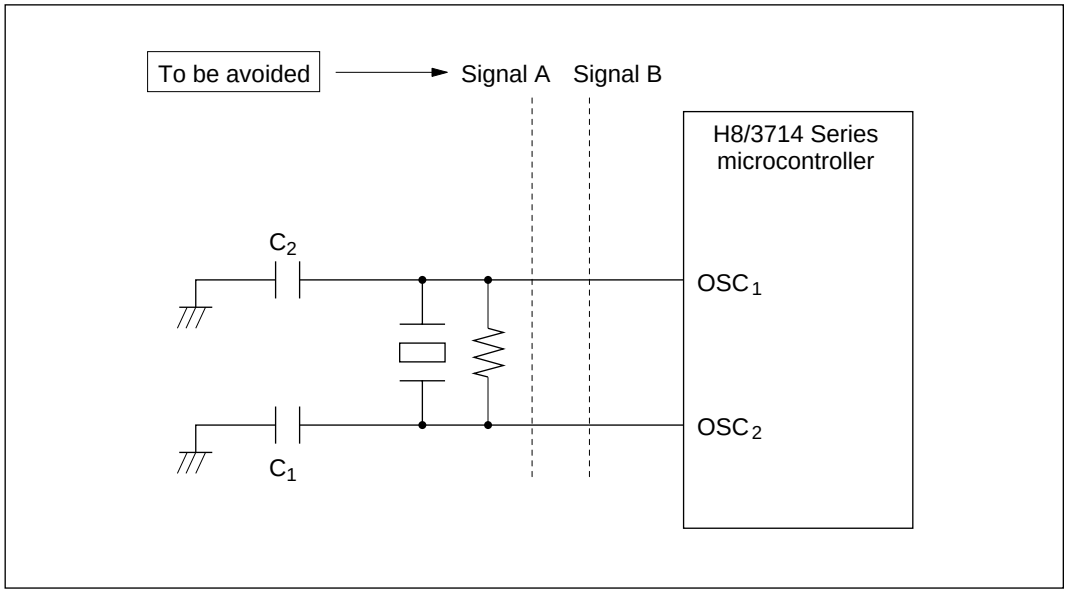


Figure 6-5 Board Design of Oscillator Circuit

4. External clock input

- Circuit configuration

  When an external clock is used, it is input at pin OSC_1. Pin OSC_2 should be left open. Figure 6-6 shows a typical connection.

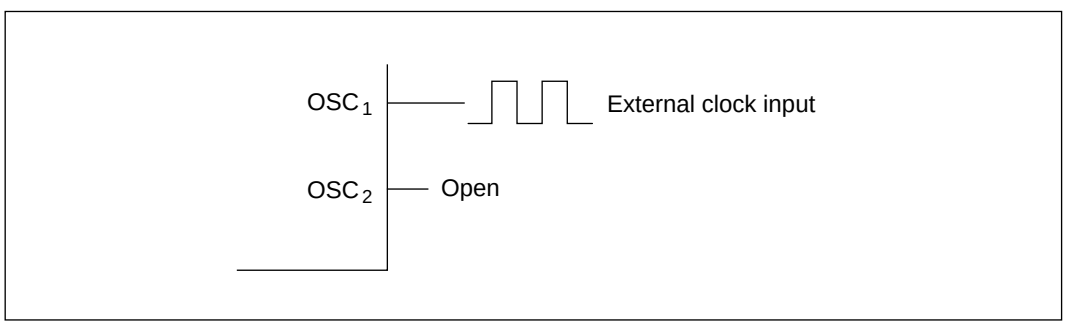


Figure 6-6 External Clock Input (Example)

- External clock

Frequency	Twice clock frequency (ϕ)
Duty cycle	45% to 55%

6.3 Subclock Generator

1. Connecting a 32.768 kHz crystal oscillator

   Clock pulses can be supplied to the subclock divider by connecting a 32.768 kHz crystal oscillator, as shown in figure 6-7. Follow the same precautions as noted for the system clock.

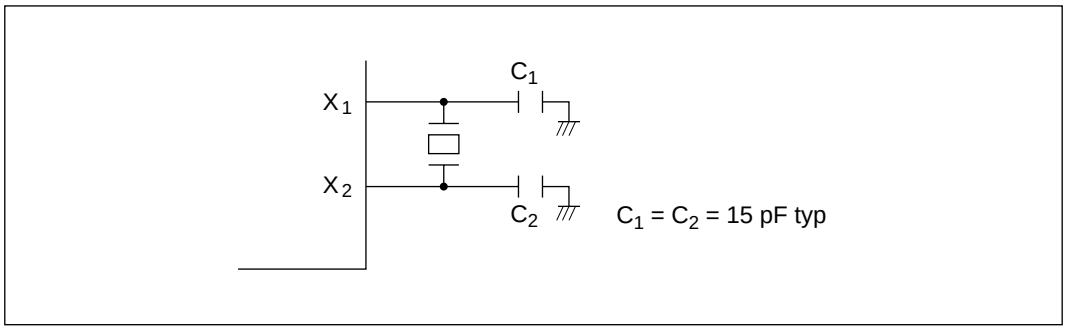


Figure 6-7 Typical Connection to Crystal Oscillator (Subclock)

Figure 6-8 shows the equivalent circuit of the crystal oscillator.

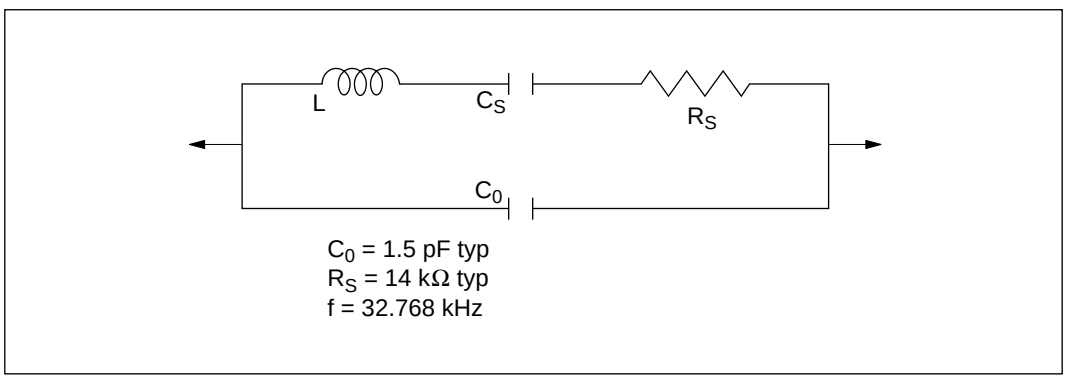


Figure 6-8 Equivalent Circuit of Crystal Oscillator

2. Pin connection when not using subclock

   When the subclock is not used, connect V_{CC} to pin X_1 and leave pin X_2 open, as shown in figure 6-9.

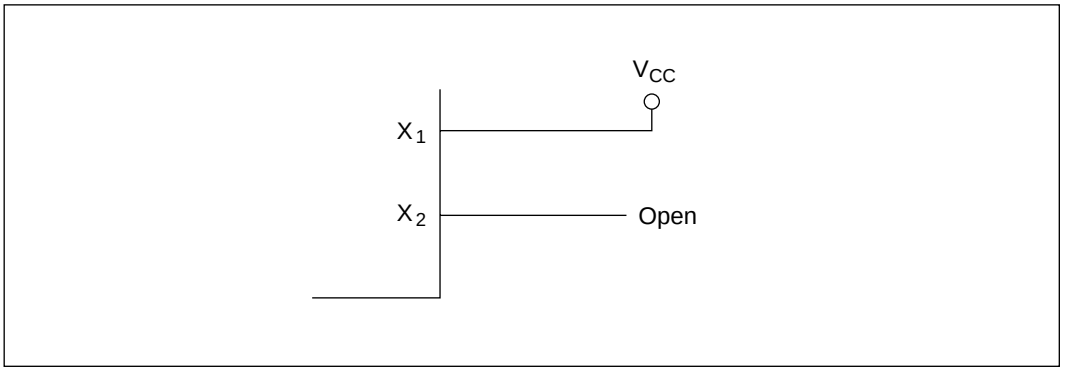


Figure 6-9 Pin Connection When Not Using Subclock

Section 7 I/O Ports

7.1 Overview

The H8/3714 Series has five 8-bit I/O ports (of which four are high-voltage ports), one 6-bit I/O port*, and one 8-bit input port. Table 7-1 indicates the functions of each port.

Ports 1 and 9 are standard input/output ports, consisting of a port control register (PCR) that controls input and output, and a port data register (PDR) for storing output data. Input or output can be assigned to individual bits.

Ports 4, 5, 6, and 7 are high-voltage ports, able to handle an applied voltage of V_{CC} – 40 V. Input and output are controlled for individual bits by reading from and writing to PDR.

Note: * Pin $P1_7$ of port 1 is a high-voltage input-only pin, while pin $P1_6$ is a standard input-only pin. Pins $P1_2$ and $P1_3$ are not present.

Reading a port gives the following results.

- Reading a standard port
  - — Reading a pin assigned to general-purpose input (PCR = 0) gives the pin level.
  - — Reading a pin assigned to general-purpose output (PCR = 1) gives the value of the corresponding PDR bit.
  - — Reading a pin assigned to an on-chip peripheral function gives the pin level.
- Reading a high-voltage port
  - — Reading a pin assigned to general-purpose input/output gives the pin level.
  - — Reading a pin assigned to digit output or segment output use gives the value of the corresponding PDR bit.

Table 1 Port Functions

Port	Description	Pins	Other Functions	Function Switching Register
Port 0	8-bit standard input port	$P0_7$ to $P0_0$/ AN_7 to AN_0	Analog data input channels 7 to 0	PMR0
Port 1	Pin $P1_7$: 1-bit high-voltage input port	$P1_7/V_{disp}$	Power supply for VFD driver	Mask option
	Pin $P1_6$: 1-bit standard input port	$P1_6/\overline{EVENT}$	Timer D event input	PMR1
	Pins $P1_5$, $P1_4$, $P1_1$, and $P1_0$: 4-bit standard I/O port	$P1_5/\overline{IRQ_5}$/ TMOE	External interrupt 5; Timer E output	PMR1 PMR4
		$P1_4/\overline{IRQ_4}$ $P1_1/\overline{IRQ_1}$ $P1_0/\overline{IRQ_0}$	External interrupts 4, 1, and 0	PMR1
Port 4	8-bit high-voltage I/O port	$P4_7$ to $P4_0$/ FS_{23} to FS_{16}	VFD segment pins 23 to 16	VFSR
Port 5	8-bit high-voltage I/O port	$P5_7$ to $P5_0$/ FS_{15} to FS_8	VFD segment pins 15 to 8	VFSR
Port 6	8-bit high-voltage I/O port	$P6_7$ to $P6_0$/ FD_7 to FD_0/ FS_0 to FS_7	VFD digit pins 7 to 0/segment pins 0 to 7	DBR VFSR VFDR
Port 7	8-bit high-voltage I/O port	$P7_7$ to $P7_0$/ FD_{15} to FD_8	VFD digit pins 15 to 8	VFDR
Port 9	8-bit standard I/O port	$P9_7$/UD	Timer C count-up/down selection	PMR2 PMR3
		$P9_6/SO_2$	Serial communication interface 2 data output	
		$P9_5/SI_2/\overline{CS}$	Serial communication interface 2 data input/chip select output	
		$P9_4/SCK_2$	Serial communication interface 2 clock I/O	
		$P9_3/SO_1$	Serial communication interface 1 data output	
		$P9_2/SI_1$	Serial communication interface 1 data input	
		$P9_1/SCK_1$	Serial communication interface 1 clock I/O	
		$P9_0$/PWM	14-bit PWM waveform output pin	

Note: Pins $P1_2$ and $P1_3$, and ports P2, P3, and P8 are not included in these versions.

7.1.1 Port Types and Mask Options

The choice of I/O pin options and the resulting states are shown in table 7-2.

Upon reset, the PDR, PCR, and PMR registers are initialized, cancelling the choices of peripheral functions. When the chip goes to a low-power mode, the on-chip peripheral function input gates are always on, so unless input levels are fixed there will be an increase in dissipated current.

Table 7-2 Choice of I/O Port Options

For Standard I/O Pins

Class	Pins	With MOS Pull-Up (type B)	No MOS Pull-Up (type C)
I/O pins	$P1_5$, $P1_4$, $P1_1$, $P1_0$, $P9_7$ to $P9_0$	With MOS pull-up	No MOS pull-up
Input-only pins	$P1_6$	With MOS pull-up	No MOS pull-up
On-chip peripheral function I/O pins	SCK_2, SCK_1 (output mode)*	With MOS pull-up	No MOS pull-up
On-chip peripheral function output pins	SO_2, SO_1, PWM, TMOE	With MOS pull-up	No MOS pull-up
On-chip peripheral function input pins	SCK_2, SCK_1 (input mode)* SI_2, SI_1, $\overline{IRQ_5}$, $\overline{IRQ_4}$, $\overline{IRQ_1}$, $\overline{IRQ_0}$ UD, $\overline{EVENT}$	With MOS pull-up	No MOS pull-up

Note: If external clock input mode is selected when the serial communication interface is used, pins SCK_2 and SCK_1 will be input-only pins.

For High-Voltage Pins

Class	Pins	No MOS Pull-Down (type D)	With MOS Pull-Down (type E)
I/O pins	$P4_7$ to $P4_0$, $P5_7$ to $P5_0$, $P6_7$ to $P6_0$, $P7_7$ to $P7_0$	No MOS pull-down	With MOS pull-down. Source of pull-down transistor connected to V_{disp} power supply.
Input-only pins	$P1_7$	No MOS pull-down	Connected to V_{disp} power supply.
On-chip peripheral function output pins	FS_{23} to FS_0, FD_{15} to FD_0	No MOS pull-down	With MOS pull-down. Source of pull-down transistor connected to V_{disp} power supply.

Table 7-3 shows the mask options with mask ROM versions. A mask ROM version is compatible with a ZTAT™ version only when C and D options are selected for all pins.

Table 7-3 Correspondence between Mask ROM and ZTAT™ Versions

Type	B	C	D	E
Mask ROM	Option	Option	Option	Option
ZTAT™	—	Fixed	Fixed	—

Notes

1. When circuit type E, "with MOS pull-down," is chosen, the source of the MOS pull-down is connected to the V_{disp} power supply. Accordingly, the mask option making pin $P1_7/V_{disp}$ a V_{disp} power supply pin must also be chosen.
2. Type C, "no MOS pull-up," is the only option available for port 0.

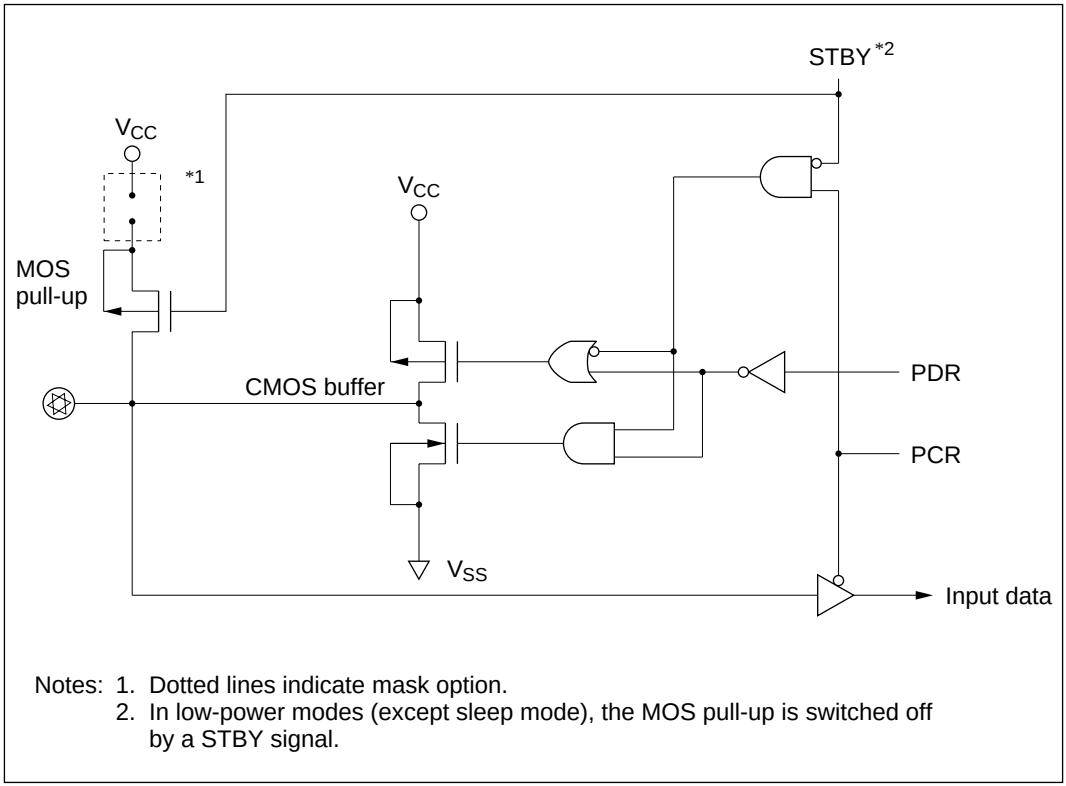
7.1.2 MOS Pull-Up

Ports 1* and 9, which are standard input/output ports, can be designated by mask options as having or not having MOS pull-up transistors for their (CMOS) outputs. (This does not apply to ZTAT™ versions.)

Figure 7-1 shows the MOS pull-up circuit configuration.

When "with MOS pull-up" is selected by mask option, the MOS pull-up will normally be on, regardless of the port data register (PDR) and port control register (PCR) settings.
(See table 7-4.)

Note: * Pin $P1_7/V_{disp}$ is a high-voltage pin, so the MOS pull-up option cannot be selected for this pin.



Notes: 1. Dotted lines indicate mask option.
2. In low-power modes (except sleep mode), the MOS pull-up is switched off by a STBY signal.

Figure 7-1 MOS Pull-Up Circuit Configuration

Table 7-4 MOS Pull-Up Control

Mask Option		With MOS Pull-Up (type B)				No MOS Pull-Up (type C)			
PCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	Off	Off	Off	On	Off	Off	Off	On
	NMOS	Off	Off	On	Off	Off	Off	On	Off
MOS pull-up		On	On	On	On	—	—	—	—

7.1.3 MOS Pull-Down

Ports 4, 5, 6, and 7, which are high-voltage I/O ports, can be designated by mask option as having or not having MOS pull-down resistors for their (PMOS open-drain) outputs. (This does not apply to ZTAT™ versions.)

Figure 7-2 shows the MOS pull-down circuit configuration.

When the "with MOS pull-down" option is chosen, the source of the MOS pull-down is connected to the V_{disp} power supply. Accordingly, the mask option making pin $P1_7/V_{disp}$ a V_{disp} power supply pin must also be chosen.

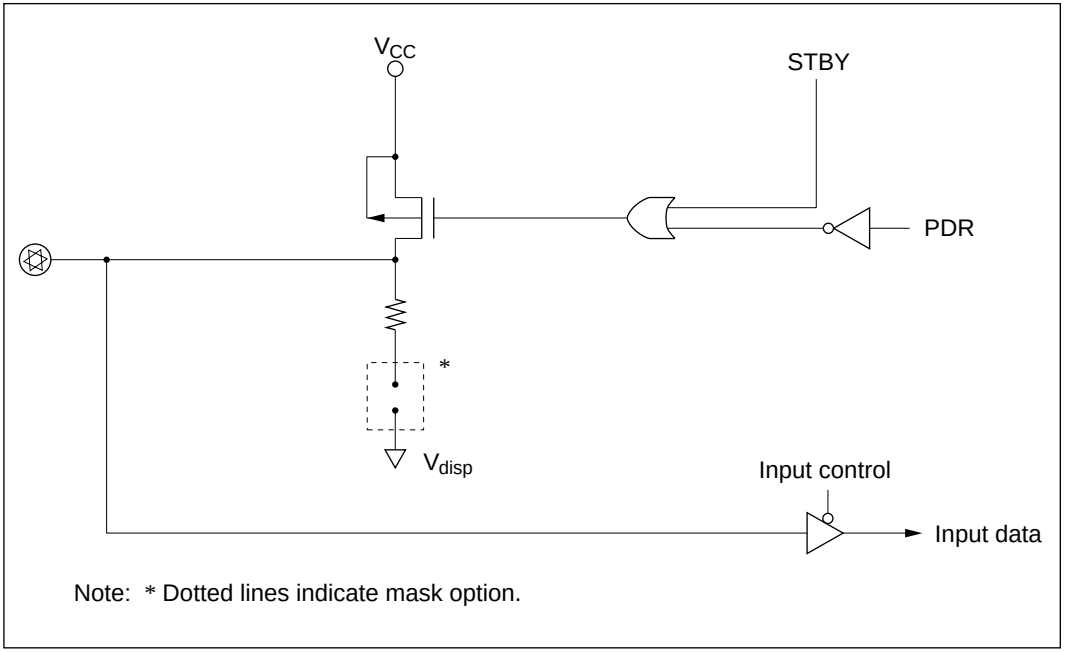


Figure 7-2 MOS Pull-Down Circuit Configuration

7.2 Port 0

7.2.1 Overview

Port 0 is an 8-bit standard input-only port. Figure 7-3 shows the pin configuration.

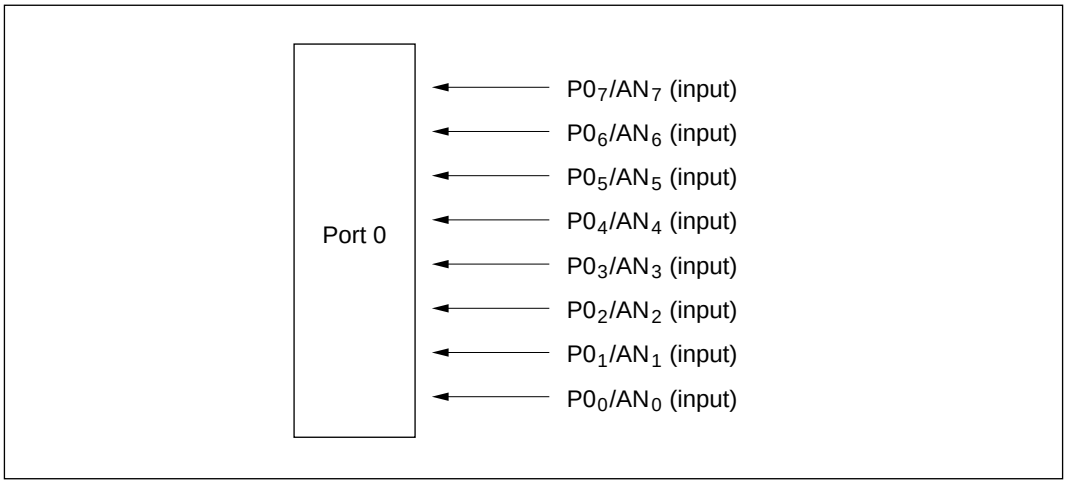


Figure 7-3 Port 0 Pin Configuration

7.2.2 Register Configuration and Description

Table 7-5 shows the port 0 register configuration.

Table 7-5 Port 0 Registers

Name	Abbrev.	R/W	Initial Value	Address
Port mode register 0	PMR0	W	H'00	H'FFEF
Port data register 0	PDR0	R	—	H'FFD0

1. Port mode register 0 (PMR0)

Bit	7	6	5	4	3	2	1	0
	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Each PMR0 bit designates whether the corresponding port 0 pin is to be used for general input or as an analog input channel to the A/D converter.

Upon reset, PMR0 is initialized to H'00.

Bit n ANn	Explanation	
0	Pin $P0_n/AN_n$ is used for general input.	(initial value)
1	Pin $P0_n/AN_n$ is an analog input channel.	

(n = 0 to 7)

2. Port data register 0 (PDR0)

Bit	7	6	5	4	3	2	1	0
	$PDR0_7$	$PDR0_6$	$PDR0_5$	$PDR0_4$	$PDR0_3$	$PDR0_2$	$PDR0_1$	$PDR0_0$
Initial value	—	—	—	—	—	—	—	—
Read/Write	R	R	R	R	R	R	R	R

When the corresponding bit in PMR0 is 0, the pin state can be read from PDR0. If the corresponding PMR0 bit is 1, PDR0 is read as 1.

7.2.3 Pin Functions

Table 7-6 gives the port 0 pin functions.

Table 7-6 Port 0 Pin Functions

Pin	Pin Functions and Selection Method
$P0_7/AN_7$ to $P0_0/AN_0$	Functions are switched as follows by means of bits AN_7 to AN_0 in PMR0.

AN_n	0	1
Pin function	$P0_n$ input pin	AN_n input pin

7.2.4 Pin States

Table 7-7 shows the port 0 pin states in each operating mode.

Table 7-7 Port 0 Pin States

Pins	Reset	Sleep	Standby	Watch	Subactive	Active
$P0_7/AN_7$ to $P0_0/AN_0$	High impedance	Previous state retained	High impedance	High impedance	High impedance	Normal operation

7.3 Port 1

7.3.1 Overview

Port 1 consists of four standard I/O pins, one standard input-only pin, and one high-voltage input-only pin. Figure 7-4 shows the pin configuration.

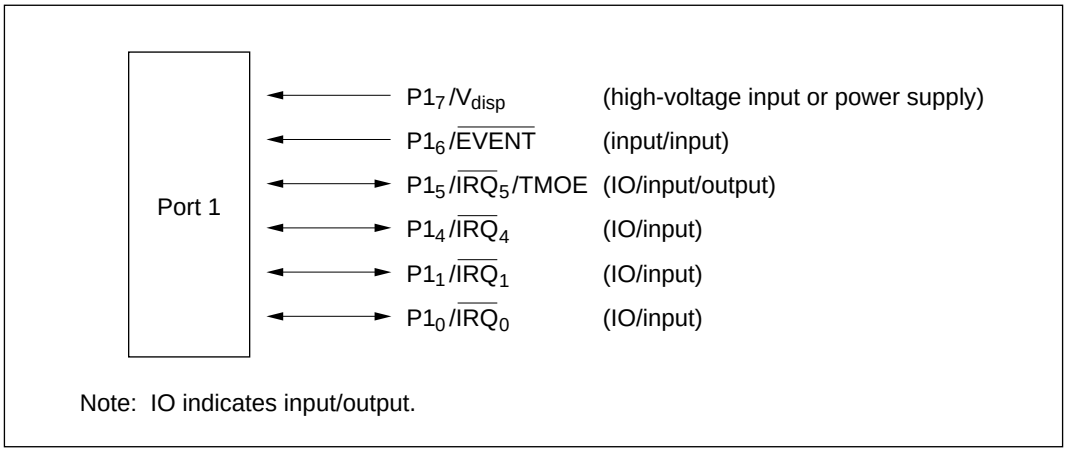


Figure 7-4 Port 1 Pin Configuration

7.3.2 Register Configuration and Description

Table 7-8 shows the port 1 register configuration.

Table 7-8 Port 1 Registers

Name	Abbrev.	R/W	Initial Value	Address
Port mode register 1	PMR1	R/W	H'0C	H'FFEB
Port control register 1	PCR1	W	H'CC	H'FFE1
Port data register 1	PDR1	R/W	Not fixed	H'FFD1
Port mode register 4	PMR4	R/W	H'0F	H'FFEE

1. Port mode register 1 (PMR1)

Bit	7	6	5	4	3	2	1	0
	NOISE CANCEL	EVENT	IRQC5	IRQC4	—	—	IRQC1	IRQC0
Initial value	0	0	0	0	1	1	0	0
Read/Write	R/W	R/W	R/W	R/W	—	—	R/W	R/W

PMR1 is an 8-bit read/write register that controls the selection of pin functions for pins $P1_6/\overline{EVENT}$, $P1_5/\overline{IRQ_5}$, $P1_4/\overline{IRQ_4}$, $P1_1/\overline{IRQ_1}$, and $P1_0/\overline{IRQ_0}$, and turns the $\overline{IRQ_0}$ noise cancellation function on and off.

Upon reset, PMR1 is initialized to H'0C.

Note: Before switching pin functions using bits IRQ5 to IRQ0 in PMR1, first disable the corresponding interrupts by clearing their interrupt enable bits. After the pin functions have been switched, issue any instruction, then clear the interrupt request flags to 0. For details see section 3.2.3 1, Port mode register (PMR1).

Bit 7: Noise cancel (NOISE CANCEL)

This bit turns the $\overline{IRQ_0}$ noise canceller function on and off. In standby, watch, and subactive modes the noise canceller function is off regardless of the setting of this bit.

Bit 7 NOISE CANCEL	Explanation	
0	Noise canceller function is off.	(initial value)
1	Noise canceller function is on. Input is sampled at intervals of 256 states. If two consecutive input values do not match, noise is assumed.	

Bit 6: $P1_6/\overline{EVENT}$ pin function switch (EVENT)

This bit selects whether pin $P1_6/\overline{EVENT}$ is used as $P1_6$ or as $\overline{EVENT}$.

Bit 6 EVENT	Explanation	
0	$P1_6/\overline{EVENT}$ pin functions as $P1_6$.*	(initial value)
1	$P1_6/\overline{EVENT}$ pin functions as $\overline{EVENT}$ (timer D event input).	

Note: * Even when pin $P1_6/\overline{EVENT}$ is used as $P1_6$, the timer D counter may increment when pin $P1_6$ is read. If timer D is used the counter must be cleared by means of the CLR bit in timer mode register D (TMD).

Bit 5: $P1_5/\overline{IRQ_5}$/TMOE pin function switch (IRQC5)

This bit selects whether pin $P1_5/\overline{IRQ_5}$/TMOE is used as $P1_5/\overline{TMOE}$ or as $\overline{IRQ_5}$.

Bit 5 IRQC5	Explanation	
0	$P1_5/\overline{IRQ_5}$/TMOE pin functions as $P1_5$/TMOE.	(initial value)
1	$P1_5/\overline{IRQ_5}$/TMOE pin functions for $\overline{IRQ_5}$ input.	

Bit 4: $P1_4/\overline{IRQ_4}$ pin function switch (IRQC4)

This bit selects whether pin $P1_4/\overline{IRQ_4}$ is used as $P1_4$ or as $\overline{IRQ_4}$.

Bit 4 IRQC4	Explanation	
0	$P1_4/\overline{IRQ_4}$ pin functions as $P1_4$.	(initial value)
1	$P1_4/\overline{IRQ_4}$ pin functions for $\overline{IRQ_4}$* input.	

Note: * Rising or falling edge sensing can be designated for pin $\overline{IRQ_4}$.
For details see 3.2.3 (2), IRQ edge select register (IEGR).

Bits 3 and 2: Reserved bits

Bits 3 and 2 are reserved; they always read 1, and cannot be modified.

Bit 1: $P1_1/\overline{IRQ_1}$ pin function switch (IRQC1)

This bit selects whether pin $P1_1/\overline{IRQ_1}$ is used as $P1_1$ or as $\overline{IRQ_1}$.

Bit 1 IRQC1	Explanation	
0	$P1_1/\overline{IRQ_1}$ pin functions as $P1_1$.	(initial value)
1	$P1_1/\overline{IRQ_1}$ pin functions for $\overline{IRQ_1}$* input.	

Note: * Rising or falling edge sensing can be designated for pin $\overline{IRQ_1}$.
For details see 3.2.3 (2), IRQ edge select register (IEGR).

Bit 0: $P1_0/\overline{IRQ_0}$ pin function switch (IRQC0)

This bit selects whether pin $P1_0/\overline{IRQ_0}$ is used as $P1_0$ or as $\overline{IRQ_0}$.

Bit 0 IRQC0	Explanation	
0	$P1_0/\overline{IRQ_0}$ pin functions as $P1_0$.	(initial value)
1	$P1_0/\overline{IRQ_0}$ pin functions for $\overline{IRQ_0}$* input.	

Note: * Rising or falling edge sensing can be designated for pin $\overline{IRQ_0}$.
For details see 3.2.3 (2), IRQ edge select register (IEGR).

2. Port control register 1 (PCR1)

Bit	7	6	5	4	3	2	1	0
	—	—	$PCR1_5$	$PCR1_4$	—	—	$PCR1_1$	$PCR1_0$
Initial value	1	1	0	0	1	1	0	0
Read/Write	—	—	W	W	—	—	W	W

PCR1 is an 8-bit register for controlling whether each of port 1 pins $P1_5$, $P1_4$, $P1_1$, and $P1_0$ functions as an input pin or output pin. Setting a PCR1 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. Bits 7, 6, 3, and 2 are reserved bits that cannot be modified and always read 1.

The settings in PCR1 and in PDR1 are valid when the affected pin is designated in PMR1 as a general I/O pin.

Upon reset, PCR1 is initialized to H'CC.

3. Port data register 1 (PDR1)

Bit	7	6	5	4	3	2	1	0
	—	—	$PDR1_5$	$PDR1_4$	—	—	$PDR1_1$	$PDR1_0$
Initial value	— *	— *	0	0	1	1	0	0
Read/Write	—	—	R/W	R/W	—	—	R/W	R/W

Note: * Pins $P1_7$ and $P1_6$ are for input only; reading PDR1 always gives the level of these pins.

PDR1 is an 8-bit register that stores data for pins $P1_5$, $P1_4$, $P1_1$, and $P1_0$. If port 1 is read while PCR1 bits are set to 1, the values stored in PDR1 are read, regardless of the actual pin states. If port 1 is read while PCR1 bits are cleared to 0, the pin states are read. Bits 3 and 2 are reserved bits that cannot be modified and always read 1.

4. Port mode register 4 (PMR4)

Bit	7	6	5	4	3	2	1	0
	TEO	TEO ON	FREQ	VRFR	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

PMR4 is an 8-bit read/write register that switches the $P1_5/\overline{IRQ_5}$/TMOE pin function and controls TMOE pin waveform output. Bits 3 to 0 are reserved; they always read 1, and cannot be modified.

Upon reset, PMR4 is initialized to H'0F.

Bit 7: Timer E output select (TEO)
Bit 6: Timer E output on/off (TEO ON)
Bit 5: Fixed frequency select (FREQ)
Bit 4: Variable frequency select (VRFR)

$P1_5/\overline{IRQ_5}$/TMOE pin functions are switched as follows, by means of bits 7 to 4 of PMR4 and bit IRQC5 of PMR1.

PMR1	**PMR4**				**Description**	
Bit 5 IRQC5	**Bit 7 TEO**	**Bit 6 TEO ON**	**Bit 5 FREQ**	**Bit 4 VRFR**	**Pin Function**	**Pin State**
0	0	0	0	0	$P1_5$ pin	Standard I/O port (initial value)
0	0	*	*	*	$P1_5$ pin	Standard I/O port
0	1	0	*	*	TMOE output pin (off)	Low level output
0	1	1	0	0	TMOE output pin (on)	Fixed frequency output: (ϕ/2048) 1.95 kHz (ϕ = 4 MHz) 0.98 kHz (ϕ = 2 MHz)
0	1	1	1	0	TMOE output pin (on)	Fixed frequency output: (ϕ/1024) 3.9 kHz (ϕ = 4 MHz) 1.95 kHz (ϕ = 2 MHz)
0	1	1	*	1	TMOE output pin (on)	Variable frequency output: toggled by timer E overflow
1	*	*	*	*	$\overline{IRQ_5}$ input pin	External interrupt input

Note: * Don't care

7.3.3 Pin Functions

Table 7-9 shows the port 1 pin functions.

Table 7-9 Port 1 Pin Functions

Pin	Pin Functions and Selection Method
$P1_7/V_{disp}$	Selected by mask option

$P1_7$ high-voltage input pin	Power supply for VFD driving (V_{disp})

$P1_6/\overline{EVENT}$	Function is switched as follows by EVENT bit in PMR1

EVENT	0	1
Pin function	$P1_6$ input pin	$\overline{EVENT}$ input pin*

Note: Timer D event input

$P1_5/\overline{IRQ_5}$/TMOE, $P1_4/\overline{IRQ_4}$, $P1_1/\overline{IRQ_1}$, $P1_0/\overline{IRQ_0}$	Function is switched as follows by bits IRQC5, IRQC4, IRQC1, and IRQC0* in PMR1 and bit n in PCR1

PMR1	0		1
$PCR1_n$	0	1	—
Pin function	$P1_n$ input pin	$P1_n$ output pin	$\overline{IRQ_n}$ input pin

Notes: 1. Before switching pin functions using bits IRQC5, IRQC4, IRQC1, and IRQC0 in PMR1, first disable the corresponding interrupts by clearing their interrupt enable bits. After the pin functions have been switched, issue any instruction, then clear the interrupt request flags to 0. For details see section 3.2.3 (1), Port mode register (PMR1).

2. Before entering power-down mode, pins set to external interrupt input by bits IRQC5, IRQC4, IRQC1, and IRQC0 in PMR1, should be kept from floating by external connection, or should be switched to general I/O in PMR1 prior to the state transition.

3. For details on the TMOE function, refer to section 7.3.2 (4), Port mode register 4 (PMR4). $\overline{IRQ_4}$, $\overline{IRQ_1}$, and $\overline{IRQ_0}$ input can be set for either rising edge or falling edge detection by register IEGR. For details, refer to section 3.2.3 (2), IRQ edge select register (IEGR). $\overline{IRQ_0}$ and $\overline{IRQ_1}$ can be used as event input pins for timer B and timer C, respectively. For details, refer to section 8, Timers.

7.3.4 Pin States

Table 7-10 shows the port 1 pin states in each operating mode.

Table 7-10 Port 1 Pin States

Pins	Reset	Sleep	Standby	Watch	Subactive	Active
$P1_7/V_{disp}$	High impedance or V_{disp}	High impedance or V_{disp}	High impedance or V_{disp}	High impedance or V_{disp}	High impedance or V_{disp}	Normal operation or V_{disp}
$P1_6/\overline{EVENT}$, $P1_5/\overline{IRQ_5}$/TMOE, $P1_4/\overline{IRQ_4}$, $P1_1/\overline{IRQ_1}$, $P1_0/\overline{IRQ_0}$	High impedance or pulled up	Previous state retained	High impedance	High impedance	High impedance	Normal operation

7.4 Port 4

7.4.1 Overview

Port 4 is an 8-bit high-voltage I/O port. Figure 7-5 shows the pin configuration.

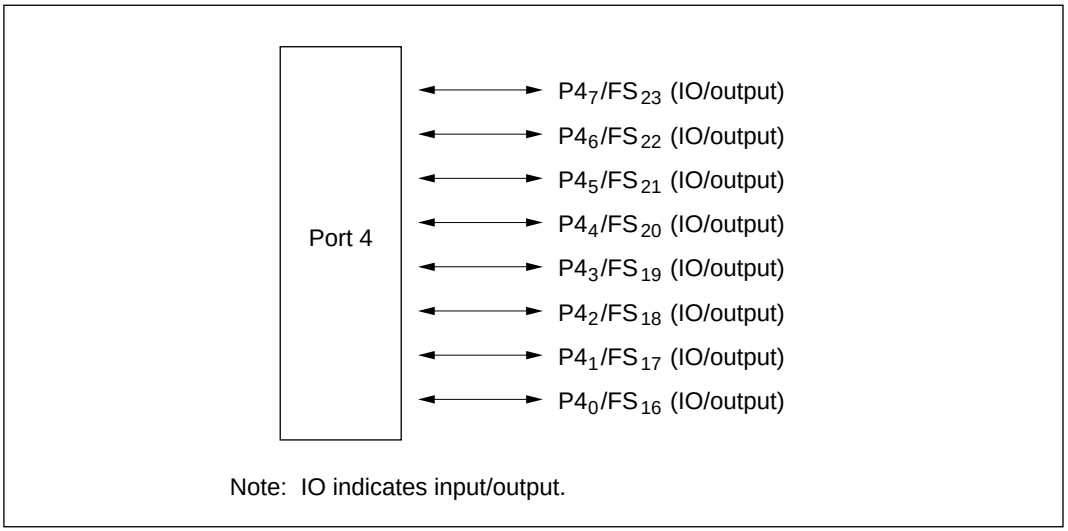


Figure 7-5 Port 4 Pin Configuration

7.4.2 Register Configuration and Description

Table 7-11 shows the port 4 register configuration.

Table 7-11 Port 4 Registers

Name	Abbrev.	R/W	Initial Value	Address
Port data register 4	PDR4	R/W	H'00	H'FFD4

1. Port data register 4 (PDR4)

Bit	7	6	5	4	3	2	1	0
	PDR4$_7$	PDR4$_6$	PDR4$_5$	PDR4$_4$	PDR4$_3$	PDR4$_2$	PDR4$_1$	PDR4$_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR4 is an 8-bit register for storing the data of port 4 pins P4$_7$ to P4$_0$.

Upon reset, PDR4 is initialized to H'00.

7.4.3 Pin Functions

Table 7-12 shows the port 4 pin functions.

Table 7-12 Port 4 Pin Functions

Pin	Pin Functions and Selection Method
$P4_7/FS_{23}$ to $P4_0/FS_{16}$	After designation of the segment pins to be used in bits SR4 to SR0 of the VFD segment control register (VFSR), bit VFDE in the digit beginning register (DBR) is set to 1 and VFD controller/driver operation is started. During key scan intervals, pins designated for segment output can be used by the CPU as general-purpose ports. Even while the VFD controller/driver is operating, it is possible to switch segment pins to general-purpose ports by writing 0 in the VFLAG bit of VFSR.

VFLAG	0	1
Pin function	Pins $P4_7$ to $P4_0$ are all general-purpose I/O pins.	Pins designated by bits SR4 to SR0 are segment output pins.* Other pins are for general I/O.

Note: * When a pin functioning as a segment output pin is read, the value of the corresponding bit in PDR4 is read.

7.4.4 Pin States

Table 7-13 shows the port 4 pin states in each operating mode.

Table 7-13 Port 4 Pin States

Pins	Reset	Sleep	Standby	Watch	Subactive	Active
$P4_7/FS_{23}$ to $P4_0/FS_{16}$	High impedance or pulled down	Previous state retained	High impedance or pulled down	High impedance or pulled down	High impedance or pulled down	Normal operation

7.5 Port 5

7.5.1 Overview

Port 5 is an 8-bit high-voltage I/O port. Figure 7-6 shows the pin configuration.

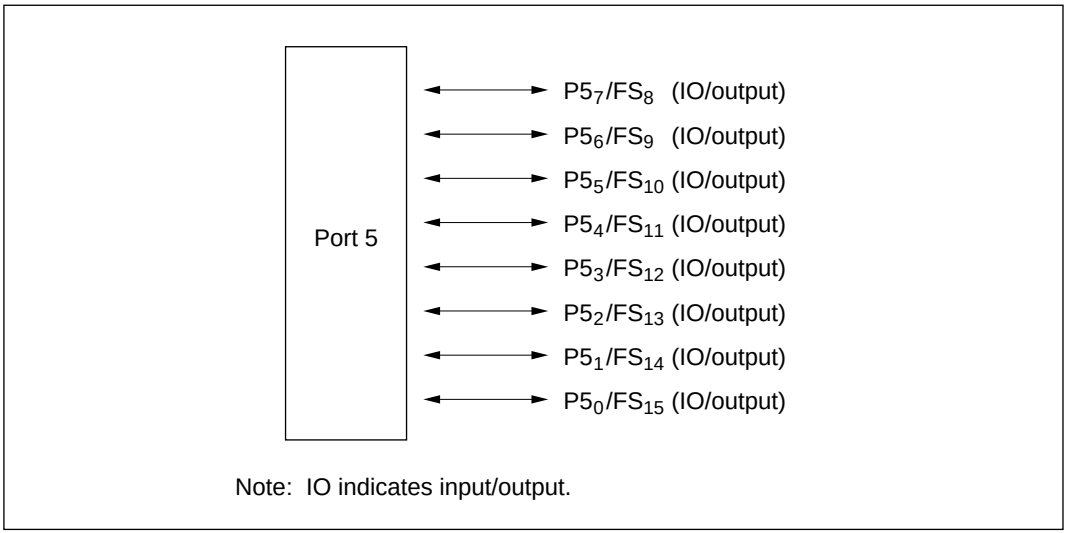


Figure 7-6 Port 5 Pin Configuration

7.5.2 Register Configuration and Description

Table 7-14 shows the port 5 register configuration.

Table 7-14 Port 5 Registers

Name	Abbrev.	R/W	Initial Value	Address
Port data register 5	PDR5	R/W	H'00	H'FFD5

1. Port data register 5 (PDR5)

Bit	7	6	5	4	3	2	1	0
	PDR5$_7$	PDR5$_6$	PDR5$_5$	PDR5$_4$	PDR5$_3$	PDR5$_2$	PDR5$_1$	PDR5$_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR5 is an 8-bit register for storing the data of port 5 pins P5$_7$ to P5$_0$.

Upon reset, PDR5 is initialized to H'00.

7.5.3 Pin Functions

Table 7-15 shows the port 5 pin functions.

Table 7-15 Port 5 Pin Functions

Pin	Pin Functions and Selection Method
$P5_7/FS_8$ to $P5_0/FS_{15}$	After designation of the segment pins to be used in bits SR4 to SR0 of the VFD segment control register (VFSR), bit VFDE in the digit beginning register (DBR) is set to 1 and VFD controller/driver operation is started. During key scan intervals, pins designated for segment output can be used by the CPU as general-purpose ports. Even while the VFD controller/driver is operating, it is possible to switch segment pins to general-purpose ports by writing 0 in the VFLAG bit of VFSR.

VFLAG	0	1
Pin function	Pins $P5_7$ to $P5_0$ are all general-purpose I/O pins.	Pins designated by bits SR4 to SR0 are segment output pins.* Other pins are for general I/O.

Note: * When a pin functioning as a segment output pin is read, the value of the corresponding bit in PDR5 is read.

7.5.4 Pin States

Table 7-16 shows the port 5 pin states in each operating mode.

Table 7-16 Port 5 Pin States

Pins	Reset	Sleep	Standby	Watch	Subactive	Active
$P5_7/FS_8$ to $P5_0/FS_{15}$	High impedance or pulled down	Previous state retained	High impedance or pulled down	High impedance or pulled down	High impedance or pulled down	Normal operation

7.6 Port 6

7.6.1 Overview

Port 6 is an 8-bit high-voltage I/O port. Figure 7-7 shows the pin configuration.

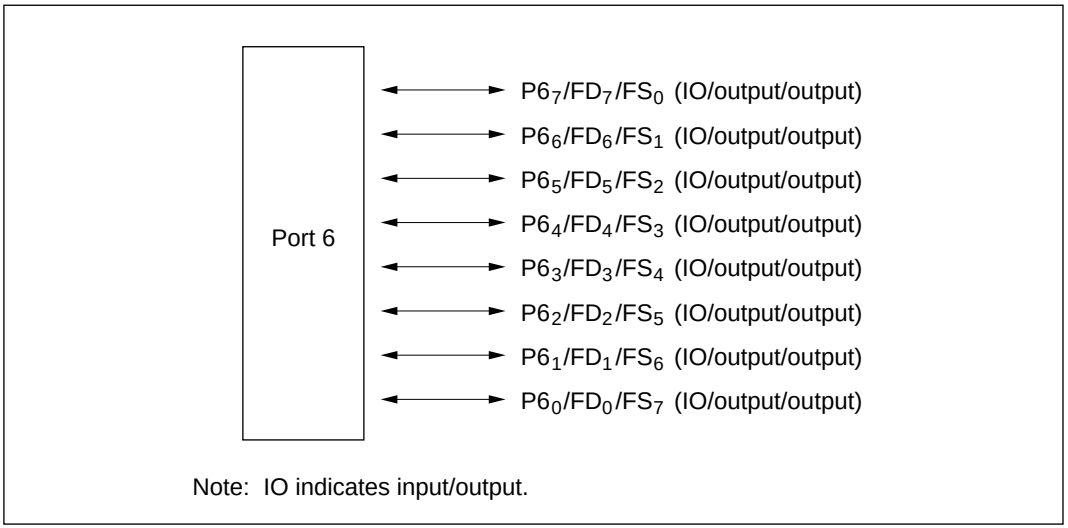


Figure 7-7 Port 6 Pin Configuration

7.6.2 Register Configuration and Description

Table 7-17 shows the port 6 register configuration.

Table 7-17 Port 6 Registers

Name	Abbrev.	R/W	Initial Value	Address
Port data register 6	PDR6	R/W	H'00	H'FFD6

1. Port data register 6 (PDR6)

Bit	7	6	5	4	3	2	1	0
	PDR6$_7$	PDR6$_6$	PDR6$_5$	PDR6$_4$	PDR6$_3$	PDR6$_2$	PDR6$_1$	PDR6$_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR6 is an 8-bit register for storing the data of port 6 pins P6$_7$ to P6$_0$.

Upon reset, PDR6 is initialized to H'00.

7.6.3 Pin Functions

Table 7-18 shows the port 6 pin functions.

Table 7-18 Port 6 Pin Functions

Pin	Pin Functions and Selection Method
$P6_7/FD_7/FS_0$ to $P6_0/FD_0/FS_7$	After designation of the digit pins and segment pins to be used in bits DR3 to DR0 of the VFD digit control register (VFDR), bits SR4 to SR0 of the VFD segment control register (VFSR), and bits DBR3 to DBR0 of the digit beginning register (DBR), bit VFDE in DBR is set to 1 and VFD controller/driver operation is started. During key scan intervals, pins designated for digit or segment output can be used by the CPU as general-purpose ports. Even while the VFD controller/driver is operating, it is possible to switch digit pins or segment pins to general-purpose ports by writing 0 in the VFLAG bit of VFSR.

VFLAG	0	1
Pin function	Pins $P6_7$ to $P6_0$ are all general-purpose I/O pins.	Pins are designated as digit output pins,* segment output pins,* or general I/O pins by bits DR3 to DR0, SR4 to SR0, and DBR3 to DBR0.

Note: * When a pin functioning as a digit output pin or segment output pin is read, the value of the corresponding bit in PDR6 is read.

7.6.4 Pin States

Table 7-19 shows the port 6 pin states in each operating mode.

Table 7-19 Port 6 Pin States

Pins	Reset	Sleep	Standby	Watch	Subactive	Active
$P6_7/FD_7/FS_0$ to $P6_0/FD_0/FS_7$	High impedance or pulled down	Previous state retained	High impedance or pulled down	High impedance or pulled down	High impedance or pulled down	Normal operation

7.7 Port 7

7.7.1 Overview

Port 7 is an 8-bit high-voltage I/O port. Figure 7-8 shows the pin configuration.

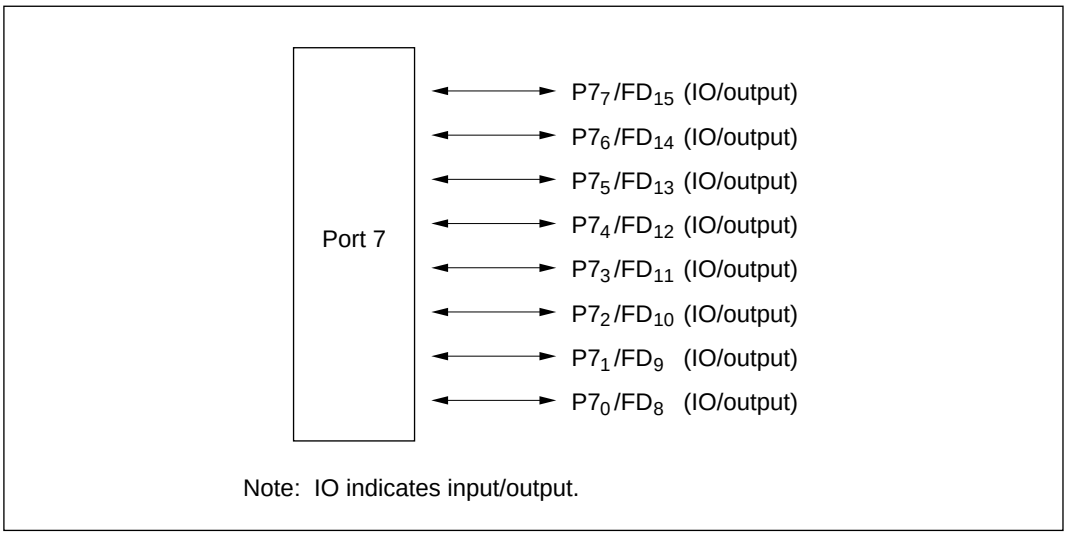


Figure 7-8 Port 7 Pin Configuration

7.7.2 Register Configuration and Description

Table 7-20 shows the port 7 register configuration.

Table 7-20 Port 7 Registers

Name	Abbrev.	R/W	Initial Value	Address
Port data register 7	PDR7	R/W	H'00	H'FFD7

1. Port data register 7 (PDR7)

Bit	7	6	5	4	3	2	1	0
	PDR7$_7$	PDR7$_6$	PDR7$_5$	PDR7$_4$	PDR7$_3$	PDR7$_2$	PDR7$_1$	PDR7$_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR7 is an 8-bit register for storing the data of port 7 pins P7$_7$ to P7$_0$.

Upon reset, PDR7 is initialized to H'00.

7.7.3 Pin Functions

Table 7-21 shows the port 7 pin functions.

Table 7-21 Port 7 Pin Functions

Pin	Pin Functions and Selection Method
$P7_7/FD_{15}$ to $P7_0/FD_8$	After designation of the digit pins to be used, in bits DR3 to DR0 of the VFD digit control register (VFDR), bit VFDE in the digit beginning register (DBR) is set to 1 and VFD controller/driver operation is started. Even while the VFD controller/driver is operating, it is possible to switch digit pins to general-purpose ports by writing 0 in the VFLAG bit of VFSR.

VFLAG	0	1
Pin function	Pins $P7_7$ to $P7_0$ are all general-purpose I/O pins.	Pins designated by bits DR3 to DR0 are digit output pins.* Other pins are for general I/O.

Note: * When a pin functioning as a digit output pin is read, the value of the corresponding bit in PDR7 is read.

7.7.4 Pin States

Table 7-22 shows the port 7 pin states in each operating mode.

Table 7-22 Port 7 Pin States

Pins	Reset	Sleep	Standby	Watch	Subactive	Active
$P7_7/FD_{15}$ to $P7_0/FD_8$	High impedance or pulled down	Previous state retained	High impedance or pulled down	High impedance or pulled down	High impedance or pulled down	Normal operation

7.8 Port 9

7.8.1 Overview

Port 9 is an 8-bit standard I/O port. Figure 7-9 shows the pin configuration.

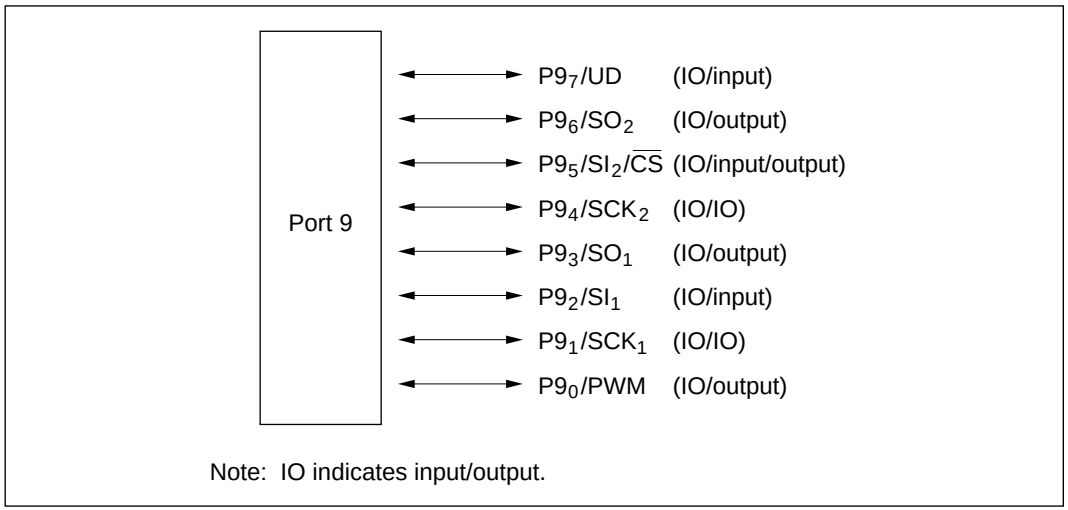


Figure 7-9 Port 9 Pin Configuration

7.8.2 Register Configuration and Description

Table 7-23 shows the port 9 register configuration.

Table 7-23 Port 9 Registers

Name	Abbrev.	R/W	Initial Value	Address
Port mode register 2	PMR2	R/W	H'00	H'FFEC
Port control register 9	PCR9	W	H'00	H'FFE9
Port data register 9	PDR9	R/W	H'00	H'FFD9

1. Port mode register 2 (PMR2)

Bit	7	6	5	4	3	2	1	0
	UP/ DOWN	SO2	SI2	SCK2	SO1	SI1	SCK1	PWM
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PMR2 is an 8-bit read/write register, controlling the selection of port 9 pin functions.

Upon reset, PMR2 is initialized to H'00.

Bit 7: $P9_7$/UD pin function switch (UP/DOWN)

This bit selects whether pin $P9_7$/UD is used for general-purpose I/O or for timer C up/down control input. Up/down control input (UD) is valid only when bit TMC6 = 1 in timer mode register C (TMC).

Bit 7 UP/DOWN	Description	
0	$P9_7$/UD pin functions for $P9_7$ input/output.	(initial value)
1	$P9_7$/UD pin functions for UD input. If bit TMC6 in TMC is set to 1, then when the UD input is high, timer C counts down, and when UD is low, timer C counts up.	

Bit 6: $P9_6/SO_2$ pin function switch (SO2)

This bit selects whether pin $P9_6/SO_2$ functions as the $P9_6$ I/O pin or the SO_2 output pin.

Bit 6 SO2	Description	
0	$P9_6/SO_2$ pin functions for $P9_6$ input/output.	(initial value)
1	$P9_6/SO_2$ pin functions for SO_2 output.	

Bit 5: $P9_5/SI_2/\overline{CS}$ pin function switch (SI2)

This bit selects whether pin $P9_5/SI_2/\overline{CS}$ functions as the $P9_5$ I/O pin or the SI_2 input/$\overline{CS}$ output pin. For the switching between SI_2 input and $\overline{CS}$ output see 11.2.5, Port Mode Register 3 (PMR3).

Bit 5 SI2	Description	
0	$P9_5/SI_2/\overline{CS}$ pin functions for $P9_5$ input/output.	(initial value)
1	$P9_5/SI_2/\overline{CS}$ pin functions for SI_2 input or $\overline{CS}$ output.	

Bit 4: $P9_4/SCK_2$ pin function switch (SCK2)

This bit selects whether pin $P9_4/SCK_2$ functions as the $P9_4$ I/O pin or the SCK_2 I/O pin.

Bit 4 SCK2	Description	
0	$P9_4/SCK_2$ pin functions for $P9_4$ input/output.	(initial value)
1	$P9_4/SCK_2$ pin functions for SCK_2 input/output. The clock input/output direction and the divider ratio are set in serial mode register 2 (SMR2).	

Bit 3: $P9_3/SO_1$ pin function switch (SO1)

This bit selects whether pin $P9_3/SO_1$ functions as the $P9_3$ I/O pin or the SO_1 output pin.

Bit 3 SO1	Description	
0	$P9_3/SO_1$ pin functions for $P9_3$ input/output.	(initial value)
1	$P9_3/SO_1$ pin functions for SO_1 output.	

Bit 2: $P9_2/SI_1$ pin function switch (SI1)

This bit selects whether pin $P9_2/SI_1$ functions as the $P9_2$ I/O pin or the SI_1 input pin.

Bit 2 SI1	Description	
0	$P9_2/SI_1$ pin functions for $P9_2$ input/output.	(initial value)
1	$P9_2/SI_1$ pin functions for SI_1 input.	

Bit 1: $P9_1/SCK_1$ pin function switch (SCK1)

This bit selects whether pin $P9_1/SCK_1$ functions as the $P9_4$ I/O pin or the SCK_1 I/O pin.

Bit 1 SCK1	Description	
0	$P9_1/SCK_1$ pin functions for $P9_1$ input/output.	(initial value)
1	$P9_1/SCK_1$ pin functions for SCK_1 input/output. The clock input/output direction and the divider ratio are set in serial mode register 1 (SMR1).	

Bit 0: $P9_0$/PWM pin function switch (PWM)

This bit selects whether pin $P9_0$/PWM pin functions as the $P9_0$ I/O pin or the PWM output pin.

Bit 0 PWM	Description	
0	$P9_0$/PWM pin functions for $P9_0$ input/output.	(initial value)
1	$P9_0$/PWM pin functions for PWM output.	

2. Port control register 9 (PCR9)

Bit	7	6	5	4	3	2	1	0
	$PCR9_7$	$PCR9_6$	$PCR9_5$	$PCR9_4$	$PCR9_3$	$PCR9_2$	$PCR9_1$	$PCR9_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PCR9 is an 8-bit register for controlling whether each of port 9 pins $P9_7$ to $P9_0$ functions as an input or output pin. Setting a PCR9 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR9 and PDR9 are valid when the affected pin is designated in PMR2 as a general-purpose I/O pin. PCR9 is a write-only register, which always reads as all 1.

Upon reset, PCR9 is initialized to H'00.

3. Port data register 9 (PDR9)

Bit	7	6	5	4	3	2	1	0
	$PDR9_7$	$PDR9_6$	$PDR9_5$	$PDR9_4$	$PDR9_3$	$PDR9_2$	$PDR9_1$	$PDR9_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR9 is an 8-bit register that stores data for port 9 pins $P9_7$ to $P9_0$. If port 9 is read while PCR9 bits are set to 1, the values stored in PDR9 are read, regardless of the actual pin states. If port 9 is read while PCR9 bits are cleared to 0, the pin states are read.

Upon reset, PDR9 is initialized to H'00.

7.8.3 Pin Functions

Table 7-24 shows the port 9 pin functions.

Table 7-24 Port 9 Pin Functions

<table>
<tr><th>Pin</th><th>Pin Functions and Selection Method</th></tr>
<tr><td>$P9_7$/UD</td><td>Functions are switched as follows by means of the UP/DOWN bit* in PMR2 and bit $PCR9_7$ in PCR9.
<table>
<tr><td>UP/DOWN</td><td colspan="2">0</td><td>1</td></tr>
<tr><td>$PCR9_7$</td><td>0</td><td>1</td><td>—</td></tr>
<tr><td>Pin function</td><td>$P9_7$ input pin</td><td>$P9_7$ output pin</td><td>UD input pin</td></tr>
</table>
Note: * Before entering power-down mode, if this pin is set to UD input by the UP/DOWN bit in PMR2, it should be kept from floating by external connection or should be set to general I/O use by clearing the UP/DOWN bit to 0 prior to the state transition.</td></tr>
<tr><td>$P9_6$/SO_2*</td><td>Functions are switched as follows by means of bit SO2 in PMR2 and bit $PCR9_6$ in PCR9.
<table>
<tr><td>SO2</td><td colspan="2">0</td><td>1</td></tr>
<tr><td>$PCR9_6$</td><td>0</td><td>1</td><td>—</td></tr>
<tr><td>Pin function</td><td>$P9_6$ input pin</td><td>$P9_6$ output pin</td><td>SO_2 output pin</td></tr>
</table>
Note: * The PMOS buffer transistor of pin $P9_6$/SO_2 can be enabled or disabled by the SO2PMOS bit in PMR3. For details see 11.2.5, Port Mode Register 3 (PMR3).</td></tr>
<tr><td>$P9_5$/SI_2/
$\overline{CS}$</td><td>Functions are switched as follows by means of bit SI2 in PMR2,* bit CS in PMR3, and bit $PCR9_5$ in PCR9.
<table>
<tr><td>SI2</td><td colspan="2">0</td><td colspan="2">1</td></tr>
<tr><td>CS</td><td colspan="2">—</td><td>0</td><td>1</td></tr>
<tr><td>$PCR9_5$</td><td>0</td><td>1</td><td>—</td><td>—</td></tr>
<tr><td>Pin function</td><td>$P9_5$ input pin</td><td>$P9_5$ output pin</td><td>SI_2 input pin</td><td>$\overline{CS}$ output pin</td></tr>
</table>
Note: * Before entering power-down mode, if this pin is set to SI_2 input by bit SI2 in PMR2, it should be kept from floating by external connection or should be set to general I/O use by clearing bit SI2 to 0 prior to the state transition.</td></tr>
</table>

Table 7-24 Port 9 Pin Functions (cont)

Pin	Pin Functions and Selection Method
$P9_4/SCK_2$	Functions are switched as follows by means of bit SCK2* in PMR2, bits PS1 and PS0* in serial control register 2 (SCR2), and bit $PCR9_4$ in PCR9.

SCK2	0		1	
PS1, 0	—		Not 11	11
$PCR9_4$	0	1	—	—
Pin function	$P9_4$ input pin	$P9_4$ output pin	SCK_2 output pin	SCK_2 input pin

Note: * Before entering power-down mode, if this pin is set to SCK_2 input by bit SCK2 in PMR2 and bits PS1 and PS0 in SCR2, it should be kept from floating by external connection, or else should be set to some other use by changing bits SCK2 and bits PS1 and PS0 prior to the state transition.

For the settings of bits PS1 and PS0 in SCR2, see 11.2.3, Serial Control Register 2 (SCR2).

$P9_3/SO_1$* Functions are switched as follows by means of bit SO1 in PMR2 and bit $PCR9_3$ in PCR9.

SO1	0		1
$PCR9_3$	0	1	—
Pin function	$P9_3$ input pin	$P9_3$ output pin	SO_1 output pin

Note: * The PMOS buffer transistor of pin $P9_3/SO_1$ can be enabled or disabled by the SO1PMOS bit in PMR3. For details see 10.2.6, Port Mode Register 3 (PMR3).

$P9_2/SI_1$ Functions are switched as follows by means of bit SI1* in PMR2 and bit $PCR9_2$ in PCR9.

SI1	0		1
$PCR9_2$	0	1	—
Pin function	$P9_2$ input pin	$P9_2$ output pin	SI_1 input pin

Note: * Before entering power-down mode, if this pin is set to SI_1 input by bit SI1 in PMR2, it should be kept from floating by external connection or should be set to general I/O use by clearing bit SI1 to 0 prior to the state transition.

Table 7-24 Port 9 Pin Functions (cont)

Pin	Pin Functions and Selection Method
$P9_1/SCK_1$	Functions are switched as follows by means of bit SCK1 in PMR2,* bits SMR13 to SMR10 in serial mode register 1 (SMR1)*, and bit $PCR9_1$ in PCR9.

SCK1	0		1	
SMR13 to 10	—		Not 1111	1111
$PCR9_1$	0	1	—	—
Pin function	$P9_1$ input pin	$P9_1$ output pin	SCK_1 output pin	SCK_1 input pin

Note: * Before entering power-down mode, if this pin is set to SCK_1 input by bit SCK1 in PMR2 and bits SMR13 to SMR10 in SMR1, it should be kept from floating by external connection, or else should be set to some other use by changing the SCK1 bit or bits SMR13 to SMR10 prior to the state transition.

For the settings of bits SMR13 to SMR10 in SMR1, see 10.2.1, Serial Mode Register 1 (SMR1).

$P9_0$/PWM — Functions are switched as follows by means of bit PWM in PMR2 and bit $PCR9_0$ in PCR9.

PWM	0		1
$PCR9_0$	0	1	—
Pin function	$P9_0$ input pin	$P9_0$ output pin	PWM output pin

7.8.4 Pin States

Table 7-25 shows the port 9 pin states in each operating mode.

Table 7-25 Port 9 Pin States

Pins	Reset	Sleep	Standby	Watch	Subactive	Active
$P9_7$/UD, $P9_6/SO_2$, $P9_5/SI_2/\overline{CS}$, $P9_4/SCK_2$, $P9_3/SO_1$, $P9_2/SI_1$, $P9_1/SCK_1$, $P9_0$/PWM	High impedance or pulled up	Previous state retained	High impedance	High impedance	High impedance	Normal operation

Section 8 Timers

8.1 Overview

The H8/3714 Series provides on-chip two prescalers (prescaler S and prescaler W) with different input clocks, and five timers (timers A through E).

Prescaler S is a 13-bit counter clocked by the system clock ($\phi = f_{OSC}/2$). Its prescaled outputs are used by timers A to C and timer E.

Prescaler W is a 5-bit counter clocked by the subclock ($\phi_{SUB} = f_X/8$). Its prescaled output is used for time-base operation by timer A.

Table 8-1 outlines the functions of timers A through E.

Table 8-1 Timer A to E Functions

Name	Functions	Operating Clock (internal)	Event Input Pin	Waveform Output Pin	Remarks
Timer A	• 8-bit interval timer	ϕ/8 to ϕ/8192 (choice of 8 sources)	—	—	—
	• Time base	ϕ_{SUB}/32 (choice of 4 overflow periods)		—	—
Timer B	• 8-bit reloadable timer • Interval timer • Event counter	ϕ/8 to ϕ/8192 (choice of 7 sources)	$P1_0/\overline{IRQ_0}$	—	—
Timer C	• 8-bit reloadable timer • Interval timer • Event counter • Choice of up- or down-counting	ϕ/8 to ϕ/8192 (choice of 7 sources)	$P1_1/\overline{IRQ_1}$	—	Counting direction can be controlled by software or hardware.
Timer D	• 8-bit event counter	—	$P1_6/\overline{EVENT}$	—	—
Timer E	• 8-bit reloadable timer • Interval timer	ϕ/8 to ϕ/8192 (choice of 8 sources)	—	$P1_5/\overline{IRQ_5}$/ TMOE	Can output square wave with 50% duty cycle

8.1.1 Prescaler Operation

1. Prescaler S (PSS)

   Prescaler S is a 13-bit counter using the system clock ($\phi = f_{OSC}/2$) as its input clock. Each input clock cycle causes prescaler S to increment once.

   Prescaler S is initialized to H'0000 by a reset, and starts counting upon return to active mode.

   In standby mode, watch mode, and subactive mode, the system clock (ϕ) pulse generator stops, so prescaler S also stops functioning. Its value is reset to H'0000.

   The CPU cannot read or write prescaler S data.

   The output from prescaler S is shared by timers A to C and E as well as serial communication interfaces 1 and 2. The frequency division ratio can be set separately for each on-chip peripheral function.

2. Prescaler W (PSW)

   Prescaler W is a 5-bit counter using the subclock ($\phi_{SUB} = f_X/8$) as its input clock.

   Prescaler W is initialized to H'00 by a reset, and starts counting upon return to active mode.

   Even in standby mode, watch mode, or subactive mode, prescaler W continues functioning so long as clock signals are supplied to pins X_1 and X_2.

   Prescaler W can be reset by setting bits TMA3 and TMA2 to 1 in timer mode register A (TMA).

   The output from prescaler W can be used as the clock source for timer A, in which case timer A functions as a time base.

   Figure 8-1 shows the clock signals supplied by prescalers S and W to peripheral modules.

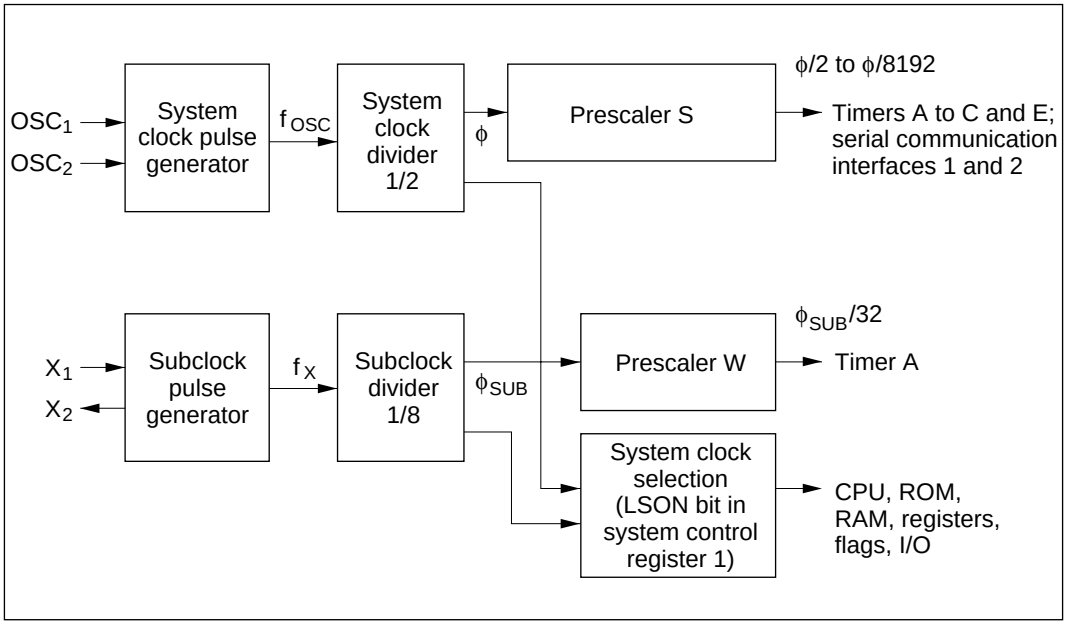


Figure 8-1 Clock Supply

8.2 Timer A

8.2.1 Overview

Timer A is an 8-bit interval timer. It can be connected to a 32.768 kHz crystal oscillator for use as a real-time clock time base.

1. Features

   Features of timer A are given below.

   - Choice of eight internal clock sources (ϕ/8192, ϕ/4096, ϕ/2048, ϕ/512, ϕ/256, ϕ/128, ϕ/32, ϕ/8).
   - Choice of four overflow periods (2 s, 1 s, 0.5 s, 125 ms) when timer A is used as a time base (using a 32.768 kHz crystal oscillator).
   - An interrupt is requested when the counter overflows.

2. Block diagram

   Figure 8-2 shows a block diagram of timer A.

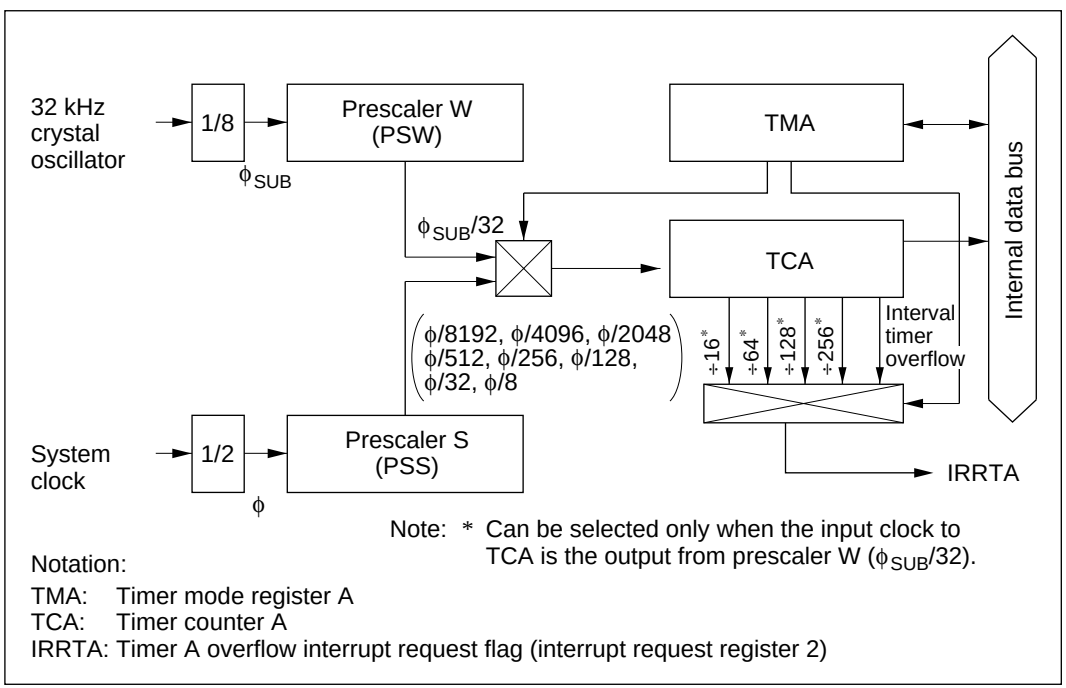


Figure 8-2 Block Diagram of Timer A

3. Register configuration

Table 8-2 shows the register configuration of timer A.

Table 8-2 Timer A Registers

Name	Abbrev.	R/W	Initial Value	Address
Timer mode register A	TMA	R/W	H'F0	H'FFC0
Timer counter A	TCA	R	H'00	H'FFC1

8.2.2 Register Descriptions

1. Timer mode register A (TMA)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	TMA3	TMA2	TMA1	TMA0
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

TMA is an 8-bit read/write register for selecting the prescaler and input clock.

Upon reset, TMA is initialized to H'F0.

Bits 7 to 4: Reserved bits

Bits 7 to 4 are reserved; they always read 1, and cannot be modified.

Bit 3: Prescaler select (TMA3)

Bit 3 selects either prescaler S or prescaler W as the clock input source for timer A.

Bit 3 TMA3	Description	
0	Prescaler S (PSS) is clock input source for timer A.	(initial value)
1	Prescaler W (PSW) is clock input source for timer A.	

Bits 2 to 0: Clock select (TMA2 to TMA0)

Bits 2 to 0 select the clock input to TCA. The selection is made as follows by the combination of these bits and bit TMA3.

Bit 3 TMA3	Bit 2 TMA2	Bit 1 TMA1	Bit 0 TMA0	Description	
				Prescaler divider ratio (interval timer) or overflow period (time base)	Operation mode
0	0	0	0	PSS, ϕ/8192 (initial value)	Interval timer mode
			1	PSS, ϕ/4096	
		1	0	PSS, ϕ/2048	
			1	PSS, ϕ/512	
	1	0	0	PSS, ϕ/256	
			1	PSS, ϕ/128	
		1	0	PSS, ϕ/32	
			1	PSS, ϕ8	
1	0	0	0	PSW, 2 s	Time-base mode
			1	PSW, 1 s	
		1	0	PSW, 0.5 s	
			1	PSW, 125 ms	
	1	0	0	PSW and TCA are reset	
			1		
		1	0		
			1		

Note: $\phi = f_{OSC}/2$

2. Timer counter A (TCA)

Bit	7	6	5	4	3	2	1	0
	TCA7	TCA6	TCA5	TCA4	TCA3	TCA2	TCA1	TCA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

TCA is an 8-bit read-only up-counter, which is incremented by internal clock input. The clock source for input to this counter is selected by bits TMA3 to TMA0 in timer mode register A (TMA). The TCA value can be read by the CPU at any time.

TCA is cleared by setting bits TMA3 and TMA2 of TMA to 1.

When TCA overflows, the IRRTA bit in interrupt request register 2 (IRR2) is set to 1.

Upon reset, TCA is initialized to H'00.

8.2.3 Timer Operation

Timer A is an 8-bit timer which can be used either as an interval timer or, if a 32.768 kHz crystal oscillator is connected, as a real-time clock time base.

1. Interval timer operation

   When bit TMA3 in timer mode register A (TMA) is cleared to 0, timer A functions as an 8-bit interval timer.

   Upon reset, TCA is cleared to H'00 and bit TMA3 is cleared to 0, so up-counting and interval timing resume immediately after the reset. The clock input to timer A is selected by bits TMA2 to TMA0 in TMA; any of eight internal clock signals output by prescaler S can be selected.

   After the count value in TCA reaches H'FF, the next clock signal input causes timer A to overflow, setting bit IRRTA to 1 in interrupt request register 2 (IRR2). If IENTA = 1 in interrupt enable register 2 (IENR2), a CPU interrupt is requested.*

   At overflow, TCA returns to H'00 and starts counting up again. In this mode timer A functions as an interval timer that generates an overflow output at intervals of 256 input clock pulses.

   Note: * For details on interrupts, see 3.2.2, Interrupts.

2. Real-time clock time base operation

   When bit TMA3 in TMA is set to 1, timer A functions as a time base for a real-time clock by counting clock signals output by prescaler W.

   The overflow period of timer A is set by bits TMA1 and TMA0 in TMA. A choice of four periods is available.

3. Count initialization

   When bits TMA3 and TMA2 are both set to 1, PSW and TCA are initialized (cleared to 0 and stopped). From this initialized state, if bit TMA3 is left set to 1 and bit TMA2 is cleared to 0, timer A begins counting from 0 in time base mode.

   From the initialized state, if bit TMA3 is cleared to 0, timer A begins counting from 0 in interval timer mode. (Bit TMA2 can be either set or cleared.) However, since prescaler S (PSS) has not been initialized, the time between clearing bit TMA3 to 0 and the first count will vary.

8.3 Timer B

8.3.1 Overview

Timer B is an 8-bit up-counter that increments each time a clock pulse is input. This timer has two operation modes, interval and auto reload.

1. Features

   Features of timer B are given below.

   - Choice of seven internal clock sources (ϕ/8192, ϕ/2048, ϕ/512, ϕ/256, ϕ/128, ϕ/32, ϕ/8) or an external clock (can be used to count external events).
   - An interrupt is requested when the counter overflows.

2. Block diagram

   Figure 8-3 shows a block diagram of timer B.

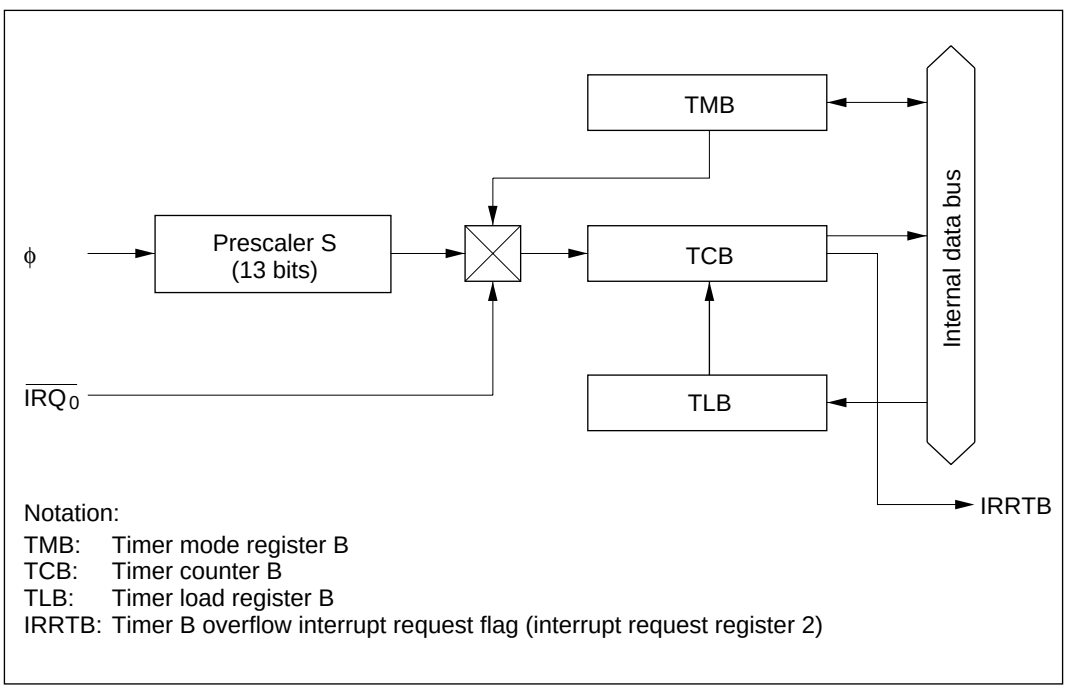


Figure 8-3 Block Diagram of Timer B

3. Pin configuration

Table 8-3 shows the timer B pin configuration.

Table 8-3 Pin Configuration

Name	Abbrev.	I/O	Function
Event input pin	$P1_0/\overline{IRQ_0}$	Input	Timer B event input

4. Register configuration

Table 8-4 shows the register configuration of timer B.

Table 8-4 Timer B Registers

Name	Abbrev.	R/W	Initial Value	Address
Timer mode register B	TMB	R/W	H'78	H'FFC2
Timer counter B	TCB	R	H'00	H'FFC3
Timer load register B	TLB	W	H'00	H'FFC3

8.3.2 Register Descriptions

1. Timer mode register B (TMB)

Bit	7	6	5	4	3	2	1	0
	TMB7	—	—	—	—	TMB2	TMB1	TMB0
Initial value	0	1	1	1	1	0	0	0
Read/Write	R/W	—	—	—	—	R/W	R/W	R/W

TMB is an 8-bit read/write register for selecting the auto-reload function and input clock.

Upon reset, TMB is initialized to H'78.

Bit 7: Auto-reload function select (TMB7)

Bit 7 selects the auto-reload function of timer B.

Bit 7 TMB7	Description	
0	Interval timer function selected.	(initial value)
1	Auto-reload function selected.	

Bits 6 to 3: Reserved bits

Bits 6 to 3 are reserved; they always read 1, and cannot be modified.

Bits 2 to 0: Clock select (TMB2 to TMB0)

Bits 2 to 0 select the clock input to TCB. For external clock counting, either the rising or falling edge can be selected.

Bit 2 TMB2	Bit 1 TMB1	Bit 0 TMB0	Description	
0	0	0	Internal clock: ϕ/8192.	(initial value)
0	0	1	Internal clock: ϕ/2048.	
0	1	0	Internal clock: ϕ/512.	
0	1	1	Internal clock: ϕ/256.	
1	0	0	Internal clock: ϕ/128.	
1	0	1	Internal clock: ϕ/32.	
1	1	0	Internal clock: ϕ/8.	
1	1	1	External clock ($P1_0/\overline{IRQ_0}$): rising or falling edge.*	

Note: * The edge of the external event signal is selected by bit IEG0 in the IRQ edge select register (IEGR). For details see 3.2.3 (2), IRQ edge select register (IEGR).

2. Timer counter B (TCB)

Bit	7	6	5	4	3	2	1	0
	TCB7	TCB6	TCB5	TCB4	TCB3	TCB2	TCB1	TCB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

TCB is an 8-bit read-only up-counter, which is incremented by internal or external clock input. The clock source for input to this counter is selected by bits TMB2 to TMB0 in timer mode register B (TMB). The TCB value can be read by the CPU at any time.

When TCB overflows from H'FF to H'00 or to the value set in TLB, the IRRTB bit in interrupt request register 2 (IRR2) is set to 1.

TCB is allocated to the same address as timer load register B (TLB).

Upon reset, TCB is initialized to H'00.

3. Timer load register B (TLB)

Bit	7	6	5	4	3	2	1	0
	TLB7	TLB6	TLB5	TLB4	TLB3	TLB2	TLB1	TLB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

TLB is an 8-bit write-only register for setting the reload value of timer counter B (TCB).

When a reload value is set in TLB, the same value is loaded into timer counter B (TCB) as well, and TCB starts counting up from that value. When TCB overflows during operation in auto-reload mode, the TLB value is loaded in TCB. Accordingly, overflow periods can be set within the range of 1 to 256 input clocks.

The same address is allocated to TLB as to TCB.

Upon reset, TLB is initialized to H'00.

8.3.3 Timer Operation

Timer B is an 8-bit multifunction timer. It can be used as an interval timer, an auto-reload timer, or an event counter. (Event counting requires an input pin setting.)

1. Timer B operation modes

   Timer B is an 8-bit up-counter which is incremented each time a clock pulse is input. The two operation modes, interval and auto-reload, are explained below.

- Interval timer operation

  When bit TMB7 in timer mode register B (TMB) is cleared to 0, timer B functions as an 8-bit interval timer.

  Upon reset, TCB is cleared to H'00 and bit TMB7 is cleared to 0, so up-counting and interval timing resume immediately after the reset. The clock input to timer B is selected from seven internal clock signals output by prescaler S, or an external clock input at pin $P1_0/\overline{IRQ_0}$. The selection is made by bits TMB2 to TMB0 of TMB.

  After the count value in TCB reaches H'FF, the next clock signal input causes timer B to overflow, setting bit IRRTB to 1 in interrupt request register 2 (IRR2). If IENTB = 1 in interrupt enable register 2 (IENR2), a CPU interrupt is requested.*

  At overflow, TCB returns to H'00 and starts counting up again.

  During interval timer operation (TMB7 = 0), when a value is set in timer load register B (TLB), the same value is set in TCB.

Note: * For details on interrupts, see 3.2.2, Interrupts.

- Auto-reload timer operation

  Setting bit TMB7 in TMB to 1 causes timer B to function as an 8-bit auto-reload timer. When a reload value is set in TLB, the same value is loaded into TCB, becoming the value from which TCB starts its count.

  After the count value in TCB reaches H'FF, the next clock signal input causes timer B to overflow. The TLB value is then loaded into TCB, and the count continues from that value. The overflow period can be set within a range from 1 to 256 input clocks, depending on the TLB value.

  The clock sources and interrupts in auto-reload mode are the same as for interval mode.

  In auto-reload mode (bit TMB7 = 1), setting a new TLB value also initializes TCB.

2. Operation on external clock

   Timer B can operate on an external clock input as an event signal at pin $P1_0/\overline{IRQ_0}$. External clock operation is selected by setting bits TMB2 to TMB0 in timer mode register B to all 1's (111). TCB can count either rising or falling edges of the input at pin $P1_0/\overline{IRQ_0}$.

   When timer B is used to count external event input, bit IRQC0 in port mode register 1 (PMR1) should be set to 1, and bit IEN0 in interrupt enable register 1 (IENR1) should be cleared to 0 to disable IRQ_0 interrupt requests.

8.4 Timer C

8.4.1 Overview

Timer C is an 8-bit up/down counter that increments or decrements each time a clock pulse is input. This timer has two operation modes, interval and auto reload.

1. Features

   Features of timer C are given below.

   - Choice of seven internal clock sources (ϕ/8192, ϕ/2048, ϕ/512, ϕ/256, ϕ/128, ϕ/32, ϕ/8) or an external clock (can be used to count external events).
   - An interrupt is requested when the counter overflows.
   - Can be switched between up- and down-counting by software or hardware control.

2. Block diagram

   Figure 8-4 shows a block diagram of timer C.

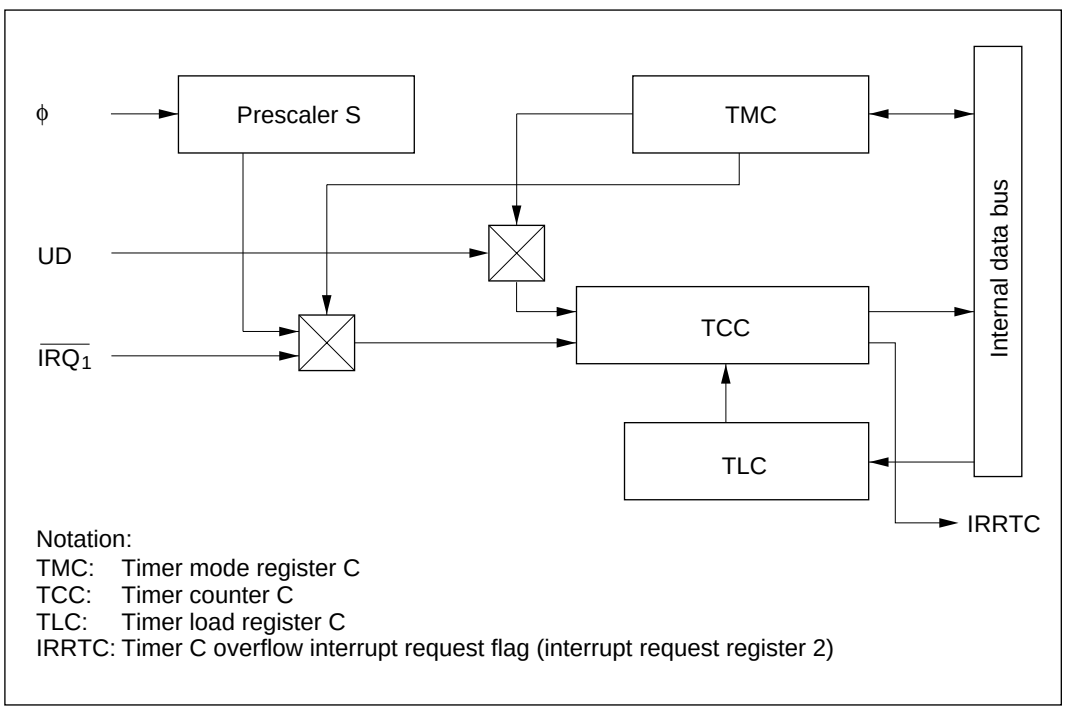


Figure 8-4 Block Diagram of Timer C

3. Pin configuration

Table 8-5 shows the timer C pin configuration.

Table 8-5 Pin Configuration

Name	Abbrev.	I/O	Function
Event input pin	$P1_1/\overline{IRQ_1}$	Input	Timer C event input
Up/down select pin	$P9_7$/UD	Input	Timer C counting direction control

4. Register configuration

Table 8-6 shows the register configuration of timer C.

Table 8-6 Timer C Registers

Name	Abbrev.	R/W	Initial Value	Address
Timer mode register C	TMC	R/W	H'18	H'FFC4
Timer counter C	TCC	R	H'00	H'FFC5
Timer load register C	TLC	W	H'00	H'FFC5

8.4.2 Register Descriptions

1. Timer mode register C (TMC)

Bit	7	6	5	4	3	2	1	0
	TMC7	TMC6	TMC5	—	—	TMC2	TMC1	TMC0
Initial value	0	0	0	1	1	0	0	0
Read/Write	R/W	R/W	R/W	—	—	R/W	R/W	R/W

TMC is an 8-bit read/write register for selecting the auto-reload function, counting direction, and input clock.

Upon reset, TMC is initialized to H'18.

Bit 7: Auto-reload function select (TMC7)

Bit 7 selects the auto-reload function of timer C.

Bit 7 TMC7	Description	
0	Interval timer function selected.	(initial value)
1	Auto-reload function selected.	

Bit 6: Counter up/down control 1 (TMC6)

This bit selects whether the counting direction of timer counter C (TCC) is controlled by hardware using pin $P9_7$/UD, or by software using bit TMC5.

Bit 5: Counter up/down control 2 (TMC5)

This bit selects whether TCC is an up-counter or down-counter. The setting of this bit is valid when bit TMC6 = 0.

Bits TMC6 and TMC5 operate as follows.

Bit 6 TMC6	Bit 5 TMC5	Description	
0	0	TCC is an up-counter.	(initial value)
0	1	TCC is a down-counter.	
1	*	TCC up/down control is by input at pin $P9_7$/UD. TCC is a down-counter if UD input is high, and an up-counter if UD input is low.	

Note: * Don't care.

Bits 4 and 3: Reserved bits

Bits 4 and 3 are reserved; they always read 1, and cannot be modified.

Bits 2 to 0: Clock select (TMC2 to TMC0)

Bits 2 to 0 select the clock input to TCC. For external clock counting, either the rising or falling edge can be selected.

Bit 2 TMC2	Bit 1 TMC1	Bit 0 TMC0	Description
0	0	0	Internal clock: ϕ/8192. (initial value)
0	0	1	Internal clock: ϕ/2048.
0	1	0	Internal clock: ϕ/512.
0	1	1	Internal clock: ϕ/256.
1	0	0	Internal clock: ϕ/128.
1	0	1	Internal clock: ϕ/32.
1	1	0	Internal clock: ϕ/8.
1	1	1	External clock ($P1_1/\overline{IRQ_1}$): rising or falling edge.*

Note: * The edge of the external clock is selected by bit IEG1 in the IRQ edge select register (IEGR). For details see 3.2.3 2, IRQ edge select register (IEGR).

2. Timer counter C (TCC)

Bit	7	6	5	4	3	2	1	0
	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

TCC is an 8-bit read-only up-/down-counter, which is incremented or decremented by internal or external clock input. The clock source for input to this counter is selected by bits TMC2 to TMC0 in timer mode register C (TMC). The TCC value can be read by the CPU at any time.

When TCC overflows (from H'FF to H'00 or to the value set in TLC) or underflows (from H'00 to H'FF or to the value set in TLC), the IRRTC bit in interrupt request register 2 (IRR2) is set to 1.

TCC is allocated to the same address as timer load register C (TLC).

Upon reset, TCC is initialized to H'00.

3. Timer load register C (TLC)

Bit	7	6	5	4	3	2	1	0
	TLC7	TLC6	TLC5	TLC4	TLC3	TLC2	TLC1	TLC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

TLC is an 8-bit write-only register for setting the reload value of TCC. When a reload value is set in TLC, the same value is loaded into timer counter C (TCC) as well, and TCC starts counting up or down from that value. When TCC overflows or underflows during operation in auto-reload mode, the TLC value is loaded in TCC. Accordingly, overflow and underflow periods can be set within the range of 1 to 256 input clocks.

The same address is allocated to TLC as to TCC.

Upon reset, TLC is initialized to H'00.

8.4.3 Timer Operation

Timer C is an 8-bit multifunction timer. It can be used as an interval timer, an auto-reload timer, or an event counter. (Event counting requires an input pin setting.)

1. Timer C operation modes

   Timer C is an 8-bit up-/down-counter which is incremented or decremented each time a clock pulse is input. The two operation modes, interval and auto-reload, are explained below.

- Interval timer operation

  When bit TMC7 in timer mode register C (TMC) is cleared to 0, timer C functions as an 8-bit interval timer.

  Upon reset, timer counter C (TCC) is initialized to H'00 and TMC to H'18, so up-counting and interval timing resume immediately after the reset. The clock input to timer C is selected from seven internal clock signals output by prescaler S, or an external clock input at pin $P1_1/\overline{IRQ_1}$. The selection is made by bits TMC2 to TMC0 in TMC.

  Either software or hardware can control whether TCC counts up or down. The selection is made by TMC bits TMC6 and TMC5.

After the count value in TCC reaches H'FF (H'00), the next clock signal input causes timer C to overflow (underflow), setting bit IRRTC to 1 in interrupt request register 2 (IRR2). If bit IENTC = 1 in interrupt enable register 2 (IENR2), a CPU interrupt is requested.*

At overflow or underflow, TCC returns to H'00 or H'FF and starts counting up or down again.

During interval timer operation (TMC7 = 0), when a value is set in timer load register C (TLC), the same value is set in TCC.

Note: * For details on interrupts, see 3.2.2, Interrupts.

- Auto-reload timer operation

  Setting bit TMC7 in TMC to 1 causes timer C to function as an 8-bit auto-reload timer. When a reload value is set in TLC, the same value is loaded into TCC, becoming the value from which TCC starts its count.

  After the count value in TCC reaches H'FF (H'00), the next clock signal input causes timer C to overflow (or underflow). The TLC value is then loaded into TCC, and the count continues from that value. The overflow (underflow) period can be set within a range from 1 to 256 input clocks, depending on the TLC value.

  The clock sources, up/down control, and interrupts in auto-reload mode are the same as for interval mode.

  In auto-reload mode (bit TMC7 = 1), setting a new TLC value also initializes TCC.

2. Operation on external clock

   Timer C can operate on an external clock input as an event signal at pin $P1_1/\overline{IRQ_1}$. External clock operation is selected by setting bits TMC2 to TMC0 in timer mode register C to all 1's (111). TCC can count either rising or falling edges of the input at pin $P1_1/\overline{IRQ_1}$.

   When timer C is used to count external event input, bit IRQC1 in port mode register 1 (PMR1) should be set to 1, and bit IEN1 in interrupt enable register 1 (IENR1) should be cleared to 0 to disable IRQ_1 interrupt requests.

3. TCC up/down control by hardware

   The counting direction of timer C can be controlled by input at pin $P9_7$/UD. When bit TMC6 in TMC is set to 1, high-level input at the UD pin selects down-counting, while low-level input selects up-counting.

   When using input at pin UD for this control function, set the UP/DOWN bit in port mode register 2 (PMR2) to 1.

8.5 Timer D

8.5.1 Overview

Timer D is an 8-bit event counter, which is incremented by input of an external event signal. Either rising or falling edges of the external event signal can be counted.

1. Features

   Features of timer D are given below.

- Choice of rising or falling edge for external event counting.
- An interrupt is requested when the counter overflows.

2. Block diagram

   Figure 8-5 shows a block diagram of timer D.

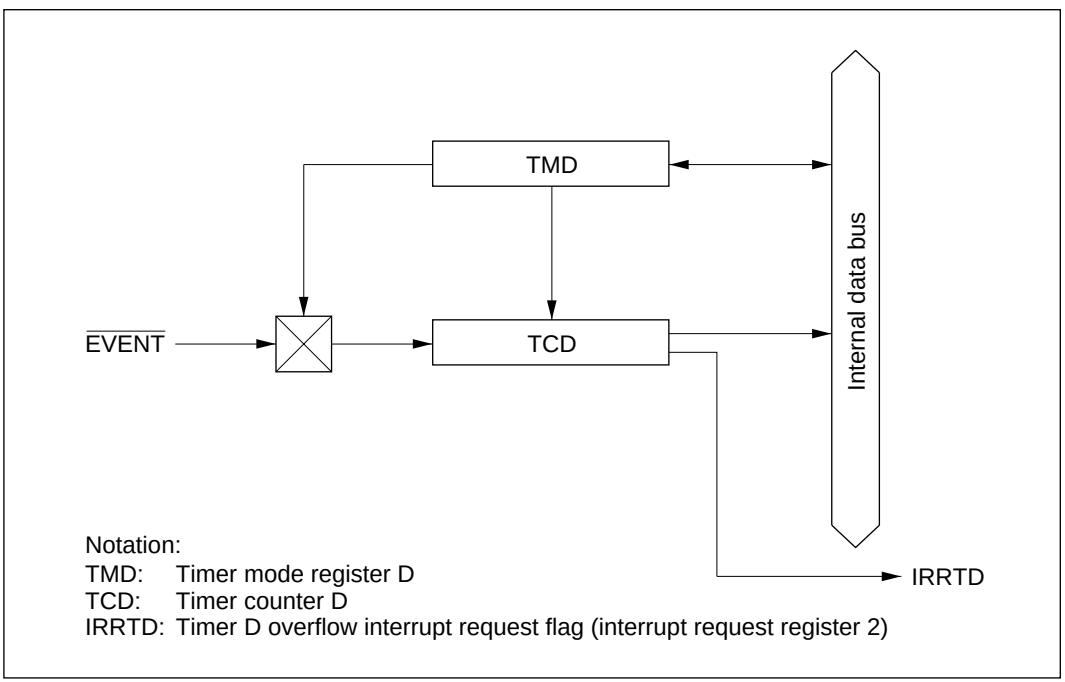


Figure 8-5 Block Diagram of Timer D

3. Pin configuration

Table 8-7 shows the timer D pin configuration.

Table 8-7 Pin Configuration

Name	Abbrev.	I/O	Function
Event input pin	$P1_6/\overline{EVENT}$	Input	Timer D event input

4. Register configuration

Table 8-8 shows the register configuration of timer D.

Table 8-8 Timer D Registers

Name	Abbrev.	R/W	Initial Value	Address
Timer mode register D	TMD	R/W*	H'7E	H'FFC6
Timer counter D	TCD	R	H'00	H'FFC7

Note: * Writing to bit 7 of TMD is possible only when writing 1 to clear the counter.

8.5.2 Register Descriptions

1. Timer mode register D (TMD)

Bit	7	6	5	4	3	2	1	0
	CLR	—	—	—	—	—	—	EDG
Initial value	0	1	1	1	1	1	1	0
Read/Write	W	—	—	—	—	—	—	R/W

TMD is an 8-bit read/write register for clearing timer counter D (TCD), and for selecting whether input at the external event pin is sensed at the rising or falling edge.

Bit 7: Counter clear (CLR)

Bit 7 initializes TCD to H'00.

Bit 7 CLR	Description	
0	After 1 is written to this bit to initialize TCD, it is cleared to 0 by hardware.	(initial value)
1	Initializes TCD to H'00.	

Bits 6 to 1: Reserved bits

Bits 6 to 1 are reserved; they always read 1, and cannot be modified.

Bit 0: Edge select (EDG)

Bit 0 selects the rising or falling edge of input at external event pin $P1_6/\overline{EVENT}$.

Bit 0 EDG	Description	
0	TCD counts falling edges of input at pin $P1_6/\overline{EVENT}$.	(initial value)
1	TCD counts rising edges of input at pin $P1_6/\overline{EVENT}$.	

2. Timer counter D (TCD)

Bit	7	6	5	4	3	2	1	0
	TCD7	TCD6	TCD5	TCD4	TCD3	TCD2	TCD1	TCD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

TCD is an 8-bit read-only up-counter, which is incremented by external clock input at pin $P1_6/\overline{EVENT}$. The input clock edge is selected by the EDG bit in timer mode register D (TMD). The TCD value can be read by the CPU at any time.

When TCD overflows from H'FF to H'00, the IRRTD bit in interrupt request register 2 (IRR2) is set to 1.

Upon reset, TCD is initialized to H'00.

8.5.3 Timer Operation

1. Operation on external clock

   Timer D operates on an external clock input at pin $P1_6/\overline{EVENT}$, used as an event input pin. The rising or falling edge of this input is selected by the EDG bit in timer mode register D (TMD).

   After the count value in TCD reaches H'FF, the next clock signal input causes timer D to overflow, setting bit IRRTD in interrupt request register 2 (IRR2) to 1 . If bit IENTD = 1 in interrupt enable register 2 (IENR2), a CPU interrupt is requested.*

   At overflow, TCD returns to H'00 and starts counting up again.

   TCD can be cleared by setting the CLR bit to 1 in TMD.

   To use external event input, the EVENT bit in port mode register 1 (PMR1) must be set to 1.

   Note: * For details on interrupts, see 3.2.2, Interrupts.

8.6 Timer E

8.6.1 Overview

Timer E is an 8-bit up-counter that increments each time a clock pulse is input. This timer has two operation modes, interval and auto reload. In addition, it can output a square wave with a 50% duty cycle, using overflow signals or signals from prescaler S.

1. Features

   Features of timer E are given below.

- Choice of eight internal clock sources (ϕ/8192, ϕ/4096, ϕ/2048, ϕ/512, ϕ/256, ϕ/128, ϕ/32, ϕ/8).
- An interrupt is requested when the counter overflows.
- Prescaler signals can provide a fixed-frequency output with a 50% duty cycle.

  When ϕ = 4 MHz, output is 1.95 kHz or 3.9 kHz.
  When ϕ = 2 MHz, output is 0.98 kHz or 1.95 kHz.

- Overflow signals can produce square wave output of any frequency with a 50% duty cycle.

2. Block diagram

Figure 8-6 shows a block diagram of timer E.

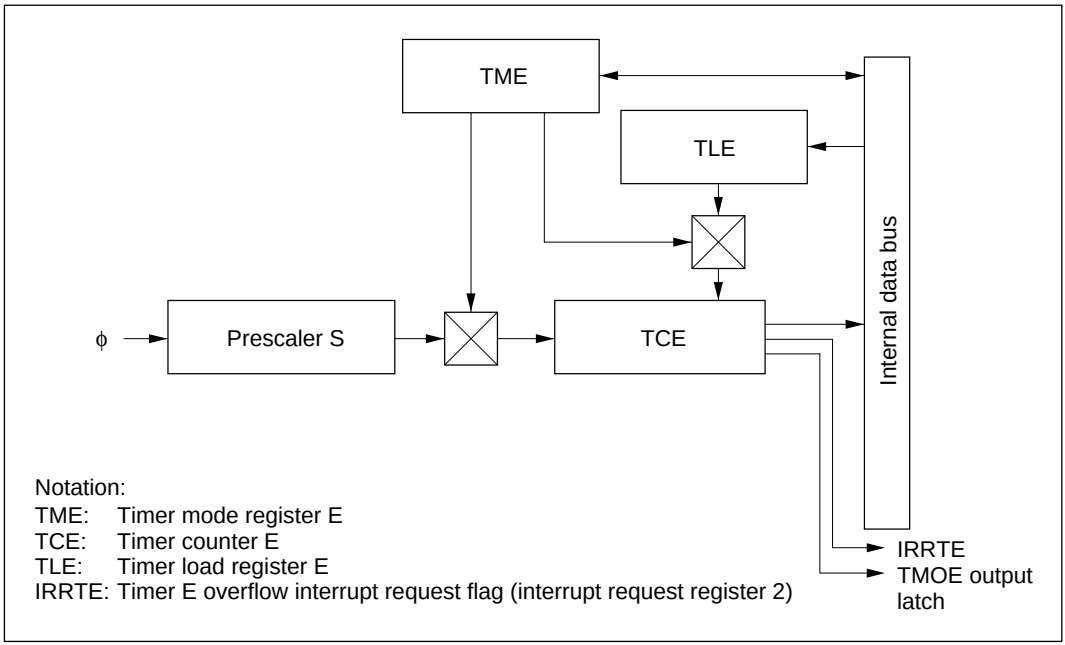


Figure 8-6 Block Diagram of Timer E

3. Pin configuration

Table 8-9 shows the timer E pin configuration.

Table 8-9 Pin Configuration

Name	Abbrev.	I/O	Function
Timer E waveform output pin	$P1_5/\overline{IRQ_5}$/TMOE	Output	Timer E output

4. Register configuration

Table 8-10 shows the register configuration of timer E.

Table 8-10 Timer E Registers

Name	Abbrev.	R/W	Initial Value	Address
Timer mode register E	TME	R/W	H'78	H'FFC8
Timer counter E	TCE	R	H'00	H'FFC9
Timer load register E	TLE	W	H'00	H'FFC9
Port mode register 4	PMR4	R/W	H'0F	H'FFEE

8.6.2 Register Descriptions

1. Timer mode register E (TME)

Bit	7	6	5	4	3	2	1	0
	TME7	—	—	—	—	TME2	TME1	TME0
Initial value	0	1	1	1	1	0	0	0
Read/Write	R/W	—	—	—	—	R/W	R/W	R/W

TME is an 8-bit read/write register for selecting the auto-reload function and input clock.

Upon reset, TME is initialized to H'78.

Bit 7: Auto-reload function select (TME7)

Bit 7 selects the auto-reload function of timer E.

Bit 7 TME7	Description	
0	Interval timer function selected.	(initial value)
1	Auto-reload function selected.	

Bits 6 to 3: Reserved bits

Bits 6 to 3 are reserved; they always read 1, and cannot be modified.

Bits 2 to 0: Clock select (TME2 to TME0)

Bits 2 to 0 select the clock input to TCE.

Bit 2 TME2	Bit 1 TME1	Bit 0 TME0	Description	
0	0	0	Internal clock: φ/8192.	(initial value)
0	0	1	Internal clock: φ/4096.	
0	1	0	Internal clock: φ/2048.	
0	1	1	Internal clock: φ/512.	
1	0	0	Internal clock: φ/256.	
1	0	1	Internal clock: φ/128.	
1	1	0	Internal clock: φ/32.	
1	1	1	Internal clock: φ/8.	

2. Timer counter E (TCE)

Bit	7	6	5	4	3	2	1	0
	TCE7	TCE6	TCE5	TCE4	TCE3	TCE2	TCE1	TCE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

TCE is an 8-bit read-only up-counter, which is incremented by internal clock input. The clock source for input to this counter is selected by bits TME2 to TME0 in timer mode register E (TME). The TCE value can be read by the CPU at any time.

When TCE overflows from H'FF to H'00 or to the value set in TLE, the IRRTE bit in interrupt request register 2 (IRR2) is set to 1.

TCE is allocated to the same address as timer load register E (TLE).

Upon reset, TCE is initialized to H'00.

3. Timer load register E (TLE)

Bit	7	6	5	4	3	2	1	0
	TLE7	TLE6	TLE5	TLE4	TLE3	TLE2	TLE1	TLE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

TLE is an 8-bit write-only register for setting the reload value of TCE.

When a reload value is set in TLE, the same value is loaded into timer counter E (TCE) as well, and TCE starts counting up from that value. When TCE overflows during operation in auto-reload mode, the TLE value is loaded in TCE. Accordingly, the overflow period can be set within the range of 1 to 256 input clocks.

The same address is allocated to TLE as to TCE.

Upon reset, TLE is initialized to H'00.

4. Port mode register 4 (PMR4)

Bit	7	6	5	4	3	2	1	0
	TEO	TEO ON	FREQ	VRFR	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

PMR4 is an 8-bit read/write register, for switching functions of pin $P1_5/\overline{IRQ_5}$/TMOE and for controlling waveform output from pin TMOE.

Upon reset, PMR4 is initialized to H'0F.

Bit 7: Timer E output select (TEO)

Bit 6: Timer E output on/off (TEO ON)

Bit 5: Fixed frequency select (FREQ)

Bit 4: Variable frequency select (VRFR)

$P1_5$/$\overline{IRQ_5}$/TMOE pin functions are switched as follows, by means of bits 7 to 4 of PMR4 and bit IRQC5 of port mode register 1 (PMR1).

PMR1	PMR4				Description	
Bit 5 IRQC5	Bit 7 TEO	Bit 6 TEO ON	Bit 5 FREQ	Bit 4 VRFR	Pin Function	Pin State
0	0	0	0	0	$P1_5$ pin	Standard I/O port (initial value)
0	0	*	*	*	$P1_5$ pin	Standard I/O port
0	1	0	*	*	TMOE output pin (off)	Low-level output
0	1	1	0	0	TMOE output pin (on)	Fixed-frequency output: (ϕ/2048) 1.95 kHz (ϕ = 4 MHz) 0.98 kHz (ϕ = 2 MHz)
0	1	1	1	0	TMOE output pin (on)	Fixed-frequency output: (ϕ/1024) 3.9 kHz (ϕ = 4 MHz) 1.95 kHz (ϕ = 2 MHz)
0	1	1	*	1	TMOE output pin (on)	Variable-frequency output: toggled by timer E overflow
1	*	*	*	*	$\overline{IRQ_5}$ input pin	External interrupt input

Note: * Don't care.

Bits 3 to 0: Reserved bits

Bits 3 to 0 are reserved; they always read 1, and cannot be modified.

8.6.3 Timer Operation

Timer E is an 8-bit up-counter that is incremented each time a clock pulse is input. It functions as an interval or auto-reload timer. It can also output a square wave having a 50% duty cycle. Each of these operation modes is explained below.

1. Interval timer operation

   When bit TME7 in timer mode register E (TME) is cleared to 0, timer E functions as an 8-bit interval timer.

   Upon reset, timer counter E (TCE) is reset to H'00 and bit TME7 is cleared to 0, so up-counting and interval timing resume immediately after the reset. The clock input to timer E is selected from eight internal clock signals output by prescaler S. The selection is made by bits TME2 to TME0 in TME.

   After the count value in TCE reaches H'FF, the next clock signal input causes timer E to overflow, setting bit IRRTE to 1 in interrupt request register 2 (IRR2). If bit IENTE = 1 in interrupt enable register 2 (IENR2), a CPU interrupt is requested.*

   At overflow, TCE returns to H'00, and starts counting up again.

   During interval timer operation (TME7 = 0), when a value is set in timer load register E (TLE), the same value is set in TCE.

   Note: * For details on interrupts, see 3.2.2, Interrupts.

2. Auto-reload timer operation

   Setting bit TME7 in TME to 1 causes timer E to function as an 8-bit auto-reload timer. When a reload value is set in TLE, the same value is loaded into TCE, becoming the value from which TCE starts its count.

   After the count value in TCE reaches H'FF, the next clock signal input causes timer E to overflow. The TLE value is then loaded into TCE, and the count continues from that value. The overflow period can be set within a range from 1 to 256 input clocks, depending on the TLE value.

   The clock sources and interrupts in auto-reload mode are the same as for interval mode.

   In auto-reload mode (bit TME7 = 1), setting a new TLE value also initializes TCE.

3. Square wave output

A 50% duty square wave can be output at pin $P1_5/\overline{IRQ_5}$/TMOE if this function is selected in port mode register 4 (PMR4) and bit IRQC5 in port mode register 1 (PMR1). When bit VRFR = 0 in PMR4, the square wave has a fixed frequency designated in the FREQ bit. For the frequencies that can be output, see 8.6.2 (4), Port mode register 4 (PMR4).

When bit VRFR = 1, timer E overflow generates a toggle output alternating between low and high level (see figure 8-7). The overflow period is selected in timer load register E (TLE), with timer E operating in auto-reload mode (bit TME7 = 1). The operating clock can be selected by means of bits TME2 to TME0. These settings can give a waveform output of any desired frequency within the range shown in table 8-11.

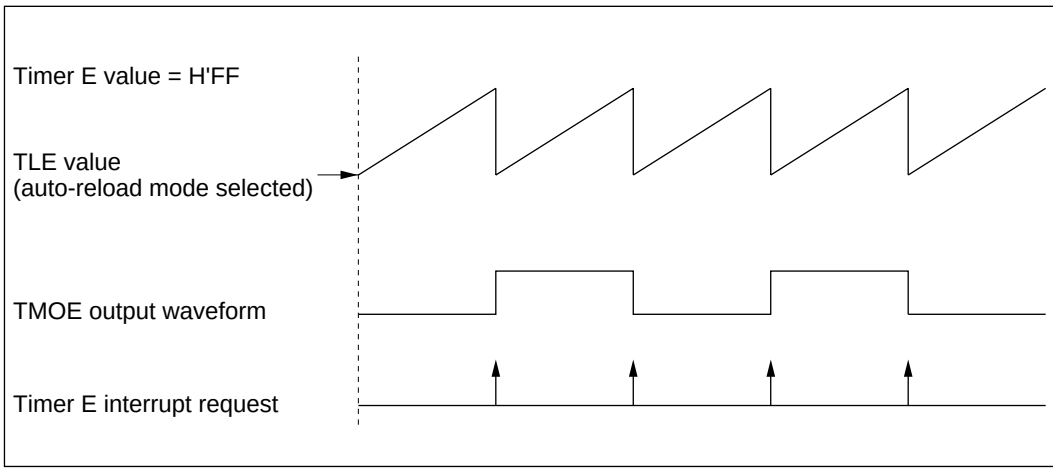


Figure 8-7 Square Wave Output Generated by Timer E Overflow

Table 8-11 Frequencies of Output Waveforms Generated by Timer E Overflow

	Output Waveform (ϕ = 2 MHz)			
	1 Count (TLE = H'FF) × 2		256 Counts (TLE = H'00) × 2	
Internal Clock	Count Time	Output Frequency	Count Time	Output Frequency
ϕ/8 (250 kHz)	8 µs	125 kz	2024 µs	488.3 Hz
ϕ/32 (62.5 kHz)	32 µs	31.25 kHz	8192 µs	122.1 Hz
ϕ/128 (15.62 kHz)	128 µs	7.8125 kHz	32.768 ms	30.5 Hz
ϕ/256 (7.8125 kHz)	256 µs	3.9063 kHz	65.536 ms	15.3 Hz
ϕ/512 (3.9062 kHz)	512 µs	1.9531 kHz	131.072 ms	7.63 Hz
ϕ/2048 (976.5 Hz)	2.048 ms	488.3 Hz	524.288 ms	1.91 Hz
ϕ/4096 (488.2 Hz)	4.096 ms	244.1 Hz	1048.576 ms	0.95 Hz
ϕ/8192 (244.1 Hz)	8.192 ms	122.1 Hz	2097.152 ms	0.477 Hz

	Output Waveform (ϕ = 4 MHz)			
	1 Count (TLE = H'FF) × 2		256 Counts (TLE = H'00) × 2	
Internal Clock	Count Time	Output Frequency	Count Time	Output Frequency
ϕ/8 (500 kHz)	4 µs	250 kz	1024 µs	976.6 Hz
ϕ/32 (125 kHz)	16 µs	62.5 kHz	4096 µs	244.1 Hz
ϕ/128 (31.25 kHz)	64 µs	15.625 kHz	16.384 ms	61.0 Hz
ϕ/256 (15.625 kHz)	128 µs	7.8125 kHz	32.768 ms	30.5 Hz
ϕ/512 (7.8125 kHz)	256 µs	3.9063 kHz	65.536 ms	15.3 Hz
ϕ/2048 (1.963 Hz)	1.024 ms	976.6 Hz	262.144 ms	3.8 Hz
ϕ/4096 (976.52 Hz)	2.048 ms	488.3 Hz	524.288 ms	1.91 Hz
ϕ/8192 (488.2 Hz)	4.096 ms	244.1 Hz	1048.576 ms	0.95 Hz

8.7 Interrupts

Timer A to E interrupts are requested when a timer overflows or underflows. Each timer is assigned its own vector address. The priority of interrupts is in the order of timer A (high) to timer E (low). Further details are given in 3.2.2, Interrupts, table 3-2, Interrupt Sources.

When timers A to E overflow, the corresponding bit IRRTA to IRRTE in interrupt request register 2 (IRR2) is set to 1. These interrupt flags are not cleared even if the interrupt is accepted. They must be cleared to 0 by software in the interrupt handler routine.

Interrupts may be enabled or disabled independently for each timer by means of bits IENTA to IENTE in interrupt enable register 2 (IENR2).

For further details see 3.2.3, Interrupt Control Registers.

8.8 Application Notes

Even when the EVENT bit in port mode register 1 (PMR1) designates the $P1_6$ usage of pin $P1_6/\overline{EVENT}$, reading the $P1_6$ pin may cause timer D to increment. When using timer D, be sure to clear timer counter D (TCD) by means of the CLR bit in timer mode register D (TMD).

Section 9 14-Bit PWM

9.1 Overview

The H8/3714 Series is provided with a 14-bit PWM (pulse width modulator) on-chip, which can be used as a D/A converter by connecting a low-pass filter.

9.1.1 Features

Features of the 14-bit PWM are as follows.

- Choice of two conversion periods
  A conversion period of 32768/ϕ, with a minimum modulation width of 2/ϕ (PWCR0 = 1), or a conversion period of 16384/ϕ, with a minimum modulation width of 1/ϕ (PWCR0 = 0), can be chosen.

- Pulse division method for less ripple

9.1.2 Block Diagram

Figure 9-1 shows a block diagram of the 14-bit PWM.

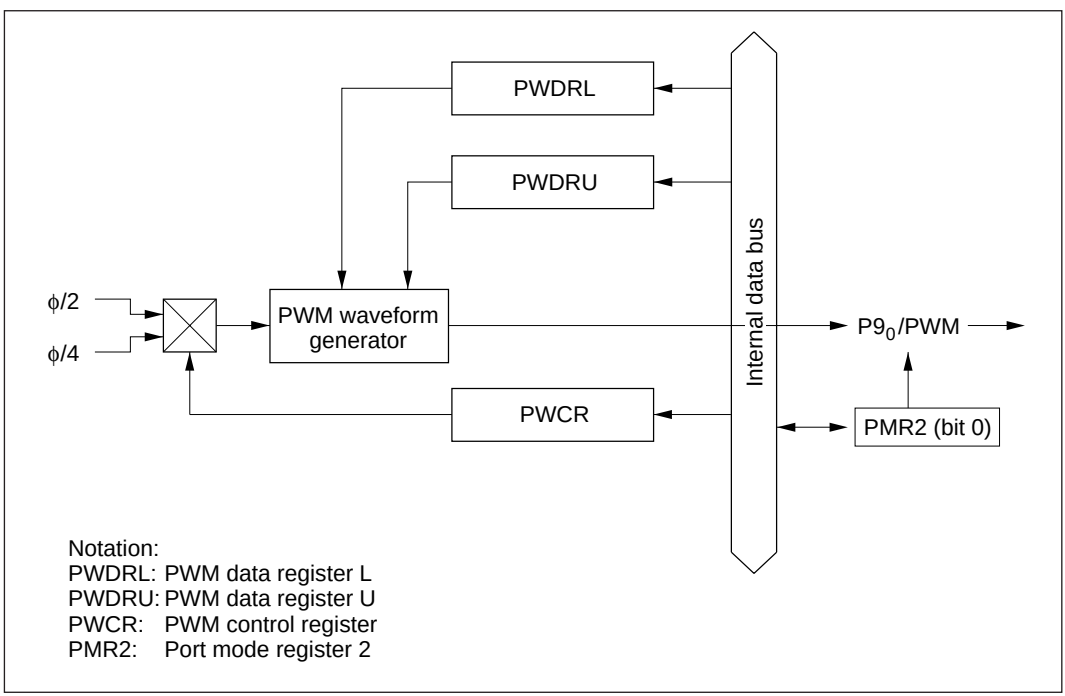


Figure 9-1 Block Diagram of 14-Bit PWM

9.1.3 Pin Configuration

Table 9-1 shows the output pin assigned to the 14-bit PWM.

Table 9-1 Pin Configuration

Name	Abbrev.	I/O	Function
PWM waveform output pin	PWM	Output	PWM waveform output

9.1.4 Register Configuration

Table 9-2 shows the register configuration of the 14-bit PWM.

Table 9-2 Register Configuration

Name	Abbrev.	R/W	Initial Value	Address
PWM control register	PWCR	W	H'FE	H'FFCC
PWM data register U	PWDRU	W	H'C0	H'FFCD
PWM data register L	PWDRL	W	H'00	H'FFCE

9.2 Register Descriptions

9.2.1 PWM Control Register (PWCR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PWCR0
Initial value	1	1	1	1	1	1	1	0
Read/Write	—	—	—	—	—	—	—	W

PWCR is an 8-bit write-only register for input clock selection.

Upon reset, PWCR is initialized to H'FE.

Bits 7 to 1: Reserved bits

Bits 7 to 1 are reserved; they always read 1, and cannot be modified.

Bit 0: Clock select (PWCR0)

Bit 0 selects the clock supplied to the 14-bit PWM. This bit is a write-only bit; it always reads 1.

Bit 0 PWCR0	Description
0	The input clock is $\phi/2$ ($t\phi = 2/\phi$). The conversion period is $16384/\phi$, with a minimum modulation width of $1/\phi$. (initial value)
1	The input clock is $\phi/4$ ($t\phi = 4/\phi$). The conversion period is $32768/\phi$, with a minimum modulation width of $2/\phi$.

Notation:
$t\phi$: Period of PWM input clock

9.2.2 PWM Data Registers U and L (PWDRU, PWDRL)

PWDRU

Bit	7	6	5	4	3	2	1	0
	—	—	PWDRU5	PWDRU4	PWDRU3	PWDRU2	PWDRU1	PWDRU0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

PWDRL

Bit	7	6	5	4	3	2	1	0
	PWDRL7	PWDRL6	PWDRL5	PWDRL4	PWDRL3	PWDRL2	PWDRL1	PWDRL0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PWDRU and PWDRL form a 14-bit write-only register, with the upper 6 bits assigned to PWDRU and the lower 8 bits to PWDRL. The value written to PWDRU and PWDRL gives the total high-level width of one PWM waveform cycle.

When 14-bit data is written to PWDRU and PWDRL, the register contents are latched in the PWM waveform generator, updating the PWM waveform generation data. The 14-bit data should always be written in the following sequence, first to PWDRL and then to PWDRU.

1. Write the lower 8 bits to PWDRL.

2. Write the upper 6 bits to PWDRU.

PWDRU and PWDRL are write-only registers. If they are read, all bits read 1.

Upon reset, PWDRU and PWDRL are initialized to H'C000.

9.3 Operation

When using the 14-bit PWM, set the registers in the following sequence.

1. Set bit PWM in port mode register 2 (PMR2) to 1 so that pin $P9_0$/PWM is designated for PWM output.

2. Set bit PWCR0 in the PWM control register (PWCR) to select a conversion period of either 32768/ϕ (PWCR0 = 1) or 16384/ϕ (PWCR0 = 0).

3. Set the output waveform data in PWM data registers U and L (PWDRU/L). Be sure to write in the correct sequence, first PWDRL then PWDRU. When data is written to PWDRU, the data in these registers will be latched in the PWM waveform generator, updating PWM waveform generation in synchronization with internal signals.

   One conversion period consists of 64 pulses, as shown in figure 9-2. The total of the high-level pulse widths during this period (T_H) corresponds to the data in PWDRU and PWDRL. This relation can be represented as follows.

   T_H = (data value in PWDRU and PWDRL + 64) × tϕ/2

   where tϕ is the PWM input clock period, either 2/ϕ (bit PWCR0 = 0) or 4/ϕ (bit PWCR0 = 1).

   If the data value in PWDRU and PWDRL is between H'3FC0 and H'3FFF, the PWM output level will be high.

   When the data value is H'0000, T_H = 64 × tϕ/2 = 32 tϕ.

   Example: Settings in order to obtain a conversion period of 8,192 µs:

   When bit PWCR0 = 0, the conversion period is 16384/ϕ, so ϕ must be 2 MHz. In this case t_{fn} = 128 µs, with 1/ϕ (resolution) = 0.5 µs.

   When bit PWCR0 = 1, the conversion period is 32768/ϕ, so ϕ must be 4 MHz. In this case t_{fn} = 128 µs, with 2/ϕ (resolution) = 0.5 µs.

   Accordingly, for a conversion period of 8,192 µs, the system clock frequency (ϕ) must be 2 MHz or 4 MHz.

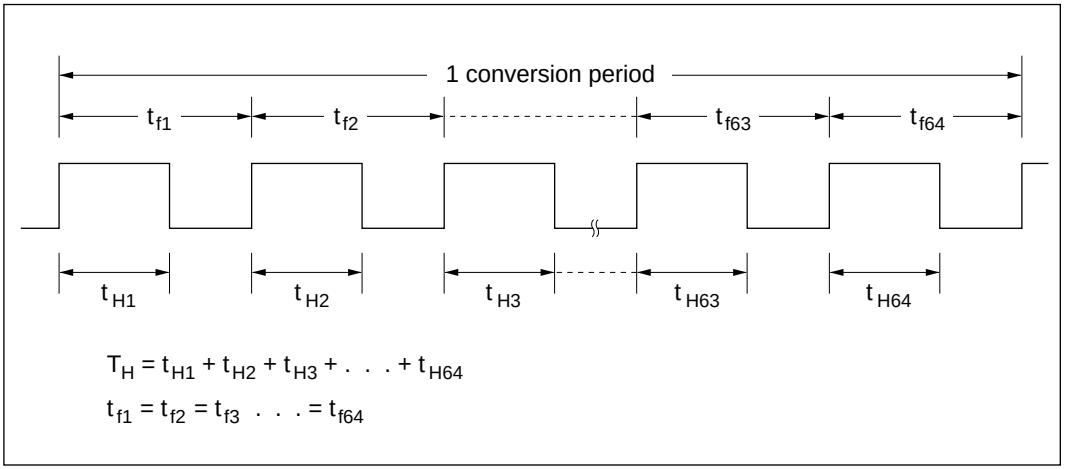


Figure 9-2 PWM Output Waveform

Section 10 SCI1

10.1 Overview

Serial communication interface 1 (SCI1) performs synchronous serial transfer of 8-bit or 16-bit data.

10.1.1 Features

SCI1 features are as follows.

- Choice of 8-bit or 16-bit data transfer
- Choice of eight internal clock sources (ϕ/1024, ϕ/256, ϕ/64, ϕ/32, ϕ/16, ϕ/8, ϕ/4, ϕ/2) or an external clock
- Interrupts requested at completion of transfer or when error occurs

10.1.2 Block Diagram

Figure 10-1 shows a block diagram of SCI1.

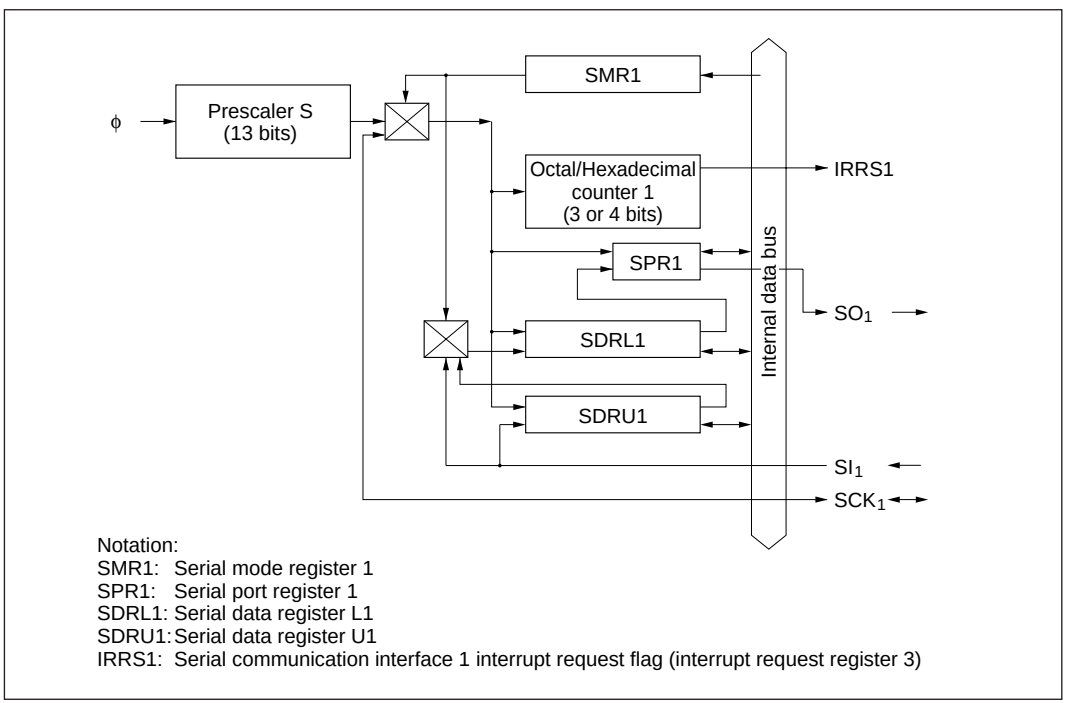


Figure 10-1 Block Diagram of SCI1

10.1.3 Pin Configuration

Table 10-1 shows the SCI1 pin configuration.

Table 10-1 Pin Configuration

Name	Abbrev.	I/O	Function
SCI1 clock pin	SCK_1	I/O	SCI1 clock input or output
SCI1 data input pin	SI_1	Input	SCI1 received data input
SCI1 data output pin	SO_1	Output	SCI1 transmit data output

10.1.4 Register Configuration

Table 10-2 shows the SCI1 register configuration.

Table 10-2 SCI1 Registers

Name	Abbrev.	R/W	Initial Value	Address
Serial mode register 1	SMR1	W	H'80	H'FFB0
Serial data register U1	SDRU1	R/W	Not fixed	H'FFB1
Serial data register L1	SDRL1	R/W	Not fixed	H'FFB2
Serial port register 1	SPR1	R/W	Not fixed	H'FFB3
Port mode register 2	PMR2	R/W	H'00	H'FFEC
Port mode register 3	PMR3	R/W	H'97	H'FFED

10.2 Register Descriptions

10.2.1 Serial Mode Register 1 (SMR1)

Bit	7	6	5	4	3	2	1	0
	—	SMR16	SMR15	SMR14	SMR13	SMR12	SMR11	SMR10
Initial value	1	0	0	0	0	0	0	0
Read/Write	—	W	W	W	W	W	W	W

SMR1 is an 8-bit write-only register, for selecting the operation mode and the prescaler divider ratio. Another function is to initialize the internal state of the serial interface, which happens at each write access to SMR1.

When SMR1 is written to, serial clock supply to serial data registers U1 and L1 (SDRU1, SDRL1) and to the octal/hexadecimal counter is stopped, and the octal/hexadecimal counter is reset to H'00. Accordingly, writing to the serial mode register while the serial interface is operating will abort data transmission or reception, and the serial communication interface 1 interrupt request flag (IRRS1) will be set.

Upon reset, SMR1 is initialized to H'80.

Bit 7: Reserved bit

Bit 7 is reserved; it always reads 1, and cannot be modified.

Bits 6 to 4: Operation mode select (SMR16 to SMR14)

Bits 6 to 4 select the SCI1 operation mode.

Bit 6 SMR16	Bit 5 SMR15	Bit 4 SMR14	Description	
0	0	0	Continuous clock output mode	(initial value)
	SMR15, SMR14 set to value other than 00		8-bit transfer mode	
1	0	0	Continuous clock output mode	
	SMR15, SMR14 set to value other than 00		16-bit transfer mode	

Bits 3 to 0: Clock select (SMR13 to SMR10)

Bits 3 to 0 select the clock supplied to SCI1.

Bit 3 SMR13	Bit 2 SMR12	Bit 1 SMR11	Bit 0 SMR10	Pin SCK_1	Clock Source	Prescaler Divider Ratio	Serial Clock Period (µs) ϕ = 4 MHz	Serial Clock Period (µs) ϕ = 2 MHz
0	0	0	0	SCK_1 output	Prescaler S	ϕ/1024 (initial value)	256	512
			1	SCK_1 output	Prescaler S	ϕ/256	64	128
		1	0	SCK_1 output	Prescaler S	ϕ/64	16	32
			1	SCK_1 output	Prescaler S	ϕ/32	8	16
	1	0	0	SCK_1 output	Prescaler S	ϕ/16	4	8
			1	SCK_1 output	Prescaler S	ϕ/8	2	4
		1	0	SCK_1 output	Prescaler S	ϕ/4	1	2
			1	SCK_1 output	Prescaler S	ϕ/2	—	1
1	0	0	0	Not used	—	—	—	—
	:	:	:					
	1	1	0					
	1	1	1	SCK_1 input	External clock	—	—	—

10.2.2 Serial Data Register U1 (SDRU1)

Bit	7	6	5	4	3	2	1	0
	SDRU17	SDRU16	SDRU15	SDRU14	SDRU13	SDRU12	SDRU11	SDRU10
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Not fixed

SDRU1 is an 8-bit read/write register. It is used as the data register for the upper 8 bits in 16-bit transfer (SDRL1 is used for the lower 8 bits).

Data written to SDRU1 is output to SDRL1 starting from the least significant bit (LSB), in synchronization with the falling edge of the serial clock. This data is than replaced by LSB-first data input at pin SI1, synchronized with the rising edge of the serial clock. In this way data is shifted in the direction from the most significant bit (MSB) toward the LSB.

SDRU1 must be written or read only after data transmission or reception is complete.
If this register is read or written while a data transfer is in progress, the data contents are not guaranteed.

The SDRU1 value upon reset is not fixed.

10.2.3 Serial Data Register L1 (SDRL1)

Bit	7	6	5	4	3	2	1	0
	SDRL17	SDRL16	SDRL15	SDRL14	SDRL13	SDRL12	SDRL11	SDRL10
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Not fixed

SDRL1 is an 8-bit read/write register. It is used as the data register in 8-bit transfer, and as the data register for the lower 8 bits in 16-bit transfer (SDRU1 is used for the upper 8 bits).

In 8-bit transfer, data written to SDRL1 is output from pin SO1 starting from the least significant bit (LSB), in synchronization with the falling edge of the serial clock. This data is then replaced by LSB-first data input at pin SI1, synchronized with the rising edge of the serial clock. In this way data is shifted in the direction from the most significant bit (MSB) toward the LSB.

In 16-bit transfer, operation is the same as for 8-bit transfer, except that input data is fed in via SDRU1.

SDRL1 must be written or read only after data transmission or reception is complete. If this register is read or written while a data transfer is in progress, the data contents are not guaranteed.

The SDRL1 value upon reset is not fixed.

10.2.4 Serial Port Register 1 (SPR1)

Bit	7	6	5	4	3	2	1	0
	SO1 LAST BIT	—	—	—	—	—	—	—
Initial value	*	1	1	1	1	1	1	1
Read/Write	R/W	—	—	—	—	—	—	—

Note: * Not fixed

SPR1 is an 8-bit read/write register, bit 7 of which is connected to the last output stage of SDRL1.

Bit 7: Extended data bit (SO1 LAST BIT)

Bit 7 holds the last bit of transmitted data after transmission ends.

Output from pin SO1 can be altered by software by modifying this bit either before or after transmission.

If this bit is written during data transmission, the data contents are not guaranteed.

Bit 7 SO1 LAST BIT	Description	
0	Output from pin SO_1 is low.	(initial value)
1	Output from pin SO_1 is high.	

Bits 6 to 0: Reserved bits

Bits 6 to 0 are reserved: they always read 1, and cannot be modified.

10.2.5 Port Mode Register 2 (PMR2)

Bit	7	6	5	4	3	2	1	0
	UP/ DOWN	SO2	SI2	SCK2	SO1	SI1	SCK1	PWM
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PMR2 is an 8-bit read/write register, for switching the port 9 pin functions. Bits 3 to 1, in combination with SMR1, set the SCI1 operation mode.

Upon reset, PMR2 is initialized to H'00.

Bits 3 to 1 are explained here. For bits 7 to 4 and bit 0, see 7.10.2 (1), Port Mode Register 2 (PMR2).

Bit 3: Pin $P9_3/SO_1$ function switch (SO1)

Bit 3 selects whether pin $P9_3/SO_1$ functions as a $P9_3$ input/output pin or as the SO_1 output pin.

Bit 3 SO1	Description	
0	Pin $P9_3/SO_1$ functions as $P9_3$ I/O pin.	(initial value)
1	Pin $P9_3/SO_1$ functions as SO_1 output pin. Setting bit SCK1 to 1 and clearing bit SI1 to 0 puts SCI1 in transmit mode.	

Bit 2: Pin $P9_2/SI_1$ function switch (SI1)

Bit 2 selects whether pin $P9_2/SI_1$ functions as a $P9_2$ input/output pin or as the SI_1 output pin.

Bit 2 SI1	Description	
0	Pin $P9_2/SI_1$ functions as $P9_2$ I/O pin.	(initial value)
1	Pin $P9_2/SI_1$ functions as SI_1 output pin. Setting bit SCK1 to 1 and clearing bit SO1 to 0 puts SCI1 in receive mode.	

Bit 1: Pin $P9_1/SCK_1$ function switch (SCK1)

Bit 1 selects whether pin $P9_1/SCK_1$ functions as a $P9_1$ input/output pin or as the SCK_1 input/output pin.

Bit 1 SCK1	Description	
0	Pin $P9_1/SCK_1$ functions as $P9_1$ I/O pin.	(initial value)
1	Pin $P9_1/SCK_1$ functions as SCK_1 I/O pin. The direction of clock I/O and the prescaler divider ratio are set in serial mode register 1 (SMR1).	

10.2.6 Port Mode Register 3 (PMR3)

Bit	7	6	5	4	3	2	1	0
	—	SO2 PMOS	CS	—	SO1 PMOS	—	—	—
Initial value	1	0	0	1	0	1	1	1
Read/Write	—	R/W	R/W	—	R/W	—	—	—

PMR3 is an 8-bit read/write register, for enabling the PMOS transistors of SCI1 and SCI2 data output pins (pins SO_1 and SO_2), and for controlling SCI2 chip select output (pin $SI_2/\overline{CS}$).

Upon reset, PMR3 is initialized to H'97.

Bit 3 is explained here. For bits 6 and 5, see 11.2.5, Port Mode Register 3 (PMR3).

Bit 3: Pin SO_1 PMOS on/off (SO1PMOS)

Bit 3 enables or disables the PMOS buffer transistor of pin $P9_3/SO_1$.

Bit 3 S01PMOS	Description	
0	The PMOS transistor of pin $P9_3/SO_1$ is enabled: CMOS output.	(initial value)
1	The PMOS transistor of pin $P9_3/SO_1$ is disabled: NMOS open-drain output.	

10.3 Operation

10.3.1 Overview

SCI1 sends and receives data in synchronization with clock pulses.

SCI1 operation modes are set by bits 6 to 4 of serial mode register 1 (SMR1) and bits 3 to 1 of port mode register 2 (PMR2) in combination, as shown in table 10-3.

Table 10-3 SCI1 Operation Mode Setting

SMR1			PMR2			
SMR16	**SMR15**	**SMR14**	**PMR23**	**PMR22**	**PMR21**	**Operation Mode**
*	*	*	0	0	0	Serial communication disabled
*	0	0	0	0	1	Continuous clock output mode
0	SMR15, SMR14 set to value other than 00		1	0	1	8-bit transmit mode
			0	1	1	8-bit receive mode
			1	1	1	8-bit transmit/receive mode
1	SMR15, SMR14 set to value other than 00		1	0	1	16-bit transmit mode
			0	1	1	16-bit receive mode
			1	1	1	16-bit transmit/receive mode

Note: * Don’t care.

SCI1 consists of SMR1, serial data register U1 (SDRU1), serial data register L1 (SDRL1), serial port register 1 (SPR1), an octal/hexadecimal counter, and a multiplexer. (See figure 10-1.)

Pin SCK_1 and the serial clock are controlled by writing data to SMR1.

SDRU1 and SDRL1 are used to write transmit data and to hold received data; these registers can be written and read by software. Data in these registers is shifted in synchronization with the serial clock, for input and output at pins SI_1 and SO_1.

SCI1 operation starts with a dummy read of SMR1. The octal/hexadecimal counter is cleared to H'0 by this dummy read, and starts counting anew from the falling edge of the serial clock (pin SCK_1), being incremented by 1 at each rising edge of the serial clock. If 8 or 16 serial clock cycles are input and the counter overflows, or if data transmission or reception is aborted, the octal/hexadecimal counter is cleared to H'0. At the same time bit IRRS1 in interrupt request register 3 (IRR3) is set to 1.

For more details on interrupts, see 3.2.2, Interrupts.

10.3.2 Data Transfer Format

Figure 10-2 shows the synchronous data transfer format. Data can be sent and received in lengths of 8 bits or 16 bits. Data is sent and received starting from the least significant bit, in LSB-first format. Transmit data is output from one falling edge of the serial clock until the next falling edge. Receive data is latched at the rising edge of the serial clock.

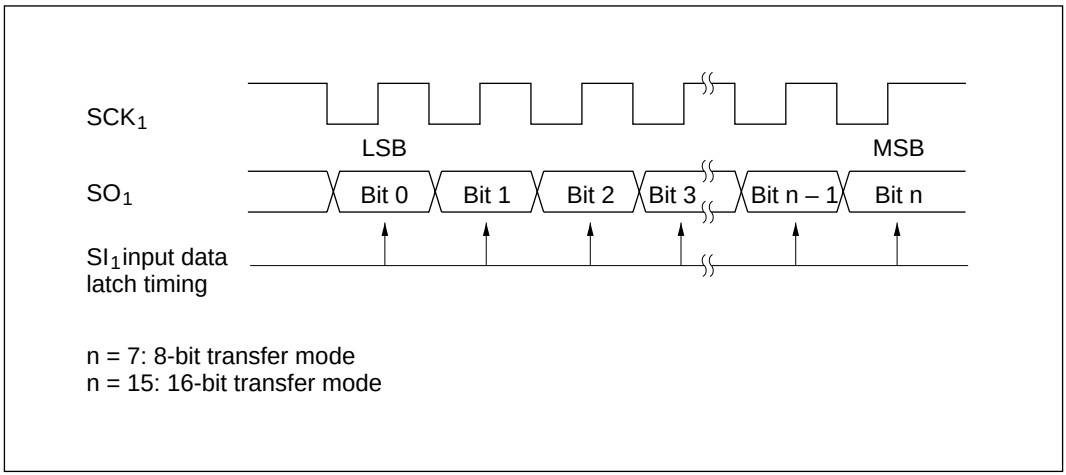


Figure 10-2 Synchronous Data Transfer Format

10.3.3 Clock

Eight internal clock sources or an external clock may be selected as the serial clock. When an internal clock is used, pin SCK_1 is the clock output pin.

10.3.4 Data Transmit/Receive

1. Initializing SCI1

   Before data is sent or received, first SCI1 must be initialized by software. This is done by writing the desired transfer conditions in serial mode register 1 (SMR1).

2. Transmitting

   A transmit operation is carried out as follows.

- Set bit SO1 in port mode register 2 (PMR2) to 1, making pin $P9_3/SO_1$ the SO_1 output pin. Also set bit SCK1 in PMR2 to 1, making pin $P9_1/SCK_1$ the SCK_1 I/O pin. If necessary, set the SO1PMOS bit in PMR3 for NMOS open-drain output at pin SO_1.

- Set bit SMR16 in SMR1 to 1 or 0, and set bits SMR15 and SMR14 to a value other than 00, designating 8- or 16-bit transfer mode. Select the serial clock with bits SMR13 to SMR10. Writing data to SMR1 initializes the internal state of SCI1.

- Write transmit data in serial data register L1 (SDRL1) and serial data register U1 (SDRU1), as follows.
  8-bit transfer mode: SDRL1
  16-bit transfer mode: Upper byte in SDRU1, lower byte in SDRL1

- Execute a dummy read of SMR1. SCI1 starts operating, and outputs the transmit data at pin SO_1.

- After data transmission is complete, bit IRRS1 in interrupt request register 3 (IRR3) is set to 1.

When an internal clock source is used, a serial clock is output from pin SCK_1 in synchronization with the transmit data. After data transmission is complete, the serial clock is not output until the next dummy read of SMR1. During this time, pin SO_1 continues to output the value of the last bit transmitted.

When an external clock source is used, data is transmitted in synchronization with the serial clock input at pin SCK_1. After data transmission is complete, if the serial clock continues to be input, transmission resumes.

Between transmissions, the output value of pin SO_1 can be changed by rewriting bit 7 (SO1 LAST BIT) in serial port register 1 (SPR1).

Executing a dummy read of SMR1 during transmission will cause a transmit error, setting bit IRRS1 in IRR3 to 1.

3. Receiving

   A receive operation is carried out as follows.

- Set bit SI1 in port mode register 2 (PMR2) to 1, making pin $P9_2/SI_1$ the SI_1 input pin. Also set bit SCK1 in PMR2 to 1, making pin $P9_1/SCK_1$ the SCK_1 I/O pin.

- Set bit SMR16 in serial mode register 1 (SMR1) to 1 or 0, and set bits SMR15 and SMR14 to a value other than 00, designating 8- or 16-bit transfer mode. Select the serial clock with bits SMR13 to SMR10. Writing data to SMR1 initializes the internal state of SCI1.

- Execute a dummy read of SMR1. SCI1 starts operating, and receive data is input at pin SI_1.

- After data reception is complete, bit IRRS1 in interrupt request register 3 (IRR3) is set to 1.

- Read the received data from SDRL1 and SDRU1, as follows.
  8-bit transfer mode: SDRL1
  16-bit transfer mode: Upper byte in SDRU1, lower byte in SDRL1

When an internal clock source is used, a dummy read of SMR1 immediately starts a data receive operation. The serial clock is output from pin SCK_1.

When an external clock source is used, after the dummy read of SMR1, data is received in synchronization with the serial clock input at pin SCK_1. After data reception is complete, if the serial clock continues to be input, reception resumes.

Executing a dummy read of SMR1 during reception will cause a receive error, setting bit IRRS1 in IRR3 to 1.

4. Simultaneous transmit/receive

   A simultaneous transmit/receive operation is carried out as follows.

- Set bits SO1, SI1, and SCK1 in PMR2 to 1, designating the SO_1 output pin, SI_1 pin, and SCK_1 pin functions. If necessary, set the SO1PMOS bit in PMR3 for NMOS open-drain output at pin SO_1.

- Set bit SMR16 in SMR1 to 1 or 0, and set bits SMR15 and SMR14 to a value other than 00, designating 8- or 16-bit transfer mode. Select the serial clock with bits SMR13 to SMR10. Writing data to SMR1 initializes the internal state of SCI1.

- Write transmit data in SDRL1 and SDRU1, as follows.
  8-bit transfer mode: SDRL1
  16-bit transfer mode: Upper byte in SDRU1, lower byte in SDRL1

- Execute a dummy read of SMR1. SCI1 starts operating: transmit data is output at pin SO_1, and receive data is input at pin SI_1.

- After data transmission and reception are complete, bit IRRS1 in IRR3 is set to 1.

- Read the received data from SDRL1 and SDRU1.
  8-bit transfer mode: SDRL1
  16-bit transfer mode: Upper byte in SDRU1, lower byte in SDRL1

In simultaneous data transmit/receive, the transmit operation and receive operation described in 10.3.4 sections 2 and 3 take place at the same time. See those sections for further details.

During a transmit/receive operation, a dummy read of SMR1 will result in a transmit/receive error, setting bit IRRS1 in IRR3 to 1.

10.3.5 SCI1 State Transitions

SCI1 has three internal states, as shown in figure 10-3.

In the serial start pending state, the internal state of the serial communication interface is initialized. In this state, the serial communication interface does not operate even if a serial clock signal is input. Executing a dummy read of SMR1 changes this state to the serial clock pending state.

In the serial clock pending state, when a serial clock signal is input the octal/hexadecimal counter starts counting up and the serial data register starts shifting, entering the transfer state. If continuous clock output mode has been selected, however, SCI1 outputs the clock signal continuously and does not enter the transfer state.

In the transfer state, when 8 or 16 transfer clock cycles are input, or if an SMR1 dummy read is executed, the octal/hexadecimal counter is reset to H'0, and SCI1 enters the serial clock pending state. Writing to SMR1 in the transfer state will reset the octal/hexadecimal counter to H'0 and change to the serial start pending state. In transitions from the transfer state to another state, the resetting of the octal/hexadecimal counter to H'0 sets bit IRRS1 in IRR3 to 1.

If an internal clock source is selected, a dummy read of SMR1 starts output of the serial clock, which stops after 8 or 16 clock output cycles.

After writing to SMR1 in the serial clock pending state or transfer state, it is necessary to write to SMR1 again in order to initialize the initial state of the serial communication interface. Writing to SMR1 changes the state to the serial start pending state.

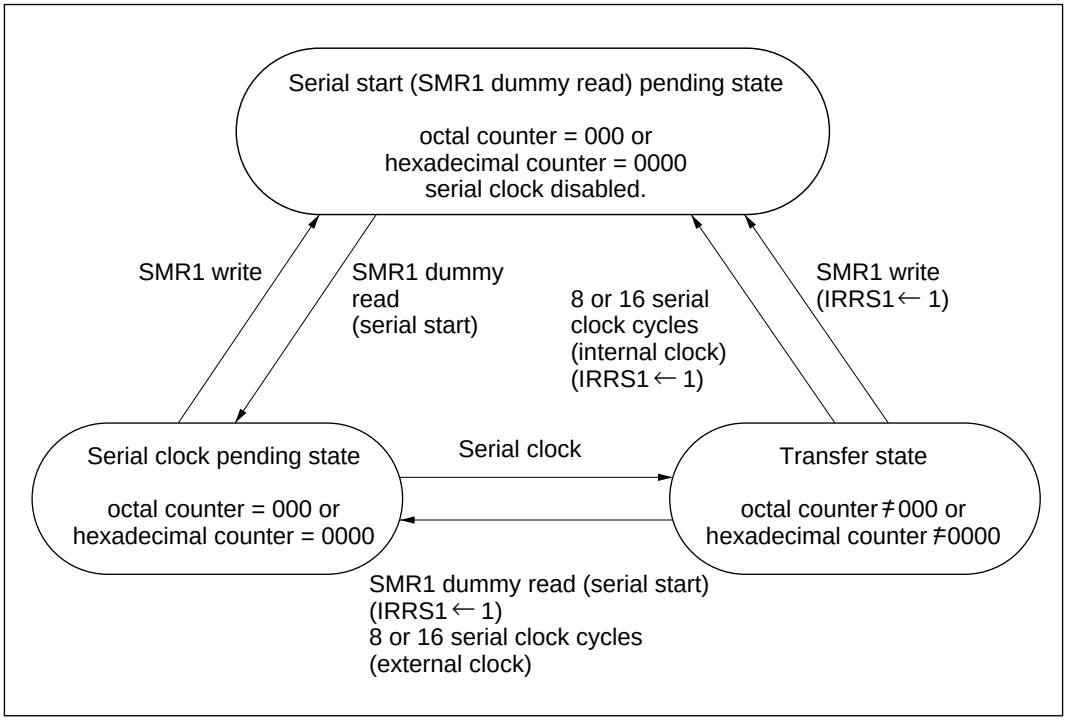


Figure 10-3 SCI1 State Transitions

10.3.6 Serial Clock Error Detection

In the transfer state, if an extraneous pulse is superimposed on the normal serial clock signal due to external noise, SCI1 may function incorrectly. Serial clock errors can be detected by means of the procedure shown in figure 10-4.

In the transfer clock pending state, if more than the normal 8 or 16 serial clock cycles are mistakenly input, SCI1 changes from the transfer state to the transfer clock pending state and then back to the transfer state. After bit IRRS1 in interrupt request register 3 (IRR3) is cleared to 0, writing a value in serial mode register 1 (SMR1) changes the state to serial start pending, and bit IRRS1 is again set to 1.

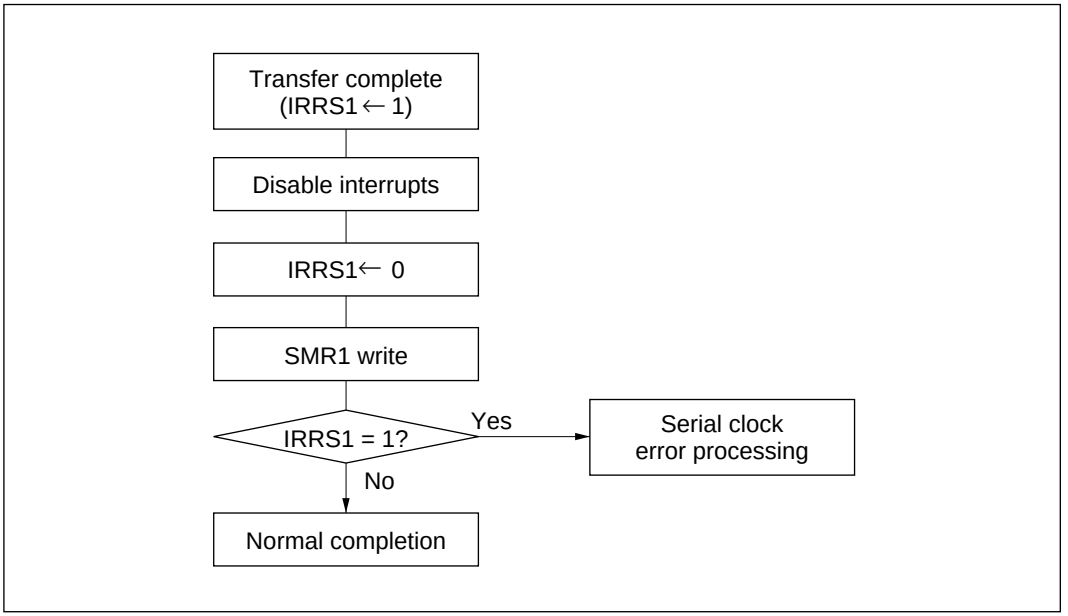


Figure 10-4 Procedure for Detecting Serial Clock Errors

10.3.7 Interrupts

SCI1 can generate interrupts for completion of transfer and for transmit/receive errors. These interrupts are assigned to the same vector address.

When an SCI1 transfer is complete, or when a transmit/receive error occurs before the transfer is complete, bit IRRS1 in interrupt request register 3 (IRR3) is set to 1. SCI1 interrupt requests can be enabled or disabled in bit IENS1 of interrupt enable register 3 (IENR3).

For further details, see 3.2.2, Interrupts.

Section 11 SCI2

11.1 Overview

Serial communication interface 2 (SCI2) has a 32-byte data buffer, for synchronous serial transfer of up to 32 bytes of data in one operation.

11.1.1 Features

SCI2 features are as follows.

- Automatic transfer of up to 32 bytes of data
- Choice of internal clock sources (ϕ/8, ϕ/4, ϕ/2) or an external clock
- Interrupts requested at completion of transfer or when error occurs

11.1.2 Block Diagram

Figure 11-1 shows a block diagram of SCI2.

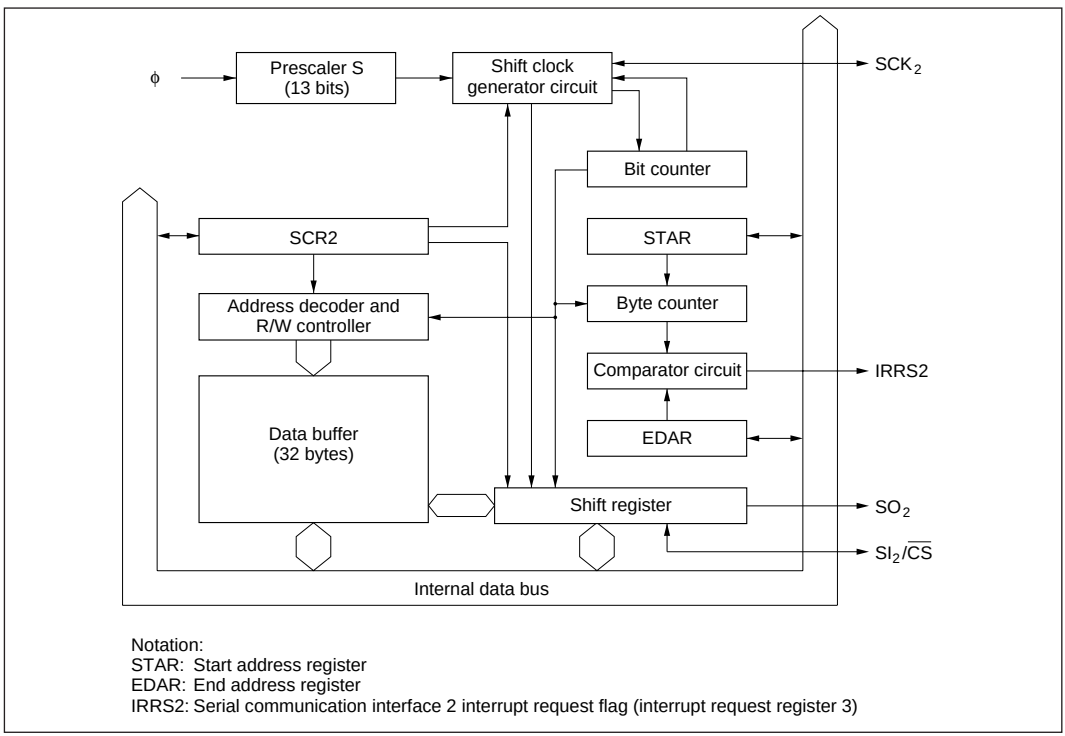


Figure 11-1 Block Diagram of SCI2

11.1.3 Pin Configuration

Table 11-1 shows the SCI2 pin configuration.

Table 11-1 Pin Configuration

Name	Abbrev.	I/O	Function
SCI2 clock pin	SCK_2	I/O	SCI2 clock input/output
SCI2 data input pin	SI_2	Input	SCI2 receive data input
SCI2 data output pin	SO_2	Output	SCI2 transmit data output
SCI2 chip select output pin	$\overline{CS}$	Output	SCI2 chip select output

Note: Functions of pins $P9_4/SCK_2$, $P9_5/SI_2/\overline{CS}$, and $P9_6/SO_2$ are switched in port mode register 2 (PMR2) and port mode register 3 (PMR3). For PMR2, see 7.10.2 1, Port mode register 2 (PMR2).

11.1.4 Register Configuration

Table 11-2 shows the SCI2 register configuration.

Table 11-2 SCI2 Registers

Name	Abbrev.	R/W	Initial Value	Address
32-byte data buffer	—	R/W	Not fixed	H'FF80 to H'FF9F
Start address register	STAR	R/W	H'E0	H'FFA0
End address register	EDAR	R/W	H'E0	H'FFA1
Serial control register 2	SCR2	R/W	H'E0	H'FFA2
Status register	STSR	R/W	H'E0/H'E8	H'FFA3
Port mode register 2	PMR2	R/W	H'00	H'FFEC
Port mode register 3	PMR3	R/W	H'97	H'FFED

11.2 Register Descriptions

11.2.1 Start Address Register (STAR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	STA4	STA3	STA2	STA1	STA0
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

STAR is an 8-bit read/write register, for designating the transfer start address in the memory area from H'FF80 to H'FF9F allocated to the 32-byte data buffer.

The 32 bytes from H'00 to H'1F designated by the lower 5 bits of STAR (bits STA4 to STA0) correspond to addresses H'FF80 to H'FF9F.

Data is sent or received continuously using the area defined in STAR and in the end address register (EDAR).

Bits 7 to 5 are reserved; they always read 1, and cannot be modified.

Upon reset, STAR is initialized to H'E0.

11.2.2 End Address Register (EDAR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	EDA4	EDA3	EDA2	EDA1	EDA0
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

EDAR is an 8-bit read/write register, for designating the transfer end address in the memory area from H'FF80 to H'FF9F allocated to the 32-byte data buffer.

The 32 bytes from H'00 to H'1F designated by the lower 5 bits of EDAR (bits EDA4 to EDA0) correspond to addresses H'FF80 to H'FF9F.

Data is sent or received continuously using the area defined in STAR and EDAR. If the same value is designated in both STAR and EDAR, only one byte of data is transferred.

Bits 7 to 5 are reserved; they always read 1, and cannot be modified.

Upon reset, EDAR is initialized to H'E0.

11.2.3 Serial Control Register 2 (SCR2)

Bit	7	6	5	4	3	2	1	0
	—	—	—	I/O	GAP2	GAP1	PS1	PS0
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

SCR2 is an 8-bit read/write register, for selecting whether SCI2 transmits or receives, for gap insertion during continuous transfer, and for serial clock selection.

Upon reset, SCR2 is initialized to H'E0.

Bits 7 to 5: Reserved bits

Bits 7 to 5 are reserved; they always read 1, and cannot be modified.

Bit 4: Transmit/receive select (I/O)

Bit 4 selects SCI2 transmit or receive mode.

Bit 4 I/O	Description	
0	SCI2 is in receive mode.	(initial value)
1	SCI2 is in transmit mode.	

Bits 3 and 2: Gap select (GAP2 to GAP1)

When data is transmitted or received continuously, gaps can be inserted at data divisions by holding the serial clock high for a length of time designated by bits 3 and 2. Bits 3 and 2 are valid when an internal clock source is selected as the serial clock (PS1 and 0 ≠ 11).
Data divisions may be placed every 8 bits or 16 bits; this is selected in bit GIT in the status register (STSR).

Bit 3 GAP2	Bit 2 GAP1	Description	
0	0	Serial clock keeps the same duty cycle even at data divisions.	(initial value)
0	1	Serial clock high level extended by one clock cycle at data divisions.	
1	0	Serial clock high level extended by two clock cycles at data divisions.	
1	1	Serial clock high level extended by eight clock cycles at data divisions.	

Bits 1 and 0: Serial clock select (PS1 to PS0)

Bits 1 and 0 select one of three internal clock sources or an external clock.

Bit 1 PS1	Bit 2 PS0	Pin SCK_2	Clock Source	Prescaler Divider Ratio	Serial Clock Period		
					ϕ = 4 MHz	ϕ = 2 MHz	ϕ = 1 MHz
0	0	SCK_2 output	Prescaler S	ϕ/2 (initial value)	*	1 µs	2 µs
0	1	SCK_2 output	Prescaler S	ϕ/4	1 µs	2 µs	4 µs
1	0	SCK_2 output	Prescaler S	ϕ/8	2 µs	4 µs	8 µs
1	1	SCK_2 input	External clock	—	—	—	—

Note: * Can be set, but operation is not guaranteed.

11.2.4 Status Register (STSR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	SO2 LAST BIT	OVR	WT	GIT	STF
Initial value	1	1	1	0	*1	0	0	0
Read/Write	—	—	—	R/W	R/W*2	R/W*2	R/W	R/W

Notes: 1. Not fixed
2. Cleared to 0 by write operation to STSR.

STSR is an 8-bit register indicating the SCI2 operation state, error status, etc. Writing to this register during data transmission may cause misoperation.

Upon reset, STSR is initialized to H'E0 or H'E8.

Bits 7 to 5: Reserved bits

Bits 7 to 5 are reserved; they always read 1, and cannot be modified.

Bit 4: Extended data bit (SO2 LAST BIT)

Bit 4 holds the last bit of transmitted data after transmission ends.

Output from pin SO_2 can be altered by software by modifying this bit either before or after transmission.

Writing to this bit during data transmission may cause misoperation.

Bit 4 SO2 LAST BIT	Description	
0	Output from pin SO_2 is low.	(initial value)
1	Output from pin SO_2 is high.	

Bit 3: Overrun flag (OVR)

If the amount of data transferred exceeds the buffer size setting, or if an extraneous pulse is superimposed on the normal serial clock due to external noise, SCI2 overruns and bit 3 is set to 1.

Bit 3 OVR	Description	
0	[Clear conditions] When STSR is written to.	(initial value)
1	[Set conditions] When overrun occurs.	

Bit 2: Waiting flag (WT)

If an attempt is made to execute a read or write instruction to the 32-byte buffer during a serial data transfer, the instruction is ignored, and bit 2 is set to 1 along with bit IRRS2 in interrupt request register 3 (IRR3).

Bit 2 WT	Description	
0	[Clear conditions] When STSR is written to.	(initial value)
1	[Set conditions] When a read/write to the 32-byte buffer is attempted during serial transfer.	

Bit 1: Gap interval flag (GIT)

Bit 1 designates whether the extended serial clock high-level interval designated in bits GAP2 and GAP1 in serial control register 2 (SCR2) occurs every 8 bits or every 16 bits. This setting is valid only for internal clock operation.

Bit 1 GIT	Description	
0	Gap specified by GAP2 and GAP1 is inserted every 16 bits.	(initial value)
1	Gap specified by GAP2 and GAP1 is inserted every 8 bits.	

Bit 0: Start/busy flag (STF)

Setting bit 0 to 1 starts an SCI2 transfer operation. This bit stays at 1 during the transfer, and is cleared to 0 after the transfer is complete. It can therefore be used as a busy flag as well. Clearing this bit to 0 during a transfer aborts the transfer, initializing SCI2. The contents of the 32-byte data buffer and of registers other than STSR are unchanged when this happens.

Bit 0 STF	Explanation	
0	[Read access] Indicates transfer not in progress.	(initial value)
	[Write access] Stops transfer.	
1	[Read access] Indicates transfer in progress.	
	[Write access] Starts transfer.	

11.2.5 Port Mode Register 3 (PMR3)

Bit	7	6	5	4	3	2	1	0
	—	SO2 PMOS	CS	—	SO1 PMOS	—	—	—
Initial value	1	0	0	1	0	1	1	1
Read/Write	—	R/W	R/W	—	R/W	—	—	—

PMR3 is an 8-bit read/write register, for enabling the PMOS transistors of SCI1 and SCI2 data output pins (pin $P9_3/SO_1$ and pin $P9_6/SO_2$), and for controlling SCI2 chip select output (pin $SI_2/\overline{CS}$).

Upon reset, PMR3 is initialized to H'97.

For bit 3, see 10.2.6, Port Mode Register 3 (PMR3).

Bit 7: Reserved bit

Bit 7 is reserved; it always reads 1, and cannot be modified.

Bit 6: Pin SO_2 PMOS on/off (SO2PMOS)

Bit 6 enables or disables the PMOS buffer transistor of pin $P9_6/SO_2$.

Bit 6 SO2PMOS	Description	
0	PMOS transistor of pin $P9_6/SO_2$ is enabled: CMOS output.	(initial value)
1	PMOS transistor of pin $P9_6/SO_2$ is disabled: NMOS open-drain output.	

Bit 5: Chip select output select (CS)

In combination with bit SI2 in port mode register 2 (PMR2), bit 5 selects the $\overline{CS}$ output function of pin $P9_5/SI_2/\overline{CS}$. The $\overline{CS}$ output pin function is valid when an internal clock source is selected as the serial clock, and only in transmit mode.

PMR2	PMR3		
Bit 5 SI2	Bit 5 CS	Description	
0	0	Pin $P9_5/SI_2/\overline{CS}$ functions as $P9_5$ I/O pin.	(initial value)
	1	Pin $P9_5/SI_2/\overline{CS}$ functions as $P9_5$ I/O pin.	
1	0	Pin $P9_5/SI_2/\overline{CS}$ functions as SI_2 input pin.	
	1	Pin $P9_5/SI_2/\overline{CS}$ functions as $\overline{CS}$ output pin.	

Bits 4 and 2 to 0: Reserved bits

These bits are reserved; they always read 1, and cannot be modified.

11.3 Operation

11.3.1 Overview

SCI2 has a 32-byte data buffer, making possible continuous transfer of up to 32 bytes of data with one operation. SCI2 transmits and receives data in synchronization with clock pulses.

Selection of transmit or receive mode and of the serial clock is made in serial control register 2 (SCR2).

The start address register (STAR) and end address register (EDAR) designate the area within the 32-byte data buffer for holding transfer data. The address range from H'FF80 to H'FF9F is allocated to this data buffer. The start and end positions of the transfer data area are indicated in the lower 5 bits of STAR and EDAR.

After parameters have been set in port mode register 2 (PMR2), port mode register 3 (PMR3), SCR2, STAR, and EDAR, then when the STF bit of the status register (STSR) is set to 1, SCI2 begins a transfer operation. STF remains set to 1 during the transfer, and is cleared to 0 when the transfer is complete. The STF bit can therefore be used as a busy flag. Clearing the STF bit to 0 during a transfer stops the transfer operation and initializes SCI2. The contents of the data buffer and of other registers are unchanged in this case.

During a transfer, the CPU cannot read or write the data buffer. If a write instruction is issued it is ignored; it has the same effect as a NOP instruction except that it takes more states. Read access during a transfer yields H'FF.

When the transfer is complete, or if a data buffer read or write is attempted during the transfer, bit IRRS2 in interrupt request register 3 (IRR3) is set to 1. In case of an overrun error or a data buffer read or write during the transfer, bit OVR or WT of STSR is set to 1.

Note: If the start address is set to a value higher than the end address, the result is as shown in figure 11-2. The data transfer wraps around from address H'FF9F to address H'FF80 and continues to the end address.

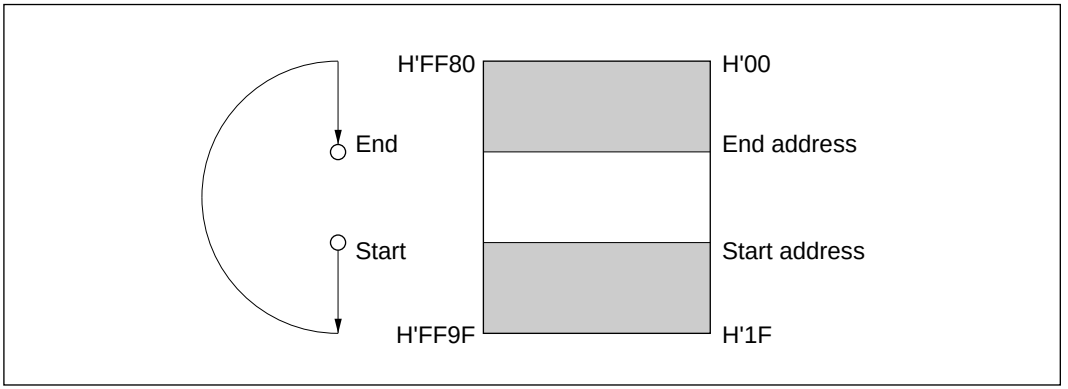


Figure 11-2 Operation When Start Address Exceeds End Address

11.3.2 Clock

Three internal clock sources or an external clock may be selected as the serial clock. When an internal clock is selected, pin SCK_2 becomes the clock output pin.

11.3.3 Data Transfer Format

Figure 11-3 shows the SCI2 data transfer format. Data is sent and received starting from the least significant bit, in LSB-first format. Transmit data is output from one falling edge of the serial clock until the next falling edge. Receive data is latched at the rising edge of the clock.

When SCI2 operates on an internal clock and is in transmit mode, a gap may be inserted at data divisions (every 8 bits or 16 bits). During this gap, the serial clock stays at the high level for a designated number of clock cycles (see figures 11-4 through 11-6).

The $\overline{CS}$ output remains low during the gap.

Gap insertion and the length of the gap are designated in bits GAP2 and GAP1 in serial control register 2 (SCR2). Bit GIT in the status register (STSR) designates whether gaps occur at 8-bit or 16-bit intervals.

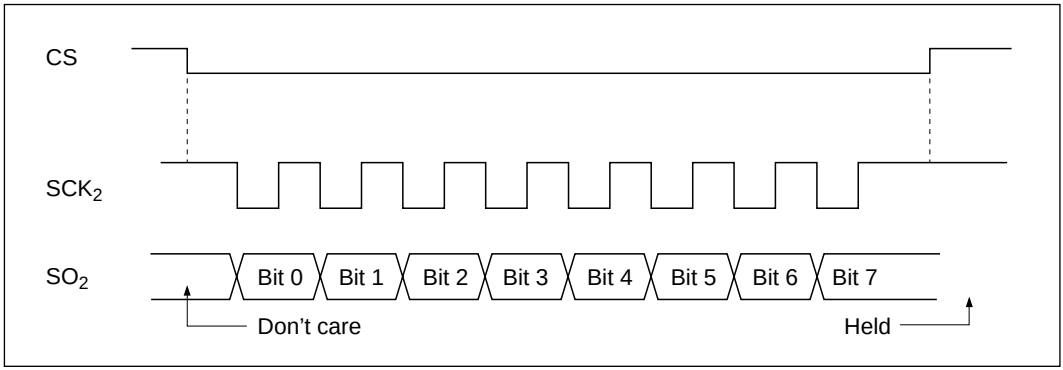


Figure 11-3 Synchronous Data Transfer Format

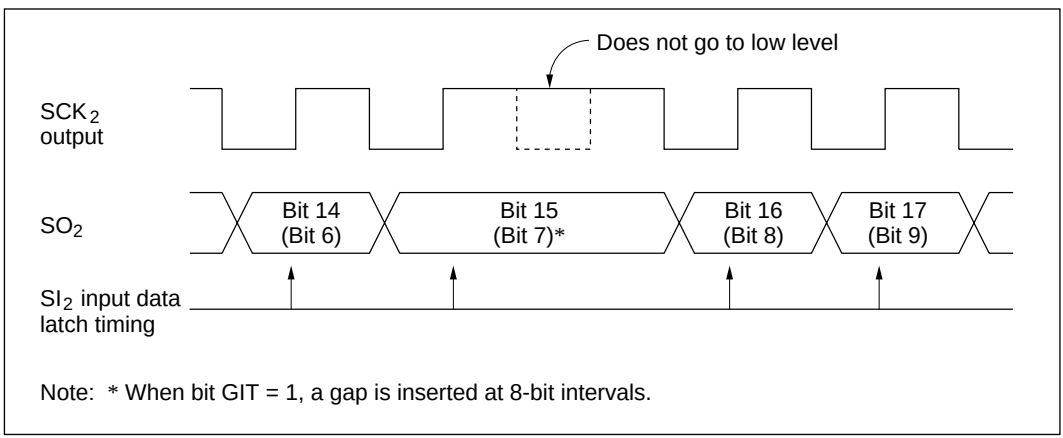


Figure 11-4 1-Clock Gap Insertion (Bits GAP2 and GAP1 = 01)

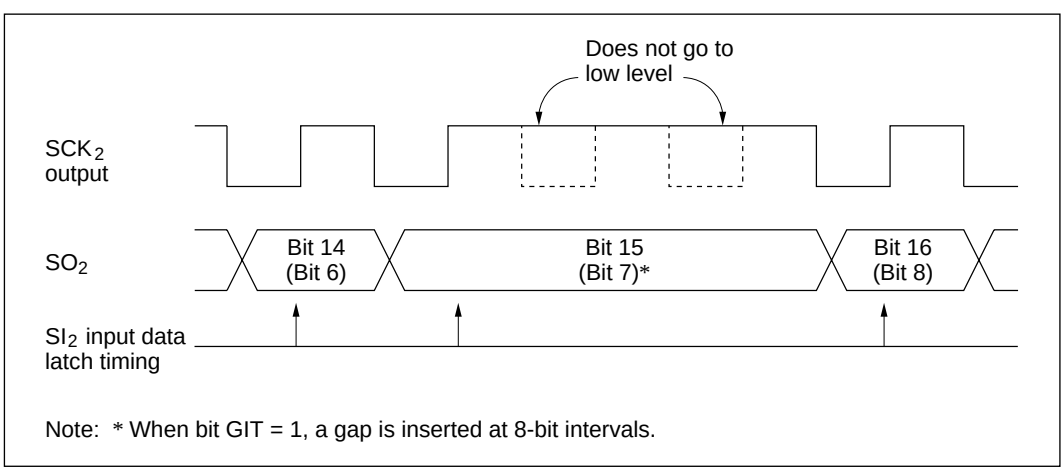


Figure 11-5 2-Clock Gap Insertion (Bits GAP2 and GAP1 = 10)

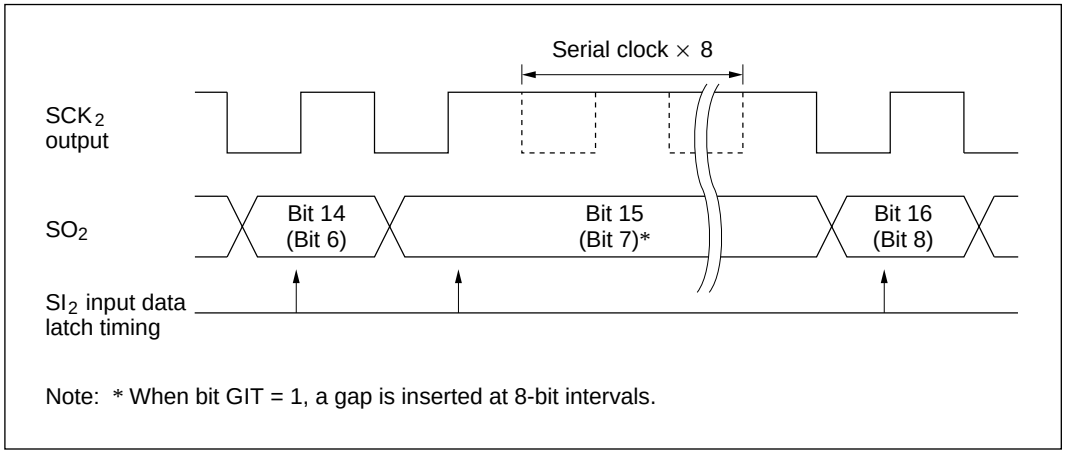


Figure 11-6 8-Clock Gap Insertion (Bits GAP2 and GAP1 = 11)

11.3.4 Data Transmit/Receive

1. SCI2 initialization

   Serial communication on SCI2 first of all requires that SCI2 be initialized by software. This involves clearing bit STF in the status register (STSR) to 0, then selecting pin functions and transfer modes in port mode register 2 (PMR2), port mode register 3 (PMR3), the start address register (STAR), the end address register (EDAR), and serial control register 2 (SCR2).

2. Transmitting

   A transmit operation is carried out as follows.

- Set bit SO2 in port mode register 2 (PMR2) to 1, making pin $P9_6/SO_2$ the SO_2 output pin. If necessary, set the SO2PMOS bit and CS bit in PMR3 for NMOS open-drain output at pin SO_2 and for chip select output at pin $P9_5/SI_2/\overline{CS}$.
- Write transmit data in the 32-byte data buffer (H'FF80 to H'FF9F).
- Set the transfer start address in the lower 5 bits of STAR.
- Set the transfer end address in the lower 5 bits of EDAR.
- In SCR2, select transmit mode (bit I/O = 1), the serial clock, and gap insertion (internal clock operation only).
- Select the data gap interval with bit GIT of STRS, then set bit STF to 1. Setting bit STF starts the transmit operation.

- After data transmission is complete, bit IRRS2 in interrupt request register 3 (IRR3) is set to 1, and bit STF in STSR is cleared to 0.

If an internal clock source is used, a serial clock is output from pin SCK_2 in synchronization with the transmit data. After data transmission is completed, the serial clock is not output until bit STF is again set. During this time, pin SO2 continues to output the value of the last bit transmitted.

When an external clock source is used, data is transmitted in synchronization with the serial clock input at pin SCK_2. After data transmission is completed, further transmission does not take place even if the serial clock continues to be input; pin SO_2 continues to output the value of the last bit transmitted.

Between transmissions, the output value of pin SO_2 can be changed by rewriting bit SO2 LAST BIT in STSR.

An attempt to read or write the data buffer during transmission will cause bit IRRS2 in IRR3 to be set to 1. Bit WT in STSR will also be set to 1.

3. Receiving

   A receive operation is carried out as follows.

- Set bit SI2 in port mode register 2 (PMR2) to 1, making pin $P9_5/SI_1$/CS the SI_2 input pin.
- Allocate an area to hold the received data in the 32-byte data buffer and set the start address in the lower 5 bits of the start address register (STAR).
- Set the transfer end address in the lower 5 bits of the end address register (EDAR).
- In serial control register 2 (SCR2), select receive mode (bit I/O = 0) and the serial clock.
- Set bit STF of the status register (STSR) to 1, starting the receive operation.
- After receiving is completed, bit IRRS2 in interrupt request register 3 (IRR3) is set to 1, and bit STF is cleared to 0.
- Read the received data from the data buffer.

If an internal clock source is used, setting bit STF to 1 in STSR immediately starts a data receive operation. The serial clock is output from pin SCK_2.

When an external clock source is used, after bit STF is set, data is received in synchronization with the clock input at pin SCK_2. After receiving is completed, no further receive operations take place until bit STF is again set, even if the serial clock continues to be input.

An attempt to read or write the data buffer during receiving will cause bit IRRS2 in IRR3 and bit WT in STSR to be set to 1. Bit OVR in STSR is set to 1 if an overrun error occurs.

When SCI2 operates on an internal clock and is in transmit mode, a gap may be inserted at data divisions (every 8 bits or 16 bits). During this gap, serial clock stays at the high level for a designated number of clock cycles (see figures 11-4 through 11-6).

Gap insertion and the length of the gap are designated in bits GAP2 and GAP1 of SCR2. Bit GIT of STSR designates whether gaps occur at 8-bit or 16-bit intervals.

11.4 Interrupts

SCI2 can generate interrupts when a transfer is completed and when the data buffer is read or written during a transfer. These interrupts are assigned to the same vector address.

When the above conditions occur, bit IRRS2 in interrupt request register 3 (IRR3) is set to 1. SCI2 interrupt requests can be enabled or disabled in bit IENS2 of interrupt enable register 3 (IENR3). For further details, see 3.2.2, Interrupts.

When an overrun error occurs, or when a read or write of the data buffer is attempted during a transfer, the OVR or WT bit in the status register (STSR) is set to 1. These bits can be used to determine the cause of the error.

11.5 Application Notes

1. Do not write to any register during a transfer (while bit STF of STSR is set to 1), since this can cause misoperation.

2. When receiving, set bit SI2 in port mode register 2 (PMR2) to 1 and clear bit CS in port mode register 3 (PMR3) to 0 to select the SI_2 pin function. If bit CS = 1 and bit SI2 = 1, selecting the $\overline{CS}$ pin function, incorrect data will be received.

Section 12 VFD Controller/Driver

12.1 Overview

The H8/3714 Series is equipped with an on-chip vacuum fluorescent display (VFD) controller/driver and high-voltage, high-current pins, for direct VFD driving.

12.1.1 Features

The VFD controller/driver has the following features.

- Maximum of 24 segment pins and 16 digit pins (20 segment pins, eight digit pins, and eight switched segment/digit pins).
- Brightness can be adjusted in eight steps (dimmer function).
- Automatic shifting of displayed digit.
- Digit pins and segment pins can be switched over to use as general-purpose high-voltage pins.
- Optional key scan interval.
- Interrupt generated when key scan interval starts.

12.1.2 Block Diagram

Figure 12-1 shows a block diagram of the VFD controller/driver.

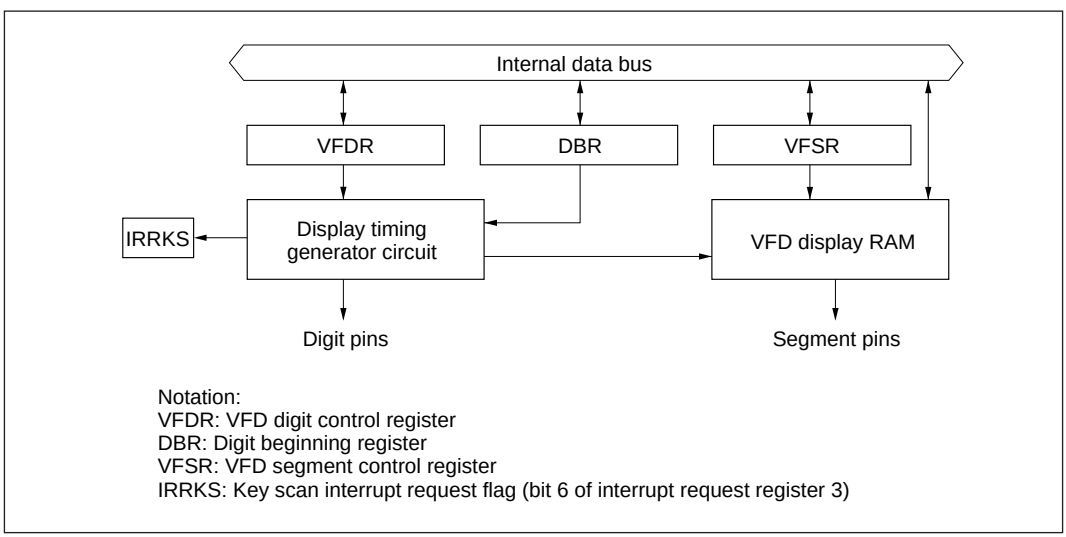


Figure 12-1 Block Diagram of VFD Controller/Driver

12.1.3 Pin Configuration

Table 12-1 shows the VFD controller/driver pin configuration.

Table 12-1 Pin Configuration

Name	Abbrev.	I/O	Function
Digit/segment pins	FD_0/FS_7 to FD_7/FS_0	Output	Digit or segment pins for vacuum fluorescent display (function selected in DBR for each bit)
Digit pins	FD_8 to FD_{15}	Output	Digit pins for vacuum fluorescent display
Segment pins	FS_8 to FS_{23}	Output	Segment pins for vacuum fluorescent display

12.1.4 Register Configuration

Table 12-2 shows the VFD controller/driver register configuration.

Table 12-2 Register Configuration

Name	Abbrev.	R/W	Initial Value	Address
VFD display RAM	—	R/W	Not fixed	H'FEC0 to H'FEFF
VFD segment control register	VFSR	R/W	H'20	H'FFB9
VFD digit control register	VFDR	R/W	H'00	H'FFBA
Digit beginning register	DBR	R/W	H'20	H'FFBB

12.2 Register Descriptions

12.2.1 VFD Digit Control Register (VFDR)

Bit	7	6	5	4	3	2	1	0
	FLMO	DM2	DM1	DM0	DR3	DR2	DR1	DR0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

VFDR is an 8-bit read/write register for control of digit output.

Upon reset, VFDR is initialized to H'00.

Bit 7: VFD mode bit (FLMO)

Bit 7 designates the time per digit (T_{digit}) and the dimmer resolution (T_{dimmer}). T_{digit} is also the time per key scan.

Bit 7 FLMO	Digit/Key Scan Time (T_{digit})			Dimmer Resolution (T_{dimmer})		
	Period	ϕ = 4 MHz	ϕ = 2 MHz	Period	ϕ = 4 MHz	ϕ = 2 MHz
0	1536/ϕ (initial value)	384 µs	768 µs	96/ϕ (initial value)	24 µs	48 µs
1	768/ϕ	192 µs	384 µs	48/ϕ	12 µs	24 µs

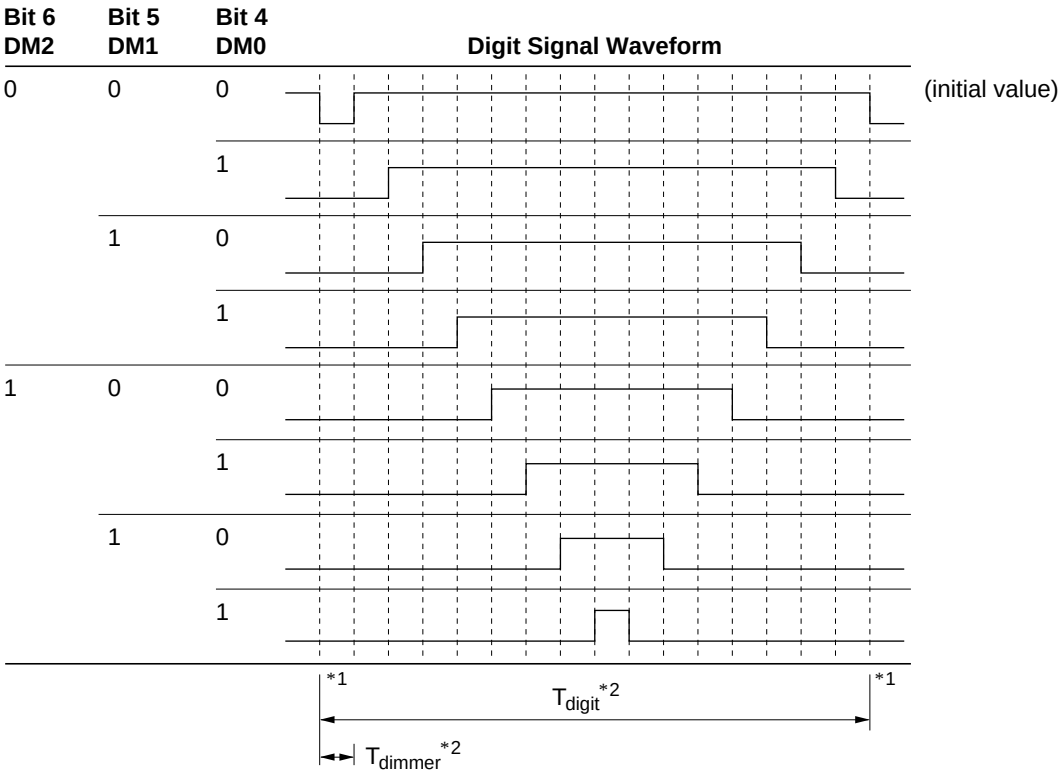
The frame period (T_{frame}) is calculated using the equation below.

$T_{frame} = T_{digit} \times (D + K)$

D: Number of digit pins used
K: 1 if key scan is used; 0 if not used

Bits 6 to 4: Digit waveform select (DM2 to DM0)

Bits 6 to 4 select the digit waveform.



Notes: 1. Segment signal transition timing
2. For T_{dimmer} and T_{digit}, see under FLMO bit.

Bits 3 to 0: Digit pin select (DR3 to DR0)

Bits 3 to 0, in combination with bits 3 to 0 of the digit beginning register (DBR), designate the digit pins used.

Bit 3 DR3	Bit 2 DR2	Bit 1 DR1	Bit 0 DR0	Pins Valid as Digit Pins	
0	0	0	0	FD_0 to FD_{15}	(initial value)
0	0	0	1	FD_0 to FD_{14}	
0	0	1	0	FD_0 to FD_{13}	
0	0	1	1	FD_0 to FD_{12}	
0	1	0	0	FD_0 to FD_{11}	
0	1	0	1	FD_0 to FD_{10}	
0	1	1	0	FD_0 to FD_9	
0	1	1	1	FD_0 to FD_8	
1	0	0	0	FD_0 to FD_7	
1	0	0	1	FD_0 to FD_6	
1	0	1	0	FD_0 to FD_5	
1	0	1	1	FD_0 to FD_4	
1	1	0	0	FD_0 to FD_3	
1	1	0	1	FD_0 to FD_2	
1	1	1	0	FD_0 to FD_1	
1	1	1	1	FD_0	

Note: For the switching between digit and segment use of pins FD_0/FS_7 to FD_7/FS_0, which can function as either digit or segment pins, see 12.2.3, Digit Beginning Register (DBR).

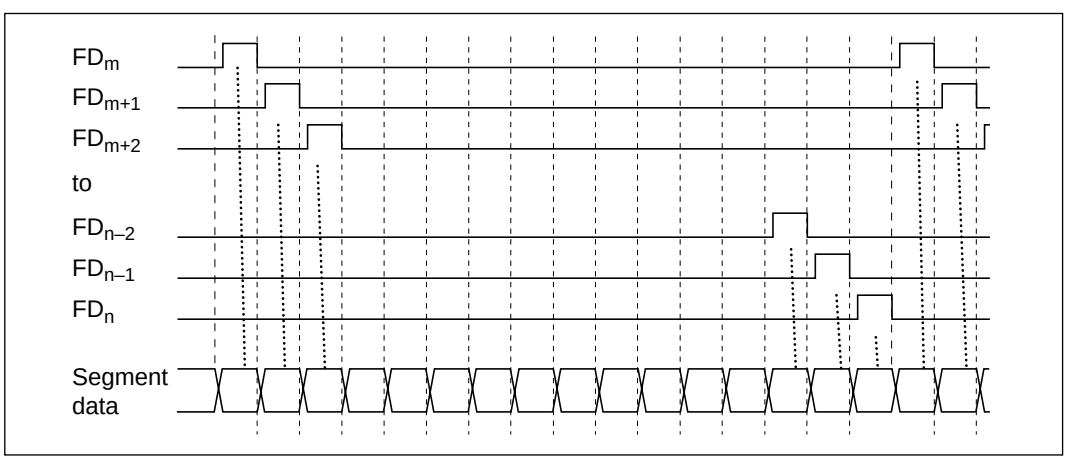


Figure 12-2 Order of Digit Output

12.2.2 VFD Segment Control Register (VFSR)

Bit	7	6	5	4	3	2	1	0
	VFLAG	KSE	—	SR4	SR3	SR2	SR1	SR0
Initial value	0	0	1	0	0	0	0	0
Read/Write	R/W	R/W	—	R/W	R/W	R/W	R/W	R/W

VFSR is an 8-bit read/write register for control of segment output.

Upon reset, VFSR is initialized to H'20.

Bit 7: VFD/port switching flag (VFLAG)

Bit 7 designates whether pins Pnn/FDnn and Pnn/FSnn are used as VFD pins (FDnn, FSnn) or as general-purpose ports (Pnn).

Bit 7 VFLAG	Description	
0	All of pins Pnn/FDnn and all of pins Pnn/FSnn function as general-purpose ports.	(initial value)
1	Pnn/FDnn and Pnn/FSnn function as VFD pins according to the designations in bits DR3 to DR0 in the VFD digit control register (VFDR), bits SR4 to SR0 in VFSR, and bits DBR3 to DBR0 in the digit beginning register (DBR).	

Note: Even when this flag is set to 1, during a key scan interval the segment pins function as general-purpose ports; for this reason, when this flag is read during a key scan interval it reads 0.

Bit 6: Key scan enable (KSE)

Bit 6 enables or disables the addition of a key scan interval (T_{digit}) to the VFD operation frame specified by the combination of bits DR3 to DR0 in the VFD digit control register, bits SR4 to SR0 in the VFD segment control register, and bits DBR3 to DBR0 in the digit beginning register.

Bit 6 KSE	Description	
0	No key scan interval.	(initial value)
1	A key scan interval can be added. See also under bit 7 (VFLAG) above.	

Bit 5: Reserved bit

Bit 5 is reserved; it always reads 1, and cannot be modified.

Bits 4 to 0: Segment pin select (SR4 to SR0)

Bits 4 to 0, in combination with bits 3 to 0 of the digit beginning register (DBR), designate the segment pins used.

Bit4 SR4	Bit 3 SR3	Bit 2 SR2	Bit 1 SR1	Bit 0 SR0	Pins Valid as Segment Pins	
0	0	0	0	0	FS_0	(initial value)
0	0	0	0	1	FS_0 to FS_1	
0	0	0	1	0	FS_0 to FS_2	
0	0	0	1	1	FS_0 to FS_3	
0	0	1	0	0	FS_0 to FS_4	
0	0	1	0	1	FS_0 to FS_5	
0	0	1	1	0	FS_0 to FS_6	
0	0	1	1	1	FS_0 to FS_7	
0	1	0	0	0	FS_0 to FS_8	
0	1	0	0	1	FS_0 to FS_9	
0	1	0	1	0	FS_0 to FS_{10}	
0	1	0	1	1	FS_0 to FS_{11}	
0	1	1	0	0	FS_0 to FS_{12}	
0	1	1	0	1	FS_0 to FS_{13}	
0	1	1	1	0	FS_0 to FS_{14}	
0	1	1	1	1	FS_0 to FS_{15}	
1	0	0	0	0	FS_0 to FS_{16}	
1	0	0	0	1	FS_0 to FS_{17}	
1	0	0	1	0	FS_0 to FS_{18}	
1	0	0	1	1	FS_0 to FS_{19}	
1	0	1	0	0	FS_0 to FS_{20}	
1	0	1	0	1	FS_0 to FS_{21}	
1	0	1	1	0	FS_0 to FS_{22}	
1	0	1	1	1	FS_0 to FS_{23}	
1	1	0	0	0		
1	1	0	0	1		
1	1	0	1	0		
1	1	0	1	1		
1	1	1	0	0		
1	1	1	0	1		
1	1	1	1	0		
1	1	1	1	1		

Note: For the switching between digit and segment use of pins FD_0/FS_7 to FD_7/FS_0, which can function as either digit or segment pins, see 12.2.3, Digit Beginning Register (DBR).

12.2.3 Digit Beginning Register (DBR)

Bit	7	6	5	4	3	2	1	0
	VFDE	DISP	—	—	DBR3	DBR2	DBR1	DBR0
Initial value	0	0	1	0	0	0	0	0
Read/Write	R/W	R/W	—	R/W	R/W	R/W	R/W	R/W

DBR is an 8-bit read/write register for on/off control of the VFD controller/driver and for switching functions of pins that can be either digit or segment pins.

Bit 7: VFD enable (VFDE)

Bit 7 switches the VFD controller/driver on and off.

Bit 7 VFDE	Description
0	VFD controller/driver is in reset state. (initial value)
1	VFD controller/driver is operative.

Note: This setting is unrelated to whether pins Pnn/FDnn and Pnn/FSnn are used as VFD pins or as general-purpose ports.

Bit 6: Display bit (DISP)

Bit 6 switches the display on and off.

Bit 6 DISP	Description
0	All segment pins (FS) are in the non-illuminating state (pulled down). (initial value) Register and RAM values are unchanged. Digit pins (FD) continue operating.
1	Display RAM data is output to segment pins (FS).

Bit 5: Reserved bit

Bit 5 is reserved; it always reads 1, and cannot be modified.

Bit 4: Reserved bit

Bit 4 is reserved, but it can be written and read.

Bits 3 to 0: Digit/segment pin function switch (DBR3 to DBR0)

Bits 3 to 0 designate the first digit pin and the first segment pin of those pins that can function both ways. Bits DR3 to DR0 of the VFD digit control register (VFDR) and bits SR4 to SR0 of VFSR must be set so that the first digit and segment pins are operational. Otherwise these pins will not function.

Bit 3 DBR3	Bit 2 DBR2	Bit 1 DBR1	Bit 0 DBR0	Functions of FD_0/FS_7 to FD_7/FS_0	
0	0	0	0	FD_0 to FD_7	(initial value)
0	0	0	1	FD_1 to FD_7, FS_7	
0	0	1	0	FD_2 to FD_7, FS_7 to FS_6	
0	0	1	1	FD_3 to FD_7, FS_7 to FS_5	
0	1	0	0	FD_4 to FD_7, FS_7 to FS_4	
0	1	0	1	FD_5 to FD_7, FS_7 to FS_3	
0	1	1	0	FD_6 to FD_7, FS_7 to FS_2	
0	1	1	1	FD_7, FS_7 to FS_1	
1	*	*	*	FS_7 to FS_0	

Notes: Digit pins (FD) and segment pins (FS) are controlled by both VFDR and VFSR. During a key scan interval, digit pins (FD) and segment pins (FS) function as general-purpose ports.

* Don’t care.

12.3 Operation

12.3.1 Overview

The VFD controller/driver may use up to 24 segment pins (FS) and up to 16 digit pins (FD). Of these, 8 pins may be used as either segment or digit pins; their function is switched in the digit beginning register (DBR). The 32 pins assigned to the VFD controller are high-voltage, high-current pins capable of directly driving a VFD.

12.3.2 Control Section

The control section consists of the VFD digit control register (VFDR), VFD segment control register (VFSR), digit beginning register (DBR), display timing generator circuit, and VFD display RAM (see figure 12-1).

Display timing is determined by the number of digits per frame. When the key scan feature is activated, the frame is extended by one digit; during that interval only, segment pins and digit pins may be used as general purpose ports by the CPU. These pins are in the non-illuminating state (pulled down) during the key scan interval.

12.3.3 RAM Bit Correspondence to Digits/Segments

VFD display data is set in the VFD display RAM at addresses H'FEC0 through H'FEFF.
Table 12-3 shows the correspondence between digit/segment pins and the VFD display RAM bits.

Table 12-3 Digit/Segment Pins and VFD Display RAM Bits

Port	Seg / Dig	— — — — — — — —	4_7 4_6 4_5 4_4 4_3 4_2 4_1 4_0	5_0 5_1 5_2 5_3 5_4 5_5 5_6 5_7	6_0 6_1 6_2 6_3 6_4 6_5 6_6 6_7	Seg / Dig	Port
		— — — — — — — —	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0		
6_0	0	H'FEC3	H'FEC2	H'FEC1	H'FEC0	0	6_0
6_1	1	H'FEC7	H'FEC6	H'FEC5	H'FEC4	1	6_1
6_2	2	H'FECB	H'FECA	H'FEC9	H'FEC8	2	6_2
6_3	3	H'FECF	H'FECE	H'FECD	H'FECC	3	6_3
6_4	4	H'FED3	H'FED2	H'FED1	H'FED0	4	6_4
6_5	5	H'FED7	H'FED6	H'FED5	H'FED4	5	6_5
6_6	6	H'FEDB	H'FEDA	H'FED9	H'FED8	6	6_6
6_7	7	H'FEDF	H'FEDE	H'FEDD	H'FEDC	7	6_7
7_0	8	H'FEE3	H'FEE2	H'FEE1	H'FEE0	8	7_0
7_1	9	H'FEE7	H'FEE6	H'FEE5	H'FEE4	9	7_1
7_2	10	H'FEEB	H'FEEA	H'FEE9	H'FEE8	10	7_2
7_3	11	H'FEEF	H'FEEE	H'FEED	H'FEEC	11	7_3
7_4	12	H'FEF3	H'FEF2	H'FEF1	H'FEF0	12	7_4
7_5	13	H'FEF7	H'FEF6	H'FEF5	H'FEF4	13	7_5
7_6	14	H'FEFB	H'FEFA	H'FEF9	H'FEF8	14	7_6
7_7	15	H'FEFF	H'FEFE	H'FEFD	H'FEFC	15	7_7
		MSB ◄——► LSB	MSB ◄——► LSB	MSB ◄——► LSB	MSB ◄——► LSB		

Note: Areas not used for display may be used as general-purpose RAM.

12.3.4 Procedure for Starting Operation

The procedure for starting operation of the VFD controller/driver is given below for a case in which digit pins FD_3 to FD_{15} and segment pins FS_5 to FS_{23} are used. It is assumed that data has already been written to the VFD display RAM area.

- Select the digit/key-scan time and dimmer resolution with bit FLMO of the VFD digit control register (VFDR), and select the digit waveform with bits DM2 to DM0. Clear bits DR3 to DR0 to 0000, making pins FD_0 to FD_{15} operational.

- Set the VFLAG bit of the VFD segment control register (VFSR) to 1, making the selected pins valid as VFD pins. Set bit KSE to enable or disable the key scan interval. Set bits SR4 to SR0 to 11011, making pins FS_0 to FS_{23} operational.

- Set bits DBR3 to DBR0 in the digit beginning register (DBR) to 0011, designating pin FD_3 as the first digit pin and pin FS_5 as the first segment pin. Set bit DISP to 1, turning the display on, and set bit VFDE to 1, starting VFD controller/driver operation.

12.4 Interrupts

When the key scan interval starts, bit IRRKS in interrupt request register 3 (IRR3) is set to 1. These VFD interrupt requests can be enabled or disabled by means of bit IENKS of interrupt enable register 3 (IENR3). For further details, see 3.2.2, Interrupts.

12.5 Occurrence of Flicker when VFD Registers are Rewritten

The VFD controller/driver is initialized whenever one of its registers (VFDR, VFSR, DBR) is rewritten. If this initialization takes place while a digit is being displayed, the contents displayed just prior to initialization will in some cases remain as an after-image in other digits. (This depends in part on the performance of the vacuum fluorescent display, but a momentary glow may be visible.) Frequent rewriting of the registers can make these after-images bright enough to appear as a false display. This problem can be avoided by employing the following programming sequence when VFD controller/driver registers are rewritten.

Step	Description
1.	DISP = 0
2.	VFLAG = 0
3.	Rewrite register (FLMO, DM0 to DM3, etc.)
4.	Wait for at least T_{digit} (display time of one digit). (Execute other routines.) If the wait time is too long, the entire display may flicker. If the key scan feature is activated, this wait time does not have to be specially programmed.
5.	VFLAG = 1
6.	DISP = 1

Section 13 A/D Converter

13.1 Overview

The H8/3714 Series includes on-chip a resistance-ladder type successive-approximation A/D converter, which can convert up to eight channels of analog input.

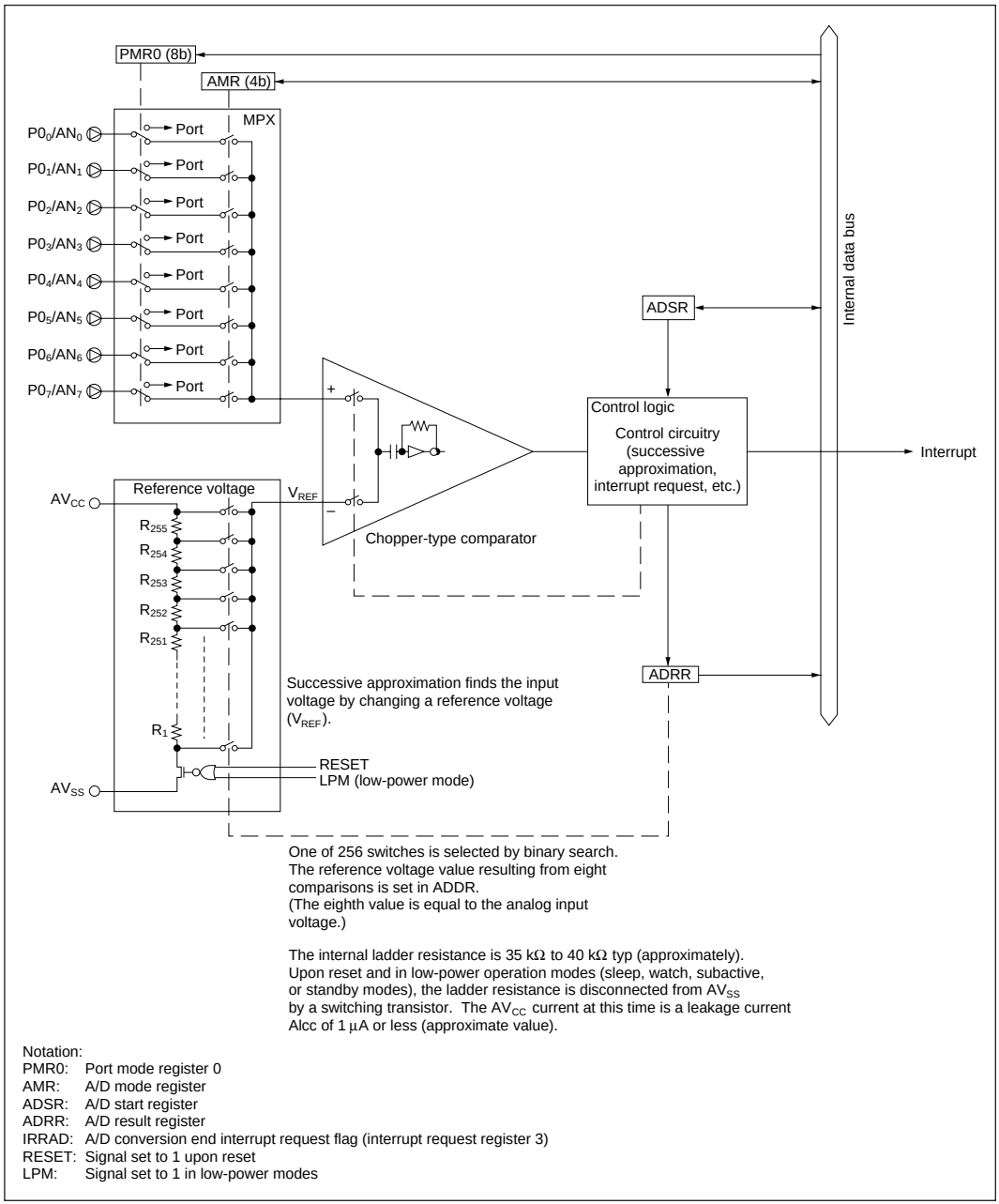
13.1.1 Features

The A/D converter has the following features.

- 8-bit resolution
- Eight input channels
- Conversion time: 14.8 µs per channel (min, at f_{osc} = 8.38 MHz)
- Built-in sample-and-hold function
- Interrupt requested on completion of A/D conversion

13.1.2 Block Diagram

Figure 13-1 shows a block diagram of the A/D converter.



Notation:
PMR0: Port mode register 0
AMR: A/D mode register
ADSR: A/D start register
ADRR: A/D result register
IRRAD: A/D conversion end interrupt request flag (interrupt request register 3)
RESET: Signal set to 1 upon reset
LPM: Signal set to 1 in low-power modes

Figure 13-1 Block Diagram of A/D Converter

13.1.3 Pin Configuration

Table 13-1 shows the A/D converter pin configuration.

Table 13-1 Pin Configuration

Name	Abbrev.	I/O	Function
Analog power supply pin	AV_{CC}	Input	Analog power supply and reference voltage
Analog ground pin	AV_{SS}	Input	Analog ground and reference voltage
Analog input pin 0	AN_0	Input	Analog input channel 0
Analog input pin 1	AN_1	Input	Analog input channel 1
Analog input pin 2	AN_2	Input	Analog input channel 2
Analog input pin 3	AN_3	Input	Analog input channel 3
Analog input pin 4	AN_4	Input	Analog input channel 4
Analog input pin 5	AN_5	Input	Analog input channel 5
Analog input pin 6	AN_6	Input	Analog input channel 6
Analog input pin 7	AN_7	Input	Analog input channel 7

13.1.4 Register Configuration

Table 13-2 shows the A/D converter register configuration.

Table 13-2 Register Configuration

Name	Abbrev.	R/W	Initial Value	Address
A/D mode register	AMR	R/W	H'78	H'FFBC
A/D start register	ADSR	R/W	H'7F	H'FFBE
A/D result register	ADRR	R	Not fixed	H'FFBD
Port mode register 0	PMR0	W	H'00	H'FFEF

13.2 Register Descriptions

13.2.1 A/D Result Register (ADRR)

Bit	7	6	5	4	3	2	1	0
	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
Initial value	*	*	*	*	*	*	*	*
Read/Write	R	R	R	R	R	R	R	R

Note: * Not fixed

The A/D result register (ADRR) is an 8-bit read-only register for holding the result of analog-to-digital conversion.

ADRR can be read by the CPU at any time, but the ADRR value during A/D conversion is not fixed.

After A/D conversion is complete, the conversion result is stored in ADRR as 8-bit data; this data is held in ADRR until the next conversion operation starts.

ADRR is not cleared on reset.

13.2.2 A/D Mode Register (AMR)

Bit	7	6	5	4	3	2	1	0
	AMR7	—	—	—	—	AMR2	AMR1	AMR0
Initial value	0	1	1	1	1	0	0	0
Read/Write	R/W	—	—	—	—	R/W	R/W	R/W

AMR is an 8-bit read/write register for selecting the A/D conversion speed and analog input pin.

Writing to AMR should be done with the A/D start flag (ADSF) cleared to 0 in the A/D start register (ADSR).

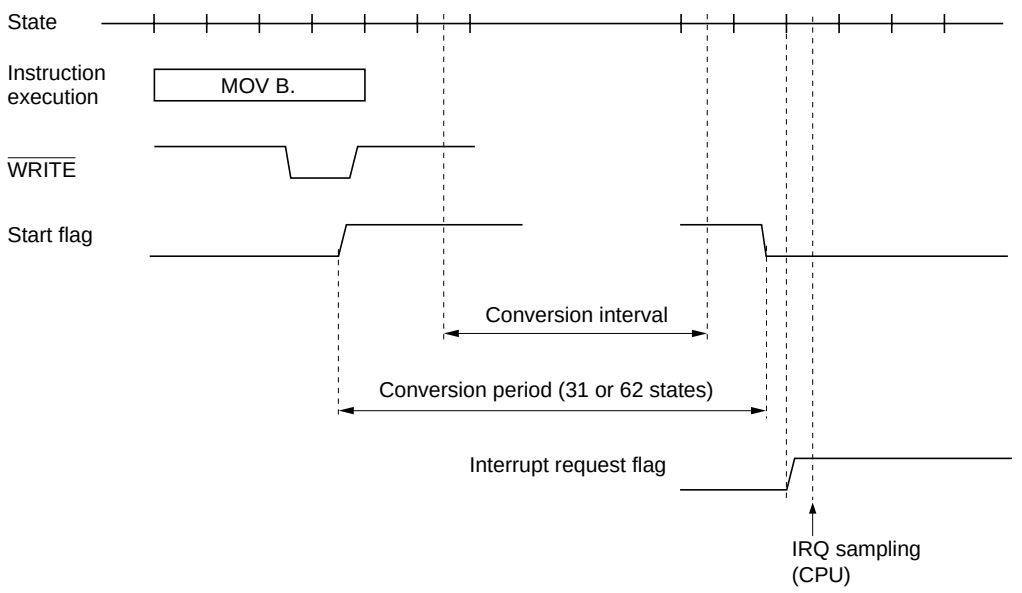
Upon reset, AMR is initialized to H'78.

Bit 7: Clock select (AMR7)

Bit 7 sets the A/D conversion speed.*1

Bit 7 AMR7	Conversion Period*2	φ = 2 MHz	φ = 4 MHz	
0	62/φ	31 µs	14.8 µs	(initial value)
1	31/φ	15.5 µs	—*1	

Notes: 1. Operation is not guaranteed if the conversion time is less than 14.8 µs. Set bit 7 for a value of at least 14.8 µs.
2. A/D conversion starts after a value of 1 is written to ADSF. The conversion period starts when the start flag is set and ends when it is reset upon completion of conversion. The actual time during which sample and hold are repeated is called the conversion interval (see figure 13-2).



Note: IRQ sampling: When conversion is complete, the start flag is reset and the interrupt request flag is set. An interrupt is recognized by the CPU in the last instruction execution state, and interrupt exception handling is executed after that instruction is completed.

Figure 13-2 Internal Operation of A/D Converter

Bits 6 to 3: Reserved bits

Bits 6 to 3 are reserved; they always read 1, and cannot be modified.

Bits 2 to 0: Channel select (AMR2 to AMR0)

Bits 2 to 0 select the analog input channel.
Settings are also required in port mode register 0 (PMR0). See 13.2.4, Port Mode Register 0 (PMR0).

Bit 2 AMR2	Bit 1 AMR1	Bit 0 AMR0	Analog Input Channel	
0	0	0	AN_0	(initial value)
0	0	1	AN_1	
0	1	0	AN_2	
0	1	1	AN_3	
1	0	0	AN_4	
1	0	1	AN_5	
1	1	0	AN_6	
1	1	1	AN_7	

13.2.3 A/D Start Register (ADSR)

Bit	7	6	5	4	3	2	1	0
	ADSF	—	—	—	—	—	—	—
Initial value	0	1	1	1	1	1	1	1
Read/Write	R/W	—	—	—	—	—	—	—

The A/D start register (ADSR) is an 8-bit read/write register for starting and stopping A/D conversion.

A/D conversion is started by writing 1 to the A/D start flag (ADSF). When conversion is complete, the converted data is set in the A/D result register (ADRR), and at the same time ADSF is cleared to 0.

Bit 7: A/D start flag (ADSF)

Bit 7 is for controlling and confirming the start and end of A/D conversion.

Bit 7 ADSF	Description	
0	[Read access] Indicates that A/D conversion has been completed or stopped.	(initial value)
	[Write access] Stops A/D conversion.	
1	[Read access] Indicates A/D conversion in progress.	
	[Write access] Starts A/D conversion.	

Bits 6 to 0: Reserved bits

Bits 6 to 0 are reserved; they always read 1, and cannot be modified.

13.2.4 Port Mode Register 0 (PMR0)

Bit	7	6	5	4	3	2	1	0
	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PMR0 is an 8-bit write-only register for designating whether each of the port 0 pins is used as a general-purpose input pin or as an analog input channel to the A/D converter. Designation is made separately for each pin.

Upon reset, PMR0 is initialized to H'00.

Bit n ANn	Description	
0	Pin $P0_n/AN_n$ is used for general-purpose input.	(initial value)
1	Pin $P0_n/AN_n$ is an analog input channel.	

(n = 0 to 7)

13.3 Operation

The A/D converter operates by successive approximations, and yields its conversion result as 8-bit data.

A/D conversion begins when software sets the A/D start flag (bit ADSF) to 1. Bit ADSF keeps a value of 1 during A/D conversion, and is cleared to 0 automatically when conversion is complete.

The completion of conversion also sets bit IRRAD in interrupt request register 3 (IRR3) to 1. An A/D conversion end interrupt is requested if bit IENAD in interrupt enable register 3 (IENR3) is set to 1.

If the conversion time or input channel needs to be changed in the A/D mode register (AMR) during A/D conversion, bit ADSF should first be cleared to 0, stopping the conversion operation, in order to avoid misoperation.

13.4 Interrupts

When A/D conversion is complete (ADSF changes from 1 to 0), bit IRRAD in interrupt request register 3 (IRR3) is set to 1.

A/D conversion end interrupts can be enabled or disabled by means of bit IENAD in interrupt enable register 3 (IENR3).

For further details see 3.2.2, Interrupts.

13.5 Typical Use

An example of how the A/D converter can be used is given below, using channel 1 (AN_1) as the analog input channel. Figure 13-3 shows the operation timing for this example.

1. Bits AMR2 to AMR0 of the A/D mode register (AMR) are set to 001, and bits AN7 to AN0 of port mode register 0 (PMR0) are set to 00000010, making AN_1 the analog input channel. Interrupt request is cleared by setting bit IRRAD to 0, A/D interrupts are enabled by setting bit IENAD to 1, and A/D conversion is started by setting bit ADSF to 1.

2. When A/D conversion is complete, bit IRRAD is set to 1, and the A/D conversion results are sent to the A/D result register (ADRR). At the same time ADSF is cleared to 0, and the A/D converter goes to the idle state.

3. Bit IENAD = 1, so an A/D conversion end interrupt is requested.

4. The A/D interrupt handling routine starts.

5. The A/D conversion result is read and processed.

6. The A/D interrupt handling routine ends.

If ADSF is set to 1 again afterward, A/D conversion starts and steps 2 through 6 take place.

Figures 13-4 and 13-5 show flow charts of procedures for using the A/D converter.

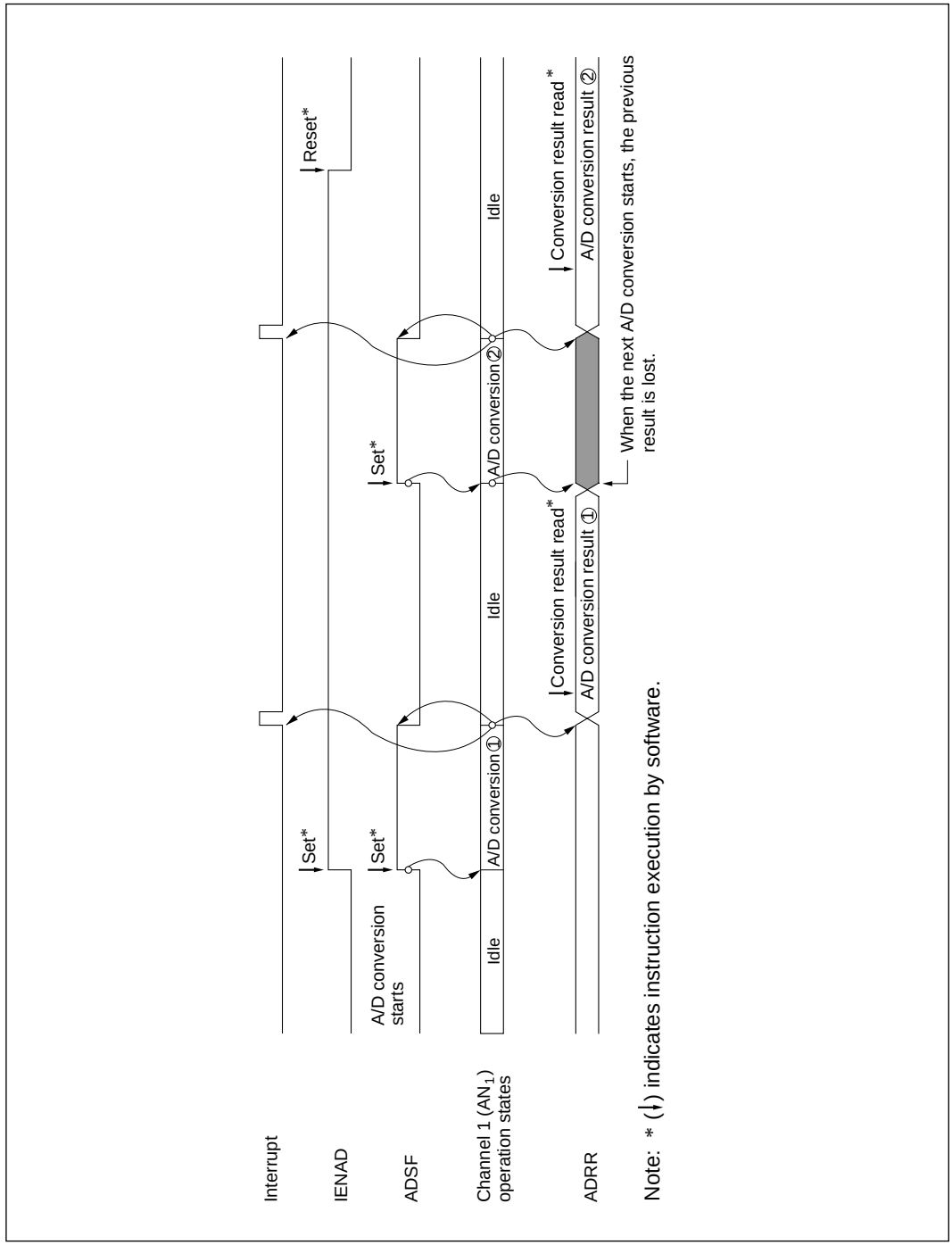


Figure 13-3 Typical A/D Converter Operation Timing

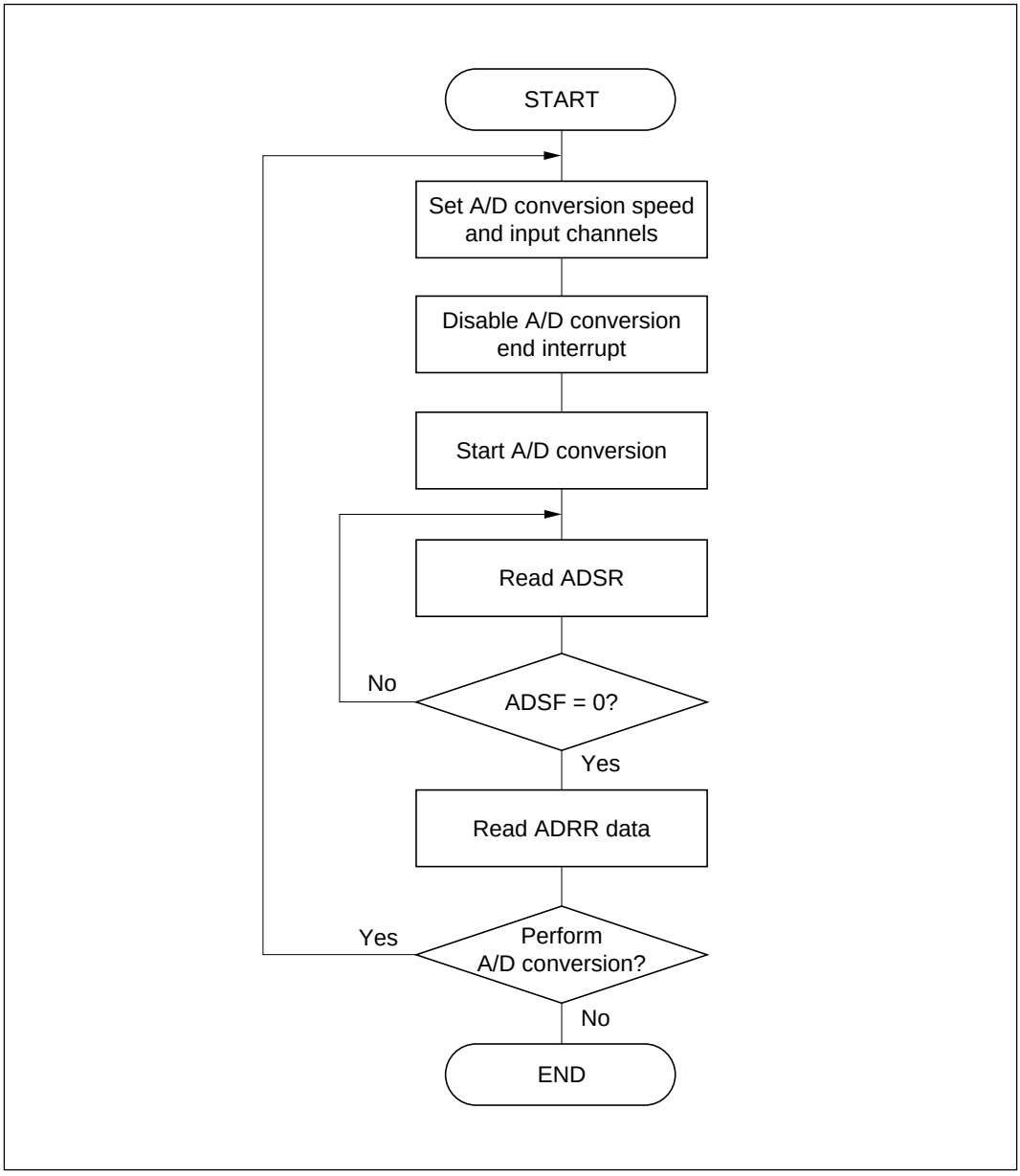


Figure 13-4 Flow Chart of Procedure for Using A/D Converter (1) (Polling by Software)

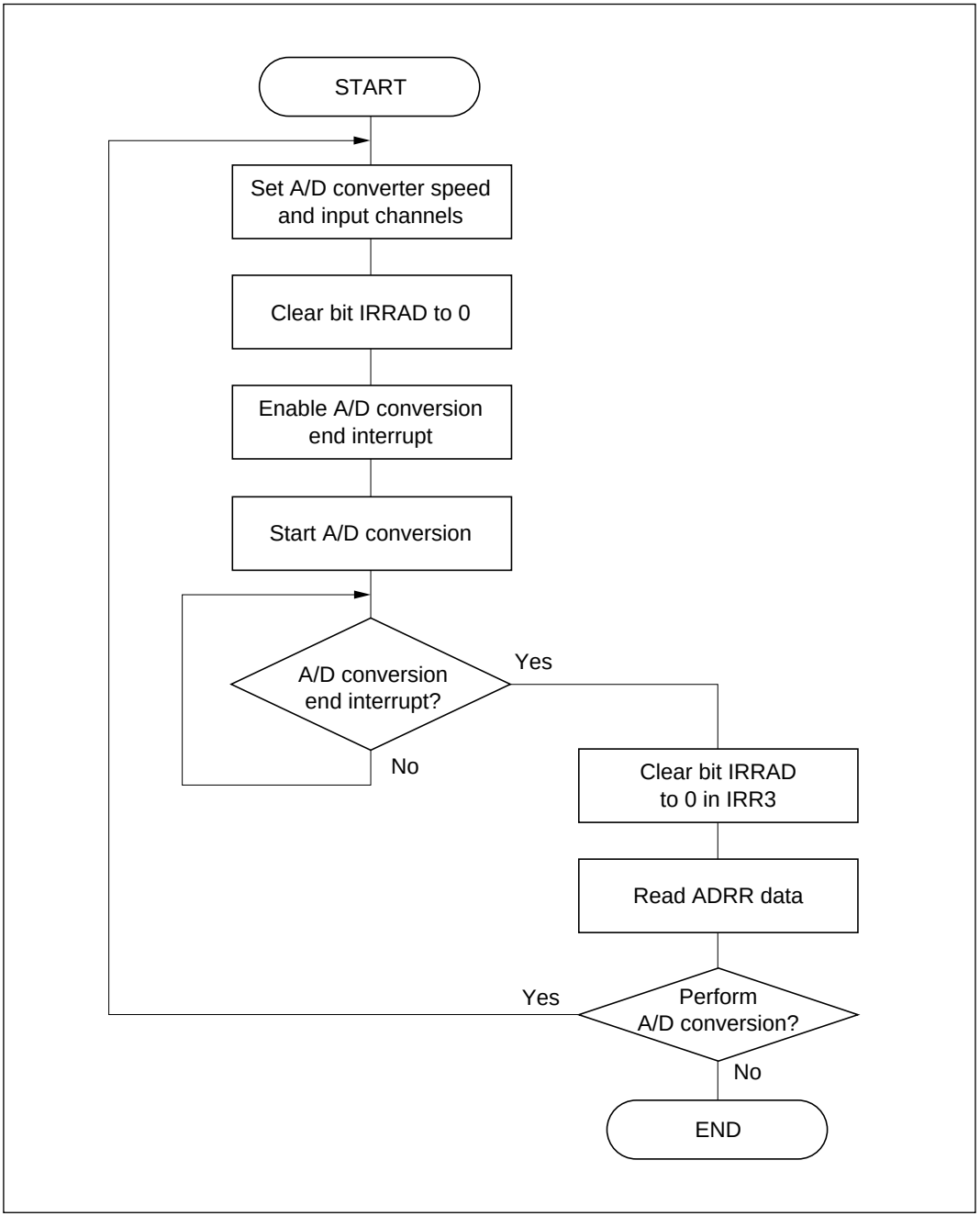


Figure 13-5 Flow Chart of Procedure for Using A/D Converter (2) (Interrupts Used)

13.6 Application Notes

1. Data in the A/D result register (ADRR) should be read only when the A/D start flag (ADSF) in the A/D start register (ADSR) is cleared to 0.

2. Changing a digital input signal at a nearby pin during A/D conversion may adversely affect conversion accuracy.

3. The pin selected as an analog input channel in the A/D mode register (AMR) must also be designated as an analog input channel in port mode register 0 (PMR0).

Section 14 Electrical Specifications

14.1 Absolute Maximum Ratings

Table 14-1 gives the absolute maximum ratings.

Table 14-1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	1, 2
Programming voltage	V_{PP}	–0.3 to +14.0	V	1, 2, 3
Analog supply voltage	AV_{CC}	–0.3 to +7.0	V	1, 2
Analog input voltage	AV_{in}	–0.3 to AV_{CC} +0.3	V	1, 2
Pin voltage (standard pins)	V_T	–0.3 to V_{CC} +0.3	V	1, 2, 4
Pin voltage (high-voltage pins)	V_T	V_{CC} –45 to V_{CC} +0.3	V	1, 2, 5
Operating temperature	T_{op}	–20 to +75	°C	1, 2
Storage temperature	T_{stg}	–55 to +125	°C	1, 2

Notes: 1. Permanent damage may occur to the chip if maximum ratings are exceeded. Normal operation should be under the conditions specified in Electrical Characteristics. Exceeding these values can result in incorrect operation and reduced reliability.
2. All voltages are referenced to V_{SS}.
3. Applies to the ZTAT™ version.
4. Applies to standard-voltage pins.
5. Applies to high-voltage pins.

14.2 HD6473714 Electrical Characteristics

14.2.1 HD6473714 DC Characteristics

Table 14-2 gives the allowable current values of the HD6473714. Table 14-3 gives the DC characteristics.

Table 14-2 Allowable Output Current Values

Conditions: V_{CC} = 4.0 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Rating	Unit	Notes
Allowable input current (sink)	I_O	2	mA	1, 2
Allowable output current (source)	$-I_O$	2	mA	2, 3
Allowable output current (source)	$-I_O$	20	mA	3, 4
Total allowable input current (sink)	ΣI_O	50	mA	5
Total allowable output current (source)	$-\Sigma I_O$	150	mA	6

Notes:
1. Allowable input current means the maximum current that can flow from each I/O pin to V_{SS}.
2. Applies to standard-voltage pins.
3. Allowable output current means the maximum current that can flow from V_{CC} to each I/O pin.
4. Applies to high-voltage pins.
5. Total allowable input current means the sum of current that can flow at one time from all I/O pins to V_{SS}.
6. Total allowable output current means the sum of current that can flow from V_{CC} to all I/O pins.

Table 14-3 DC Characteristics

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating Min	Rating Typ	Rating Max	Unit	Notes
Input high voltage	V_{IH}	$\overline{RES}$		0.8 V_{CC}	—	V_{CC} +0.3	V	
		$\overline{IRQ_0}$, $\overline{IRQ_1}$, $\overline{IRQ_4}$, $\overline{IRQ_5}$ SCK_1, SCK_2 SI_1, SI_2	V_{CC} = 2.7 to 5.5 V incl. subactive mode	0.9 V_{CC}	—	V_{CC} +0.3		
		$\overline{EVENT}$, UD	V_{CC} = 2.7 to 5.5 V incl. subactive mode	0.7 V_{CC}	—	V_{CC} +0.3	V	
		OSC_1		V_{CC} –0.5	—	V_{CC} +0.3	V	
			V_{CC} = 2.7 to 5.5 V incl. subactive mode	V_{CC} –0.3	—	V_{CC} +0.3		
		$P0_0$ to $P0_7$ $P1_0$, $P1_1$, $P1_4$ to $P1_6$ $P9_0$ to $P9_7$	V_{CC} = 2.7 to 5.5 V incl. subactive mode	0.7 V_{CC}	—	V_{CC} +0.3	V	
		$P4_0$ to $P4_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P1_7$	V_{CC} = 2.7 to 5.5 V incl. subactive mode	0.7 V_{CC}	—	V_{CC} +0.3	V	
Input low voltage	V_{IL}	$\overline{RES}$, SCK_1, SCK_2		–0.3	—	0.2 V_{CC}	V	
		$\overline{IRQ_0}$, $\overline{IRQ_1}$, $\overline{IRQ_4}$, $\overline{IRQ_5}$ SI_1, SI_2	V_{CC} = 2.7 to 5.5 V incl. subactive mode	–0.3	—	0.1 V_{CC}		
		$\overline{EVENT}$, UD	V_{CC} = 2.7 to 5.5 V incl. subactive mode	–0.3	—	0.3 V_{CC}	V	
		OSC_1		–0.3	—	0.5	V	
			V_{CC} = 2.7 to 5.5 V incl. subactive mode	–0.3	—	0.3		
		$P0_0$ to $P0_7$ $P1_0$, $P1_1$, $P1_4$ to $P1_6$ $P9_0$ to $P9_7$	V_{CC} = 2.7 to 5.5 V incl. subactive mode	–0.3	—	0.3 V_{CC}	V	
		$P4_0$ to $P4_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P1_7$	V_{CC} = 2.7 to 5.5 V incl. subactive mode	V_{CC} –40	—	0.3 V_{CC}	V	

Note: Connect the TEST pin to V_{SS}.

Table 14-3 DC Characteristics (cont)

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating Min	Rating Typ	Rating Max	Unit	Notes
Output high voltage	V_{OH}	$P1_0$, $P1_1$, $P1_4$, $P1_5$ $P9_0$ to $P9_7$ PWM, SO1, SO_2, SCK_1, SCK_2	$-I_{OH}$ = 1.0 mA	V_{CC} –1.0	—	—	V	
			$-I_{OH}$ = 0.5 mA	V_{CC} –0.5	—	—		
			V_{CC} = 2.7 to 5.5 V $-I_{OH}$ = 0.3 mA	V_{CC} –0.5	—	—		
		$P4_0$ to $P4_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$	$-I_{OH}$ = 15 mA	V_{CC} –3.0	—	—	V	
			$-I_{OH}$ = 10 mA	V_{CC} –2.0	—	—		
			$-I_{OH}$ = 4 mA	V_{CC} –1.0	—	—		
			V_{CC} = 2.7 to 5.5 V $-I_{OH}$ = 4 mA	—	V_{CC} –1.0	—	V	Reference value
Output low voltage	V_{OL}	$P1_0$, $P1_1$, $P1_4$, $P1_5$ $P9_0$ to $P9_7$	V_{CC} = 4.0 to 5.5 V I_{OL} = 1.6 mA	—	—	0.4	V	
		PWM, SO_1, SO_2, SCK_1, SCK_2	V_{CC} = 2.7 to 5.5 V I_{OL} = 0.5 mA	—	0.4	—	V	Reference value
		$P4_0$ to $P4_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$	Pull-down resistance 150 kΩ; pull-down voltage V_{CC} –40 V	—	—	V_{CC} –37	V	
Input leakage current	$\lvert I_{IL} \rvert$	$\overline{RES}$	V_{IN} = 0.0 to V_{CC}	—	—	40	µA	

Table 14-3 DC Characteristics (cont)

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating Min	Rating Typ	Rating Max	Unit	Notes
I/O leakage current	$\|I_{IL}\|$	TEST SCK_1, SCK_2 SI_1, SI_2 $\overline{IRQ_0}$, $\overline{IRQ_1}$, $\overline{IRQ_4}$, $\overline{IRQ_5}$ $\overline{EVENT}$, UD OSC_1 $P0_0$ to $P0_7$ $P1_0$, $P1_1$ $P1_4$ to $P1_6$ $P9_0$ to $P9_7$	V_{IN} = 0.0 to V_{CC}	—	—	1	µA	
		$P4_0$ to $P4_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P1_7$	V_{IN} = V_{CC} –40 to V_{CC}	—	—	20	µA	
Input capacitance	C_{IN}	Input pins other than power supply pins and I/O pins	f = 1 MHz, V_{IN} = 0 V T_a = 25°C	—	—	20	pF	
		$P1_6/\overline{EVENT}$		—	—	35		
		$\overline{RES}$		—	—	70		

Table 14-3 DC Characteristics (cont)

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Power dissipation when CPU operating in active mode	I_{OPE}	V_{CC}	V_{CC} = 5 V, f_{OSC} = 8 MHz	—	17	—	mA	Reference value 1
			V_{CC} = 5 V, f_{OSC} = 4 MHz	—	9	—		
			V_{CC} = 3 V, f_{OSC} = 4 MHz	—	6	—		
Power dissipation during reset in active mode	I_{RES}	V_{CC}	V_{CC} = 5 V, f_{OSC} = 8 MHz	—	6	9	mA	1
			V_{CC} = 5 V, f_{OSC} = 4 MHz	—	3	5		
			V_{CC} = 3 V, f_{OSC} = 4 MHz	—	1.5	—		
Power dissipation in sleep mode	I_{SLEEP}	V_{CC}	V_{CC} = 5 V, f_{OSC} = 8 MHz	—	2.5	3.5	mA	1
			V_{CC} = 5 V, f_{OSC} = 4 MHz	—	1.5	2.0		
			V_{CC} = 3 V, f_{OSC} = 4 MHz	—	1.0	—		
Power dissipation in subactive mode	I_{SUB}	V_{CC}	**V_{CC} = 2.7 V** 32 kHz crystal oscillator used	—	6	20	µA	
				—	11	—	µA	2
			V_{CC} = 5.0 V 32 kHz crystal oscillator used	—	16	—	µA	Reference value
				—	22	—	µA	2
Power dissipation in watch mode	I_{WATCH}	V_{CC}	V_{CC} = 2.7 V 32 kHz crystal oscillator used	—	3.2	6	µA	
				—	3.8	—	µA	2
			V_{CC} = 5.0 V 32 kHz crystal oscillator used	—	10	—	µA	Reference value
				—	12	—	µA	2
Power dissipation in standby mode	I_{STBY}	V_{CC}	32 kHz crystal oscillator not used X_1 = V_{CC}	—	—	10	µA	

Table 14-3 DC Characteristics (cont)

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
RAM data retention voltage in standby mode	V_{STBY}	V_{CC}	32 kHz crystal oscillator not used $X_1 = V_{CC}$	2	—	—	V	

Notes: 1. Does not include current flowing to output buffer.
2. Reference value when bypass capacitor of 47 µF is connected between V_{CC} and V_{SS}.

14.2.2 HD6473714 AC Characteristics

Table 14-4 gives the control signal timing of the HD6473714. Table 14-5 gives the serial interface timing.

Table 14-4 Control Signal Timing

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Clock pulse generator frequency	f_{OSC}	OSC_1, OSC_2,		2	—	8.4	MHz	
			V_{CC} = 2.7 to 5.5 V	2	—	4.2		
Clock cycle time	t_{CYC}	OSC_1, OSC_2,		119	—	500	ns	Figure 14-1
			V_{CC} = 2.7 to 5.5 V	238	—	500		
Instruction cycle time	ϕ			238	—	1000	ns	
			V_{CC} = 2.7 to 5.5 V	476	—	1000		
Subclock pulse generator frequency	f_x	X_1, X_2	V_{CC} = 2.7 to 5.5 V	—	32.768	—	kHz	
Subclock cycle time	t_{subcyc}	X_1, X_2	V_{CC} = 2.7 to 5.5 V	—	30.5	—	µs	
Subactive instruction cycle time	ϕ_{SUB}		V_{CC} = 2.7 to 5.5 V	—	244.14	—	µs	
Oscillator settling time (crystal oscillator)	t_{rc}	OSC_1, OSC_2,		—	—	40	ms	
			V_{CC} = 2.7 to 5.5 V	—	—	60		
Oscillator settling time (ceramic oscillator)	t_{rc}	OSC_1, OSC_2,		—	—	20	ms	
			V_{CC} = 2.7 to 5.5 V	—	—	40		
Oscillator settling time	t_{rc}	X_1, X_2	V_{CC} = 2.7 to 5.5 V	—	—	2	s	
External clock pulse width (high)	t_{CPH}	OSC_1		40	—	—	ns	Figure 14-1
			V_{CC} = 2.7 to 5.5 V	100	—	—		
External clock pulse width (low)	t_{CPL}	OSC_1		40	—	—	ns	
			V_{CC} = 2.7 to 5.5 V	100	—	—		
External clock rise time	t_{CPr}	OSC_1		—	—	20	ns	
			V_{CC} = 2.7 to 5.5 V	—	—	20		
External clock fall time	t_{CPf}	OSC_1		—	—	20	ns	
			V_{CC} = 2.7 to 5.5 V	—	—	20		

Table 14-4 Control Signal Timing (cont)

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating Min	Rating Typ	Rating Max	Unit	Reference Diagram
$\overline{RES}$ pin pulse width (low)	t_{REL}	$\overline{RES}$	V_{CC} = 2.7 to 5.5 V	10	—	—	ϕ	Figure 14-2
$\overline{IRQ}$ pin pulse width (high)	t_{IH}	$\overline{IRQ_0}$, $\overline{IRQ_1}$, $\overline{IRQ_4}$, $\overline{IRQ_5}$	V_{CC} = 2.7 to 5.5 V	2	—	—	ϕ ϕ_{SUB}	Figure 14-3
$\overline{IRQ}$ pin pulse width (low)	t_{IL}	$\overline{IRQ_0}$, $\overline{IRQ_1}$, $\overline{IRQ_4}$, $\overline{IRQ_5}$	V_{CC} = 2.7 to 5.5 V	2	—	—	ϕ ϕ_{SUB}	
$\overline{EVENT}$ pin pulse width (high)	t_{EVH}	$\overline{EVENT}$	V_{CC} = 2.7 to 5.5 V	2	—	—	ϕ	Figure 14-4
$\overline{EVENT}$ pin pulse width (low)	t_{EVL}	$\overline{EVENT}$	V_{CC} = 2.7 to 5.5 V	2	—	—	ϕ	
UD pin minimum high/low width	t_{UDH} t_{UDL}	UD	V_{CC} = 2.7 to 5.5 V	2	—	—	ϕ	Figure 14-5

Table 14-5 Serial Interface Timing

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating Min	Rating Typ	Rating Max	Unit	Reference Diagram
Output serial clock cycle time	t_{scyc}	SCK_1, SCK_2	V_{CC} = 2.7 to 5.5 V	2	—	—	ϕ	Figure 14-6
Output serial clock pulse width (high)	t_{SCKH}	SCK_1, SCK_2	V_{CC} = 2.7 to 5.5 V	0.4	—	—	t_{scyc}	
Output serial clock pulse width (low)	t_{SCKL}	SCK_1, SCK_2	V_{CC} = 2.7 to 5.5 V	0.4	—	—	t_{scyc}	
Output serial clock rise time	t_{SCKr}	SCK_1, SCK_2		—	—	60	ns	
			V_{CC} = 2.7 to 5.5 V	—	—	80		
Output serial clock fall time	t_{SCKf}	SCK_1, SCK_2		—	—	60	ns	
			V_{CC} = 2.7 to 5.5 V	—	—	80		
Input serial clock cycle time	t_{scyc}	SCK_1, SCK_2	V_{CC} = 2.7 to 5.5 V	1	—	—	ϕ	
Input serial clock pulse width (high)	t_{SCKH}	SCK_1, SCK_2	V_{CC} = 2.7 to 5.5 V	0.4	—	—	t_{scyc}	

Table 14-5 Serial Interface Timing (cont)

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Input serial clock pulse width (low)	t_{SCKL}	SCK_1, SCK_2	V_{CC} = 2.7 to 5.5 V	0.4	—	—	t_{scyc}	Figure 14-6
Input serial clock rise time	t_{SCKr}	SCK_1, SCK_2		—	—	60	ns	
			V_{CC} = 2.7 to 5.5 V	—	—	80		
Input serial clock fall time	t_{SCKf}	SCK_1, SCK_2		—	—	60	ns	
			V_{CC} = 2.7 to 5.5 V	—	—	80		
Serial output data delay time	t_{dSO}	SO_1, SO_2		—	—	200	ns	
			V_{CC} = 2.7 to 5.5 V	—	—	350		
Serial input data setup time	t_{sSI}	SI_1, SI_2		230	—	—	ns	
			V_{CC} = 2.7 to 5.5 V	470	—	—		
Serial input data hold time	t_{hSI}	SI_1, SI_2		230	—	—	ns	
			V_{CC} = 2.7 to 5.5 V	470	—	—		
Transfer pending time	t_{SCK2}	SCK_2	When pin SCK_2 is input pin	0.2	—	40	µs	Figure 14-7
			When pin SCK_2 is input pin V_{CC} = 2.7 to 5.5 V	0.4	—	40		
			When pin SCK_2 is output pin V_{CC} = 2.7 to 5.5 V	—	—	1	t_{scyc}	
Transfer end acknowledge time	t_{CS}	$\overline{CS}$	V_{CC} = 2.7 to 5.5 V	3	—	4	ϕ	

14.2.3 HD6473714 A/D Converter Characteristics

Table 14-6 gives the HD6473714 A/D converter characteristics.

Table 14-6 A/D Converter Characteristics

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Analog supply voltage	AV_{CC}	AV_{CC}		V_{CC} –0.3	V_{CC}	V_{CC} +0.3	V	
Analog input voltage	AV_{IN}	AN_0 to AN_7		AV_{SS}	—	AV_{CC}	V	
Analog supply current	AI_{CC}	AV_{CC}	AV_{CC} = 5 V	—	—	200	µA	
	AI_{STOP}		Reset and power-down mode	—	—	10	µA	
Analog input capacitance	C_{AIN}	AN_0 to AN_7		—	—	30	pF	
Allowable signal source impedance	R_{AIN}	AN_0 to AN_7		—	—	10	kΩ	
Resolution				—	—	8	Bit	
Absolute accuracy			V_{CC} = AV_{CC} = 5 V	—	—	±2.5	LSB	
			V_{CC} = AV_{CC} = 4.0 to 5.5 V	—	±2.5	—		Reference value
Conversion time				31	15.5	14.8	µs	

14.3 HD6433712, HD6433713 and HD6433714 Electrical Characteristics

14.3.1 HD6433712, HD6433713 and HD6433714 DC Characteristics

Table 14-7 gives the allowable current values of the HD6433712, HD6433713 and HD6433714. Table 14-8 gives the DC characteristics.

Table 14-7 Allowable Output Current Values

Conditions: V_{CC} = 4.0 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Rating	Unit	Notes
Allowable input current (sink)	I_O	2	mA	1, 2
Allowable output current (source)	$-I_O$	2	mA	2, 3
Allowable output current (source)	$-I_O$	20	mA	3, 4
Total allowable input current (sink)	ΣI_O	50	mA	5
Total allowable output current (source)	$-\Sigma I_O$	150	mA	6
Total allowable output current to V_{disp}	$-\Sigma I_O$	30	mA	7

Notes:
1. Allowable input current means the maximum current that can flow from each I/O pin to V_{SS}.
2. Applies to standard-voltage pins.
3. Allowable output current means the maximum current that can flow from V_{CC} to each I/O pin.
4. Applies to high-voltage pins.
5. Total allowable input current means the sum of current that can flow at one time from all I/O pins to V_{SS}.
6. Total allowable output current means the sum of current that can flow from V_{CC} to all I/O pins.
7. Total allowable output current to V_{disp} is the sum of current that can flow from all I/O pins to V_{disp}.

Table 14-8 DC Characteristics

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating Min	Rating Typ	Rating Max	Unit	Notes
Input high voltage	V_{IH}	$\overline{RES}$		0.8 V_{CC}	—	V_{CC} +0.3	V	
		$\overline{IRQ_0}$, $\overline{IRQ_1}$, $\overline{IRQ_4}$, $\overline{IRQ_5}$ SCK_1, SCK_2 SI_1, SI_2	V_{CC} = 2.5 to 5.5 V incl. subactive mode	0.9 V_{CC}	—	V_{CC} +0.3		
		$\overline{EVENT}$, UD	V_{CC} = 2.5 to 5.5 V incl. subactive mode	0.7 V_{CC}	—	V_{CC} +0.3	V	
		OSC_1		V_{CC} –0.5	—	V_{CC} +0.3	V	
			V_{CC} = 2.5 to 5.5 V incl. subactive mode	V_{CC} –0.3	—	V_{CC} +0.3		
		$P0_0$ to $P0_7$ $P1_0$, $P1_1$ $P1_4$ to $P1_6$ $P9_0$ to $P9_7$	V_{CC} = 2.5 to 5.5 V incl. subactive mode	0.7 V_{CC}	—	V_{CC} +0.3	V	
		$P4_0$ to $P4_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P1_7$	V_{CC} = 2.5 to 5.5 V incl. subactive mode	0.7 V_{CC}	—	V_{CC} +0.3	V	
Input low voltage	V_{IL}	$\overline{RES}$, SCK_1, SCK_2		–0.3	—	0.2 V_{CC}	V	
		$\overline{IRQ_0}$, $\overline{IRQ_1}$, $\overline{IRQ_4}$, $\overline{IRQ_5}$ SI_1, SI_2	V_{CC} = 2.5 to 5.5 V incl. subactive mode	–0.3	—	0.1 V_{CC}		
		$\overline{EVENT}$, UD	V_{CC} = 2.5 to 5.5 V incl. subactive mode	–0.3	—	0.3 V_{CC}	V	
		OSC_1		–0.3	—	0.5	V	
			V_{CC} = 2.5 to 5.5 V incl. subactive mode	–0.3	—	0.3		
		$P0_0$ to $P0_7$ $P1_0$, $P1_1$ $P1_4$ to $P1_6$ $P9_0$ to $P9_7$	V_{CC} = 2.5 to 5.5 V incl. subactive mode	–0.3	—	0.3 V_{CC}	V	
		$P4_0$ to $P4_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P1_7$	V_{CC} = 2.5 to 5.5 V incl. subactive mode	V_{CC} –40	—	0.3 V_{CC}	V	

Note: Connect the TEST pin to V_{SS}.

Table 14-8 DC Characteristics (cont)

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating Min	Rating Typ	Rating Max	Unit	Notes
Output high voltage	V_{OH}	$P1_0$, $P1_1$ $P1_4$, $P1_5$ $P9_0$ to $P9_7$ PWM, SO1, SO_2, SCK_1, SCK_2	$-I_{OH}$ = 1.0 mA	V_{CC} –1.0	—	—	V	
			$-I_{OH}$ = 0.5 mA	V_{CC} –0.5	—	—		
			V_{CC} = 2.7 to 5.5 V $-I_{OH}$ = 0.3 mA	V_{CC} –0.5	—	—		
		$P4_0$ to $P4_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$	$-I_{OH}$ = 15 mA	V_{CC} –3.0	—	—	V	
			$-I_{OH}$ = 10 mA	V_{CC} –2.0	—	—		
			$-I_{OH}$ = 4 mA	V_{CC} –1.0	—	—		
			V_{CC} = 2.7 to 5.5 V $-I_{OH}$ = 4 mA	—	V_{CC} –1.0	—	V	Reference value
Output low voltage	V_{OL}	$P1_0$, $P1_1$ $P1_4$, $P1_5$ $P9_0$ to $P9_7$ PWM, SO_1, SO_2, SCK_1, SCK_2	V_{CC} = 4.0 to 5.5 V I_{OL} = 1.6 mA	—	—	0.4	V	
			V_{CC} = 2.7 to 5.5 V I_{OL} = 0.5 mA	—	0.4	—	V	Reference value
		$P4_0$ to $P4_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$	V_{disp} = V_{CC} –40 V	—	—	V_{CC} –37	V	With MOS pull-down
			Pull-down resistance 150 kΩ; pull-down voltage V_{CC} –40 V	—	—	V_{CC} –37		
Input leakage current	$\|I_{IL}\|$	$\overline{RES}$	Mask ROM version: V_{IN} = 0.0 to V_{CC}	—	—	1	µA	

Table 14-8 DC Characteristics (cont)

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating Min	Rating Typ	Rating Max	Unit	Notes
I/O leakage current	$\|I_{IL}\|$	TEST SCK_1, SCK_2 SI_1, SI_2 $\overline{IRQ_0}$, $\overline{IRQ_1}$ $\overline{IRQ_4}$, $\overline{IRQ_5}$ $\overline{EVENT}$, UD OSC_1 $P0_0$ to $P0_7$ $P1_0$, $P1_1$ $P1_4$ to $P1_6$ $P9_0$ to $P9_7$	V_{IN} = 0.0 to V_{CC}	—	—	1	µA	
		$P4_0$ to $P4_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P1_7$	V_{IN} = V_{CC} –40 to V_{CC}	—	—	20	µA	Not including pins with MOS pull-down
Pull-up MOS current	$-I_p$	$P1_0$, $P1_1$ $P1_4$ to $P1_6$ $P9_0$ to $P9_7$	V_{CC} = 5 V, V_{IN} = 0 V	50	—	300	µA	
			V_{CC} = 2.7 V, V_{IN} = 0 V	—	25	—		Reference value
Pull-down MOS current	I_d	$P4_0$ to $P4_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$	V_{disp} = V_{CC} –36 V_{IN} = V_{CC}	120	—	800	µA	
			V_{disp} = V_{CC} –18 V_{IN} = V_{CC}	—	280	—		Reference value
Input capacitance	C_{IN}	Input pins other than power supply pins and I/O pins	f = 1 MHz, V_{IN} = 0 V T_a = 25°C	—	—	15	pF	
		$P1_7$		—	—	30		

Table 14-8 DC Characteristics (cont)

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Power dissipation when CPU operating in active mode	I_{OPE}	V_{CC}	V_{CC} = 5 V, f_{OSC} = 8 MHZ	—	15	—	mA	Reference value 1
			V_{CC} = 5 V, f_{OSC} = 4 MHz	—	8	—		
			V_{CC} = 3 V, f_{OSC} = 4 MHz	—	5	—		
Power dissipation during reset in active mode	I_{RES}	V_{CC}	V_{CC} = 5 V, f_{OSC} = 8 MHz	—	5	8	mA	1
			V_{CC} = 5 V, f_{OSC} = 4 MHz	—	2.5	4		
			V_{CC} = 3 V, f_{OSC} = 4 MHz	—	1.3	—		
Power dissipation in sleep mode	I_{SLEEP}	V_{CC}	V_{CC} = 5 V, f_{OSC} = 8 MHz	—	2	3	mA	1
			V_{CC} = 5 V, f_{OSC} = 4 MHz	—	1	1.5		
			V_{CC} = 3 V, f_{OSC} = 4 MHz	—	0.6	—		
Power dissipation in subactive mode	I_{SUB}	V_{CC}	V_{CC} = 2.5 V 32 kHz crystal oscillator used	—	5	20	µA	
				—	9	—	µA	2
			V_{CC} = 5.0 V 32 kHz crystal oscillator used	—	13	—	µA	Reference value
				—	20	—	µA	2
Power dissipation in watch mode	I_{WATCH}	V_{CC}	V_{CC} = 2.5 V 32 kHz crystal oscillator used	—	2.2	5	µA	
				—	2.8	—	µA	2
			V_{CC} = 5.0 V 32 kHz crystal oscillator used	—	6	—	µA	Reference value
				—	8	—	µA	2
Power dissipation in standby mode	I_{STBY}	V_{CC}	32 kHz crystal oscillator not used X_1 = V_{CC}	—	—	5	µA	

Table 14-8 DC Characteristics (cont)

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
RAM data retention voltage in standby mode	V_{STBY}	V_{CC}	32 kHz crystal oscillator not used $X_1 = V_{CC}$	2	—	—	V	

Notes: 1. Does not include current flowing to pull-up MOS or output buffer.
2. Reference value when bypass capacitor of 47 µF is connected between V_{CC} and V_{SS}.

14.3.2 HD6433712, HD6433713 and HD6433714 AC Characteristics

Table 14-9 gives the control signal timing of the HD6433712, HD6433713 and HD6433714. Table 14-10 gives the serial interface timing.

Table 14-9 Control Signal Timing

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Clock pulse generator frequency	f_{OSC}	OSC_1, OSC_2,		2	—	8.4	MHz	
			V_{CC} = 2.7 to 5.5 V	2	—	4.2		
Clock cycle time	t_{CYC}	OSC_1, OSC_2,		119	—	500	ns	Figure 14-1
			V_{CC} = 2.7 to 5.5 V	238	—	500		
Instruction cycle time	ϕ			238	—	1000	ns	
			V_{CC} = 2.7 to 5.5 V	476	—	1000		
Subclock pulse generator frequency	f_x	X_1, X_2	V_{CC} = 2.5 to 5.5 V	—	32.768	—	kHz	
Subclock cycle time	t_{subcyc}	X_1, X_2	V_{CC} = 2.5 to 5.5 V	—	30.5	—	µs	
Subactive instruction cycle time	ϕ_{SUB}		V_{CC} = 2.5 to 5.5 V	—	244.14	—	µs	
Oscillator settling time (crystal oscillator)	t_{rc}	OSC_1, OSC_2,		—	—	40	ms	
			V_{CC} = 2.7 to 5.5 V	—	—	60		
Oscillator settling time (ceramic oscillator)	t_{rc}	OSC_1, OSC_2,		—	—	20	ms	
			V_{CC} = 2.7 to 5.5 V	—	—	40		
Oscillator settling time	t_{rc}	X_1, X_2	V_{CC} = 2.7 to 5.5 V	—	—	2	s	
External clock pulse width (high)	t_{CPH}	OSC_1		40	—	—	ns	Figure 14-1
			V_{CC} = 2.7 to 5.5 V	100	—	—		
External clock pulse width (low)	t_{CPL}	OSC_1		40	—	—	ns	
			V_{CC} = 2.7 to 5.5 V	100	—	—		
External clock rise time	t_{CPr}	OSC_1		—	—	20	ns	
			V_{CC} = 2.7 to 5.5 V	—	—	20		
External clock fall time	t_{CPf}	OSC_1		—	—	20	ns	
			V_{CC} = 2.7 to 5.5 V	—	—	20		

Table 14-9 Control Signal Timing (cont)

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating Min	Rating Typ	Rating Max	Unit	Reference Diagram
$\overline{RES}$ pin pulse width (low)	t_{REL}	$\overline{RES}$	V_{CC} = 2.7 to 5.5 V	10	—	—	ϕ	Figure 14-2
$\overline{IRQ}$ pin pulse width (high)	t_{IH}	$\overline{IRQ_0}$, $\overline{IRQ_1}$ $\overline{IRQ_4}$, $\overline{IRQ_5}$	V_{CC} = 2.7 to 5.5 V	2	—	—	ϕ ϕ_{SUB}	Figure 14-3
$\overline{IRQ}$ pin pulse width (low)	t_{IL}	$\overline{IRQ_0}$, $\overline{IRQ_1}$ $\overline{IRQ_4}$, $\overline{IRQ_5}$	V_{CC} = 2.7 to 5.5 V	2	—	—	ϕ ϕ_{SUB}	
$\overline{EVENT}$ pin pulse width (high)	t_{EVH}	$\overline{EVENT}$	V_{CC} = 2.7 to 5.5 V	2	—	—	ϕ	Figure 14-4
$\overline{EVENT}$ pin pulse width (low)	t_{EVL}	$\overline{EVENT}$	V_{CC} = 2.7 to 5.5 V	2	—	—	ϕ	
UD pin minimum high/low width	t_{UDH} t_{UDL}	UD	V_{CC} = 2.7 to 5.5 V	2	—	—	ϕ	Figure 14-5

Table 14-10 Serial Interface Timing

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating Min	Rating Typ	Rating Max	Unit	Reference Diagram
Output serial clock cycle timing	t_{scyc}	SCK_1, SCK_2	V_{CC} = 2.7 to 5.5 V	2	—	—	ϕ	Figure 14-6
Output serial clock pulse width (high)	t_{SCKH}	SCK_1, SCK_2	V_{CC} = 2.7 to 5.5 V	0.4	—	—	t_{scyc}	
Output serial clock pulse width (low)	t_{SCKL}	SCK_1, SCK_2	V_{CC} = 2.7 to 5.5 V	0.4	—	—	t_{scyc}	
Output serial clock rise time	t_{SCKr}	SCK_1, SCK_2		—	—	60	ns	
			V_{CC} = 2.7 to 5.5 V	—	—	80		
Output serial clock fall time	t_{SCKf}	SCK_1, SCK_2		—	—	60	ns	
			V_{CC} = 2.7 to 5.5 V	—	—	80		
Input serial clock cycle timing	t_{scyc}	SCK_1, SCK_2	V_{CC} = 2.7 to 5.5 V	1	—	—	ϕ	
Input serial clock pulse width (high)	t_{SCKH}	SCK_1, SCK_2	V_{CC} = 2.7 to 5.5 V	0.4	—	—	t_{scyc}	

Table 14-10 Serial Interface Timing (cont)

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Input serial clock pulse width (low)	t_{SCKL}	SCK_1, SCK_2	V_{CC} = 2.7 to 5.5 V	0.4	—	—	t_{scyc}	Figure 14-6
Input serial clock rise time	t_{SCKr}	SCK_1, SCK_2		—	—	60	ns	
			V_{CC} = 2.7 to 5.5 V	—	—	80		
Input serial clock fall time	t_{SCKf}	SCK_1, SCK_2		—	—	60	ns	
			V_{CC} = 2.7 to 5.5 V	—	—	80		
Serial output data delay time	t_{dSO}	SO_1, SO_2		—	—	200	ns	
			V_{CC} = 2.7 to 5.5 V	—	—	350		
Serial input data setup time	t_{sSI}	SI_1, SI_2		230	—	—	ns	
			V_{CC} = 2.7 to 5.5 V	470	—	—		
Serial input data hold time	t_{hSI}	SI_1, SI_2		230	—	—	ns	
			V_{CC} = 2.7 to 5.5 V	470	—	—		
Transfer pending time	t_{SCK2}	SCK_2	When pin SCK_2 is input pin	0.2	—	40	µs	Figure 14-7
			When pin SCK_2 is input pin V_{CC} = 2.7 to 5.5 V	0.4	—	40		
			When pin SCK_2 is output pin V_{CC} = 2.7 to 5.5 V	—	—	1	t_{scyc}	
Transfer end acknowledge time	t_{CS}	$\overline{CS}$	V_{CC} = 2.7 to 5.5 V	3	—	4	ϕ	

14.3.3 HD6433712, HD6433713 and HD6433714 A/D Converter Characteristics

Table 14-11 gives the HD6433712, HD6433713 and HD6433714 A/D converter characteristics.

Table 14-11 A/D Converter Characteristics

Conditions: Unless otherwise indicated, V_{CC} = 4.0 to 5.5 V, V_{disp} = V_{CC} – 40 to V_{CC}, V_{SS} = 0.0 V, T_a = –20 to +75°C

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Analog supply voltage	AV_{CC}	AV_{CC}		V_{CC} –0.3	V_{CC}	V_{CC} +0.3	V	
Analog input voltage	AV_{IN}	AN_0 to AN_7		AV_{SS}	—	AV_{CC}	V	
Analog supply current	AI_{CC}	AV_{CC}	AV_{CC} = 5 V	—	—	200	µA	
	AI_{STOP}		Reset and power-down mode	—	—	10	µA	
Analog input capacitance	C_{AIN}	AN_0 to AN_7		—	—	30	pF	
Allowable signal source impedance	R_{AIN}	AN_0 to AN_7		—	—	10	kΩ	
Resolution				—	—	8	Bit	
Absolute accuracy			V_{CC} = AV_{CC} = 5 V	—	—	±2.5	LSB	
			V_{CC} = AV_{CC} = 4.0 to 5.5 V	—	±2.5	—		Reference value
Conversion time				31	15.5	14.8	µs	

14.4 Operational Timing

This section provides operational timing diagrams (figures 14-1 to 14-8).

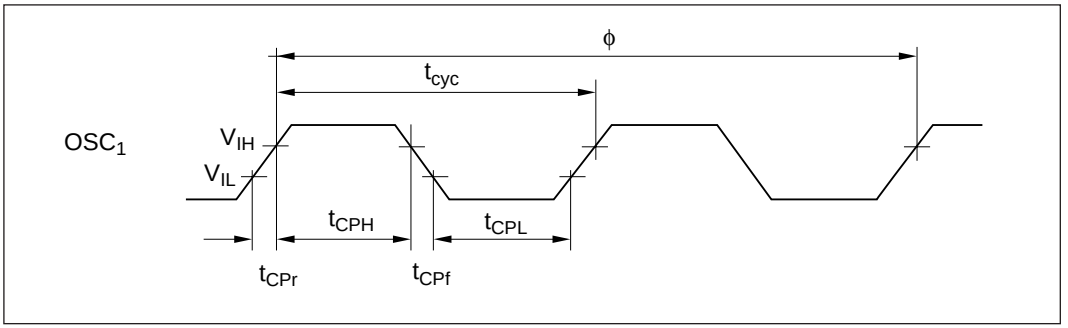


Figure 14-1 System Clock Input Timing

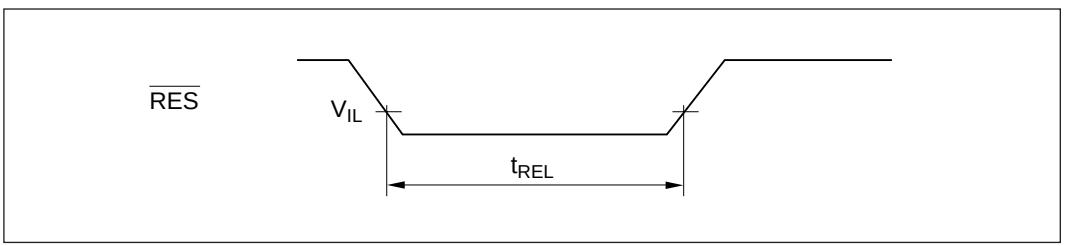


Figure 14-2 $\overline{\text{RES}}$ Pin Pulse Width (Low)

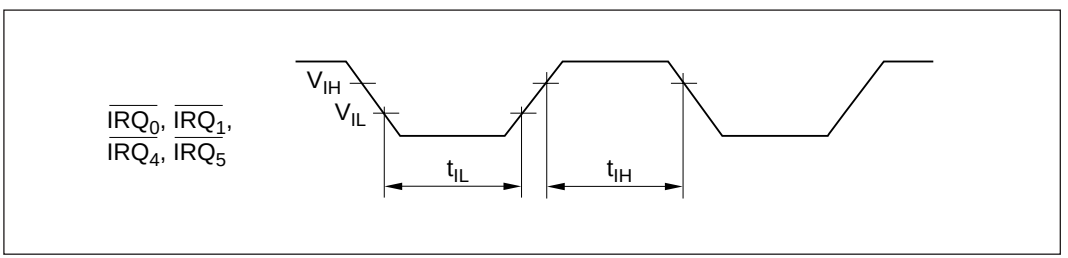


Figure 14-3 $\overline{\text{IRQ}}$ Pin Input Timing

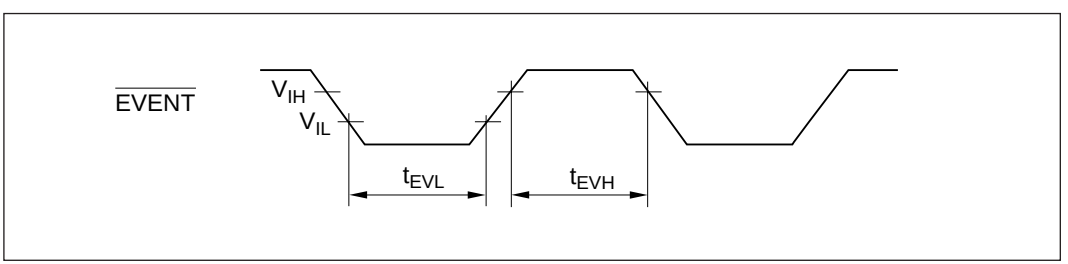


Figure 14-4 $\overline{\text{EVENT}}$ Pin Minimum Pulse Widths

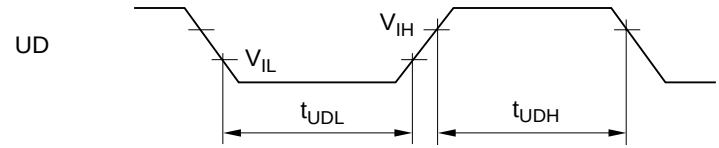
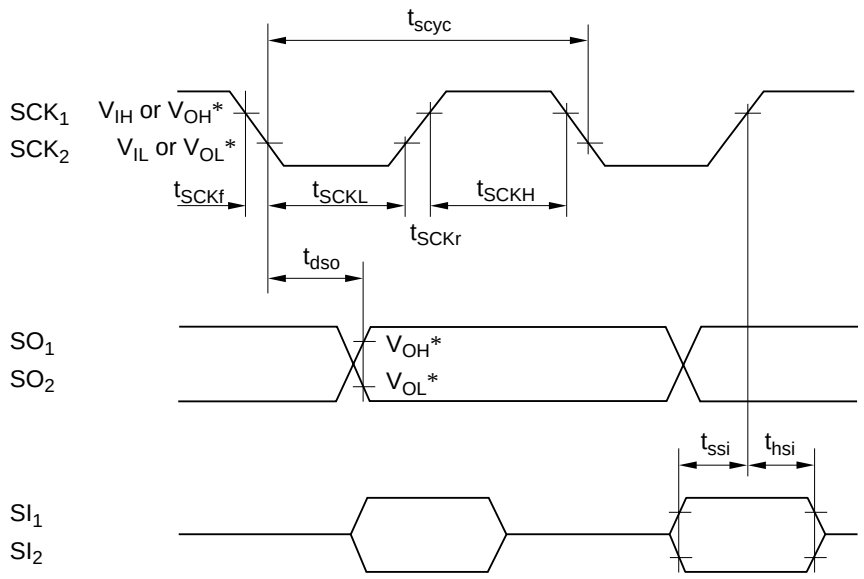
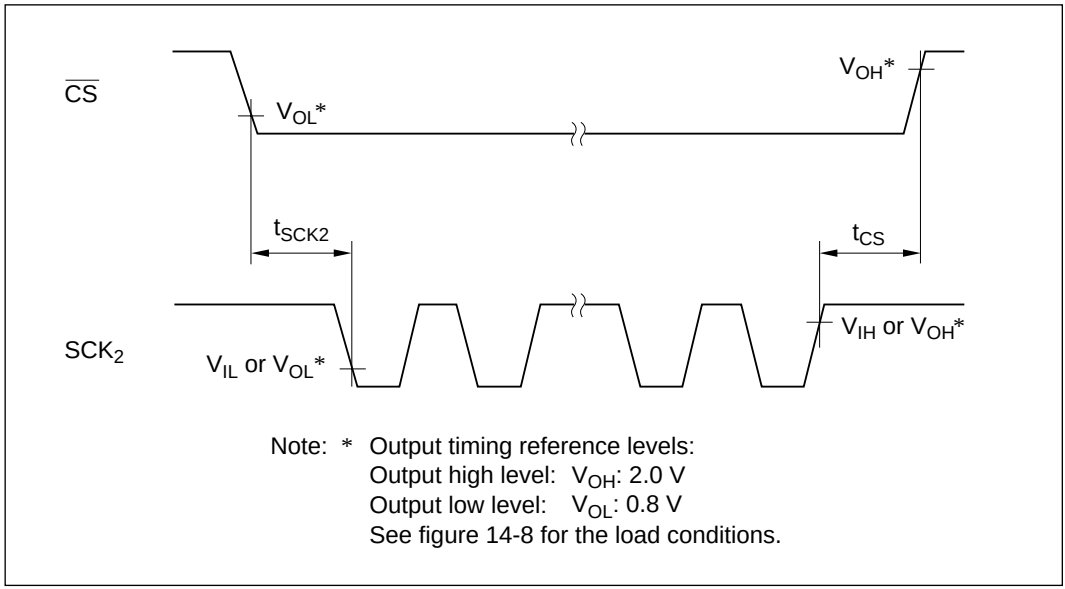


Figure 14-5 UD Pin Minimum High/Low Width



Note: * Output timing reference levels:
Output high level: V_{OH}: 2.0 V
Output low level: V_{OL}: 0.8 V
See figure 14-8 for the load conditions.

Figure 14-6 SCI I/O Timing



Note: * Output timing reference levels:
Output high level: V_{OH}: 2.0 V
Output low level: V_{OL}: 0.8 V
See figure 14-8 for the load conditions.

Figure 14-7 Serial Communication Interface 2 Chip Select Timing

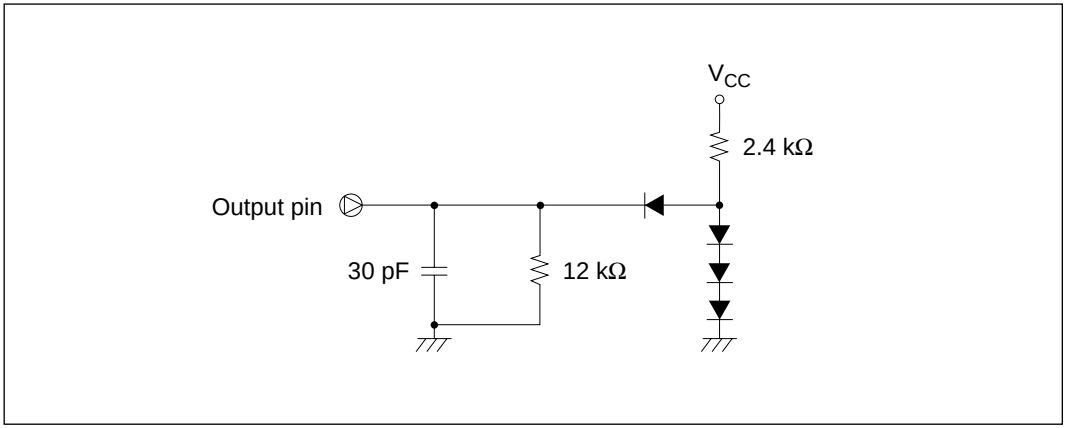


Figure 14-8 Output Load Conditions

14.5 Differences in Electrical Characteristics between HD6473714 and HD6433712/HD6433713/HD6433714

Table 14-12 shows the difference in electrical characteristics between the HD6473714 and HD6433712/HD6433713/HD6433714.

Table 14-12 Differences in Electrical Characteristics between HD6473714 and HD6433712/HD6433713/HD6433714

				Mask ROM Version			ZTAT™ Version			
Item	**Symbol**	**Applicable Pins**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Operation range in subactive mode		V_{CC}		2.5	—	5.5	2.7	—	5.5	V
Input leakage current	$\|I_{IL}\|$	$\overline{RES}$		—	—	1	—	—	40	µA
Input capacitance	C_{IN}	P16/$\overline{EVENT}$		—	—	15	—	—	35	pF
		P17/V_{disp}		—	—	30	—	—	20	
		$\overline{RES}$		—	—	15	—	—	70	
Power dissipation when CPU operating in active mode	I_{OPE}	V_{CC}	V_{CC} = 5 V, f_{OSC} = 8 MHz	—	15	—	—	17	—	mA
			V_{CC} = 5 V, f_{OSC} = 4 MHz	—	8	—	—	9	—	
			V_{CC} = 3 V, f_{OSC} = 4 MHz	—	5	—	—	6	—	
Power dissipation during reset in active mode	I_{RES}	V_{CC}	V_{CC} = 5 V, f_{OSC} = 8 MHz	—	5	8	—	6	9	mA
			V_{CC} = 5 V, f_{OSC} = 4 MHz	—	2.5	4	—	3	5	
			V_{CC} = 3 V, f_{OSC} = 4 MHz	—	1.3	—	—	1.5	—	
Power dissipation in sleep mode	I_{SLEEP}	V_{CC}	V_{CC} = 5 V, f_{OSC} = 8 MHz	—	2	3	—	2.5	3.5	
			V_{CC} = 5 V, f_{OSC} = 4 MHz	—	1	1.5	—	1.5	2	
			V_{CC} = 3 V, f_{OSC} = 4 MHz	—	0.6	—	—	1	—	

Table 14-12 Differences in Electrical Characteristics between HD6473714 and HD6433713/HD6433714 (cont)

Item	Symbol	Applicable Pins	Test Conditions	Mask ROM Version			ZTAT™ Version			Unit
				Min	Typ	Max	Min	Typ	Max	
Power dissipation in subactive mode	I_{SUB}	V_{CC}	V_{CC} = 2.5 V (no bypass capacitor)	—	5	20				µA
			V_{CC} = 2.5 V (47 µF bypass capacitor)	—	9	—				
			V_{CC} = 2.7 V (no bypass capacitor)				—	6	20	
			V_{CC} = 2.7 V (47 µF bypass capacitor)				—	11	—	
			V_{CC} = 5 V (no bypass capacitor)	—	13	—	—	16	—	
			V_{CC} = 5 V (47 µF bypass capacitor)	—	20	—	—	22	—	
Power dissipation in watch mode	I_{WATCH}	V_{CC}	V_{CC} = 2.5 V (no bypass capacitor)	—	2.2	5				µA
			V_{CC} = 2.5 V (47 µF bypass capacitor)	—	2.8	—				
			V_{CC} = 2.7 V (no bypass capacitor)				—	3.2	6	
			V_{CC} = 2.7 V (47 µF bypass capacitor)				—	3.8	—	
			V_{CC} = 5 V (no bypass capacitor)	—	6	—	—	10	—	
			V_{CC} = 5 V (47 µF bypass capacitor)	—	8	—	—	12	—	
Power dissipation in standby mode	I_{STBY}	V_{CC}		—	—	5	—	—	10	µA

Appendix A CPU Instruction Set

A.1 Instruction Notation

Operation Notation

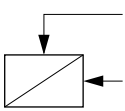
Rd8/16	General register (destination) (8 or 16 bits)
Rs8/16	General register (source) (8 or 16 bits)
Rn8/16	General register (8 or 16 bits)
CCR	Condition code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
PC	Program counter
SP	Stack pointer
#xx: 3/8/16	Immediate data (3, 8, or 16 bits)
d: 8/16	Displacement (8 or 16 bits)
@aa: 8/16	Absolute address (8 or 16 bits)
+	Addition
–	Subtraction
×	Multiplication
÷	Division
∧	AND logical
∨	OR logical
⊕	Exclusive OR logical
→	Move
¬	Logical complement

Condition Code Notation

Symbol	
↕	Modified according to the instruction result
*	Not fixed (value not guaranteed)
0	Always cleared to 0
—	Not affected by the instruction execution result

A.2 Operation Code Map

Table A-1 is an operation code map. It shows the operation codes contained in the first byte of the instruction code (bits 15 to 8 of the first instruction word).



Instruction when first bit of byte 2 (bit 7 of first instruction word) is 0.

Instruction when first bit of byte 2 (bit 7 of first instruction word) is 1.

Table A-1 Operation Code Map

HI \ LO	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SLEEP	STC	LDC	ORC	XORC	ANDC	LDC	ADD		INC	ADDS	MOV		ADDX	DAA
1	SHLL / SHAL	SHLR / SHAR	ROTXL / ROTL	ROTXR / ROTR	OR	XOR	AND	NOT / NEG	SUB		DEC	SUBS	CMP		SUBX	DAS
2	MOV															
3																
4	BRA	BRN	BHI	BLS	BCC	BCS	BNE	BEQ	BVC	BVS	BPL	BMI	BGE	BLT	BGT	BLE
5	MULXU	DIVXU			RTS	BSR	RTE		JMP					JSR		
6	BSET	BNOT	BCLR	BTST				BST / BIST	MOV*							
7					BOR / BIOR	BXOR / BIXOR	BAND / BIAND	BLD / BILD		MOV		EEPMOV	Bit manipulation instruction			
8	ADD															
9	ADDX															
A	CMP															
B	SUBX															
C	OR															
D	XOR															
E	AND															
F	MOV															

Note: * The PUSH and POP instructions are identical in machine language to MOV instructions.

A.3 Number of States Required for Execution

Table A-2 Instruction Set

Mnemonic	Operand Size	Operation	Addressing Mode/ Instruction Length (bytes)									Condition Code						No. of States
			#xx:8/16	Rn	@Rn	@(d:16, Rn)	@–Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	|	I	H	N	Z	V	C	
MOV.B #xx:8, Rd	B	#xx:8 → Rd8	2									—	—	↕	↕	0	—	2
MOV.B Rs, Rd	B	Rs8 → Rd8		2								—	—	↕	↕	0	—	2
MOV.B @Rs, Rd	B	@Rs16 → Rd8			2							—	—	↕	↕	0	—	4
MOV.B @(d:16, Rs), Rd	B	@(d:16, Rs16)→ Rd8				4						—	—	↕	↕	0	—	6
MOV.B @Rs+, Rd	B	@Rs16 → Rd8 Rs16+1 → Rs16					2					—	—	↕	↕	0	—	6
MOV.B @aa:8, Rd	B	@aa:8 → Rd8						2				—	—	↕	↕	0	—	4
MOV.B @aa:16, Rd	B	@aa:16 → Rd8						4				—	—	↕	↕	0	—	6
MOV.B Rs, @Rd	B	Rs8 → @Rd16			2							—	—	↕	↕	0	—	4
MOV.B Rs, @(d:16, Rd)	B	Rs8 → @(d:16, Rd16)				4						—	—	↕	↕	0	—	6
MOV.B Rs, @—Rd	B	Rd16–1 → Rd16 Rs8 → @Rd16					2					—	—	↕	↕	0	—	6
MOV.B Rs, @aa:8	B	Rs8 → @aa:8						2				—	—	↕	↕	0	—	4
MOV.B Rs, @aa:16	B	Rs8 → @aa:16						4				—	—	↕	↕	0	—	6
MOV.W #xx:16, Rd	W	#xx:16 → Rd	4									—	—	↕	↕	0	—	4
MOV.W Rs, Rd	W	Rs16 → Rd16		2								—	—	↕	↕	0	—	2
MOV.W @Rs, Rd	W	@Rs16 → Rd16			2							—	—	↕	↕	0	—	4
MOV.W @(d:16, Rs), Rd	W	@(d:16, Rs16) → Rd16				4						—	—	↕	↕	0	—	6
MOV.W @Rs+, Rd	W	@Rs16 → Rd16 Rs16+2 → Rs16					2					—	—	↕	↕	0	—	6
MOV.W @aa:16, Rd	W	@aa:16 → Rd16						4				—	—	↕	↕	0	—	6
MOV.W Rs, @Rd	W	Rs16 → @Rd16			2							—	—	↕	↕	0	—	4
MOV.W Rs, @(d:16, Rd)	W	Rs16 → @(d:16, Rd16)				4						—	—	↕	↕	0	—	6
MOV.W Rs, @—Rd	W	Rd16–2 → Rd16 Rs16 → @Rd16					2					—	—	↕	↕	0	—	6
MOV.W Rs, @aa:16	W	Rs16 → @aa:16						4				—	—	↕	↕	0	—	6
POP Rd	W	@SP → Rd16 SP+2 → SP					2					—	—	↕	↕	0	—	6
PUSH Rs	W	SP–2 → SP Rs16 → @SP					2					—	—	↕	↕	0	—	6

Table A-2 Instruction Set (cont)

Mnemonic	Operand Size	Operation	Addressing Mode/ Instruction Length (bytes)									Condition Code						No. of States
			#xx:8/16	Rn	@Rn	@(d:16, Rn)	@–Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	|	I	H	N	Z	V	C	
EEPMOV	—	if R4L≠0 then Repeat @R5 → @R6 R5+1 → R5 R6+1 → R6 R4L–1 → R4L Until R4L=0 else next									4	—	—	—	—	—	—	④
ADD.B #xx:8, Rd	B	Rd8+#xx:8 → Rd8	2									—	↕	↕	↕	↕	↕	2
ADD.B Rs, Rd	B	Rd8+Rs8 → Rd8		2								—	↕	↕	↕	↕	↕	2
ADD.W Rs, Rd	W	Rd16+Rs16 → Rd16		2								—	①	↕	↕	↕	↕	2
ADDX.B #xx:8, Rd	B	Rd8+#xx:8 +C → Rd8	2									—	↕	↕	②	↕	↕	2
ADDX.B Rs, Rd	B	Rd8+Rs8 +C → Rd8		2								—	↕	↕	②	↕	↕	2
ADDS.W #1, Rd	W	Rd16+1 → Rd16		2								—	—	—	—	—	—	2
ADDS.W #2, Rd	W	Rd16+2 → Rd16		2								—	—	—	—	—	—	2
INC.B Rd	B	Rd8+1 → Rd8		2								—	—	↕	↕	↕	—	2
DAA.B Rd	B	Rd8 decimal adjust → Rd8		2								—	*	↕	↕	*	③	2
SUB.B Rs, Rd	B	Rd8–Rs8 → Rd8		2								—	↕	↕	↕	↕	↕	2
SUB.W Rs, Rd	W	Rd16–Rs16 → Rd16		2								—	①	↕	↕	↕	↕	2
SUBX.B #xx:8, Rd	B	Rd8–#xx:8–C → Rd8	2									—	↕	↕	②	↕	↕	2
SUBX.B Rs, Rd	B	Rd8–Rs8–C → Rd8		2								—	↕	↕	②	↕	↕	2
SUBS.W #1, Rd	W	Rd16–1 → Rd16		2								—	—	—	—	—	—	2
SUBS.W #2, Rd	W	Rd16–2 → Rd16		2								—	—	—	—	—	—	2
DEC.B Rd	B	Rd8–1 → Rd8		2								—	—	↕	↕	↕	—	2
DAS.B Rd	B	Rd8 decimal adjust → Rd8		2								—	*	↕	↕	*	—	2
NEG.B Rd	B	0–Rd → Rd		2								—	↕	↕	↕	↕	↕	2
CMP.B #xx:8, Rd	B	Rd8–#xx:8	2									—	↕	↕	↕	↕	↕	2
CMP.B Rs, Rd	B	Rd8–Rs8		2								—	↕	↕	↕	↕	↕	2
CMP.W Rs, Rd	W	Rd16–Rs16		2								—	①	↕	↕	↕	↕	2

Table A-2 Instruction Set (cont)

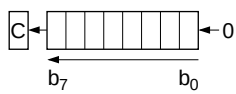
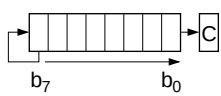
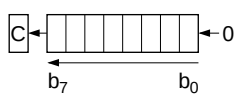
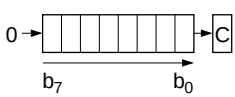
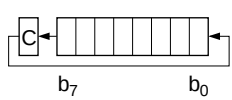
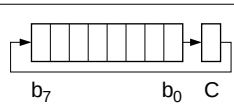
Mnemonic	Operand Size	Operation	Addressing Mode/ Instruction Length (bytes)									Condition Code						No. of States
			#xx:8/16	Rn	@Rn	@(d:16, Rn)	@–Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	|	I	H	N	Z	V	C	
MULXU.B Rs, Rd	B	Rd8 × Rs8 → Rd16		2								—	—	—	—	—	—	14
DIVXU.B Rs, Rd	B	Rd16÷Rs8 → Rd16 (RdH: remainder, RdL: quotient)		2								—	—	⑤	⑥	—	—	14
AND.B #xx:8, Rd	B	Rd8∧#xx:8 → Rd8	2									—	—	↕	↕	0	—	2
AND.B Rs, Rd	B	Rd8∧Rs8 → Rd8		2								—	—	↕	↕	0	—	2
OR.B #xx:8, Rd	B	Rd8∨#xx:8 → Rd8	2									—	—	↕	↕	0	—	2
OR.B Rs, Rd	B	Rd8∨Rs8 → Rd8		2								—	—	↕	↕	0	—	2
XOR.B #xx:8, Rd	B	Rd8⊕#xx:8 → Rd8	2									—	—	↕	↕	0	—	2
XOR.B Rs, Rd	B	Rd8⊕Rs8 → Rd8		2								—	—	↕	↕	0	—	2
NOT.B Rd	B	$\overline{Rd}$ → Rd		2								—	—	↕	↕	0	—	2
SHAL.B Rd	B			2								—	—	↕	↕	↕	↕	2
SHAR.B Rd	B			2								—	—	↕	↕	0	↕	2
SHLL.B Rd	B			2								—	—	↕	↕	0	↕	2
SHLR.B Rd	B			2								—	—	0	↕	0	↕	2
ROTXL.B Rd	B			2								—	—	↕	↕	0	↕	2
ROTXR.B Rd	B			2								—	—	↕	↕	0	↕	2

Table A-2 Instruction Set (cont)

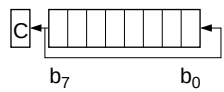
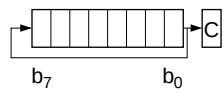
Mnemonic	Operand Size	Operation	Addressing Mode/ Instruction Length (bytes)									Condition Code						No. of States
			#xx:8/16	Rn	@Rn	@(d:16, Rn)	@–Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	|	I	H	N	Z	V	C	
ROTL.B Rd	B			2								—	—	↕	↕	0	↕	2
ROTR.B Rd	B			2								—	—	↕	↕	0	↕	2
BSET #xx:3, Rd	B	(#xx:3 of Rd8) ← 1		2								—	—	—	—	—	—	2
BSET #xx:3, @Rd	B	(#xx:3 of @Rd16) ← 1			4							—	—	—	—	—	—	8
BSET #xx:3, @aa:8	B	(#xx:3 of @aa:8) ← 1						4				—	—	—	—	—	—	8
BSET Rn, Rd	B	(Rn8 of Rd8) ← 1		2								—	—	—	—	—	—	2
BSET Rn, @Rd	B	(Rn8 of @Rd16) ← 1			4							—	—	—	—	—	—	8
BSET Rn, @aa:8	B	(Rn8 of @aa:8) ← 1						4				—	—	—	—	—	—	8
BCLR #xx:3, Rd	B	(#xx:3 of Rd8) ← 0		2								—	—	—	—	—	—	2
BCLR #xx:3, @Rd	B	(#xx:3 of @Rd16) ← 0			4							—	—	—	—	—	—	8
BCLR #xx:3, @aa:8	B	(#xx:3 of @aa:8) ← 0						4				—	—	—	—	—	—	8
BCLR Rn, Rd	B	(Rn8 of Rd8) ← 0		2								—	—	—	—	—	—	2
BCLR Rn, @Rd	B	(Rn8 of @Rd16) ← 0			4							—	—	—	—	—	—	8
BCLR Rn, @aa:8	B	(Rn8 of @aa:8) ← 0						4				—	—	—	—	—	—	8
BNOT #xx:3, Rd	B	(#xx:3 of Rd8) ← $\overline{\text{(\#xx:3 of Rd8)}}$		2								—	—	—	—	—	—	2
BNOT #xx:3, @Rd	B	(#xx:3 of @Rd16) ← $\overline{\text{(\#xx:3 of @Rd16)}}$			4							—	—	—	—	—	—	8
BNOT #xx:3, @aa:8	B	(#xx:3 of @aa:8) ← $\overline{\text{(\#xx:3 of @aa:8)}}$						4				—	—	—	—	—	—	8
BNOT Rn, Rd	B	(Rn8 of Rd8) ← $\overline{\text{(Rn8 of Rd8)}}$		2								—	—	—	—	—	—	2
BNOT Rn, @Rd	B	(Rn8 of @Rd16) ← $\overline{\text{(Rn8 of @Rd16)}}$			4							—	—	—	—	—	—	8
BNOT Rn, @aa:8	B	(Rn8 of @aa:8) ← $\overline{\text{(Rn8 of @aa:8)}}$						4				—	—	—	—	—	—	8

Table A-2 Instruction Set (cont)

Mnemonic	Operand Size	Operation	Addressing Mode/ Instruction Length (bytes)									Condition Code						No. of States
			#xx:8/16	Rn	@Rn	@(d:16, Rn)	@–Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	|	I	H	N	Z	V	C	
BTST #xx:3, Rd	B	$(\overline{\#xx:3 \text{ of } Rd8}) \rightarrow Z$		2								—	—	—	↕	—	—	2
BTST #xx:3, @Rd	B	$(\overline{\#xx:3 \text{ of } @Rd16}) \rightarrow Z$			4							—	—	—	↕	—	—	6
BTST #xx:3, @aa:8	B	$(\overline{\#xx:3 \text{ of } @aa:8}) \rightarrow Z$						4				—	—	—	↕	—	—	6
BTST Rn, Rd	B	$(\overline{Rn8 \text{ of } Rd8}) \rightarrow Z$		2								—	—	—	↕	—	—	2
BTST Rn, @Rd	B	$(\overline{Rn8 \text{ of } @Rd16}) \rightarrow Z$			4							—	—	—	↕	—	—	6
BTST Rn, @aa:8	B	$(\overline{Rn8 \text{ of } @aa:8}) \rightarrow Z$						4				—	—	—	↕	—	—	6
BLD #xx:3, Rd	B	(#xx:3 of Rd8) → C		2								—	—	—	—	—	↕	2
BLD #xx:3, @Rd	B	(#xx:3 of @Rd16) → C			4							—	—	—	—	—	↕	6
BLD #xx:3, @aa:8	B	(#xx:3 of @aa:8) → C						4				—	—	—	—	—	↕	6
BILD #xx:3, Rd	B	$(\overline{\#xx:3 \text{ of } Rd8}) \rightarrow C$		2								—	—	—	—	—	↕	2
BILD #xx:3, @Rd	B	$(\overline{\#xx:3 \text{ of } @Rd16}) \rightarrow C$			4							—	—	—	—	—	↕	6
BILD #xx:3, @aa:8	B	$(\overline{\#xx:3 \text{ of } @aa:8}) \rightarrow C$						4				—	—	—	—	—	↕	6
BST #xx:3, Rd	B	C → (#xx:3 of Rd8)		2								—	—	—	—	—	—	2
BST #xx:3, @Rd	B	C → (#xx:3 of @Rd16)			4							—	—	—	—	—	—	8
BST #xx:3, @aa:8	B	C → (#xx:3 of @aa:8)						4				—	—	—	—	—	—	8
BIST #xx:3, Rd	B	$\overline{C} \rightarrow$ (#xx:3 of Rd8)		2								—	—	—	—	—	—	2
BIST #xx:3, @Rd	B	$\overline{C} \rightarrow$ (#xx:3 of @Rd16)			4							—	—	—	—	—	—	8
BIST #xx:3, @aa:8	B	$\overline{C} \rightarrow$ (#xx:3 of @aa:8)						4				—	—	—	—	—	—	8
BAND #xx:3, Rd	B	C∧(#xx:3 of Rd8) → C		2								—	—	—	—	—	↕	2
BAND #xx:3, @Rd	B	C∧(#xx:3 of @Rd16) → C			4							—	—	—	—	—	↕	6
BAND #xx:3, @aa:8	B	C∧(#xx:3 of @aa:8) → C						4				—	—	—	—	—	↕	6
BIAND #xx:3, Rd	B	$C \wedge (\overline{\#xx:3 \text{ of } Rd8}) \rightarrow C$		2								—	—	—	—	—	↕	2
BIAND #xx:3, @Rd	B	$C \wedge (\overline{\#xx:3 \text{ of } @Rd16}) \rightarrow C$			4							—	—	—	—	—	↕	6
BIAND #xx:3, @aa:8	B	$C \wedge (\overline{\#xx:3 \text{ of } @aa:8}) \rightarrow C$						4				—	—	—	—	—	↕	6
BOR #xx:3, Rd	B	C∨(#xx:3 of Rd8) → C		2								—	—	—	—	—	↕	2
BOR #xx:3, @Rd	B	C∨(#xx:3 of @Rd16) → C			4							—	—	—	—	—	↕	6
BOR #xx:3, @aa:8	B	C∨(#xx:3 of @aa:8) → C						4				—	—	—	—	—	↕	6
BIOR #xx:3, Rd	B	$C \vee (\overline{\#xx:3 \text{ of } Rd8}) \rightarrow C$		2								—	—	—	—	—	↕	2
BIOR #xx:3, @Rd	B	$C \vee (\overline{\#xx:3 \text{ of } @Rd16}) \rightarrow C$			4							—	—	—	—	—	↕	6

Table A-2 Instruction Set (cont)

Mnemonic	Operand Size	Operation	Branching Condition	Addressing Mode/ Instruction Length (bytes)									Condition Code						No. of States
				#xx:8/16	Rn	@Rn	@(d:16, Rn)	@–Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	|	I	H	N	Z	V	C	
BIOR #xx:3, @aa:8	B	C∨(#xx:3 of @aa:8) → C							4				—	—	—	—	—	↕	6
BXOR #xx:3, Rd	B	C⊕(#xx:3 of Rd8) → C			2								—	—	—	—	—	↕	2
BXOR #xx:3, @Rd	B	C⊕(#xx:3 of @Rd16) → C				4							—	—	—	—	—	↕	6
BXOR #xx:3, @aa:8	B	C⊕(#xx:3 of @aa:8) → C							4				—	—	—	—	—	↕	6
BIXOR #xx:3, Rd	B	C⊕(#xx:3 of Rd8) → C			2								—	—	—	—	—	↕	2
BIXOR #xx:3, @Rd	B	C⊕(#xx:3 of @Rd16) → C				4							—	—	—	—	—	↕	6
BIXOR #xx:3, @aa:8	B	C⊕(#xx:3 of @aa:8) → C							4				—	—	—	—	—	↕	6
BRA d:8 (BT d:8)	—	PC ← PC+d:8								2			—	—	—	—	—	—	4
BRN d:8 (BF d:8)	—	PC ← PC+2								2			—	—	—	—	—	—	4
BHI d:8	—	If condition is true then PC ← PC+d:8 else next;	C ∨ Z = 0							2			—	—	—	—	—	—	4
BLS d:8	—		C ∨ Z = 1							2			—	—	—	—	—	—	4
BCC d:8 (BHS d:8)	—		C = 0							2			—	—	—	—	—	—	4
BCS d:8 (BLO d:8)	—		C = 1							2			—	—	—	—	—	—	4
BNE d:8	—		Z = 0							2			—	—	—	—	—	—	4
BEQ d:8	—		Z = 1							2			—	—	—	—	—	—	4
BVC d:8	—		V = 0							2			—	—	—	—	—	—	4
BVS d:8	—		V = 1							2			—	—	—	—	—	—	4
BPL d:8	—		N = 0							2			—	—	—	—	—	—	4
BMI d:8	—		N = 1							2			—	—	—	—	—	—	4
BGE d:8	—		N⊕V = 0							2			—	—	—	—	—	—	4
BLT d:8	—		N⊕V = 1							2			—	—	—	—	—	—	4
BGT d:8	—		Z ∨ (N⊕V) = 0							2			—	—	—	—	—	—	4
BLE d:8	—		Z ∨ (N⊕V) = 1							2			—	—	—	—	—	—	4
JMP @Rn	—	PC ← Rn16				2							—	—	—	—	—	—	4
JMP @aa:16	—	PC ← aa:16							4				—	—	—	—	—	—	6
JMP @@aa:8	—	PC ← @aa:8									2		—	—	—	—	—	—	8
BSR d:8	—	SP–2 → SP PC → @SP PC ← PC+d:8								2			—	—	—	—	—	—	6

Table A-2 Instruction Set (cont)

Mnemonic	Operand Size	Operation	Addressing Mode/ Instruction Length (bytes)									Condition Code						No. of States
			#xx:8/16	Rn	@Rn	@(d:16, Rn)	@–Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	|	I	H	N	Z	V	C	
JSR @Rn	—	SP–2 → SP PC → @SP PC ← Rn16			2							—	—	—	—	—	—	6
JSR @aa:16	—	SP–2 → SP PC → @SP PC ← aa:16						4				—	—	—	—	—	—	8
JSR @@aa:8		SP–2 → SP PC → @SP PC ← @aa:8								2		—	—	—	—	—	—	8
RTS	—	PC ← @SP SP+2 → SP									2	—	—	—	—	—	—	8
RTE	—	CCR ← @SP SP+2 → SP PC ← @SP SP+2 → SP									2	↕	↕	↕	↕	↕	↕	10
SLEEP	—	Transit to sleep mode.									2	—	—	—	—	—	—	2
LDC #xx:8, CCR	B	#xx:8 → CCR	2									↕	↕	↕	↕	↕	↕	2
LDC Rs, CCR	B	Rs8 → CCR		2								↕	↕	↕	↕	↕	↕	2
STC CCR, Rd	B	CCR → Rd8		2								—	—	—	—	—	—	2
ANDC #xx:8, CCR	B	CCR∧#xx:8 → CCR	2									↕	↕	↕	↕	↕	↕	2
ORC #xx:8, CCR	B	CCR∨#xx:8 → CCR	2									↕	↕	↕	↕	↕	↕	2
XORC #xx:8, CCR	B	CCR⊕#xx:8 → CCR	2									↕	↕	↕	↕	↕	↕	2
NOP	—	PC ← PC+2									2	—	—	—	—	—	—	2

Notes: ① Set to 1 when there is a carry or borrow from bit 11; otherwise cleared to 0.
② If the result is zero, the previous value of the flag is retained; otherwise the flag is cleared to 0.
③ Set to 1 if decimal adjustment produces a carry; otherwise cleared to 0.
④ The number of states required for execution is 4n+9 (n = value of R4L).
⑤ Set to 1 if the divisor is negative; otherwise cleared to 0.
⑥ Set to 1 if the divisor is zero; otherwise cleared to 0.

Appendix B On-Chip Registers

B.1 On-Chip Registers (1)

Addr. (Last Byte)	Register Name	Bit Names								Module Name
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'A0	STAR	—	—	—	STA4	STA3	STA2	STA1	STA0	SCI2
H'A1	EDAR	—	—	—	EDA4	EDA3	EDA2	EDA1	EDA0	
H'A2	SCR2	—	—	—	I/O	GAP2	GAP1	PS1	PS0	
H'A3	STSR	—	—	—	SO2 LAST BIT	OVR	WT	GIT	STF	
H'A4 to H'AF	—	Not used								—
H'B0	SMR1	—	SMR16	SMR15	SMR14	SMR13	SMR12	SMR11	SMR10	SCI1
H'B1	SDRU1	SDRU17	SDRU16	SDRU15	SDRU14	SDRU13	SDRU12	SDRU11	SDRU10	
H'B2	SDRL1	SDRL17	SDRL16	SDRL15	SDRL14	SDRL13	SDRL12	SDRL11	SDRL10	
H'B3	SPR1	SO1 LAST BIT	—	—	—	—	—	—	—	
H'B4	—	—	—	—	—	—	—	—	—	—
H'B5	—	—	—	—	—	—	—	—	—	
H'B6	—	—	—	—	—	—	—	—	—	
H'B7	—	—	—	—	—	—	—	—	—	
H'B8	—	—	—	—	—	—	—	—	—	
H'B9	VFSR	VFLAG	KSE	—	SR4	SR3	SR2	SR1	SR0	VFD con-troller/ driver
H'BA	VFDR	FLMO	DM2	DM1	DM0	DR3	DR2	DR1	DR0	
H'BB	DBR	VFDE	DISP	—	—	DBR3	DBR2	DBR1	DBR0	
H'BC	AMR	AMR7	—	—	—	—	AMR2	AMR1	AMR0	A/D con-verter
H'BD	ADRR	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	
H'BE	ADSR	ADSF	—	—	—	—	—	—	—	
H'BF	—	—	—	—	—	—	—	—	—	

Notation: SCI1: Serial communication interface 1
SCI2: Serial communication interface 2

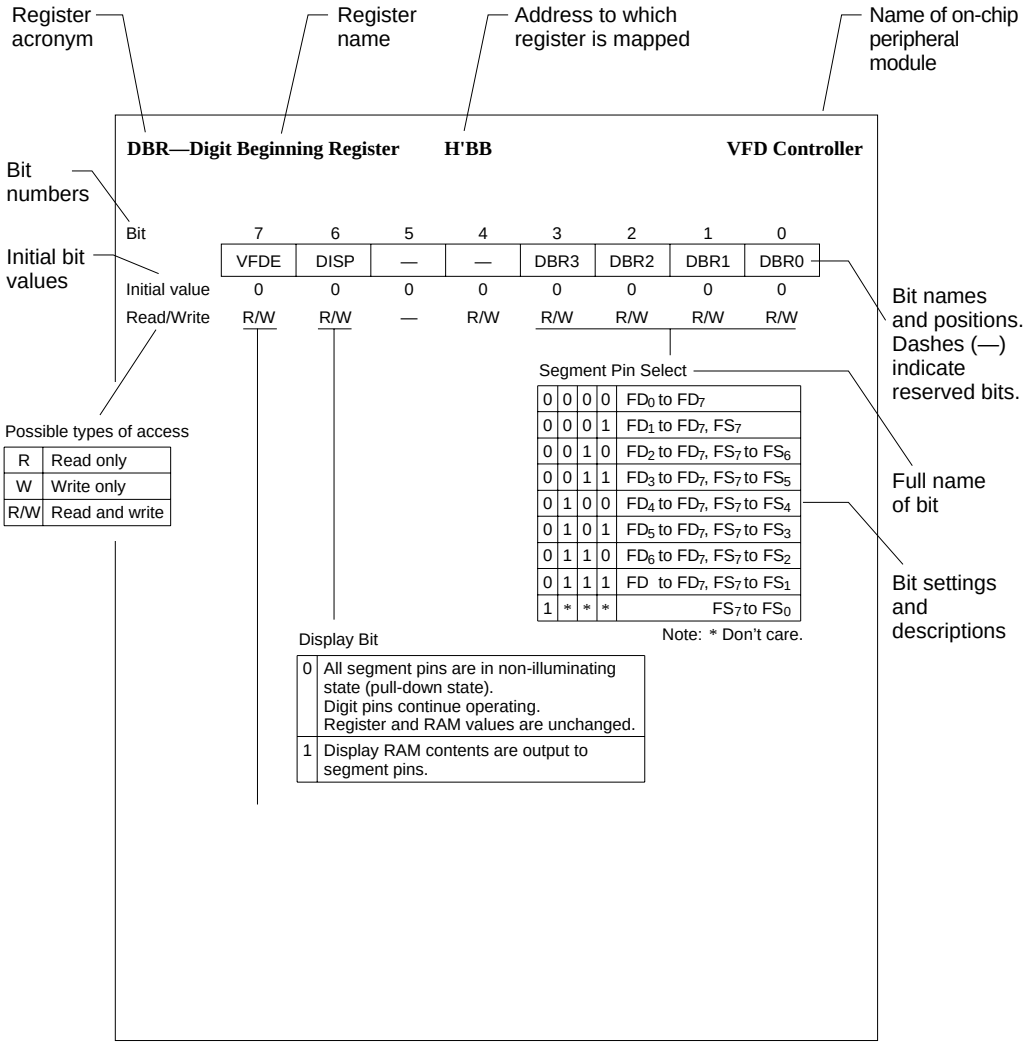
B.1 On-Chip Registers (1) (cont)

Addr. (Last Byte)	Register Name	Bit Names								Module Name
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'C0	TMA	—	—	—	—	TMA3	TMA2	TMA1	TMA0	Timer A
H'C1	TCA	TCA7	TCA6	TCA5	TCA4	TCA3	TCA2	TCA1	TCA0	
H'C2	TMB	TMB7	—	—	—	—	TMB2	TMB1	TMB0	Timer B
H'C3	TLB/TCB	TLB7/ TCB7	TLB6/ TCB6	TLB5/ TCB5	TLB4/ TCB4	TLB3/ TCB3	TLB2/ TCB2	TLB1/ TCB1	TLB0/ TCB0	
H'C4	TMC	TMC7	TMC6	TMC5	—	—	TMC2	TMC1	TMC0	Timer C
H'C5	TLC/TCC	TLC7/ TCC7	TLC6/ TCC6	TLC5/ TCC5	TLC4/ TCC4	TLC3/ TCC3	TLC2/ TCC2	TLC1/ TCC1	TLC0/ TCC0	
H'C6	TMD	CLR	—	—	—	—	—	—	EDG	Timer D
H'C7	TCD	TCD7	TCD6	TCD5	TCD4	TCD3	TCD2	TCD1	TCD0	
H'C8	TME	TME7	—	—	—	—	TME2	TME1	TME0	Timer E
H'C9	TLE/TCE	TLE7/ TCE7	TLE6/ TCE6	TLE5/ TCE5	TLE4/ TCE4	TLE3/ TCE3	TLE2/ TCE2	TLE1/ TCE1	TLE0/ TCE0	
H'CA	—	—	—	—	—	—	—	—	—	
H'CB	—	—	—	—	—	—	—	—	—	
H'CC	PWCR	—	—	—	—	—	—	—	PWCR0	14-bit PWM
H'CD	PWDRU	—	—	PWDRU5	PWDRU4	PWDRU3	PWDRU2	PWDRU1	PWDRU0	
H'CE	PWDRL	PWDRL7	PWDRL6	PWDRL5	PWDRL4	PWDRL3	PWDRL2	PWDRL1	PWDRL0	
H'CF	—	—	—	—	—	—	—	—	—	
H'D0	PDR0	$PDR0_7$	$PDR0_6$	$PDR0_5$	$PDR0_4$	$PDR0_3$	$PDR0_2$	$PDR0_1$	$PDR0_0$	I/O ports
H'D1	PDR1	—	—	$PDR1_5$	$PDR1_4$	—	—	$PDR1_1$	$PDR1_0$	
H'D2	—	—	—	—	—	—	—	—	—	
H'D3	—	—	—	—	—	—	—	—	—	
H'D4	PDR4	$PDR4_7$	$PDR4_6$	$PDR4_5$	$PDR4_4$	$PDR4_3$	$PDR4_2$	$PDR4_1$	$PDR4_0$	
H'D5	PDR5	$PDR5_7$	$PDR5_6$	$PDR5_5$	$PDR5_4$	$PDR5_3$	$PDR5_2$	$PDR5_1$	$PDR5_0$	
H'D6	PDR6	$PDR6_7$	$PDR6_6$	$PDR6_5$	$PDR6_4$	$PDR6_3$	$PDR6_2$	$PDR6_1$	$PDR6_0$	
H'D7	PDR7	$PDR7_7$	$PDR7_6$	$PDR7_5$	$PDR7_4$	$PDR7_3$	$PDR7_2$	$PDR7_1$	$PDR7_0$	
H'D8	—	—	—	—	—	—	—	—	—	
H'D9	PDR9	$PDR9_7$	$PDR9_6$	$PDR9_5$	$PDR9_4$	$PDR9_3$	$PDR9_2$	$PDR9_1$	$PDR9_0$	
H'DA	—	—	—	—	—	—	—	—	—	
H'DB	—	—	—	—	—	—	—	—	—	
H'DC	—	—	—	—	—	—	—	—	—	
H'DD	—	—	—	—	—	—	—	—	—	
H'DE	—	—	—	—	—	—	—	—	—	
H'DF	—	—	—	—	—	—	—	—	—	

B.1 On-Chip Registers (1) (cont)

Addr. (Last Byte)	Register Name	Bit Names								Module Name
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'E0	—	—	—	—	—	—	—	—	—	I/O ports
H'E1	PCR1	—	—	$PCR1_5$	$PCR1_4$	—	—	$PCR1_1$	$PCR1_0$	
H'E2	—	—	—	—	—	—	—	—	—	
H'E3	—	—	—	—	—	—	—	—	—	
H'E4	—	—	—	—	—	—	—	—	—	
H'E5	—	—	—	—	—	—	—	—	—	
H'E6	—	—	—	—	—	—	—	—	—	
H'E7	—	—	—	—	—	—	—	—	—	
H'E8	—	—	—	—	—	—	—	—	—	
H'E9	PCR9	$PCR9_7$	$PCR9_6$	$PCR9_5$	$PCR9_4$	$PCR9_3$	$PCR9_2$	$PCR9_1$	$PCR9_0$	
H'EA	—	—	—	—	—	—	—	—	—	
H'EB	PMR1	NOISE CANCEL	EVENT	IRQC5	IRQC4	—	—	IRQC1	IRQC0	
H'EC	PMR2	UP/ DOWN	SO2	SI2	SCK2	SO1	SI1	SCK1	PWM	
H'ED	PMR3	—	SO2 PMOS	CS	—	SO1 PMOS	—	—	—	
H'EE	PMR4	TEO	TEO ON	FREQ	VRFR	—	—	—	—	
H'EF	PMR0	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	
H'F0	SYSCR1	SSBY	STS2	STS1	STS0	LSON	—	—	—	System control
H'F1	SYSCR2	—	—	—	—	DTON	—	—	—	
H'F2	IEGR	—	—	—	IEG4	—	—	IEG1	IEG0	
H'F3	IENR1	—	—	IEN5	IEN4	—	—	IEN1	IEN0	
H'F4	IENR2	—	—	IENDT	IENTE	IENTD	IENTC	IENTB	IENTA	
H'F5	IENR3	IENAD	IENKS	—	—	—	—	IENS2	IENS1	
H'F6	IRR1	—	—	IRRI5	IRRI4	—	—	IRRI1	IRRI0	
H'F7	IRR2	—	—	IRRDT	IRRTE	IRRTD	IRRTC	IRRTB	IRRTA	
H'F8	IRR3	IRRAD	IRRKS	—	—	—	—	IRRS2	IRRS1	
H'F9	—	—	—	—	—	—	—	—	—	
H'FA	—	—	—	—	—	—	—	—	—	
H'FB	—	—	—	—	—	—	—	—	—	
H'FC	—	—	—	—	—	—	—	—	—	
H'FD	—	—	—	—	—	—	—	—	—	
H'FE	—	—	—	—	—	—	—	—	—	
H'FF	—	—	—	—	—	—	—	—	—	

B.2 On-Chip Registers (2)



STAR—Start Address Register **H'A0** **SCI2**

Bit	7	6	5	4	3	2	1	0
	—	—	—	STA4	STA3	STA2	STA1	STA0
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

Designates transfer starting address in range from H'FF80 to H'FF9F.

EDAR—End Address Register **H'A1** **SCI2**

Bit	7	6	5	4	3	2	1	0
	—	—	—	EDA4	EDA3	EDA2	EDA1	EDA0
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

Designates transfer end address in range from H'FF80 to H'FF9F.

SCR2—Serial Control Register **H'A2** **SCI2**

Bit	7	6	5	4	3	2	1	0
	—	—	—	I/O	GAP2	GAP1	PS1	PS0
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

Transmit/Receive Select

0	Receive mode
1	Transmit mode

Gap Select

0	0	No gap insertion
0	1	1-clock gap insertion
1	0	2-clock gap insertion
1	1	8-clock gap insertion

Serial Clock Select

0	0	$\phi/2$, SCK_2 is output pin
0	1	$\phi/4$, SCK_2 is output pin
1	0	$\phi/8$, SCK_2 is output pin
1	1	External clock, SCK_2 is input pin

Bit	7	6	5	4	3	2	1	0
	—	—	—	SO2 LAST BIT	OVR	WT	GIT	STF
Initial value	1	1	1	0	Not fixed	0	0	0
Read/Write	—	—	—	R/W	R/W*	R/W*	R/W	R/W

Extended Data Bit

0	Pin SO_2 output low
1	Pin SO_2 output high

Waiting Flag

0	[Clear condition] When STSR is written
1	[Set condition] When 32-byte data buffer is read or written during transfer

Overrun Flag

0	[Clear condition] When STSR is written
1	[Set condition] When overrun occurs

Gap Interval Flag

0	Insert gap every 16 bits
1	Insert gap every 8 bits

Start/Busy Flag

0	[Read] Transfer stopped [Write] Transfer aborted
1	[Read] Transfer in progress [Write] Starts transfer

Note: * Cleared to 0 by a write access to STSR.

SMR1—Serial Mode Register 1 **H'B0** **SCI1**

Bit	7	6	5	4	3	2	1	0
	—	SMR16	SMR15	SMR14	SMR13	SMR12	SMR11	SMR10
Initial value	1	0	0	0	0	0	0	0
Read/Write	—	W	W	W	W	W	W	W

Operation Mode Select

0	0	0	Clock continuous output mode
	Not 00		8-bit transfer mode
1	0	0	Clock continuous output mode
	Not 00		16-bit transfer mode

Clock Select

0	0	0	0	ϕ/1024, SCK_1 is output pin
			1	ϕ/256, SCK_1 is output pin
		1	0	ϕ/64, SCK_1 is output pin
			1	ϕ/32, SCK_1 is output pin
	1	0	0	ϕ/16, SCK_1 is output pin
			1	ϕ/8, SCK_1 is output pin
		1	0	ϕ/4, SCK_1 is output pin
			1	ϕ/2, SCK_1 is output pin
1	0	0	0	Not used
			1	Not used
		1	0	Not used
			1	Not used
	1	0	0	Not used
			1	Not used
		1	0	Not used
			1	External clock, SCK_1 is input pin

SDRU1—Serial Data Register U1 **H'B1** **SCI1**

Bit	7	6	5	4	3	2	1	0
	SDRU17	SDRU16	SDRU15	SDRU14	SDRU13	SDRU12	SDRU11	SDRU10
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Used to set transmit data and store received data.
8-bit transfer mode: not used
16-bit transfer mode: upper 8-bits of data register

Note: * Not fixed

SDRL1—Serial Data Register L1 **H'B2** **SCI1**

Bit	7	6	5	4	3	2	1	0
	SDRL17	SDRL16	SDRL15	SDRL14	SDRL13	SDRL12	SDRL11	SDRL10
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Used to set transmit data and store received data.
8-bit transfer mode: data register
16-bit transfer mode: lower 8-bits of data register

Note: * Not fixed

SPR1—Serial Port Register 1 **H'B3** **SCI1**

Bit	7	6	5	4	3	2	1	0
	SO1 LAST BIT	—	—	—	—	—	—	—
Initial value	*	1	1	1	1	1	1	1
Read/Write	R/W	—	—	—	—	—	—	—

Extended Data Bit

0	Pin SO_1 output low
0	Pin SO_1 output high

Note: * Not fixed

Bit	7	6	5	4	3	2	1	0
	VFLAG	KSE	—	SR4	SR3	SR2	SR1	SR0
Initial value	0	0	1	0	0	0	0	0
Read/Write	R/W	R/W	—	R/W	R/W	R/W	R/W	R/W

Key Scan Enable

0	No key scan interval
1	Key scan interval added

Segment Pin Select

0	0	0	0	0	FS_0	1	0	0	0	0	FS_0 to FS_{16}
0	0	0	0	1	FS_0 to FS_1	1	0	0	0	1	FS_0 to FS_{17}
0	0	0	1	0	FS_0 to FS_2	1	0	0	1	0	FS_0 to FS_{18}
0	0	0	1	1	FS_0 to FS_3	1	0	0	1	1	FS_0 to FS_{19}
0	0	1	0	0	FS_0 to FS_4	1	0	1	0	0	FS_0 to FS_{20}
0	0	1	0	1	FS_0 to FS_5	1	0	1	0	1	FS_0 to FS_{21}
0	0	1	1	0	FS_0 to FS_6	1	0	1	1	0	FS_0 to FS_{22}
0	0	1	1	1	FS_0 to FS_7	1	0	1	1	1	FS_0 to FS_{23}
0	1	0	0	0	FS_0 to FS_8	1	1	0	0	0	
0	1	0	0	1	FS_0 to FS_9	1	1	0	0	1	
0	1	0	1	0	FS_0 to FS_{10}	1	1	0	1	0	
0	1	0	1	1	FS_0 to FS_{11}	1	1	0	1	1	
0	1	1	0	0	FS_0 to FS_{12}	1	1	1	0	0	
0	1	1	0	1	FS_0 to FS_{13}	1	1	1	0	1	
0	1	1	1	0	FS_0 to FS_{14}	1	1	1	1	0	
0	1	1	1	1	FS_0 to FS_{15}	1	1	1	1	1	

VFD/Port Switching Flag

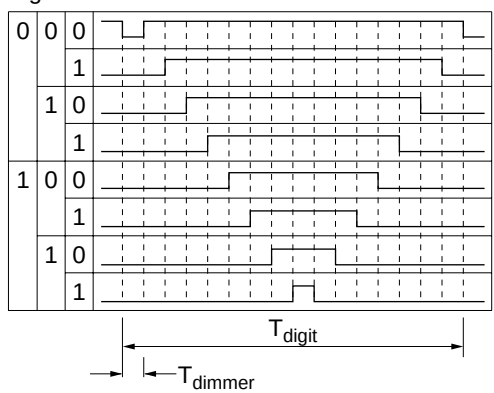
0	All pins doubling as general-purpose ports and VFD pins are used as general-purpose ports.
1	Pins designated as digit or segment pins function as VFD pins.

Bit	7	6	5	4	3	2	1	0
	FLMO	DM2	DM1	DM0	DR3	DR2	DR1	DR0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Digit Pin Select

0	0	0	0	FD_0 to FD_{15}	1	0	0	0	FD_0 to FD_7
0	0	0	1	FD_0 to FD_{14}	1	0	0	1	FD_0 to FD_6
0	0	1	0	FD_0 to FD_{13}	1	0	1	0	FD_0 to FD_5
0	0	1	1	FD_0 to FD_{12}	1	0	1	1	FD_0 to FD_4
0	1	0	0	FD_0 to FD_{11}	1	1	0	0	FD_0 to FD_3
0	1	0	1	FD_0 to FD_{10}	1	1	0	1	FD_0 to FD_2
0	1	1	0	FD_0 to FD_9	1	1	1	0	FD_0 to FD_1
0	1	1	1	FD_0 to FD_8	1	1	1	1	FD_0

Digit Waveform Select



VFD Mode Bit

0	T_{digit} = 1536/ϕ, T_{dimmer} = 96/ϕ
1	T_{digit} = 768/ϕ, T_{dimmer} = 48/ϕ

Bit	7	6	5	4	3	2	1	0
	VFDE	DISP	—	—	DBR3	DBR2	DBR1	DBR0
Initial value	0	0	1	0	0	0	0	0
Read/Write	R/W	R/W	—	R/W	R/W	R/W	R/W	R/W

Digit/Segment Pin Function Select

0	0	0	0	FD_0 to FD_7
0	0	0	1	FD_1 to FD_7, FS_7
0	0	1	0	FD_2 to FD_7, FS_7 to FS_6
0	0	1	1	FD_3 to FD_7, FS_7 to FS_5
0	1	0	0	FD_4 to FD_7, FS_7 to FS_4
0	1	0	1	FD_5 to FD_7, FS_7 to FS_3
0	1	1	0	FD_6 to FD_7, FS_7 to FS_2
0	1	1	1	FD_7, FS_7 to FS_1
1	*	*	*	FS_7 to FS_0

Note: * Don't care.

Display Bit

0	All segment pins are in non-illuminating state (pulled down). Digit pins continue operating. Register and RAM values are unchanged.
1	Display RAM contents are output to segment pins.

VFD Enable

0	VFD controller/driver is in reset state.
1	VFD controller/driver is in active state.

AMR—A/D Mode Register **H'BC** **A/D Converter**

Bit	7	6	5	4	3	2	1	0
	AMR7	—	—	—	—	AMR2	AMR1	AMR0
Initial value	0	1	1	1	1	0	0	0
Read/Write	R/W	—	—	—	—	R/W	R/W	R/W

Clock Select

0	Conversion period is 62/ϕ
1	Conversion period is 31/ϕ

Channel Select

0	0	0	Analog input pin is AN_0
		1	Analog input pin is AN_1
	1	0	Analog input pin is AN_2
		1	Analog input pin is AN_3
1	0	0	Analog input pin is AN_4
		1	Analog input pin is AN_5
	1	0	Analog input pin is AN_6
		1	Analog input pin is AN_7

ADRR—A/D Result Register **H'BD** **A/D Converter**

Bit	7	6	5	4	3	2	1	0
	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
Initial value	*	*	*	*	*	*	*	*
Read/Write	R	R	R	R	R	R	R	R

A/D Conversion Result

Note: * Not fixed

ADSR—A/D Start Register **H'BE** **A/D Converter**

Bit	7	6	5	4	3	2	1	0
	ADSF	—	—	—	—	—	—	—
Initial value	0	1	1	1	1	1	1	1
Read/Write	R/W	—	—	—	—	—	—	—

A/D Start Flag

0	[Read] A/D conversion stopped or complete [Write] A/D conversion aborted
1	[Read] A/D conversion in progress [Write] Starts A/D conversion

---

TMA—Timer Mode Register A **H'C0** **Timer A**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	TMA3	TMA2	TMA1	TMA0
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Clock Select

0	0	0	0	Input source PSS, ϕ/8192
			1	Input source PSS, ϕ/4096
		1	0	Input source PSS, ϕ/2048
			1	Input source PSS, ϕ/512
	1	0	0	Input source PSS, ϕ/256
			1	Input source PSS, ϕ/128
		1	0	Input source PSS, ϕ/32
			1	Input source PSS, ϕ/8
1	0	0	0	Input source PSW, 2 s
			1	Input source PSW, 1 s
		1	0	Input source PSW, 0.5 s
			1	Input source PSW, 125 ms
	1	0	0	PSW and TCA reset
			1	
		1	0	
			1	

TCA—Timer Counter A **H'C1** **Timer A**

Bit	7	6	5	4	3	2	1	0
	TCA7	TCA6	TCA5	TCA4	TCA3	TCA2	TCA1	TCA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Count Value

TMB—Timer Mode Register B **H'C2** **Timer B**

Bit	7	6	5	4	3	2	1	0
	TMB7	—	—	—	—	TMB2	TMB1	TMB0
Initial value	0	1	1	1	1	0	0	0
Read/Write	R/W	—	—	—	—	R/W	R/W	R/W

Clock Select

0	0	0	Internal clock, φ/8192
		1	Internal clock, φ/2048
	1	0	Internal clock, φ/512
		1	Internal clock, φ/256
1	0	0	Internal clock, φ/128
		1	Internal clock, φ/32
	1	0	Internal clock, φ/8
		1	External clock, choice of rising or falling edge

Auto Reload Function Select

0	Free-running timer
1	Auto-reload timer

TCB—Timer Counter B **H'C3** **Timer B**

Bit	7	6	5	4	3	2	1	0
	TCB7	TCB6	TCB5	TCB4	TCB3	TCB2	TCB1	TCB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Count Value

TLB—Timer Load Register B **H'C3** **Timer B**

Bit	7	6	5	4	3	2	1	0
	TLB7	TLB6	TLB5	TLB4	TLB3	TLB2	TLB1	TLB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Reload Value Setting

TMC—Timer Mode Register C **H'C4** **Timer C**

Bit	7	6	5	4	3	2	1	0
	TMC7	TMC6	TMC5	—	—	TMC2	TMC1	TMC0
Initial value	0	0	0	1	1	0	0	0
Read/Write	R/W	R/W	R/W	—	—	R/W	R/W	R/W

Clock Select

0	0	0	Internal clock, φ/8192
		1	Internal clock, φ/2048
	1	0	Internal clock, φ/512
		1	Internal clock, φ/256
1	0	0	Internal clock, φ/128
		1	Internal clock, φ/32
	1	0	Internal clock, φ/8
		1	External clock, choice of rising or falling edge

Count-Up/Down Control

0	0	Up-counter
	1	Down-counter
1	*	Hardware control via pin $P9_7$/UD. High is down, low is up.

Note: * Don't care.

Auto-Reload Function Select

0	Free-running timer
1	Auto-reload timer

TCC—Timer Counter C **H'C5** **Timer C**

Bit	7	6	5	4	3	2	1	0
	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Count Value

TLC—Timer Load Register C **H'C5** **Timer C**

Bit	7	6	5	4	3	2	1	0
	TLC7	TLC6	TLC5	TLC4	TLC3	TLC2	TLC1	TLC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Reload Value Setting

TMD—Timer Mode Register D **H'C6** **Timer D**

Bit	7	6	5	4	3	2	1	0
	CLR	—	—	—	—	—	—	EDG
Initial value	0	1	1	1	1	1	1	0
Read/Write	W	—	—	—	—	—	—	R/W

Edge Select

0	Incremented at falling edge of $\overline{\text{EVENT}}$ pin input
1	Incremented at rising edge of $\overline{\text{EVENT}}$ pin input

Counter Clear

0	After this bit is set to 1 and TCD is initialized, it is automatically cleared by hardware.
1	TCD is initialized to H'00.

TCD—Timer Counter D **H'C7** **Timer D**

Bit	7	6	5	4	3	2	1	0
	TCD7	TCD6	TCD5	TCD4	TCD3	TCD2	TCD1	TCD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Count Value

TME—Timer Mode Register E **H'C8** **Timer E**

Bit	7	6	5	4	3	2	1	0
	TME7	—	—	—	—	TME2	TME1	TME0
Initial value	0	1	1	1	1	0	0	0
Read/Write	R/W	—	—	—	—	R/W	R/W	R/W

Auto-Reload Function Select

0	Free-running timer
1	Auto-reload timer

Clock Select

0	0	0	Internal clock, φ/8192
		1	Internal clock, φ/4096
	1	0	Internal clock, φ/2048
		1	Internal clock, φ/512
1	0	0	Internal clock, φ/256
		1	Internal clock, φ/128
	1	0	Internal clock, φ/32
		1	Internal clock, φ/8

TCE—Timer Counter E **H'C9** **Timer E**

Bit	7	6	5	4	3	2	1	0
	TCE7	TCE6	TCE5	TCE4	TCE3	TCE2	TCE1	TCE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Count Value

TLE—Timer Load Register E **H'C9** **Timer E**

Bit	7	6	5	4	3	2	1	0
	TLE7	TLE6	TLE5	TLE4	TLE3	TLE2	TLE1	TLE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Reload Value Setting

PWCR—PWM Control Register **H'CC** **14-bit PWM**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PWCR0
Initial value	1	1	1	1	1	1	1	0
Read/Write	—	—	—	—	—	—	—	W

Clock Select

0	The input clock is $\phi/2$. The conversion period is $16384/\phi$, with a minimum modulation width of $1/\phi$.
1	The input clock is $\phi/4$. The conversion period is $32768/\phi$, with a minimum modulation width of $2/\phi$.

PWDRU—PWM Data Register U **H'CD** **14-bit PWM**

Bit	7	6	5	4	3	2	1	0
	—	—	PWDRU5	PWDRU4	PWDRU3	PWDRU2	PWDRU1	PWDRU0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

Upper 6 Bits of Data for PWM Waveform Generation

PWDRL—PWM Data Register L **H'CE** **14-bit PWM**

Bit	7	6	5	4	3	2	1	0
	PWDRL7	PWDRL6	PWDRL5	PWDRL4	PWDRL3	PWDRL2	PWDRL1	PWDRL0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Lower 8 Bits of Data for PWM Waveform Generation

PDR0—Port Data Register 0 **H'D0** **I/O Ports**

Bit	7	6	5	4	3	2	1	0
	$PDR0_7$	$PDR0_6$	$PDR0_5$	$PDR0_4$	$PDR0_3$	$PDR0_2$	$PDR0_1$	$PDR0_0$
Initial value	—	—	—	—	—	—	—	—
Read/Write	R	R	R	R	R	R	R	R

PDR1—Port Data Register 1 **H'D1** **I/O Ports**

Bit	7	6	5	4	3	2	1	0
	—	—	$PDR1_5$	$PDR1_4$	—	—	$PDR1_1$	$PDR1_0$
Initial value	— *	— *	0	0	1	1	0	0
Read/Write	—	—	R/W	R/W	—	—	R/W	R/W

Note: * Pins $P1_6$ and $P1_7$ are input-only pins; whenever they are read, the pin level is read out.

PDR4—Port Data Register 4 **H'D4** **I/O Ports**

Bit	7	6	5	4	3	2	1	0
	$PDR4_7$	$PDR4_6$	$PDR4_5$	$PDR4_4$	$PDR4_3$	$PDR4_2$	$PDR4_1$	$PDR4_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR5—Port Data Register 5 **H'D5** **I/O Ports**

Bit	7	6	5	4	3	2	1	0
	$PDR5_7$	$PDR5_6$	$PDR5_5$	$PDR5_4$	$PDR5_3$	$PDR5_2$	$PDR5_1$	$PDR5_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR6—Port Data Register 6 **H'D6** **I/O Ports**

Bit	7	6	5	4	3	2	1	0
	$PDR6_7$	$PDR6_6$	$PDR6_5$	$PDR6_4$	$PDR6_3$	$PDR6_2$	$PDR6_1$	$PDR6_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR7—Port Data Register 7 **H'D7** **I/O Ports**

Bit	7	6	5	4	3	2	1	0
	$PDR7_7$	$PDR7_6$	$PDR7_5$	$PDR7_4$	$PDR7_3$	$PDR7_2$	$PDR7_1$	$PDR7_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR9—Port Data Register 9 **H'D9** **I/O Ports**

Bit	7	6	5	4	3	2	1	0
	$PDR9_7$	$PDR9_6$	$PDR9_5$	$PDR9_4$	$PDR9_3$	$PDR9_2$	$PDR9_1$	$PDR9_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PCR1—Port Control Register 1 **H'E1** **I/O Ports**

Bit	7	6	5	4	3	2	1	0
	—	—	$PCR1_5$	$PCR1_4$	—	—	$PCR1_1$	$PCR1_0$
Initial value	1	1	0	0	1	1	0	0
Read/Write	—	—	W	W	—	—	W	W

Port 1 I/O Select

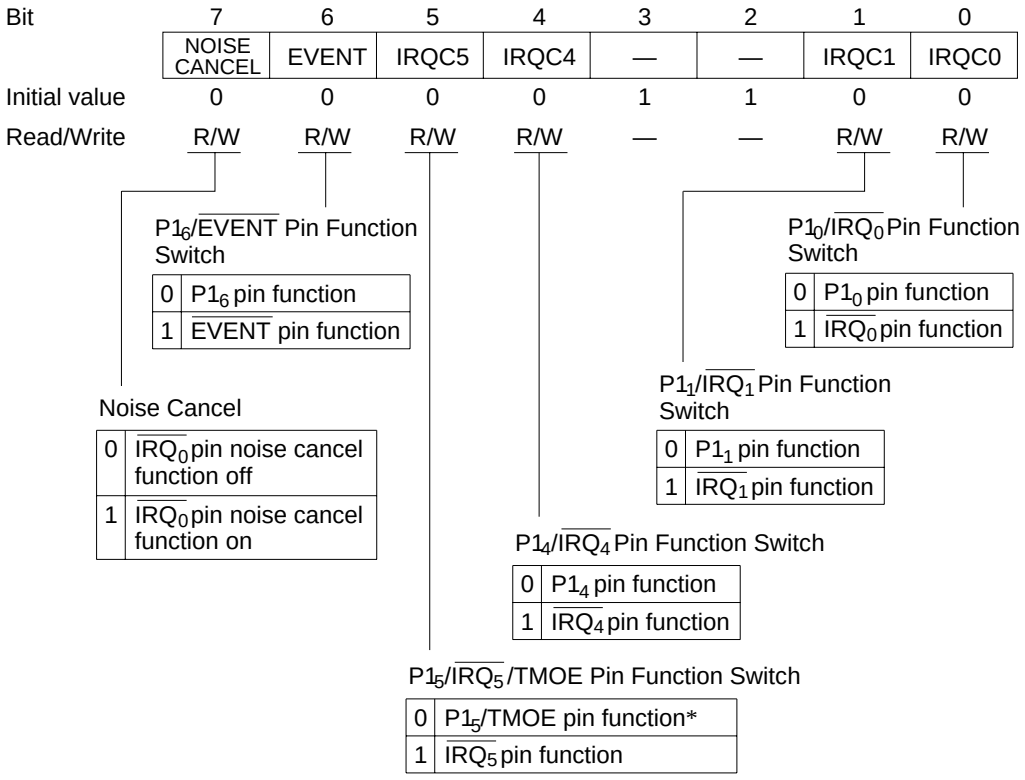
0	Input port
1	Output port

PCR9—Port Control Register 9 **H'E9** **I/O Ports**

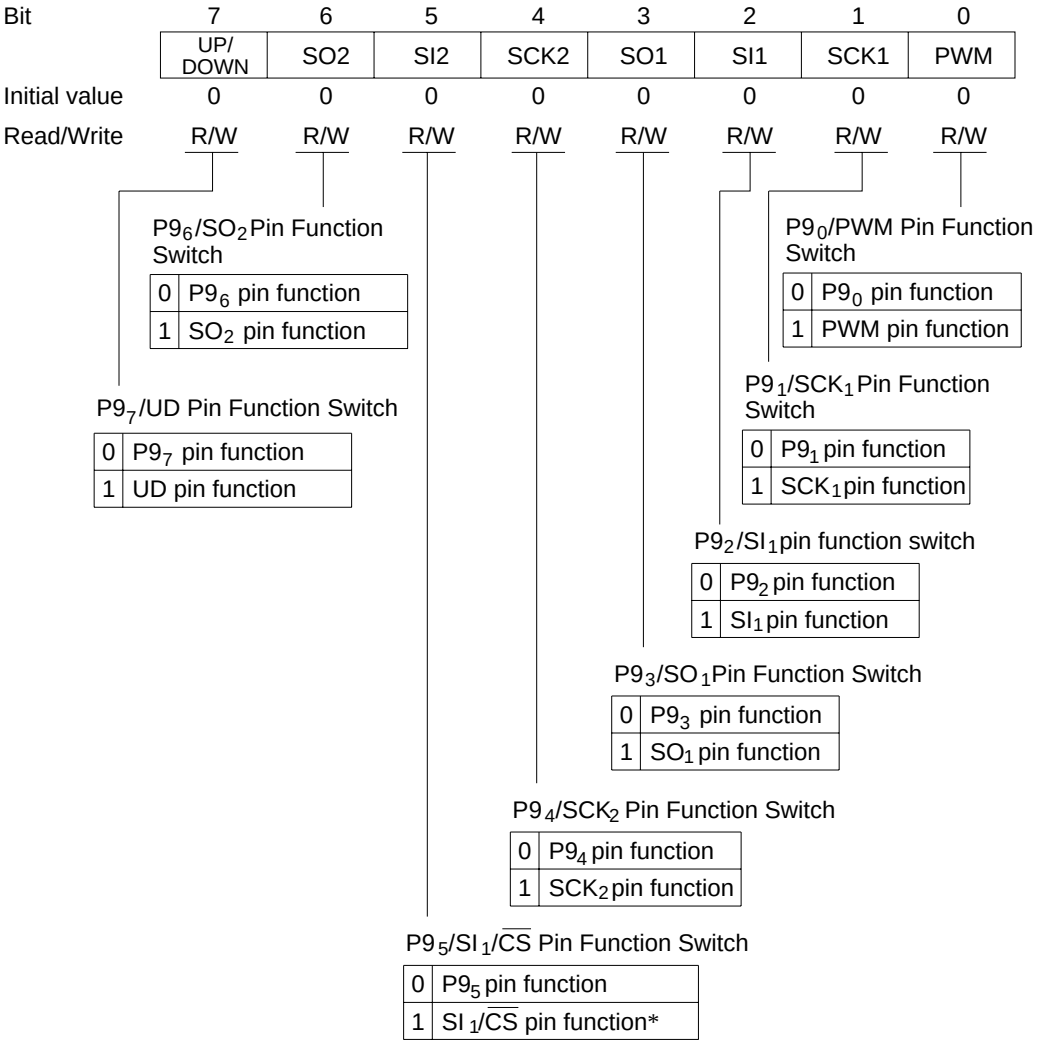
Bit	7	6	5	4	3	2	1	0
	$PCR9_7$	$PCR9_6$	$PCR9_5$	$PCR9_4$	$PCR9_3$	$PCR9_2$	$PCR9_1$	$PCR9_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 9 I/O Select

0	Input port
1	Output port



Note: * For the switching between $P1_5$ and TMOE pin functions see under PMR4.



Note: * For the switching between SI_1 and $\overline{CS}$ pin functions see under PMR3.

Bit	7	6	5	4	3	2	1	0
	—	SO2 PMOS	CS	—	SO1 PMOS	—	—	—
Initial value	1	0	0	1	0	1	1	1
Read/Write	—	R/W	R/W	—	R/W	—	—	—

SO_1 Pin PMOS On/Off

0	SO_1 pin PMOS buffer on. CMOS output.
1	SO_1 pin PMOS off. NMOS open-drain output.

Chip Select Output Select

PMR2 SI2	PMR3 CS	$P9_5/SI_2/\overline{CS}$ pin function switch
0	0	$P9_5$ pin function
	1	
1	0	SI_2 pin function
	1	$\overline{CS}$ pin function

SO_2 Pin PMOS On/Off

0	SO_2 pin PMOS buffer on. CMOS output.
1	SO_2 pin PMOS off. NMOS open-drain output.

PMR4—Port Mode Register 4 **H'EE** **I/O Ports**

Bit	7	6	5	4	3	2	1	0
	TEO	TEO ON	FREQ	VRFR	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Timer E Output Control

PMR1	PMR4				$P1_5/\overline{IRQ_5}$/TMOE Pin Function Switch	Pin Status
IRQC5	TEO	TEO ON	FREQ	VRFR		
0	0	*	*	*	$P1_5$ pin function	Standard I/O port
0	1	0	*	*	TMOE pin function (off)	Low-level output
0	1	1	0	0	TMOE pin function (on)	Fixed-frequency output: $\phi/2048$
0	1	1	1	0	TMOE pin function (on)	Fixed-frequency output: $\phi/1024$
0	1	1	*	1	TMOE pin function (on)	Variable-frequency output: output toggles at each timer E overflow
1	*	*	*	*	$\overline{IRQ_5}$ pin function	External interrupt input

Note: * Don't care.

PMR0—Port Mode Register 0 **H'EF** **I/O Ports**

Bit	7	6	5	4	3	2	1	0
	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Analog Input Select

0	General-purpose input port
1	Analog input channel

SYSCR1—System Control Register 1 **H'F0** **System Control**

Bit	7	6	5	4	3	2	1	0
	SSBY	STS2	STS1	STS0	LSON	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W*1	R/W	R/W	R/W	R/W	R/W	—	—

Low-Speed On Flag*2

0	CPU runs on system clock (φ)
1	CPU runs on subclock (ϕ_{SUB})

Standby Timer Select

0	0	0	Wait time = 8192 states
0	0	1	Wait time = 16384 states
0	1	0	Wait time = 32768 states
0	1	1	Wait time = 65536 states
1	*3	*3	Wait time = 131072 states

Standby

0	Sleep mode entered after SLEEP instruction is executed.
1	Standby mode entered after SLEEP instruction is executed.

Notes: 1. Write is enabled in active mode only.
2. This relates to the transitions between operation modes, so functioning depends on the combination of this bit with other control bits and interrupts. For details see 3.3, System Modes.
3. Don't care.

SYSCR2—System Control Register 2 **H'F1** **System Control**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	DTON	—	—	—
Initial value	1	1	1	1	0	1	0	0
Read/Write	—	—	—	—	W*	—	R/W	R/W

Direct Transfer On Flag

0	In subactive mode, watch mode is entered when a SLEEP instruction is executed.
1	In subactive mode, if LSON bit = 0, active mode is entered via watch mode when a SLEEP instruction is executed.

Note: * Write is enabled in subactive mode only.

IEGR—IRQ Edge Select Register **H'F2** **System Control**

Bit	7	6	5	4	3	2	1	0
	—	—	—	IEG4	—	—	IEG1	IEG0
Initial value	1	1	1	0	1	1	0	0
Read/Write	—	—	—	R/W	—	—	R/W	R/W

$\overline{IRQ_4}$ Input Edge Select

0	Rising edge detected.
1	Falling edge detected.

$\overline{IRQ_0}$ Input Edge Select

0	Rising edge detected.
1	Falling edge detected.

$\overline{IRQ_1}$ Input Edge Select

0	Rising edge detected.
1	Falling edge detected.

IENR1—Interrupt Enable Register 1 **H'F3** **System Control**

Bit	7	6	5	4	3	2	1	0
	—	—	IEN5	IEN4	—	—	IEN1	IEN0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

$\overline{IRQ_5}$ Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

$\overline{IRQ_4}$ Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

$\overline{IRQ_0}$ Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

$\overline{IRQ_1}$ Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

IENR2—Interrupt Enable Register 2 **H'F4** **System Control**

Bit	7	6	5	4	3	2	1	0
	—	—	IENDT	IENTE	IENTD	IENTC	IENTB	IENTA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DTON Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

Timer A Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

Timer E Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

Timer B Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

Timer D Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

Timer C Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

IENR3—Interrupt Enable Register 3 **H'F5** **System Control**

Bit	7	6	5	4	3	2	1	0
	IENAD	IENKS	—	—	—	—	IENS2	IENS1
Initial value	0	0	1	1	1	1	0	0
Read/Write	R/W	R/W	—	—	—	—	R/W	R/W

Key Scan Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

SCI1 Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

A/D Conversion Complete Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

SCI2 Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

Bit	7	6	5	4	3	2	1	0
	—	—	IRRI5	IRRI4	—	—	IRRI1	IRRI0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	R/W*	R/W*	—	—	R/W*	R/W*

$\overline{IRQ_5}$ Interrupt Request

0	No interrupt request
1	Interrupt request raised

$\overline{IRQ_4}$ Interrupt Request

0	No interrupt request
1	Interrupt request raised

$\overline{IRQ_0}$ Interrupt Request

0	No interrupt request
1	Interrupt request raised

$\overline{IRQ_1}$ Interrupt Request

0	No interrupt request
1	Interrupt request raised

Note: * Only 0 can be written, to clear the flag.

IRR2—Interrupt Request Register 2 **H'F7** **System Control**

Bit	7	6	5	4	3	2	1	0
	—	—	IRRDT	IRRTE	IRRTD	IRRTC	IRRTB	IRRTA
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

DTON Interrupt Request

0	No interrupt request
1	Interrupt request

Timer A Interrupt Request

0	No interrupt request
1	Interrupt request

Timer E Interrupt Request

0	No interrupt request
1	Interrupt request

Timer B Interrupt Request

0	No interrupt request
1	Interrupt request

Timer D Interrupt Request

0	No interrupt request
1	Interrupt request

Timer C Interrupt Request

0	No interrupt request
1	Interrupt request

Note: * Only 0 can be written, to clear the flag.

IRR3—Interrupt Request Register 3 **H'F8** **System Control**

Bit	7	6	5	4	3	2	1	0
	IRRAD	IRRKS	—	—	—	—	IRRS2	IRRS1
Initial value	0	0	1	1	1	1	0	0
Read/Write	R/W*	R/W*	—	—	—	—	R/W*	R/W*

Key Scan Interrupt Request

0	No interrupt request
1	Interrupt request

SCI1 Interrupt Request

0	No interrupt request
1	Interrupt request

A/D Conversion Complete Interrupt Request

0	No interrupt request
1	Interrupt request

SCI2 Interrupt Request

0	No interrupt request
1	Interrupt request

Note: * Only 0 can be written, to clear the flag.

Appendix C I/O Port Block Diagrams

C.1 Port 0 Block Diagram

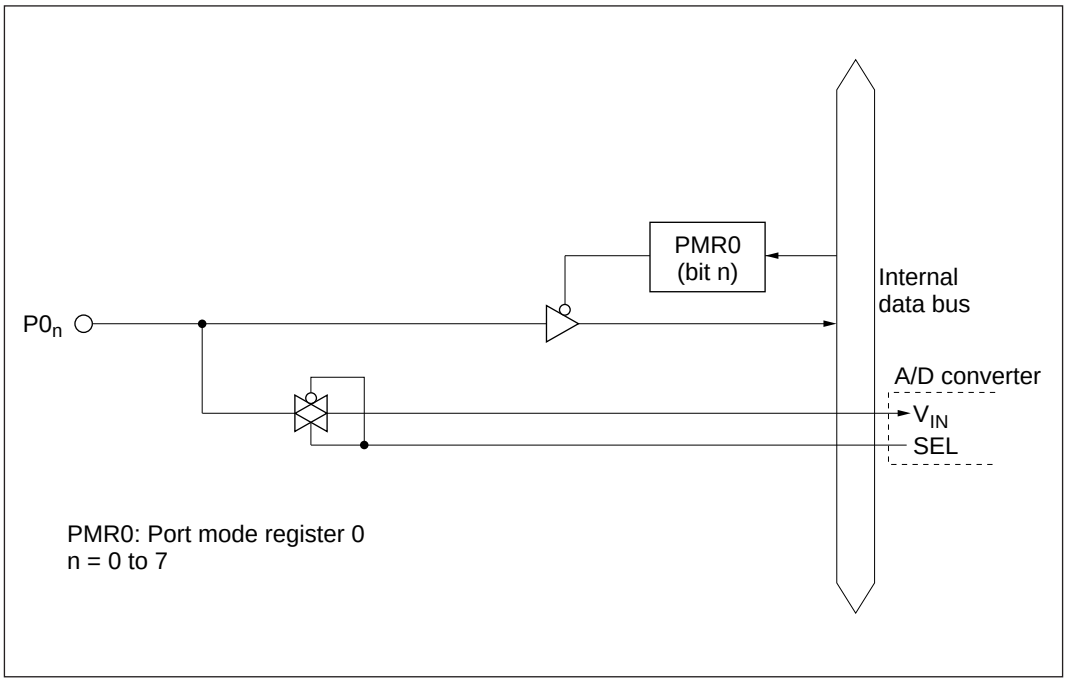


Figure C-1 Port 0 Block Diagram

C.2 Port 1 Block Diagram

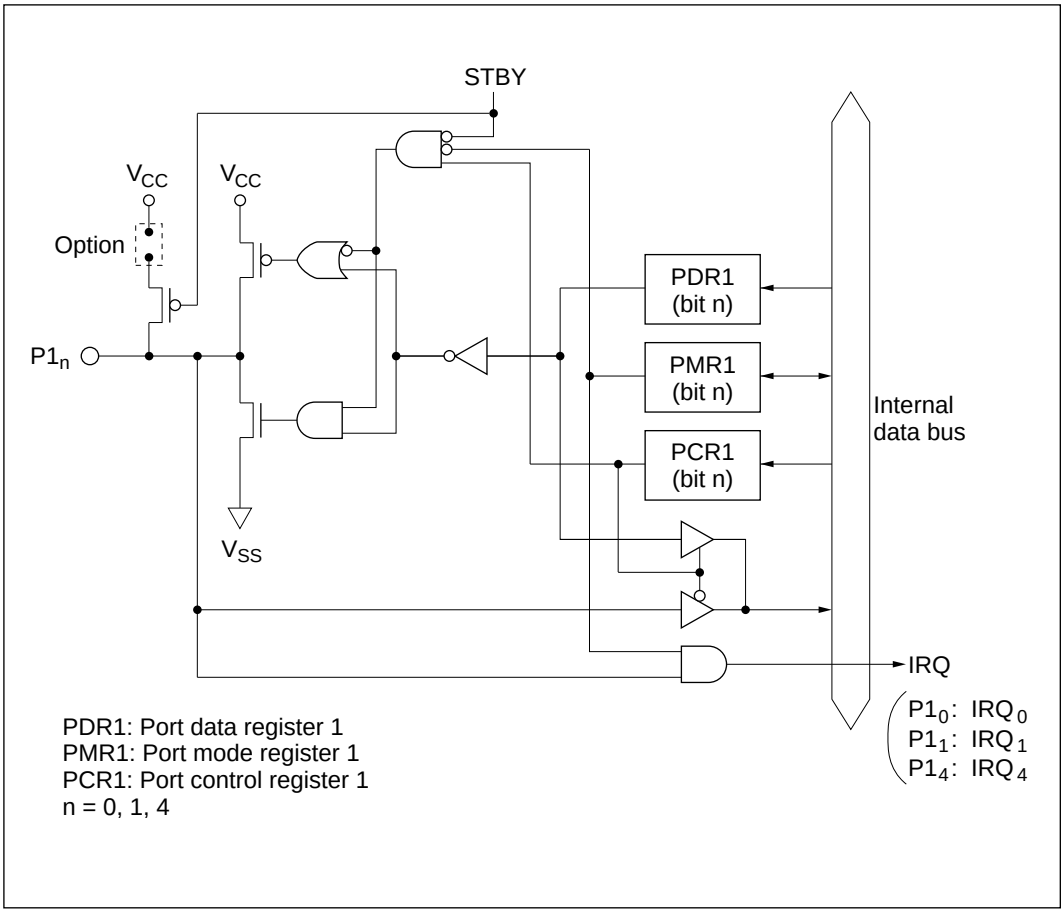


Figure C-2 (a) Port 1 Block Diagram (Pins $P1_0$, $P1_1$, and $P1_4$)

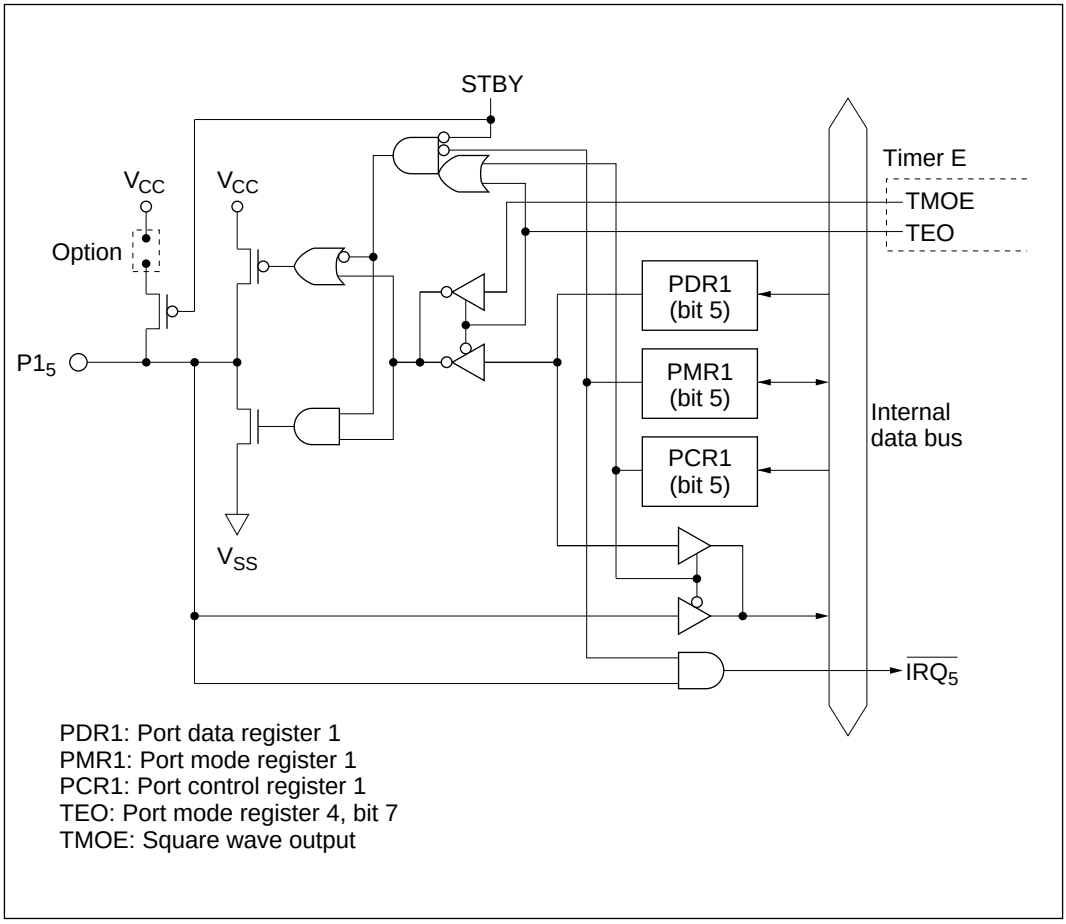


Figure C-2 (b) Port 1 Block Diagram (Pin $P1_5$)

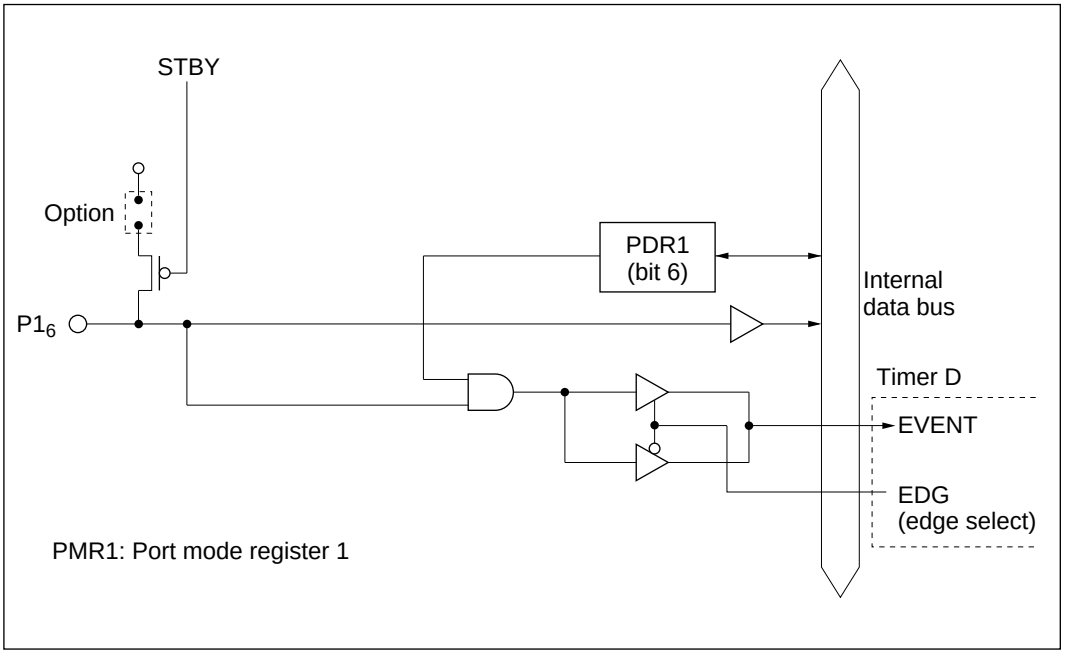


Figure C-2 (c) Port 1 Block Diagram (Pin P1$_6$)

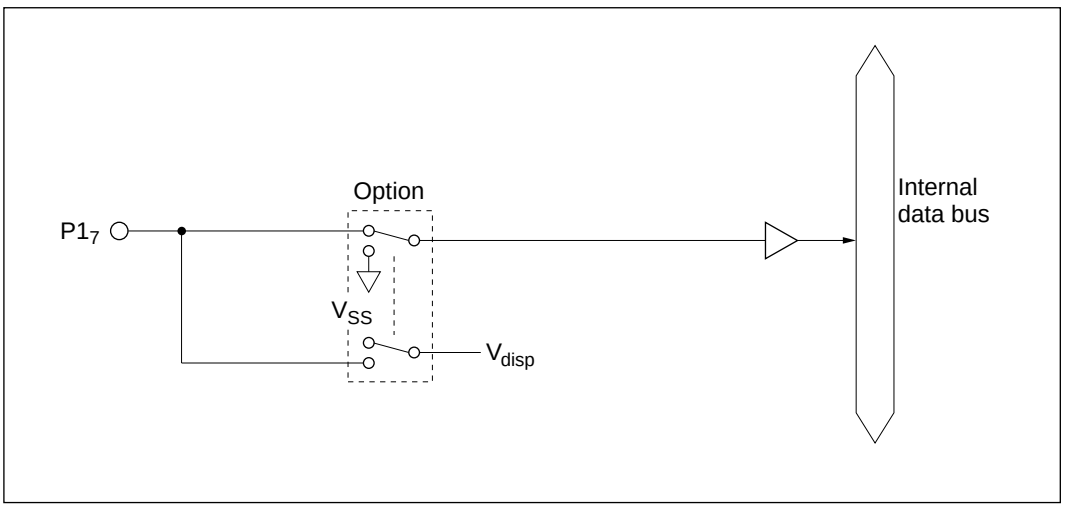


Figure C-2 (d) Port 1 Block Diagram (Pin P1$_7$)

C.3 Port 4 Block Diagram

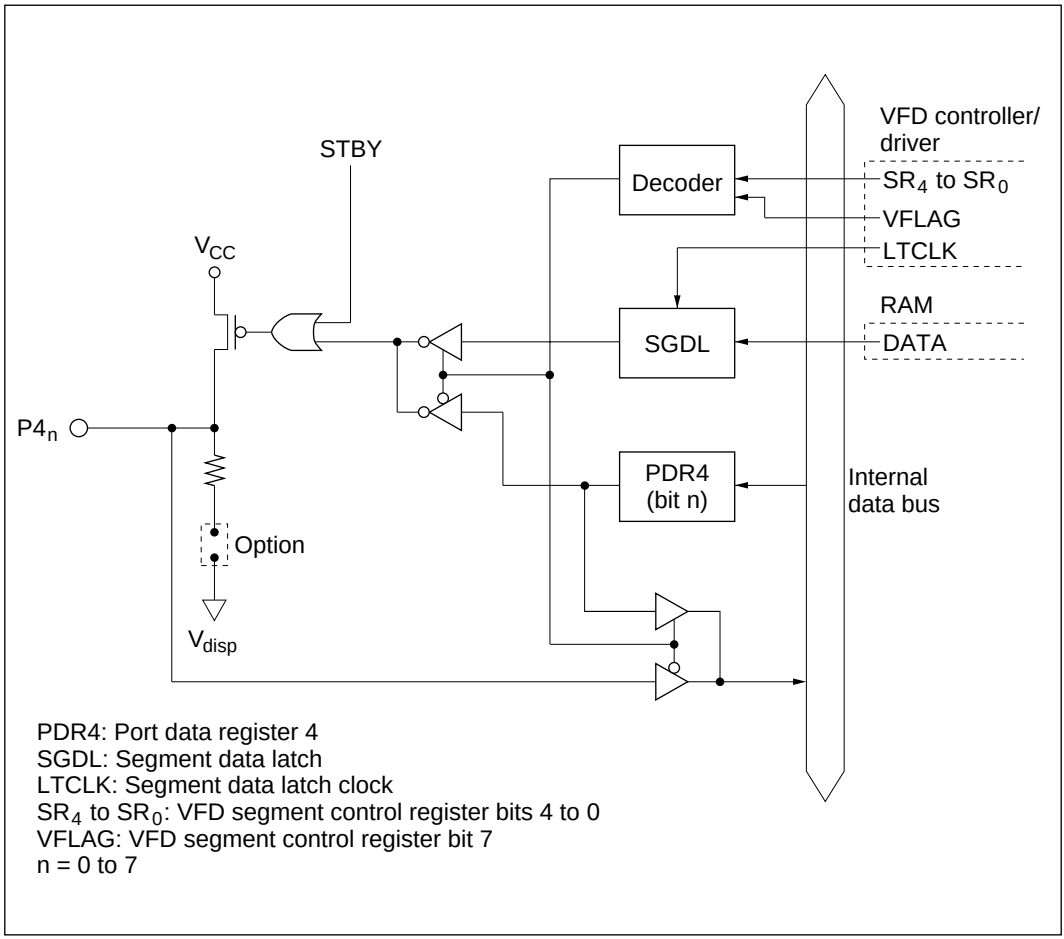


Figure C-3 Port 4 Block Diagram

C.4 Port 5 Block Diagram

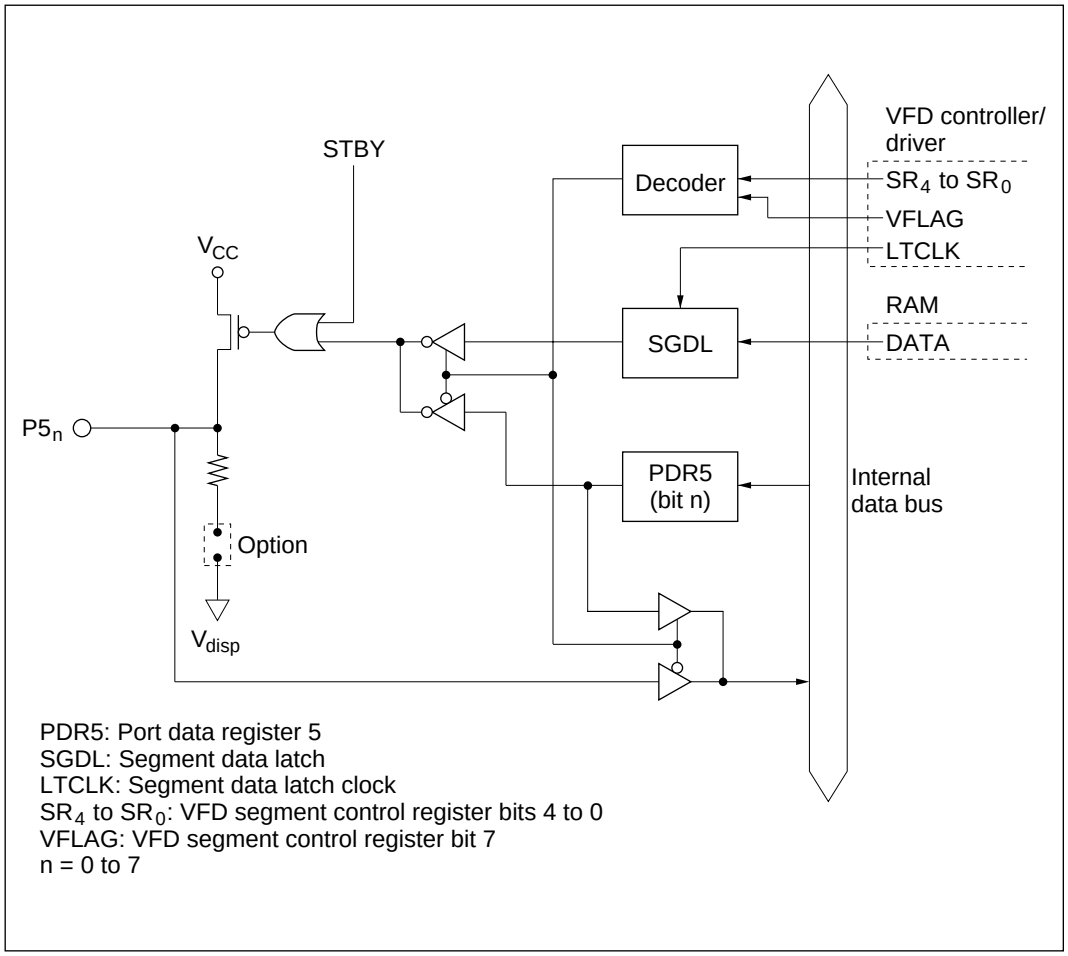
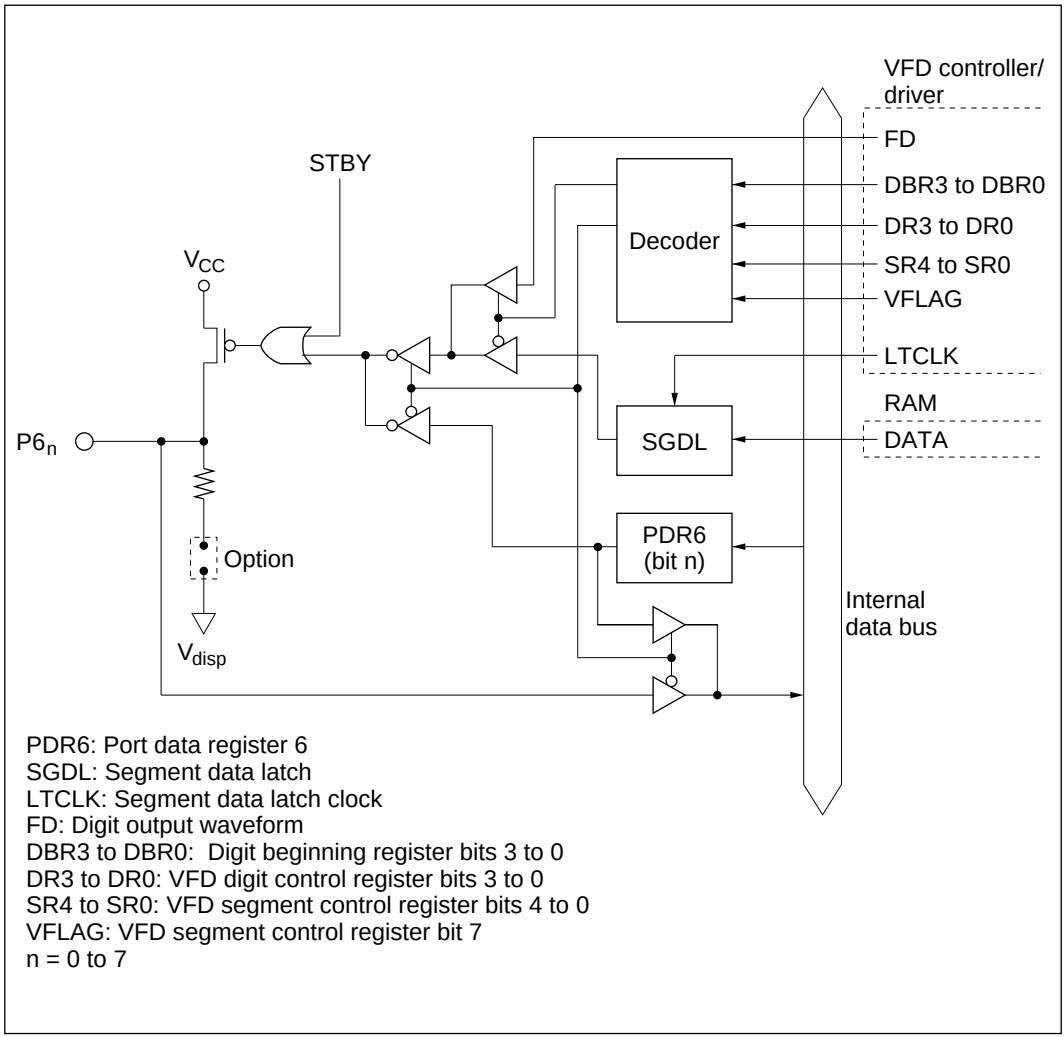


Figure C-4 Port 5 Block Diagram

C.5 Port 6 Block Diagram



PDR6: Port data register 6
SGDL: Segment data latch
LTCLK: Segment data latch clock
FD: Digit output waveform
DBR3 to DBR0: Digit beginning register bits 3 to 0
DR3 to DR0: VFD digit control register bits 3 to 0
SR4 to SR0: VFD segment control register bits 4 to 0
VFLAG: VFD segment control register bit 7
n = 0 to 7

Figure C-5 Port 6 Block Diagram

C.6 Port 7 Block Diagram

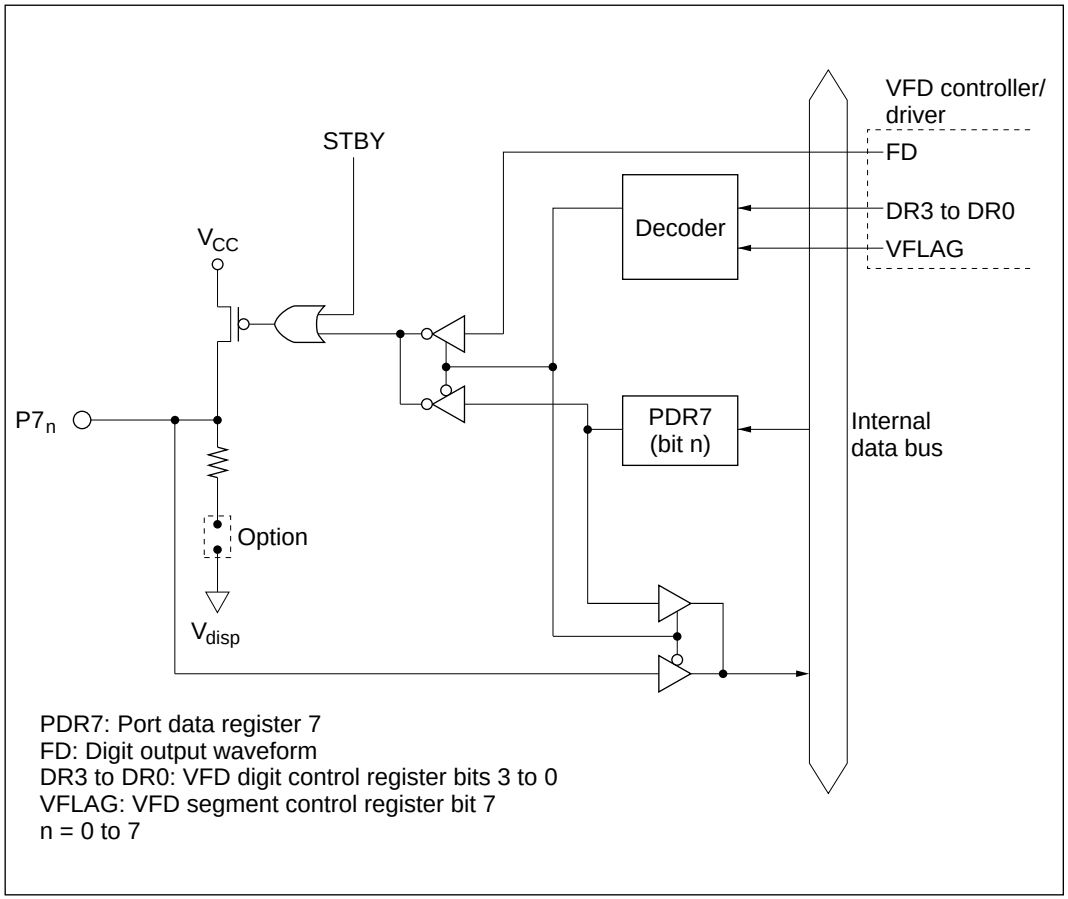


Figure C-6 Port 7 Block Diagram

C.7 Port 9 Block Diagram

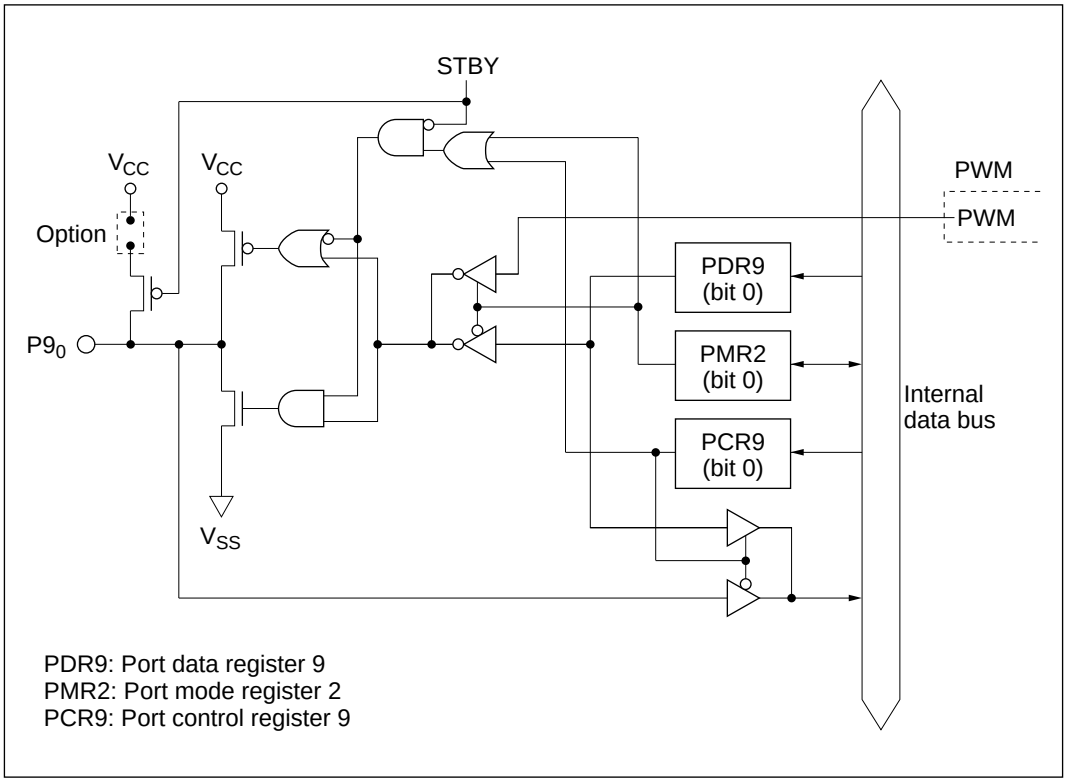


Figure C-7 (a) Port 9 Block Diagram (Pin $P9_0$)

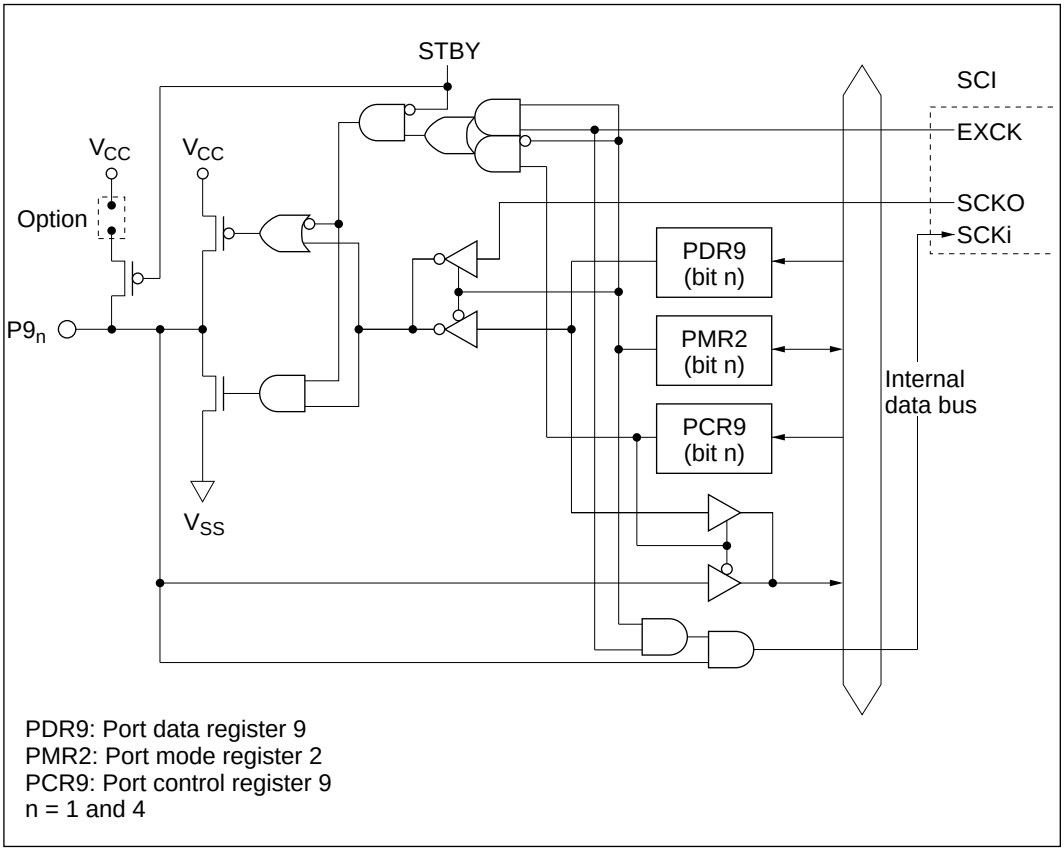


Figure C-7 (b) Port 9 Block Diagram (Pins $P9_1$ and $P9_4$)

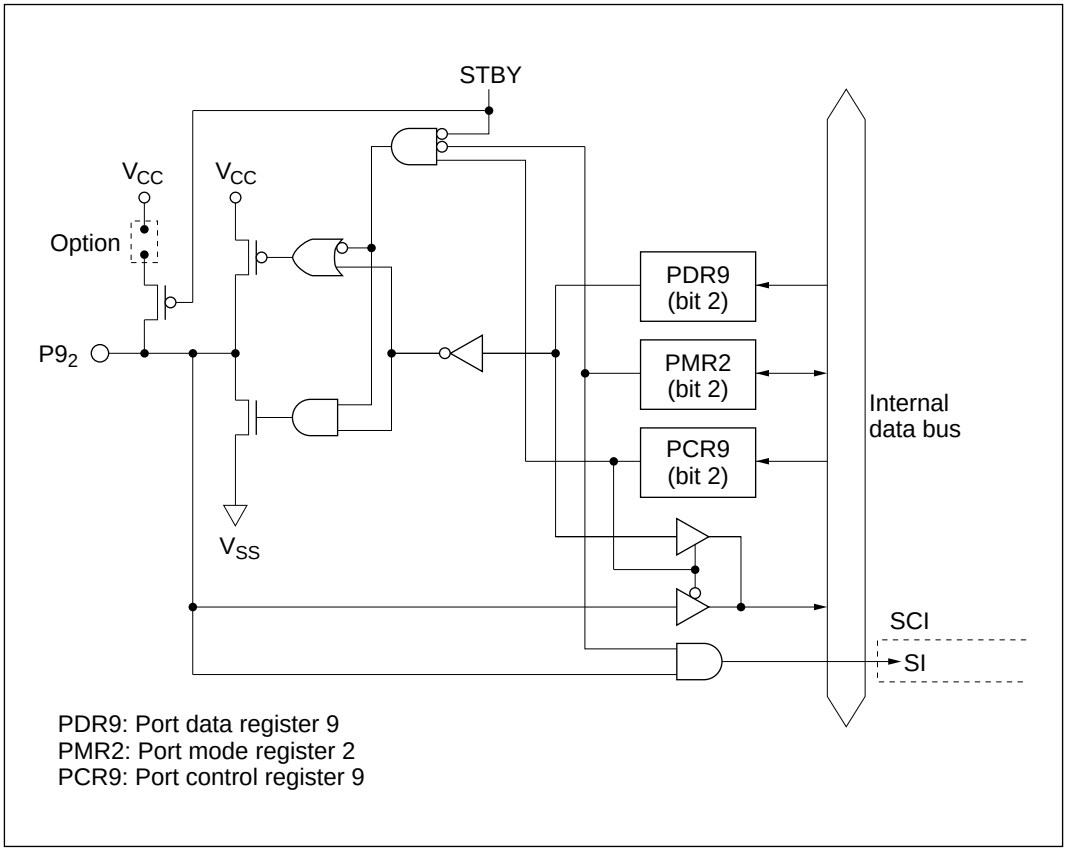


Figure C-7 (c) Port 9 Block Diagram (Pin $P9_2$)

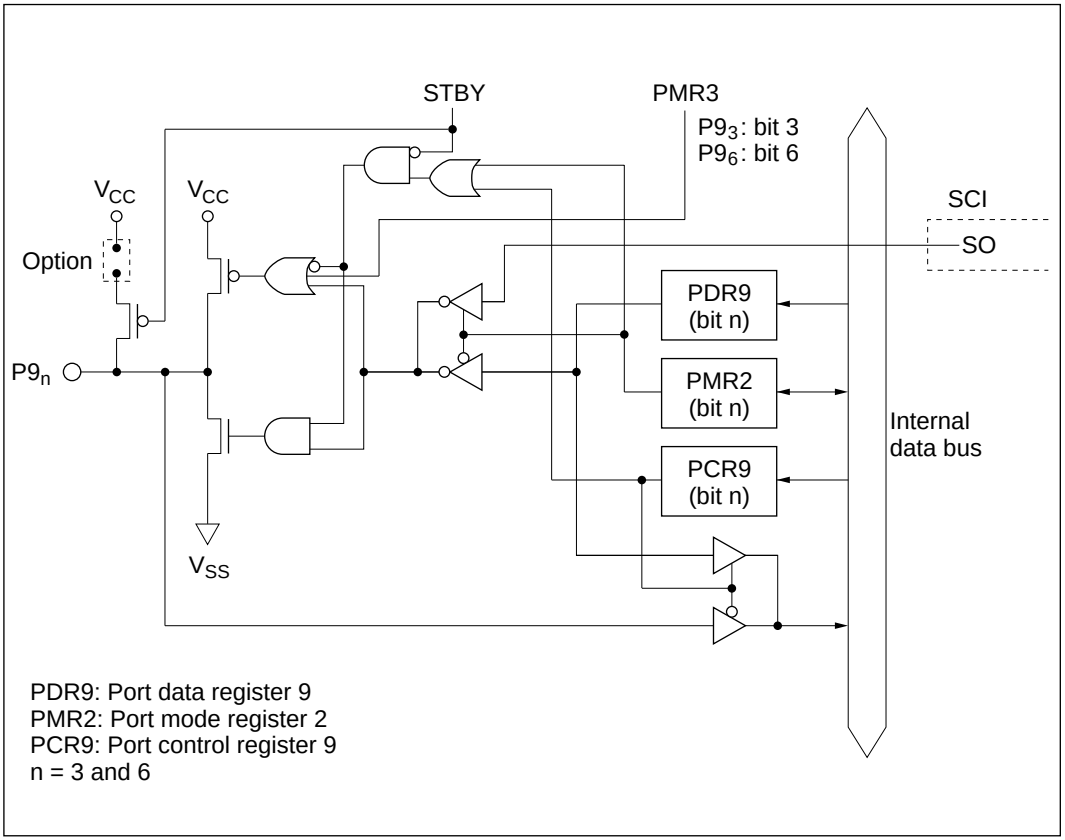


Figure C-7 (d) Port 9 Block Diagram (Pins $P9_3$ and $P9_6$)

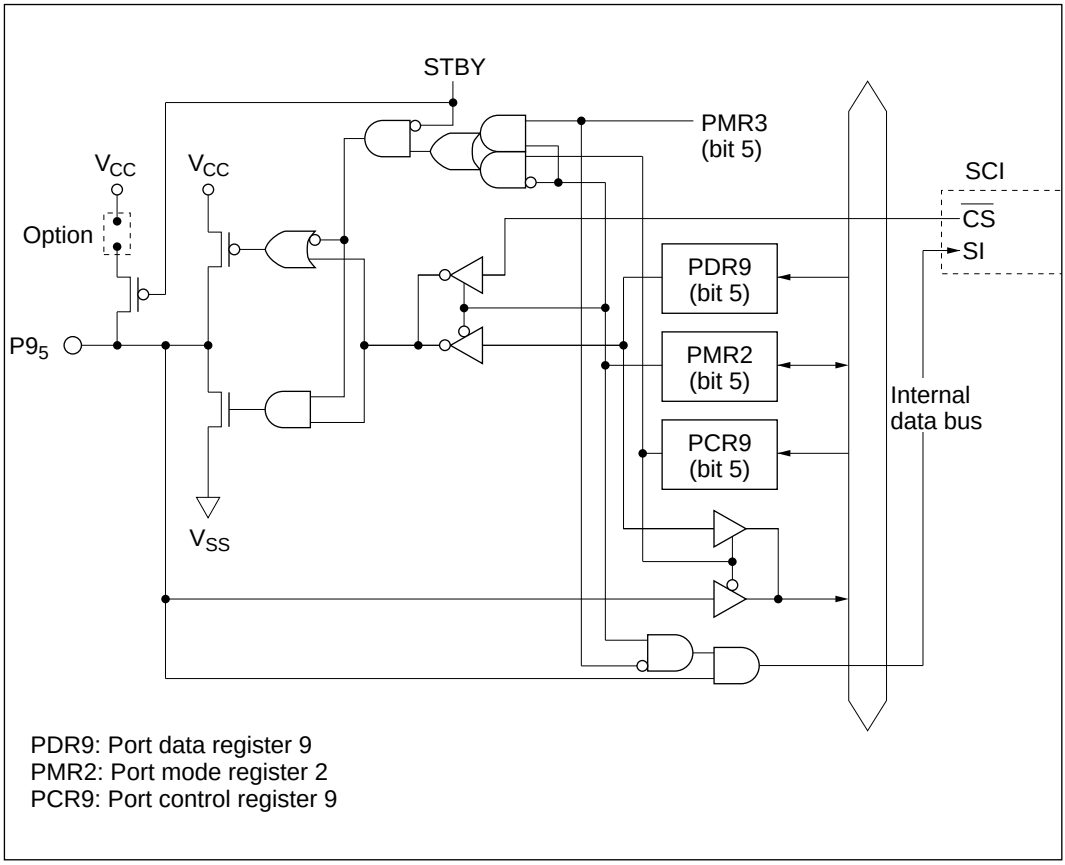


Figure C-7 (e) Port 9 Block Diagram (Pin $P9_5$)

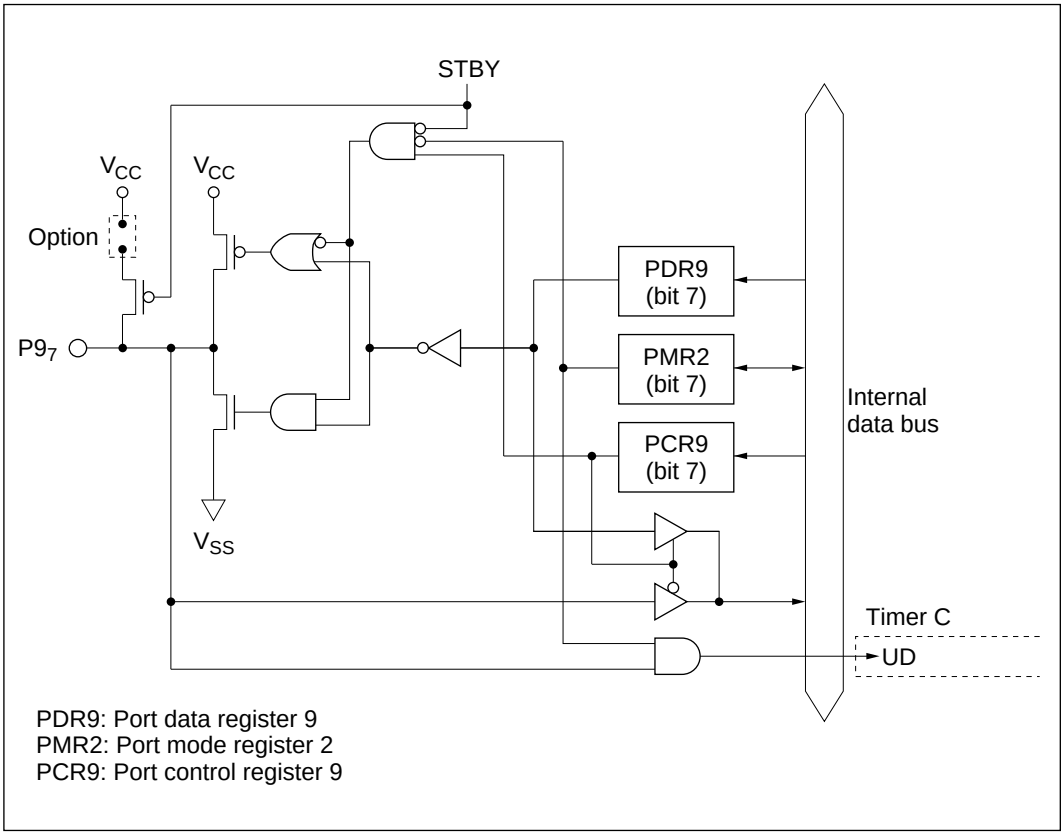


Figure C-7 (f) Port 9 Block Diagram (Pin $P9_7$)

Appendix D Port States in Each Processing State

Table D-1 Port States

		Mode				
Port Pins	**Reset**	**Sleep**	**Standby**	**Watch**	**Subactive**	**Active**
$P0_7$ to $P0_0$	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Standard input port
$P1_7$	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	High-voltage input port
$P1_6$	Hi-Z or pulled up	Hi-Z or pulled up	Hi-Z	Hi-Z	Hi-Z	Standard input port
$P1_5$, $P1_4$, $P1_1$, $P1_0$	Hi-Z or pulled up	prev. state	Hi-Z	Hi-Z	Hi-Z	Standard I/O port
$P4_7$ to $P4_0$	Hi-Z or pulled down	prev. state	Hi-Z or pulled down	Hi-Z or pulled down	Hi-Z or pulled down	High-voltage I/O port
$P5_7$ to $P5_0$	Hi-Z or pulled down	prev. state	Hi-Z or pulled down	Hi-Z or pulled down	Hi-Z or pulled down	High-voltage I/O port
$P6_7$ to $P6_0$	Hi-Z or pulled down	prev. state	Hi-Z or pulled down	Hi-Z or pulled down	Hi-Z or pulled down	High-voltage I/O port
$P7_7$ to $P7_0$	Hi-Z or pulled down	prev. state	Hi-Z or pulled down	Hi-Z or pulled down	Hi-Z or pulled down	High-voltage I/O port
$P9_7$ to $P9_0$	Hi-Z or pulled up	prev. state	Hi-Z	Hi-Z	Hi-Z	Standard I/O port

Notation:
Hi-Z: High-impedance state
Prev. state: Input pins are in high-impedance state. Output pins hold their previous output.
Hi-Z or pulled up: Standard ports for which the pull-up MOS mask option is chosen are pulled up; ports without the pull-up MOS option are in the high-impedance state.
Hi-Z or pulled down: High-voltage ports for which the pull-down MOS mask option is chosen are pulled down; ports without the pull-down MOS option are in the high-impedance state.

Notes:
1. When MOS pull-up is chosen as a mask option with standard ports, the pull-ups are always on in active mode and sleep mode, regardless of the port control register (PCR) and port data register (PDR) settings. The pull-ups are off in power-down modes other than sleep mode.
2. The input gates of pins selected for peripheral function input remain on even in power-down modes. Their input levels must be held fixed in order to avoid increased power dissipation.
3. The states indicated above for $P1_7$ apply when this pin is designated as a high-voltage input pin by mask option.

Appendix E List of Mask Options

HD6433712, HD6433713 and HD6433714

Please indicate the selected specifications by marking the appropriate box (with an × or √ mark). The shaded boxes cannot be selected.

Date of order	, 19
Company	
Address	
Name	
ROM code name	
Part no.	☐ HD6433712 ☐ HD6433713 ☐ HD6433714

(1) I/O Options

B: With MOS pull-up C: No MOS pull-up
D: No MOS pull-down E: With MOS pull-down

Pin	I/O		I/O option			
			B	C	D	E
$P1_0/\overline{IRQ_0}$	Standard pins	I/O				
$P1_1/\overline{IRQ_1}$		I/O				
$P1_4/\overline{IRQ_4}$		I/O				
$P1_5/\overline{IRQ_5}$/TMOE		I/O				
$P1_6/\overline{EVENT}$		I				
$P4_0/FS_{16}$	High-voltage pins	I/O				
$P4_1/FS_{17}$		I/O				
$P4_2/FS_{18}$		I/O				
$P4_3/FS_{19}$		I/O				
$P4_4/FS_{20}$		I/O				
$P4_5/FS_{21}$		I/O				
$P4_6/FS_{22}$		I/O				
$P4_7/FS_{23}$		I/O				
$P5_0/FS_{15}$		I/O				
$P5_1/FS_{14}$		I/O				
$P5_2/FS_{13}$		I/O				
$P5_3/FS_{12}$		I/O				
$P5_4/FS_{11}$		I/O				
$P5_5/FS_{10}$		I/O				
$P5_6/FS_9$		I/O				
$P5_7/FS_8$		I/O				
$P1_7/V_{disp}$		I	Fill in (2) below			

Pin	I/O		I/O option			
			B	C	D	E
$P6_0/FD_0/FS_7$	High-voltage pins	I/O				
$P6_1/FD_1/FS_6$		I/O				
$P6_2/FD_2/FS_5$		I/O				
$P6_3/FD_3/FS_4$		I/O				
$P6_4/FD_4/FS_3$		I/O				
$P6_5/FD_5/FS_2$		I/O				
$P6_6/FD_6/FS_1$		I/O				
$P6_7/FD_7/FS_0$		I/O				
$P7_0/FD_8$		I/O				
$P7_1/FD_9$		I/O				
$P7_2/FD_{10}$		I/O				
$P7_3/FD_{11}$		I/O				
$P7_4/FD_{12}$		I/O				
$P7_5/FD_{13}$		I/O				
$P7_6/FD_{14}$		I/O				
$P7_7/FD_{15}$		I/O				
$P9_0$/PWM	Standard pins	I/O				
$P9_1/SCK_1$		I/O				
$P9_2/SI_1$		I/O				
$P9_3/SO_1$		I/O				
$P9_4/SCK_2$		I/O				
$P9_5/SI_2/\overline{CS}$		I/O				
$P9_6/SO_2$		I/O				
$P9_7$/UD		I/O				

(2) $P1_7/V_{disp}$

☐ $P1_7$: No MOS pull-down (D)
☐ V_{disp}

Note: If E (MOS pull-down) is selected as an option for one or more high-voltage pins, V_{disp} must be selected for the $P1_7/V_{disp}$ pin.

(3) Package

☐ FP-64A
☐ DP-64S

(4) Oscillator at OSC_1 and OSC_2

☐ Crystal oscillator	f_{OSC} =	MHz
☐ Ceramic oscillator	f_{OSC} =	MHz
☐ External clock	f_{OSC} =	MHz

(5) Oscillator at X_1 and X_2

☐ Used	f_x = 32.768 kHz
☐ Not used	$X_1 = V_{CC}$

Notes: 1. The wide temperature range specification and I specification are special specifications. There is no J specification for these products. Please contact your local Hitachi representative for details.
2. ROM data submitted in an EPROM must be written starting from address H'0000 in accordance with the memory map of the particular microcontroller. For data outside the ROM area on the memory map use H'FF.

Appendix F Rise Time and Fall Time of High-Voltage Pins

With the mask ROM versions there is a choice of high-voltage pin output configurations. Either PMOS open-drain (D) or MOS pull-down (E) may be selected. (Only PMOS open-drain is available as the output configuration of high-voltage pins on ZTAT™ versions.)

The rise time t_r and fall time t_f of high-voltage pin output are as follows.

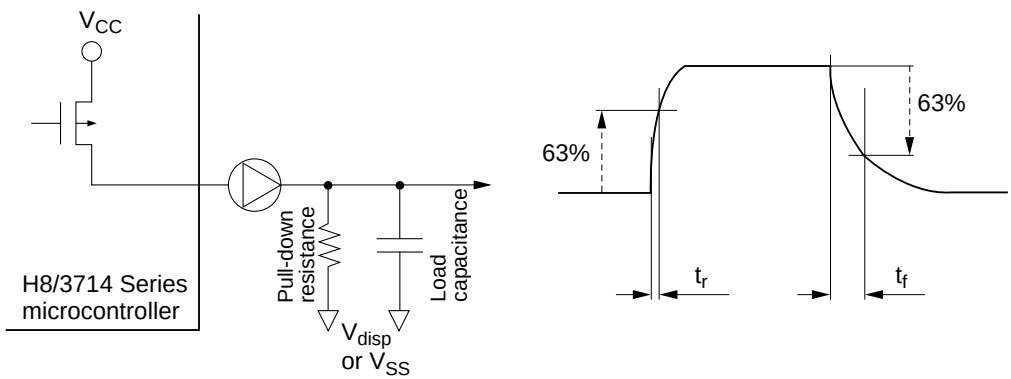
It is possible to estimate t_r and t_f from the time constant $\tau = C \cdot R$ (time up to 63% of rise or fall).

t_r: The time constant is determined by the PMOS on-resistance and load capacitance. The DC on-resistance is approximately 200 Ω (based on $V_{OH} = V_{CC} - 3$ V at $-I_{OH} = 15$ mA, 3/0.015 = 200). The AC on-resistance however, includes the non-saturation state when the PMOS transistor turns on (it is not a constant-current source), resulting in a longer time constant. Assuming a load capacitance of 30 pF at high-voltage pins, the minimum value is approximately 20 ns.

t_f: The time constant is determined by the pull-down resistance and load capacitance (including wiring capacitance, etc.). As an example, assuming a pull-down resistance of 5 kΩ and load capacitance of 30 pF, the following is derived.

$$t_f \geq 5 \times 10^3 \times 30 \times 10^{-12} = 150 \times 10^{-9} \text{ (150 ns)}$$

MOS pull-down resistance varies from 45 kΩ to 300 kΩ, so all due care must be taken in timing design.



Note: If pull-down resistance is made too small in an attempt to speed up the fall time, $-I_{OH}$ will increase, limiting the output high-level voltage (V_{OH}). Pull-down resistance must be set to a suitable value taking into consideration both operation speed and the output high level.

Appendix G Package Dimensions

Figures G-1 and G-2 show the external dimensions of the FP-64A and DP-64S packages, respectively, for the H8/3712, H8/3713 and H8/3714.

Unit: mm

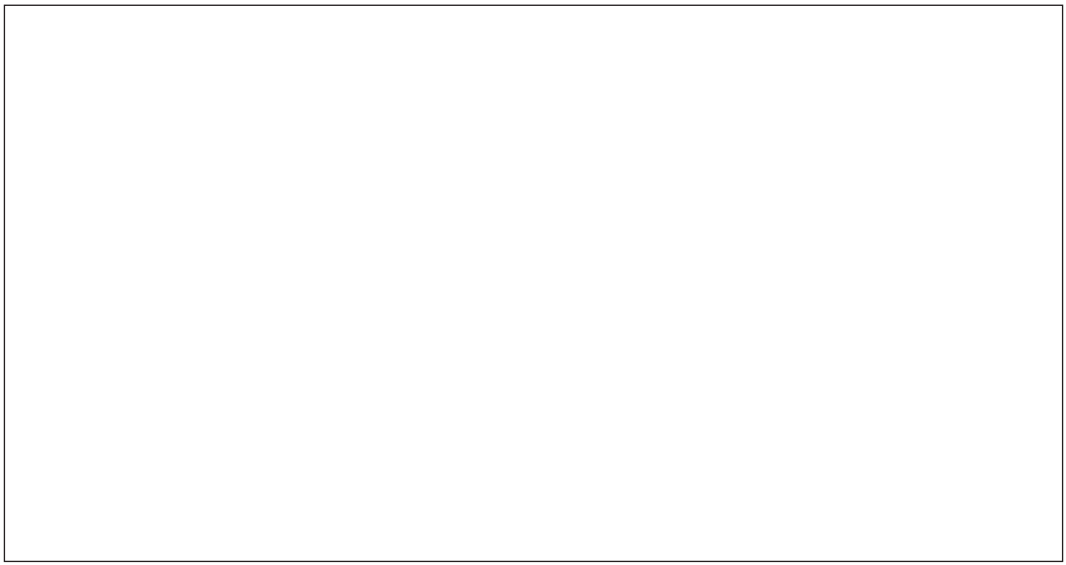


Figure G-1 External Dimensions (FP-64A)

Unit: mm

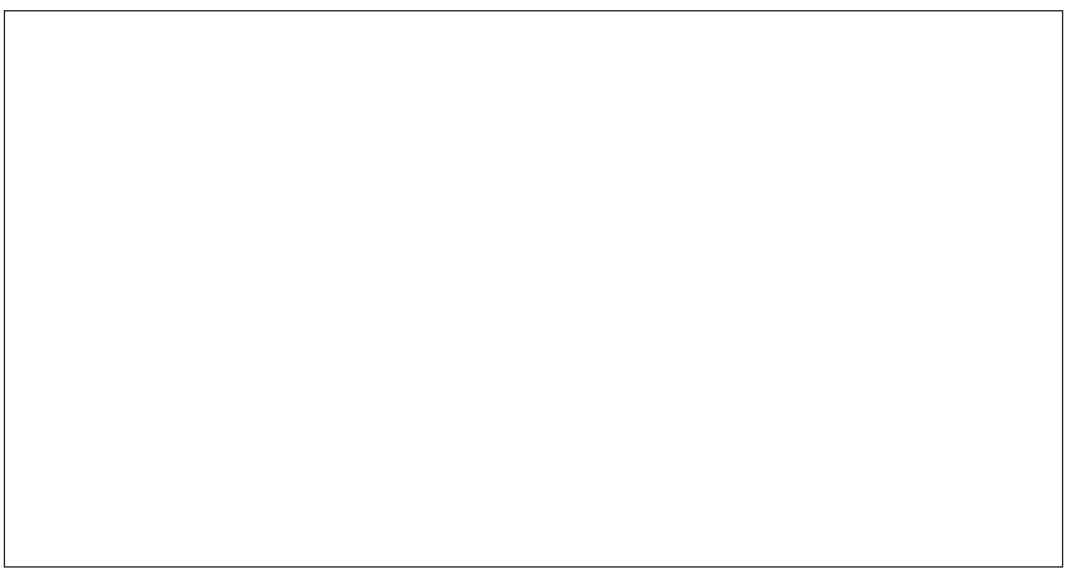


Figure G-2 External Dimensions (DP-64S)