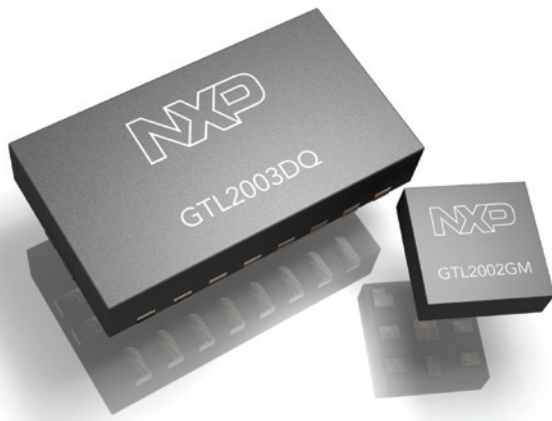




NXP bidirectional low-voltage translators GTL20xx

Low cost bidirectional voltage translation without directional control

Unlike level-shifting bus switches, which only translate between fixed voltages, these bidirectional low-voltage translators can translate any voltage between 1 and 5 V to any other voltage between 1 and 5 V. They also reduce ON-state resistance and minimize propagation delay.

Key features

- ▶ No directional control required for bidirectional voltage translations
- ▶ Low RON resistance ($6.5\ \Omega$) between input and output pins (Sn/Dn)
- ▶ Propagation delay: 1.5 ns (typ)
- ▶ Channel off-state capacitance: 7.5 pF
- ▶ Very low (5 μ A) standby current
- ▶ No power supply required – prevents latch-ups
- ▶ Very small QFN package options

Applications

- ▶ Uni- and bidirectional translation for any voltage between 1 and 5 V
- ▶ Bidirectional translation of low-voltage and legacy I²C-bus signals
- ▶ Shifting processor sideband I/O signals between GTL and LVTTTL/TTL levels

The NXP family of Gunning Transceiver Logic (GTL) bidirectional low-voltage translators includes the 22-bit GTL2000, the 2-bit GTL2002, the 8-bit GTL2003, and the 10-bit GTL2010.

Each delivers high-speed translation between different voltage levels with low ON-state resistance and minimal propagation delay.

They can translate any voltage between 1 and 5 V to any other voltage between 1 and 5 V as long as there is at least 1 V difference between the voltage levels, so they offer greater design flexibility than level-shifting bus switches, which only translate between fixed voltages.

Each GTL20xx device includes NMOS pass transistors (Sn and Dn pins) with a common gate (G_{REF} pin) and a reference transistor (S_{REF} and D_{REF} pins).

When one of the Sn or Dn ports is low, the clamp is in the ON-state and the Sn and Dn ports are linked through a low ON-resistance connection. Assuming the higher voltage is applied on the Dn port, when the Dn port is high, the voltage on the Sn port is limited to the voltage set by S_{REF} . When the Sn port is high, the Dn port is pulled to a higher voltage by a pull-up resistor.

This set-up enables seamless translation between user-selected voltages, without the need for directional control signals. All transistors have the same electrical characteristics so deviation from one output to another in voltage and propagation delay is kept to a minimum. The transistors also provide excellent ESD protection in case the low-voltage devices that are less resistant to ESD.

The translators can be used in any

