GTL1655

16-bit LVTTL-to-GTL/GTL+ bus transceiver with live insertion

Rev. 01 — 11 May 2004 **Product data**

1. Description

The GTL1655 is a 16-bit bus transceiver that incorporates HIGH-drive LOW-output-impedance (100 mA/12 Ω) with LVTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTL logic level translation.

The device is configured as two 8-bit transceivers that share a common clock and a master output enable pin, but also have individual latch timing and output enable signals. D-type flip-flops and D-type latches enable three modes of data transfer; Clocked, Latched, or Transparent. The GTL1655 provides the ideal interface between cards operating at LVTTL levels and backplanes using GTL/GTL+ signal levels. The combination of reduced output swing, reduced input threshold levels and configurable edge control provides the higher speed operation of GTL/GTL+ backplanes.

The GTL1655 can be used at GTL (V_{TT} = 1.2 V, V_{REF} = 0.8 V) or GTL+ (V_{TT} = 1.5 V, V_{REF} = 1.0 V) signalling levels. Port A and the control inputs are compliant with LVTTL signal levels and are 5 V tolerant. Port B is designed to operate at GTL or GTL+ signal levels, with V_{REF} providing the reference voltage input.

The latch enable pins (nLEAB and nLEBA), the output enable pins ($n\overline{OEAB}$, $n\overline{OEBA}$) and the clock pin (CP) are used to control the data flow through the two 8-bit transceivers (n = 1 or 2). When nLEAB is set HIGH, the device will operate in the transparent mode Port A to Port B. HIGH-to-LOW transitions of nLEAB will latch A data independently of CP HIGH or LOW (latched mode). LOW-to-HIGH transitions of CP will clock A data to the B port if nLEAB is LOW (clocked mode). Using the control pins nLEBA, $n\overline{OEBA}$ and CP in the same way, data flow from Port B to Port A can be controlled. The $\overline{OE}$ pin can be used to disable all of the I/O pins.

To optimize signal integrity, the GTL1655 features an adjustable edge rate control (V_{ERC}). By adjusting V_{ERC} between GND and V_{CC}, a designer can adjust the Port B edge rate to suit an application's load conditions.

The GTL1655 permits true live insertion capability by incorporating:

- BIAS V_{CC}, to pre-charge outputs and avoid disturbing active data during card insertion.
- I_{off} to disable current flow through powered-off I/Os.
- Power-up 3-state, which ensures outputs are high-impedance during power-up, thus preventing bus contention issues. Once V_{CC} is above 1.5 V, the power-up 3-state circuit relinquishes control of the outputs to the $\overline{OE}$ pin. To ensure the outputs remain 3-state, the $\overline{OE}$ pin should be tied to V_{CC} via a pull-up resistor.

2. Features

- Combination of D-type latches and D-type flip-flops for transceiver operation in clocked, latched or transparent mode
- Logic level translation between LVTTL and GTL/GTL+ signals
- HIGH-drive LOW-output-impedance (100 mA/12 Ω) on Port B
- Configurable rise and fall times on Port B
- Supports live insertion (I_{off}, Power-up 3-state, and BIAS V_{CC})
- Bus Hold on Port A inputs
- Over voltage tolerance on Port A
- Minimized switching noise through use of distributed V_{CC} and GND pins
- Available in TSSOP64 package
- Industrial temperature range (–40 °C to +85 °C)
- ESD protection
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - CDM EIA/JESD22-C101 exceeds 1000 V
- Latch-up EIA/JEDS78 exceeds 200 mA

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq$ 2.5 ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	propagation delay, nAn to nBn	V_{CC} = 3.3 V; V_{ERC} = GND; V_{TT} = 1.5 V; V_{REF} = 1 V	-	3.9	-	ns
		V_{CC} = 3.3 V; V_{ERC} = GND; V_{TT} = 1.5 V; V_{REF} = 1 V	-	4.4	-	ns
	propagation delay, nBn to nAn	V_{CC} = 3.3 V	-	2.6	-	ns
t_{PHL}	propagation delay, nAn to nBn	V_{CC} = 3.3 V; V_{ERC} = GND; V_{TT} = 1.5 V; V_{REF} = 1 V	-	3.1	-	ns
		V_{CC} = 3.3 V; V_{ERC} = GND; V_{TT} = 1.5 V; V_{REF} = 1 V	-	2.7	-	ns
	propagation delay, nBn to nAn	V_{CC} = 3.3 V	-	4.2	-	ns
C_i	input capacitance (control pins)	$V_i = V_{CC}$ or GND	-	3	-	pF
$C_{I/O}$	I/O capacitance, Port A	$V_i = V_{CC}$ or GND	-	7	-	pF
	I/O capacitance, Port B	$V_i = V_{CC}$ or GND	-	8	-	pF

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
GTL1655DGG	TSSOP64	plastic thin shrink small outline package; 64 leads; body width 6.1 mm	SOT646-1

Standard packing quantities and other packaging data are available at www.philipslogic.com/packaging.

4.1 Ordering options

Table 3: Part marking

Type number	Topside mark	Temperature range
GTL1655DGG	GTL1655DGG	T_{amb} = –40 °C to +85 °C

5. Pinning information

5.1 Pinning

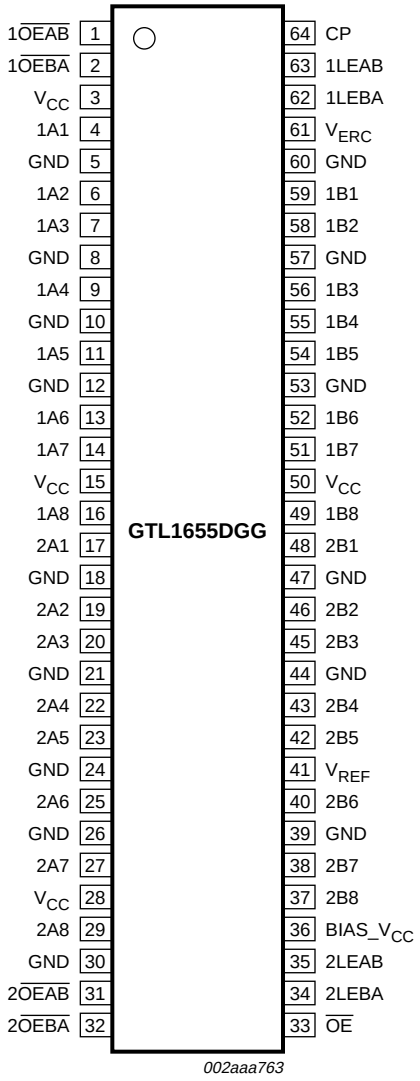


Fig 1. TSSOP64 pin configuration.

5.2 Pin description

Table 4: Pin description

Symbol	Pin	Description
$1\overline{OEAB}$	1	output enable 1A-to-1B (active-LOW)
$1\overline{OEBA}$	2	output enable 1B-to-1A (active-LOW)
V_{CC}	3, 15, 28, 50	DC supply voltage
1A1 to 1A8	4, 6, 7, 9, 11, 13, 14, 16	data inputs/outputs port 1A
GND	5, 8, 10, 12, 18, 21, 24, 26, 30, 39, 44, 47, 53, 57, 60	ground (0 V)
2A1 to 2A8	17, 19, 20, 22, 23, 25, 27, 29	data inputs/outputs port 2A
$2\overline{OEAB}$	31	output enable 2A-to-2B (active-LOW)
$2\overline{OEBA}$	32	output enable 2B-to-2A (active-LOW)
$\overline{OE}$	33	output enable, all I/O pins (active-LOW)
2LEBA	34	latch enable 2B-to-2A
2LEAB	35	latch enable 2A-to-2B
BIAS_V_{CC}	36	bias supply voltage
2B8 to 2B1	37, 38, 40, 42, 43, 45, 46, 48	data inputs/outputs port 2B
V_{REF}	41	reference voltage
1B8 to 1B1	49, 51, 52, 54, 55, 56, 58, 59	data inputs/outputs port 1B
V_{ERC}	61	edge-rate control voltage Port B
1LEBA	62	latch enable 2B-to-2A
1LEAB	63	latch enable 1A-to-1B
CP	64	clock input

6. Functional description

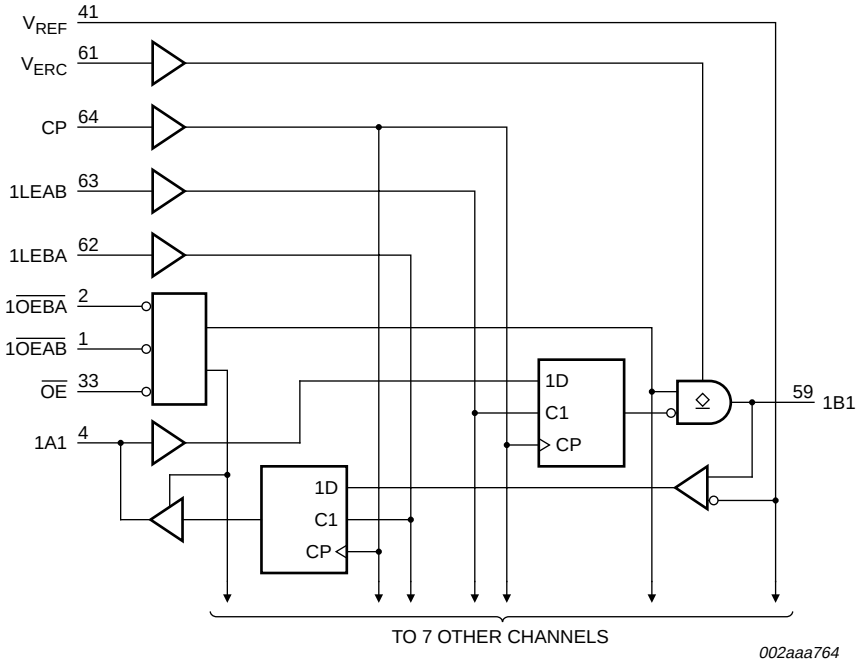


Fig 2. Logic diagram.

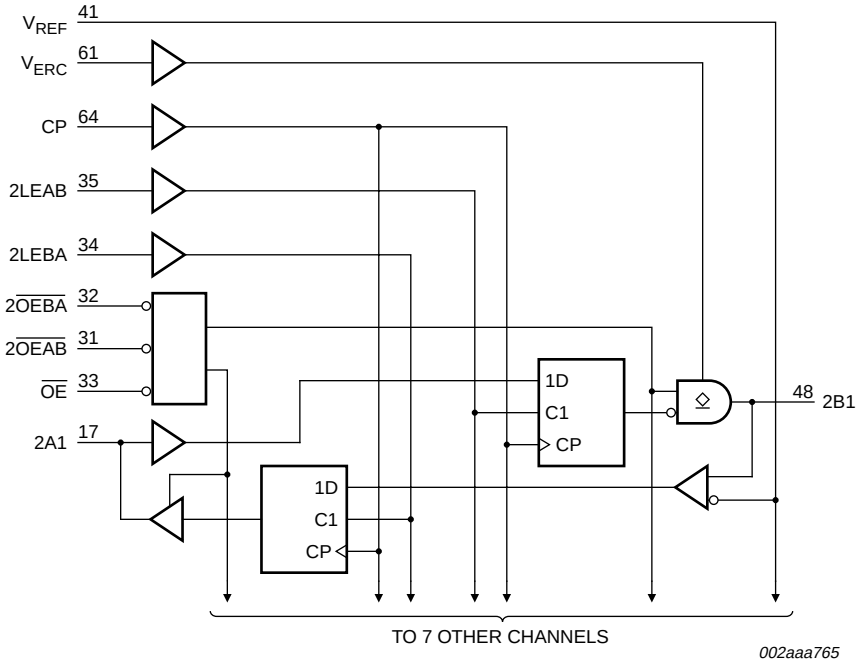


Fig 3. Logic diagram.

6.1 Function table

Table 5: Function table

See Table note [1].

Inputs				Output	Mode
$\overline{OEAB}$	LEAB	CP	Port A	Port B	
H	X	X	X	Z	isolation
L	H	X	L	L	transparent
L	H	X	H	H	transparent
L	L	↑	L	L	registered
L	L	↑	H	H	registered
L	L	H	X	B0[2]	previous state
L	L	L	X	B0[3]	previous state

Table 6: Output Enable function table

See Table note [1].

Inputs			Outputs	
$\overline{OE}$	$\overline{OEAB}$	$\overline{OEBA}$	Port A	Port B
L	L	L	active	active
L	L	H	Z	active
L	H	L	active	Z
L	H	H	Z	Z
H	X	X	Z	Z

Table 7: Port B edge-rate control (V_{ERC}) function table

See Table note [1].

Input V_{ERC}		Output port B edge-rate
Logic level	Nominal voltage	
H	V_{CC}	slow
L	GND	fast

[1] A-to-B data flow is shown. B-to-A is similar, but uses $\overline{OEBA}$, LEBA, and CP. It is not recommended to set $\overline{OEAB}$ and $\overline{OEBA}$ LOW at the same time.

X — don't care

H — HIGH voltage level

L — LOW voltage level

Z — high-impedance OFF-state

↑ — LOW-to-HIGH transition

[2] Output level before the indicated steady-state input conditions were established, provided that CP was HIGH before LEAB went LOW.

[3] Output level before the indicated steady-state input conditions were established.

7. Limiting values

Table 8: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). See Table note [1] and Table note [2]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	DC supply voltage			–0.5	+4.6	V
BIAS V_{CC}	BIAS supply voltage			–0.5	+4.6	V
I_{IK}	input clamping diode current	$V_i < 0$ V		-	–50	mA
V_i	DC input voltage	port A	[3]	–0.5	+7.0	V
		port B; V_{ERC}, V_{REF}	[3]	–0.5	+4.6	V
V_o	DC output voltage	output in HIGH or power-OFF state; port A		–0.5	+7.0	V
		output in HIGH or power-OFF state; port B		–0.5	+4.6	V
$I_{OL(d)}$	DC LOW-level diode output current	port A		-	48	mA
		port B		-	200	mA
$I_{OH(d)}$	DC HIGH-level diode output current	port A		-	48	mA
T_{stg}	storage temperature			–65	+150	°C

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under Section 8 “Recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[3] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

8. Recommended operating conditions

Table 9: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
BIAS V_{CC}	DC supply voltage		3.0	3.6	V
V_{TT}	termination voltage	GTL	1.14	1.26	V
		GTL+	1.35	1.65	V
V_{REF}	GTL reference voltage	GTL	0.74	0.87	V
		GTL+	0.87	1.10	V
V_I	input voltage	port B	0	V_{TT}	V
		except port B	0	5.5	V
V_{IH}	HIGH-level input voltage	port B	V_{REF} + 50 mV	-	V
		except port B	2.0	-	V
		V_{ERC}	V_{CC} – 0.6	-	V
V_{IL}	LOW-level input voltage	port B	-	V_{REF} – 50 mV	V
		except port B	-	0.8	V
		V_{ERC}	-	0.6	V
$\|I_{IK}\|$	input clamp current		-	18	mA
I_{OH}	HIGH-level output current	port A	-	–24	mA
I_{OL}	LOW-level output current	port A	-	24	mA
		port B	-	100	mA
$\Delta t/\Delta V_{CC}$	power-up ramp rate		200	-	µs/V
T_{amb}	operating ambient temperature		–40	85	°C

9. Static characteristics

Table 10: DC characteristics

T_{amb} = −40 °C to +85 °C; values otherwise stated V_{REF} = 1 V; V_{TT} = 1.5 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IK}	input clamp voltage	V_{CC} = 3.0 V; I_{IK} = 19 mA		-	-	−1.2	V
V_{OH}	HIGH-level output voltage	port A	V_{CC} = 3.0 V to 3.6 V; I_{OH} = −100 µA	V_{CC} − 0.2	-	-	V
			V_{CC} = 3.0 V; I_{OH} = −12 mA	2.4	-	-	V
			V_{CC} = 3.0 V; I_{OH} = −24 mA	2.2	-	-	V
V_{OL}	LOW-level output voltage	port A	V_{CC} = 3.0 to 3.6 V; I_{OL} = 100 µA	-	-	0.2	V
			V_{CC} = 3.0 V; I_{OL} = 12 mA	-	-	0.4	V
			V_{CC} = 3.0 V; I_{OL} = 24 mA	-	-	0.55	V
		port B	V_{CC} = 3.0 V; I_{OL} = 40 mA	-	-	0.2	V
			V_{CC} = 3.0 V; I_{OL} = 80 mA	-	-	0.4	V
			V_{CC} = 3.0 V; I_{OL} = 100 mA	-	-	0.5	V
I_I	input leakage current	control pins	V_{CC} = 3.6 V; V_I = V_{CC} or GND	-	-	± 10	µA
		port B	V_{CC} = 3.6 V; V_I = V_{TT} or GND	-	-	± 10	µA
I_{off}	output OFF current	port A + control pin	V_{CC} = 0 V; V_o = 0 V to 3.6 V	-	-	± 100	µA
		port B	V_{CC} = 0 V; V_o = 0 V to 1.5 V	-	-	± 300	µA
I_{HOLD}	bus hold current, A outputs	port A	V_{CC} = 3.0 V; V_I = 0.8 V	75	-	-	µA
			V_{CC} = 3.0 V; V_I = 2.0 V	−75	-	-	µA
	overdrive current	port A	V_{CC} = 3.6 V; V_I = 0 V to V_{CC} [2]	-	-	± 500	µA
I_{OZH}	HIGH OFF-state output current	port B	V_{CC} = 3.6 V; V_o = 1.5 V	-	-	10	µA
I_{OZL}	LOW OFF-state output current	port B	V_{CC} = 3.6 V; V_o = 0.4 V	-	-	−10	µA
I_{OZ}	OFF-state output current	port A	V_{CC} = 3.6 V; V_o = V_{CC} or GND [3]	-	-	10	µA
I_{OZPU}	power-up 3-state output current	V_{CC} = 0 to 3.6 V; V_o = 0.5 V to 3 V; $\overline{OE}$ = LOW		-	-	± 50	µA
I_{OZPD}	power-down 3-state output current	V_{CC} = 3.6 to 0 V; V_o = 0.5 V to 3 V; $\overline{OE}$ = LOW		-	-	± 50	µA

Table 10: DC characteristics…*continued*

T_{amb} = −40 °C to +85 °C; values otherwise stated V_{REF} = 1 V; V_{TT} = 1.5 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{CC}	quiescent supply current	outputs HIGH	V_{CC} = 3.6 V; V_i = V_{CC} or GND; I_o = 0 mA	-	-	45	mA
		outputs LOW	V_{CC} = 3.6 V; V_i = V_{CC} or GND; I_o = 0 mA	-	-	45	mA
		disabled	V_{CC} = 3.6 V; V_i = V_{CC} or GND; I_o = 0 mA	-	-	45	mA
ΔI_{CC}	additional quiescent supply current per input pin; except port B	V_{CC} = 3.6 V; one input at V_{CC} − 0.6 V; port A or control inputs at V_{CC} or GN D [4]		-	0.1	-	mA
C_i	input capacitance	control pins	V_{CC} = 3.6 V; V_i = V_{CC} or 0	-	3	5	pF
C_{IO}	I/O capacitance	port A	V_{CC} = 3.6 V; V_i = V_{CC} or 0	-	7	8	pF
		port B	V_{CC} = 3.6 V; V_i = V_{CC} or 0	-	8	10	pF

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[3] For I/O ports, this parameter I_{OZ} includes the input leakage current.

[4] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Table 11: Live insertion characteristics

T_{amb} = −40 °C to +85 °C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CC} (BIAS V_{CC})	supply current	V_{CC} = 0 V to 3.0 V; V (port B) = 0 to 1.2 V; V_i (BIAS V_{CC}) = 3.0 V to 3.6 V		-	-	5	mA
		V_{CC} = 3.0 V to 3.6 V; V (port B) = 0 to 1.2 V; V_i (BIAS V_{CC}) = 3.0 V to 3.6 V		-	-	10	µA
V_o	output voltage	port B	V_{CC} = 0 V; V_i (BIAS V_{CC}) = 3.3 V	1	-	1.2	V
I_o	output current	port B	V_{CC} = 0 V; V (port B) = 0.4 V; V_i (BIAS V_{CC}) = 3 V to 3.6 V	−1	-	-	µA
			V_{CC} = 0 V to 3.6 V; $\overline{OE}$ = 3.3 V; V (port B) = 0 V to 1.5 V	-	-	300	µA
			V_{CC} = 0 V to 1.5 V; $\overline{OE}$ = 0 V to 3.3 V; V (port B) = 0 V to 1.5 V	-	-	300	µA

10. Dynamic characteristics

Table 12: Timing requirements over recommended supply voltage

V_{TT} = 1.2 V; V_{REF} = 0.8 V and V_{ERC} = V_{CC} or GND for GTL (unless otherwise noted; see Figures 15 and 16).
T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_W	pulse duration	CP HIGH or LOW; see Figures 4 and 5	3.0	-	-	ns
		LE HIGH; see Figures 6 and 7	3.0	-	-	ns
t_{su}	set-up time	data before CP↑; see Figures 4 and 5	2.7	-	-	ns
		data before LE↓; see Figures 6 and 7	2.8	-	-	ns
t_h	hold time	data after CP↑; see Figures 4 and 5	0.4	-	-	ns
		data after LE↓; see Figures 6 and 7	1.2	-	-	ns

Table 13: Port A to Port B switching

V_{TT} = 1.2 V; V_{REF} = 0.8 V and V_{ERC} = V_{CC} or GND for GTL (see Figure 16).
T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PLH}	A to B	$\overline{OEAB}$ = $\overline{OE}$ = 0 V; LEAB = 3 V	V_{ERC} = V_{CC}; see Figure 10	3.1	5.3	6.2	ns
t_{PHL}				2.2	3.8	6.2	ns
t_{PLH}	CP to B	$\overline{OEAB}$ = $\overline{OE}$ = 0 V; LEAB = 0 V	V_{ERC} = V_{CC}; see Figure 4	3.4	5.9	7.2	ns
t_{PHL}				2.4	4.1	6.0	ns
t_{PLH}	LEAB to B	$\overline{OEAB}$ = $\overline{OE}$ = 0 V; CP = 0 or 3 V	V_{ERC} = V_{CC}; see Figure 8	3.3	5.7	7.0	ns
t_{PHL}				2.6	4.6	6.8	ns
t_{PLH}	$\overline{OEAB}$ or $\overline{OE}$ to B	LEAB = 3.0 V; Port A = 0 V	V_{ERC} = V_{CC}; see Figure 12	2.7	5.3	6.5	ns
t_{PHL}				2.5	3.9	6.4	ns
t_{PLH}	A to B	$\overline{OEAB}$ = $\overline{OE}$ = 0 V; LEAB = 3 V	V_{ERC} = GND; see Figure 10	2.3	4.4	5.3	ns
t_{PHL}				1.7	2.7	4.4	ns
t_{PLH}	CP to B	$\overline{OEAB}$ = $\overline{OE}$ = 0 V; LEAB = 0 V	V_{ERC} = GND; see Figure 4	2.7	5.2	6.1	ns
t_{PHL}				1.8	3.7	5.3	ns
t_{PLH}	LEAB to B	$\overline{OEAB}$ = $\overline{OE}$ = 0 V; CP = 0 or 3 V	V_{ERC} = GND; see Figure 8	2.5	4.8	6.5	ns
t_{PHL}				2.0	3.6	5.3	ns
t_{PLH}	$\overline{OEAB}$ or $\overline{OE}$ to B	LEAB = 3.0 V; Port A = 0 V	V_{ERC} = GND; see Figure 12	2.0	4.8	6.2	ns
t_{PHL}				2.0	3.1	4.9	ns
$\Delta V/\Delta t$	output slew rate	0.6 V to 1.0 V	V_{ERC} = V_{CC}	-	-	1	V/ns
			V_{ERC} = GND	-	-	1	V/ns
$t_{sk(o)}$	output edge skew	measured at V_{REF}		-	-	1	ns

Table 14: Port B to Port A switching

V_{TT} = 1.2 V; V_{REF} = 0.8 V for GTL (see Figure 15).
T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{max}	maximum frequency			160	-	-	MHz
t_{PLH}	B to A	$\overline{OEBA}$ = $\overline{OE}$ = 0 V; LEBA = 3 V	see Figure 11	1.8	2.6	4.9	ns
t_{PHL}				2.3	4.2	5.3	ns
t_{PLH}	CP to A	$\overline{OEBA}$ = $\overline{OE}$ = 0 V; LEBA = 0 V	see Figure 5	1.5	3.1	4.4	ns
t_{PHL}				1.5	3.7	4.6	ns
t_{PLH}	LEBA to A	$\overline{OEBA}$ = $\overline{OE}$ = 0 V	see Figure 9	1.3	2.7	4.0	ns
t_{PHL}				1.4	3.1	3.9	ns
t_{PZL}	$\overline{OEBA}$ or $\overline{OE}$ to A	LEBA = 3.0 V; Port B = 0 V	see Figure 13	1.3	3.1	5.1	ns
t_{PLZ}				1.7	2.8	6.1	ns
t_{PZH}		LEBA = 3 V; Port B = V_{TT}	see Figure 14	1.3	3.3	5.1	ns
t_{PHZ}				1.7	3.3	6.1	ns
$t_{sk(o)}$	output edge skew	measured at 1.5 V		-	-	1	ns

Table 15: Timing requirements over recommended supply voltage

V_{TT} = 1.5 V; V_{REF} = 1 V and V_{ERC} = V_{CC} or GND for GTL+ (unless otherwise noted).
T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_W	pulse duration	CP HIGH or LOW; see Figures 4 and 5	3.0	-	-	ns
		LE HIGH; see Figures 6 and 7	3.0	-	-	ns
t_{su}	set-up time	data before CP↑; see Figures 4 and 5	2.7	-	-	ns
		data before LE↓; see Figures 6 and 7	2.8	-	-	ns
t_h	hold time	data after CP↑; see Figures 4 and 5	0.4	-	-	ns
		data after LE↓; see Figures 6 and 7	1.2	-	-	ns

Table 16: Port A to Port B switching

V_{TT} = 1.5 V; V_{REF} = 1 V and V_{ERC} = V_{CC} or GND for GTL+ (see Figures 15 and 16).
T_{amb} = −40 °C to +85 °C.

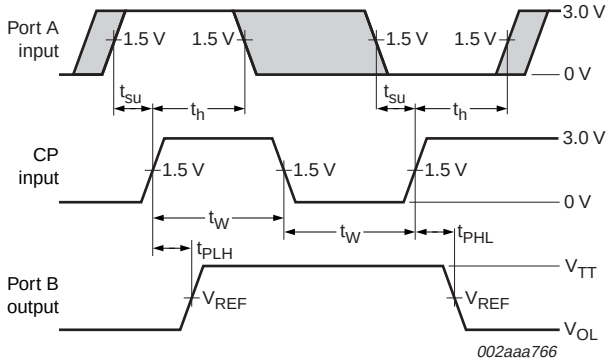
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PLH}	A to B	$\overline{OEAB}$ = $\overline{OE}$ = 0 V; LEAB = 3 V	V_{ERC} = V_{CC}; see Figure 10	3.0	4.7	6.1	ns
t_{PHL}				2.3	4.4	6.5	ns
t_{PLH}	CP to B	$\overline{OEAB}$ = $\overline{OE}$ = 0 V; LEAB = 0 V	V_{ERC} = V_{CC}; see Figure 4	3.3	5.3	7.0	ns
t_{PHL}				2.7	4.7	6.2	ns
t_{PLH}	LEAB to B	$\overline{OEAB}$ = $\overline{OE}$ = 0 V; CP = 0 or 3 V	V_{ERC} = V_{CC}; see Figure 8	3.2	5.2	6.8	ns
t_{PHL}				2.8	5.2	7.1	ns
t_{PLH}	$\overline{OEAB}$ or $\overline{OE}$ to B	LEAB = 3.0 V; Port A = 0 V	V_{ERC} = V_{CC}; see Figure 12	3.2	4.8	6.5	ns
t_{PHL}				2.6	4.6	6.6	ns
t_{PLH}	A to B	$\overline{OEAB}$ = $\overline{OE}$ = 0 V; LEAB = 3 V	V_{ERC} = GND; see Figure 10	2.3	3.9	5.2	ns
t_{PHL}				1.7	3.1	4.5	ns
t_{PLH}	CP to B	$\overline{OEAB}$ = $\overline{OE}$ = 0 V; LEAB = 0 V	V_{ERC} = GND; see Figure 4	2.5	4.8	6.0	ns
t_{PHL}				1.9	4.1	5.4	ns
t_{PLH}	LEAB to B	$\overline{OEAB}$ = $\overline{OE}$ = 0 V; CP = 0 or 3 V	V_{ERC} = GND; see Figure 8	2.5	4.3	6.5	ns
t_{PHL}				2.1	4.0	5.4	ns
t_{PLH}	$\overline{OEAB}$ or $\overline{OE}$ to B	LEAB = 3.0 V; Port A = 0 V	V_{ERC} = GND; see Figure 12	2.1	4.4	6.1	ns
t_{PHL}				2.0	3.4	5.0	ns
$\Delta V/\Delta t$	output slew rate	0.6 V to 1.3 V	V_{ERC} = V_{CC}	-	-	1	V/ns
			V_{ERC} = GND	-	-	1	V/ns
$t_{sk(o)}$	output edge skew	measured at V_{REF}		-	-	1	ns

Table 17: Port B to Port A switching

V_{TT} = 1.5 V; V_{REF} = 1 V for GTL+ (see Figures 15 and 16).
T_{amb} = −40 °C to +85 °C.

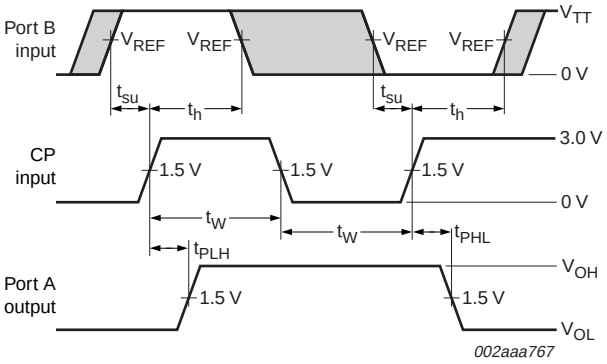
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{max}	maximum frequency			160	-	-	MHz
t_{PLH}	B to A	$\overline{OEBA}$ = $\overline{OE}$ = 0 V; LEBA = 3 V	see Figure 11	1.8	2.6	4.9	ns
t_{PHL}				2.3	4.2	5.3	ns
t_{PLH}	CP to A	$\overline{OEBA}$ = $\overline{OE}$ = 0 V; LEBA = 0 V	see Figure 5	1.5	3.1	4.4	ns
t_{PHL}				1.5	3.7	4.6	ns
t_{PLH}	LEBA to A	$\overline{OEBA}$ = $\overline{OE}$ = 0 V	see Figure 9	1.3	2.7	4.0	ns
t_{PHL}				1.4	3.1	3.9	ns
t_{PZL}	$\overline{OEBA}$ or $\overline{OE}$ to A	LEBA = 3.0 V; Port B = 0 V	see Figure 13	1.3	3.1	5.1	ns
t_{PLZ}				1.7	2.8	6.1	ns
t_{PZH}		LEBA = 3 V; Port B = V_{TT}	see Figure 14	1.3	3.3	5.1	ns
t_{PHZ}				1.7	3.3	6.1	ns
$t_{sk(o)}$	output edge skew	measured at 1.5 V		-	-	1	ns

10.1 AC waveforms



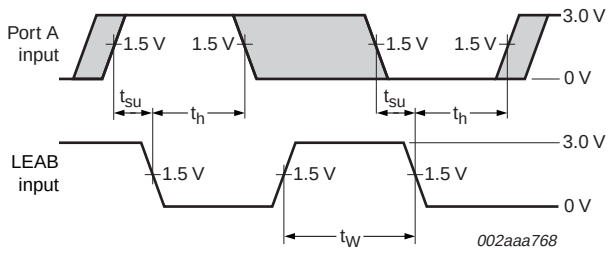
Test condition: $\overline{OEAB}$ = $\overline{OE}$ = 0 V

Fig 4. CP to B timing.



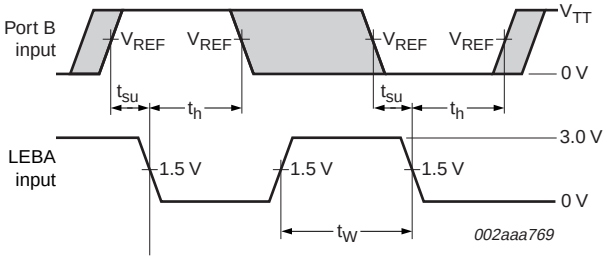
Test condition: $\overline{OEAB}$ = $\overline{OE}$ = 0 V; LEBA = 0 V

Fig 5. CP to A timing.



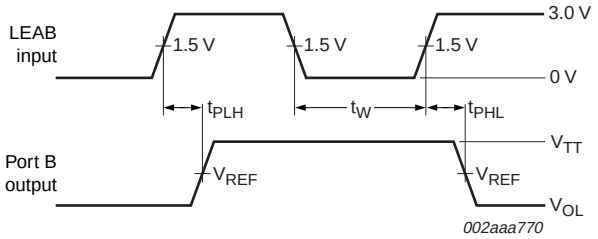
Test condition: $\overline{OEAB}$ = $\overline{OE}$ = 0 V

Fig 6. LEAB set-up and hold times.



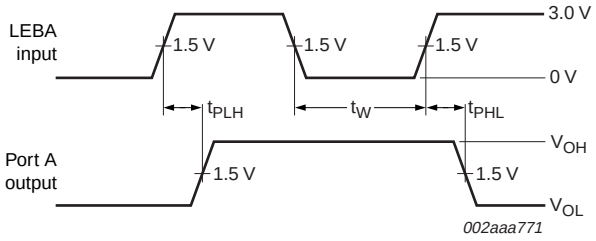
Test condition: $\overline{OEAB}$ = $\overline{OE}$ = 0 V

Fig 7. LEBA set-up and hold times.



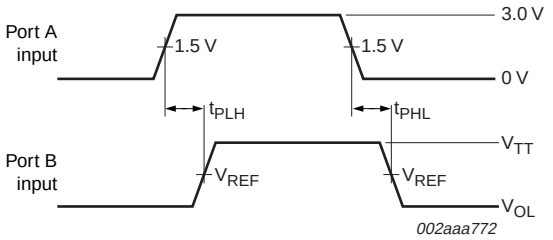
Test condition: $\overline{OEAB}$ = $\overline{OE}$ = 0 V; CP = 0 V or 3 V

Fig 8. LEAB to B propagation delay.



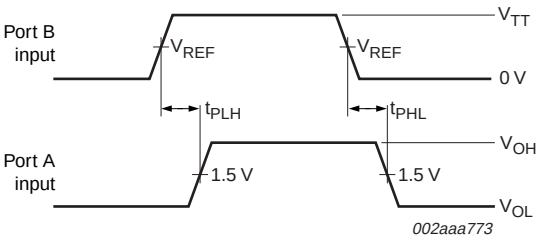
Test condition: $\overline{OEAB}$ = $\overline{OE}$ = 0 V; CP = 0 V or 3 V

Fig 9. LEBA to A propagation delay.



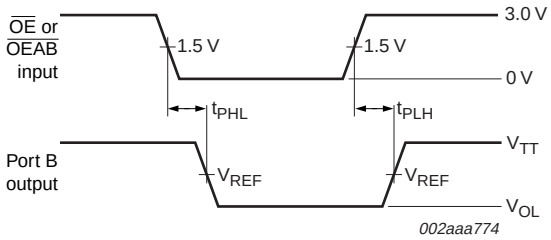
Test conditions: $\overline{OEAB}$ = $\overline{OE}$ = 0 V; LEAB = 3 V

Fig 10. A to B propagation delay.



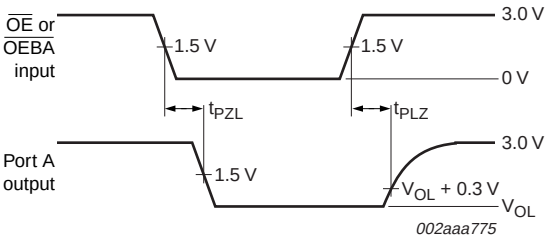
Test conditions: $\overline{OEBA}$ = $\overline{OE}$ = 0 V; LEBA = 3 V

Fig 11. B to A propagation delay.



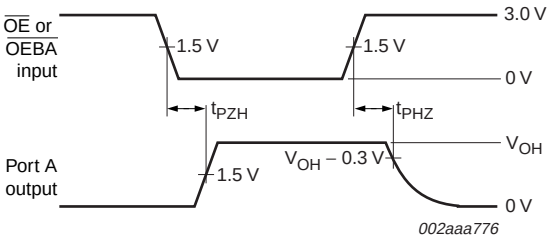
Test conditions: LEAB = 3 V; Port A = 0 V

Fig 12. $\overline{OE}$ or $\overline{OEAB}$ to B propagation delay.



Test conditions: LEBA = 3 V; Port B = 0 V

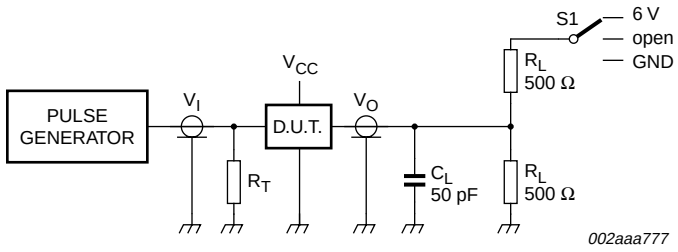
Fig 13. $\overline{OE}$ or $\overline{OEBA}$ to A propagation delay.



Test conditions: LEBA = 3 V; Port B = V_{TT}

Fig 14. $\overline{OE}$ or $\overline{OEBA}$ to A propagation delay.

11. Test information

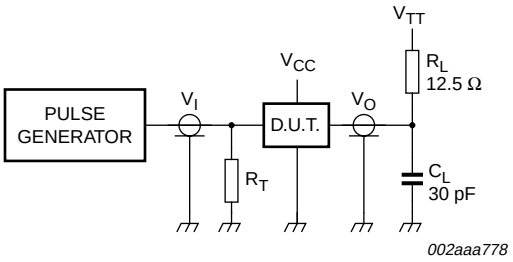


R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generator.

Fig 15. Load circuitry for Port A output switching times.



R_L = Load resistor.

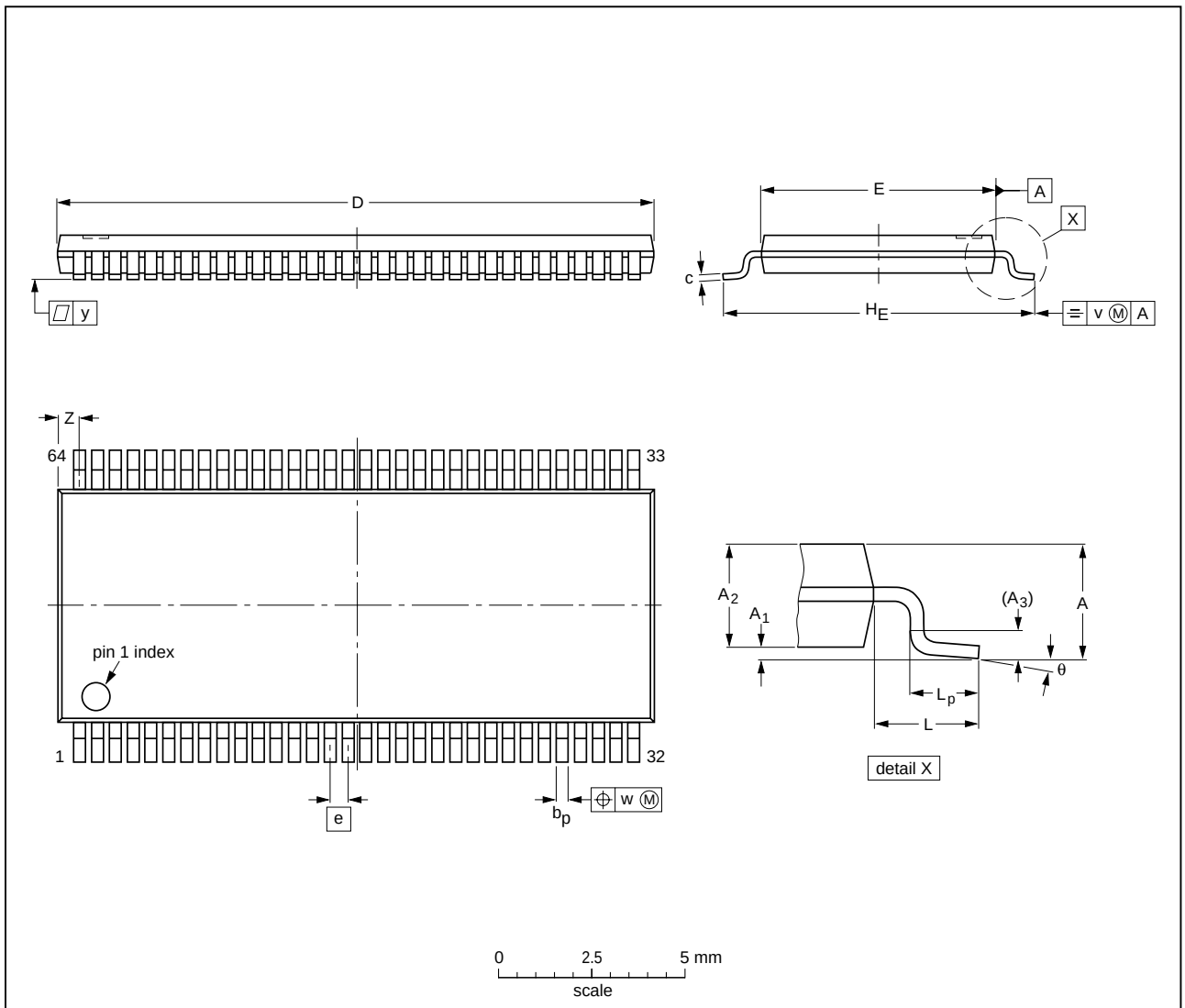
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generator.

Fig 16. Load circuitry for Port B output switching times.

12. Package outline

TSSOP64: plastic thin shrink small outline package; 64 leads; body width 6.1 mm **SOT646-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.27 0.17	**0.2** **0.1**	17.1 16.9	6.2 6.0	0.5	8.3 7.9	1	0.75 0.45	0.2	0.08	0.1	0.89 0.61	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT646-1		MO-153				~~00-08-21~~ 03-02-18

Fig 17. TSSOP64 package outline (SOT646-1).

13. Soldering

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.5 Package related soldering information

Table 18: Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

14. Revision history

Table 19: Revision history

Rev	Date	CPCN	Description
01	20040511	-	Product data (9397 750 12936).

15. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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For sales office addresses, send e-mail to: **sales.addresses@www.semiconductors.philips.com**. **Fax: +31 40 27 24825**

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