GENLINX™ GS9004D
Serial Digital Cable Equalizer

DATA SHEET

FEATURES

- **automatic cable equalization**
- **typically greater than 300 m of high quality cable at 270 Mb/s**
- **typically 300 m of high quality cable at 360 Mb/s**
- **drop in replacement for GS9004C**
- **capability to drive 50 Ω loads (to V_{TT})**
- **fully compatible with SMPTE 259M and operational to 400 Mb/s**
- **signal strength indicator**
- **output 'eye' monitor**
- **14 pin SOIC packaging**
- **single +5 or -5 volt power supply operation**
- **Pb-free and Green**

APPLICATIONS

- Front-end cable equalization for digital video systems
- Input equalization for serial digital distribution amplifiers, routers, production switchers and other receiving equipment

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Pb-Free and Green
GS9004DCKB	14 pin SOIC	0°C to 70°C	No
GS9004DCTB	14 pin SOIC Tape	0°C to 70°C	No
GS9004DCKBE3	14 pin SOIC	0°C to 70°C	Yes

DEVICE DESCRIPTION

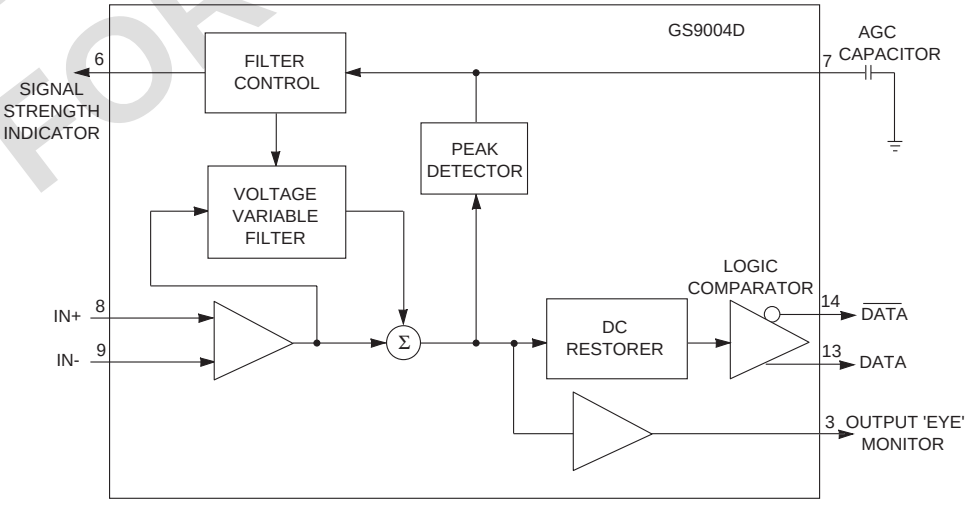
The Gennum GS9004D is an improved monolithic automatic cable equalizer developed for SMPTE/EBU scrambled NRZI Serial Digital Video signals.

While there are no plans to discontinue the GS9004D, Gennum has developed a successor product with improved features and performance called the GS9024. The GS9024 is recommended for new designs.

This device features DC restoration to pass the Pathological Test Signals and fully automatic equalization in order to meet the SMPTE 259M Serial Interface Standard. The DATA and $\overline{DATA}$ outputs typically deliver 800 mV (p-p) equalized signals into 50 Ω loads (to V_{TT}). These signals can be used to feed cable driver circuits for Serial Distribution Amplifier applications.

This device also incorporates an analog signal strength indicator (SSI) which provides a 0.5 V to 0 V output relative to V_{CC}, indicating the amount of equalization being applied to the signal.

The GS9004D features an OUTPUT 'EYE' MONITOR (OEM), which allows verification of signal integrity after equalization, prior to reslicing. Operating with a single +5 or -5 volt supply, the GS9004D typically draws 52 mA of current.



FUNCTIONAL BLOCK DIAGRAM

NOT RECOMMENDED FOR NEW DESIGNS

Revision Date: July 2004

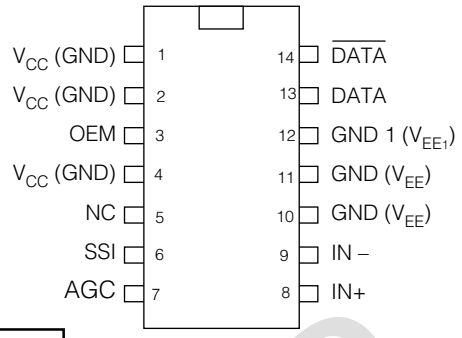
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ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage (V_S)	5.5 V
Input Voltage Range (any input)	V_{CC}+0.5 to V_{EE} -0.5 V
DC Input Current (any one input)	10 mA
Power Dissipation	500 mW
Operating Temperature Range	$0°C \le T_A \le 70°C$
Storage Temperature Range	$-65°C \le T_S \le 150°C$
Lead Temperature (soldering, 10 sec)	260°C

GS9004D PIN CONNECTIONS



PIN DESCRIPTIONS (I = INPUT, O = OUTPUT, S = SUPPLY function)

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	V_{CC} (GND)	S	Most positive supply voltage (ECL outputs)
2	V_{CC}(GND)	S	Most positive supply voltage (DC Restore/Eye Monitor)
3	OEM	O	Output 'Eye' Monitor
4	V_{CC}(GND)	S	Most positive supply voltage (Equalizer)
5	NC		No Connection
6	SSI	O	Signal Strength Indicator
7	AGC	I	AGC capacitor connection
8	IN+	I	Non-inverting signal
9	IN-	I	Inverting signal
10	GND(V_{EE})	S	Most negative supply voltage
11	GND(V_{EE})	S	Most negative supply voltage
12	GND1(V_{EE1})	S	Most negative supply voltage for EYE MONITOR
13	DATA	O	DATA (true)
14	$\overline{DATA}$	O	DATA (inverse)

GS9004D DC ELECTRICAL CHARACTERISTICS

Conditions: V_S = 5 V, T_A = 0° to 70°C, R_L = 100 Ω, to (V_{CC} -2) volts, unless otherwise shown.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_S	Operating Range	4.75	5.0	5.25	V	
Power Consumption	P_D		-	285	360	mW	
		With MONITOR active	-	330	415	mW	
Supply Current	I_S		-	52	72	mA	
		With MONITOR active	-	60	83	mA	
Serial Data Output - High	$V_{OH\ MIN}$	T_A = 25°C	-1.025	-	-0.88	V	with respect to V_{CC}
- Low	$V_{OL\ MAX}$	T_A = 25°C	-1.8	-	-1.6	V	with respect to V_{CC}

GS9004D AC ELECTRICAL CHARACTERISTICS

Conditions: V_S = 5 V, T_A = 0° to 70°C, R_L = 100 Ω, to (V_{CC} -2) volts, unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Output Signal Swing	V_O	T_A = 25°C	700	800	900	mV	
Input Resistance(IN+, IN-)	R_{IN}		4k	5k	-	Ω	see fig. 5
Input Capacitance(IN+, IN-)	C_{IN}	T_A = 25°C	-	1.3	-	pF	see fig. 5
Output 'Eye' Monitor	V_{OEM}	R_L = 50Ω, To V_{CC}	-	40	-	mV p-p	
Signal Strength Output	V_{SS}		4.4	-	5	V	
GS9004C GAIN	A_V	T_A = 25°C f=135 MHz	30	33	-	dB	
JITTER (Added) 270Mb/s	t_J	T_A = 25°C, 300m of 8281 cable.	-	600	-	ps p-p	Test setup 1

NOT RECOMMENDED FOR NEW DESIGNS

GS9004D CABLE EQUALIZER - DETAILED DEVICE DESCRIPTION

The GS9004D Cable Equalizer is a bipolar integrated circuit used to equalize SMPTE 259M signals from a co-axial cable. The device is implemented as a fourteen pin SOIC, powered from a single five volt supply. With an operating frequency up to 400 Mb/s, the equalizer consumes about 285 mW of power.

The Serial Digital signal is connected to the input (pins 8, 9) either differentially or single ended with the unused input being decoupled. The equalized signal is generated by passing the cable signal through a voltage variable filter having a characteristic which closely matches the inverse cable loss characteristic. Additionally, the variation of the filter characteristic with control voltage is designed to imitate the variation of the inverse cable loss characteristic as the cable length is varied.

The amplitude of the equalized signal is monitored by a peak detector circuit which produces an output current with a polarity corresponding to the difference between the desired peak signal level and the actual peak signal level.

This output is integrated by an external AGC filter capacitor (AGC CAP pin 7), providing a steady control voltage for the voltage variable filter.

A separate signal strength indicator output, (SSI pin 6), proportional to the amount of AGC, is also provided. As the filter characteristic is varied automatically by the application of negative feedback, the amplitude of the equalized signal is kept at a constant level which is representative of the original amplitude at the transmitter.

The equalized signal is then DC restored, effectively restoring the logic threshold of the equalized signal to its correct level irrespective of shifts due to AC coupling.

As the final stage of signal conditioning, a comparator converts the analog output of the DC restorer to a regenerated digital output signal having pseudo-ECL voltage levels. These outputs, $\overline{\text{DATA}}$ and DATA, are available from pins 13 and 14 respectively.

An OUTPUT 'EYE' MONITOR (pin 3) allows verification of signal integrity after equalization, prior to reslicing.

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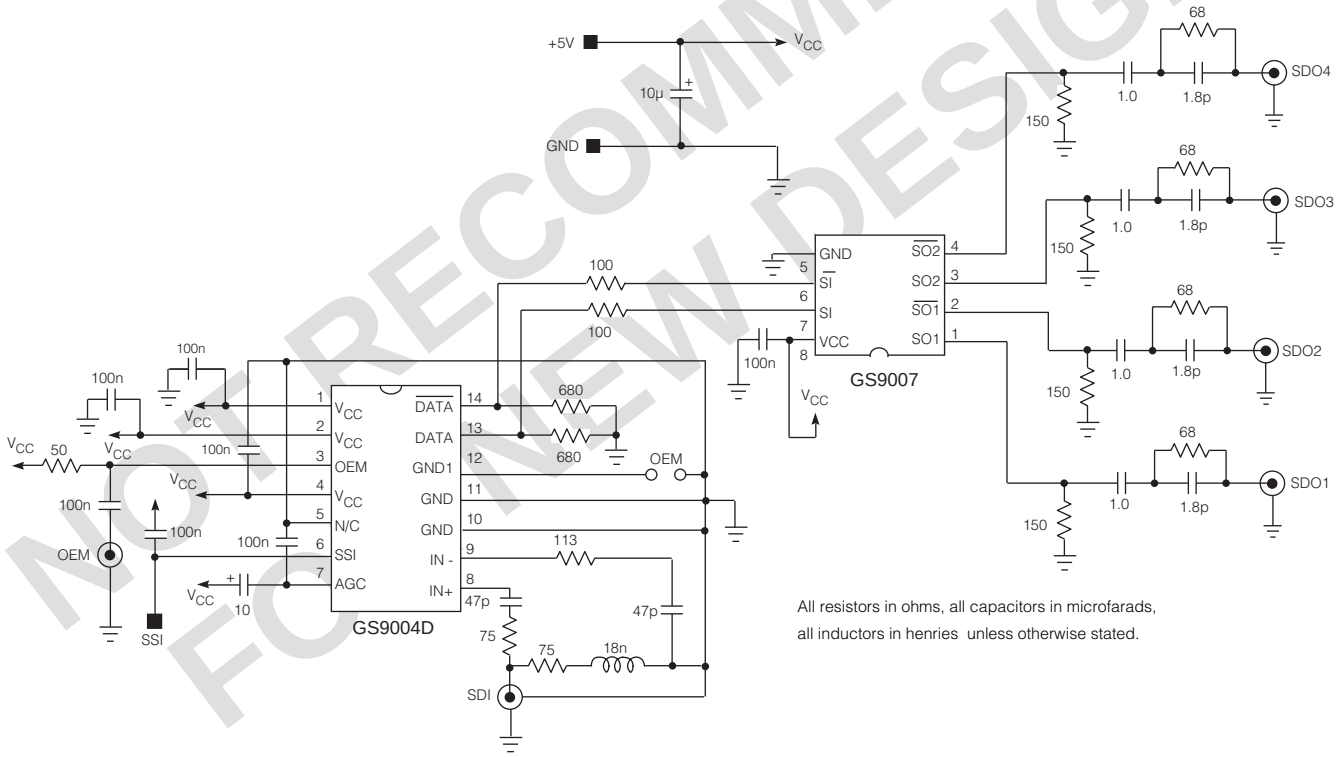


Fig. 1 Test Circuit

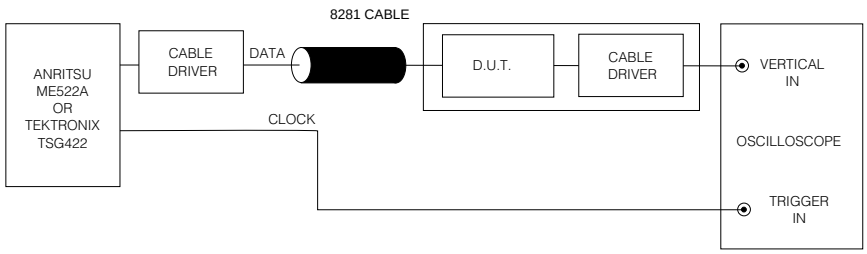


Fig. 2 Test Set-up 1

TYPICAL PERFORMANCE CURVES (unless otherwise shown V_S = 5V, T_A = 25°C)

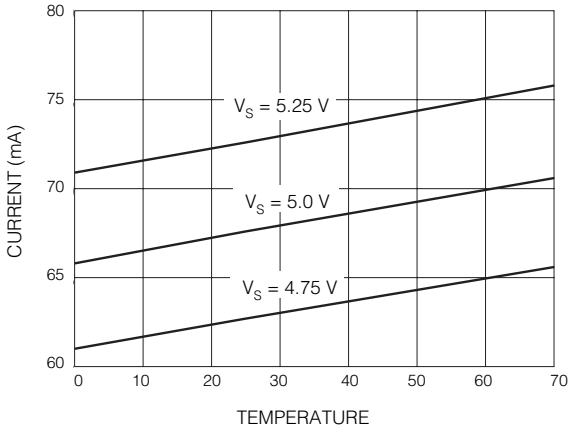


Fig. 3 Supply Current vs Temperature

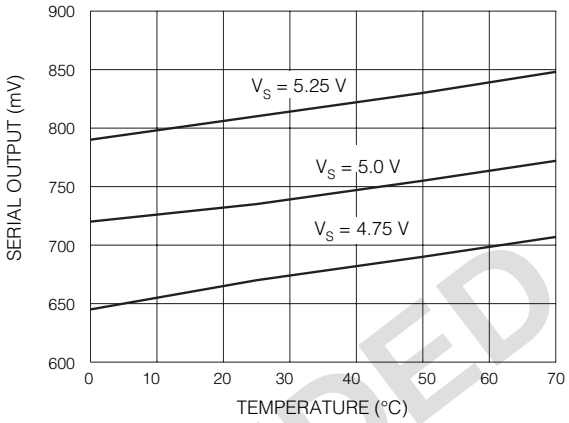


Fig. 4 Data and $\overline{\text{Data}}$ Output Voltage vs Temperature

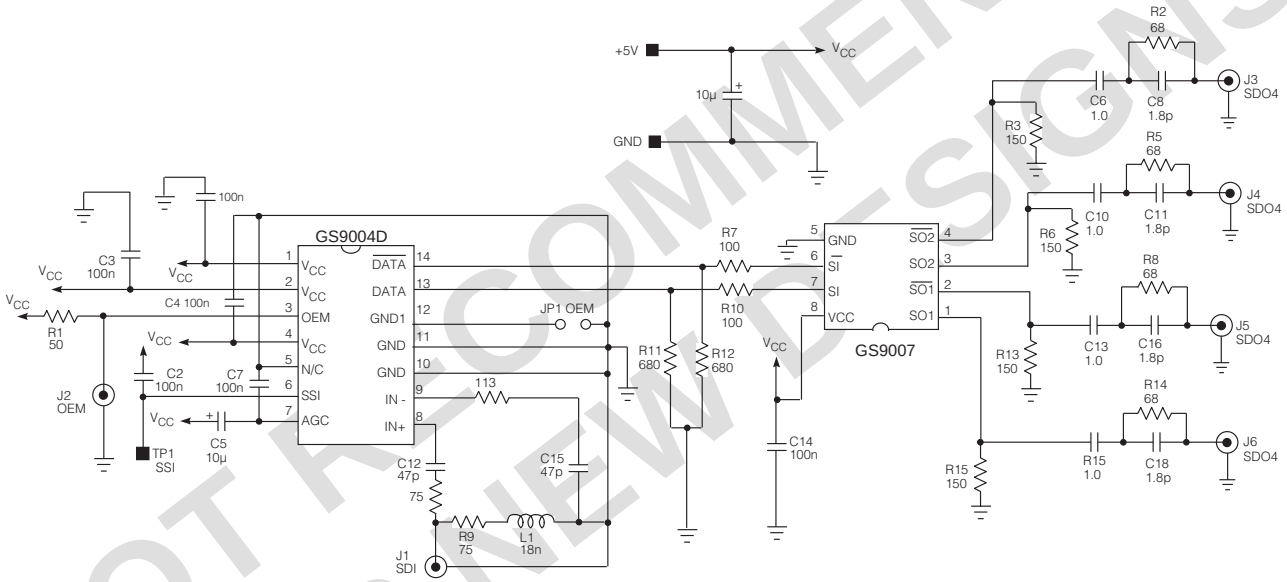


Fig. 5 Typical Application Circuit

All resistors in ohms, all capacitors in microfarads unless otherwise stated.

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REVISION NOTES:
New document.

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