TQFP, FP-BGA
Commercial Temp
Industrial Temp

64K x 24
1.5Mb Asynchronous SRAM

8, 9, 10, 12, 15 ns
3.3 V V_{DD}
Center V_{DD} and V_{SS}

Features

- Fast access time: 8, 9, 10, 12, 15 ns
- CMOS low power operation: 190/170/160/130/110 mA at minimum cycle time.
- Single 3.3 V ± 0.3 V power supply
- All inputs and outputs are TTL-compatible
- Fully static operation
- Industrial Temperature Option: –40 to 85°C
- Package
  - T: 100-pin TQFP package
  - U: 6 mm x 8 mm Fine Pitch Ball Grid Array
  - GT: Pb-Free 100-pin TQFP available

Description

The GS71024 is a high speed CMOS static RAM organized as 65,536 words by 24 bits. Static design eliminates the need for external clocks or timing strobes. The GS71024 operates on a single 3.3 V power supply, and all inputs and outputs are TTL-compatible. The GS71024 is available in a 6 mm x 8 mm Fine Pitch BGA package, as well as in a 100-pin TQFP package.

Fine Pitch BGA Bump Configuration

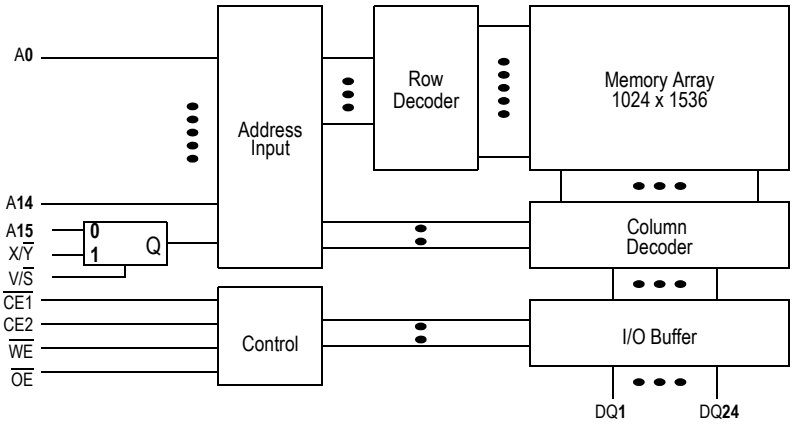
	1	2	3	4	5	6
A	DQ	A_3	A_2	A_1	A_0	DQ
B	DQ	DQ	CE2	$\overline{WE}$	DQ	DQ
C	DQ	DQ	$\overline{CE1}$	$\overline{OE}$	DQ	DQ
D	V_{SS}	DQ	A_5	A_4	DQ	V_{DD}
E	V_{DD}	DQ	A_7	A_6	DQ	V_{SS}
F	DQ	DQ	A_9	A_8	DQ	DQ
G	DQ	DQ	A_{11}	A_{10}	DQ	DQ
H	DQ	A_{15}	A_{14}	A_{13}	A_{12}	DQ

6 mm x 8 mm, 0.75 mm Bump Pitch
Top View

Pin Descriptions

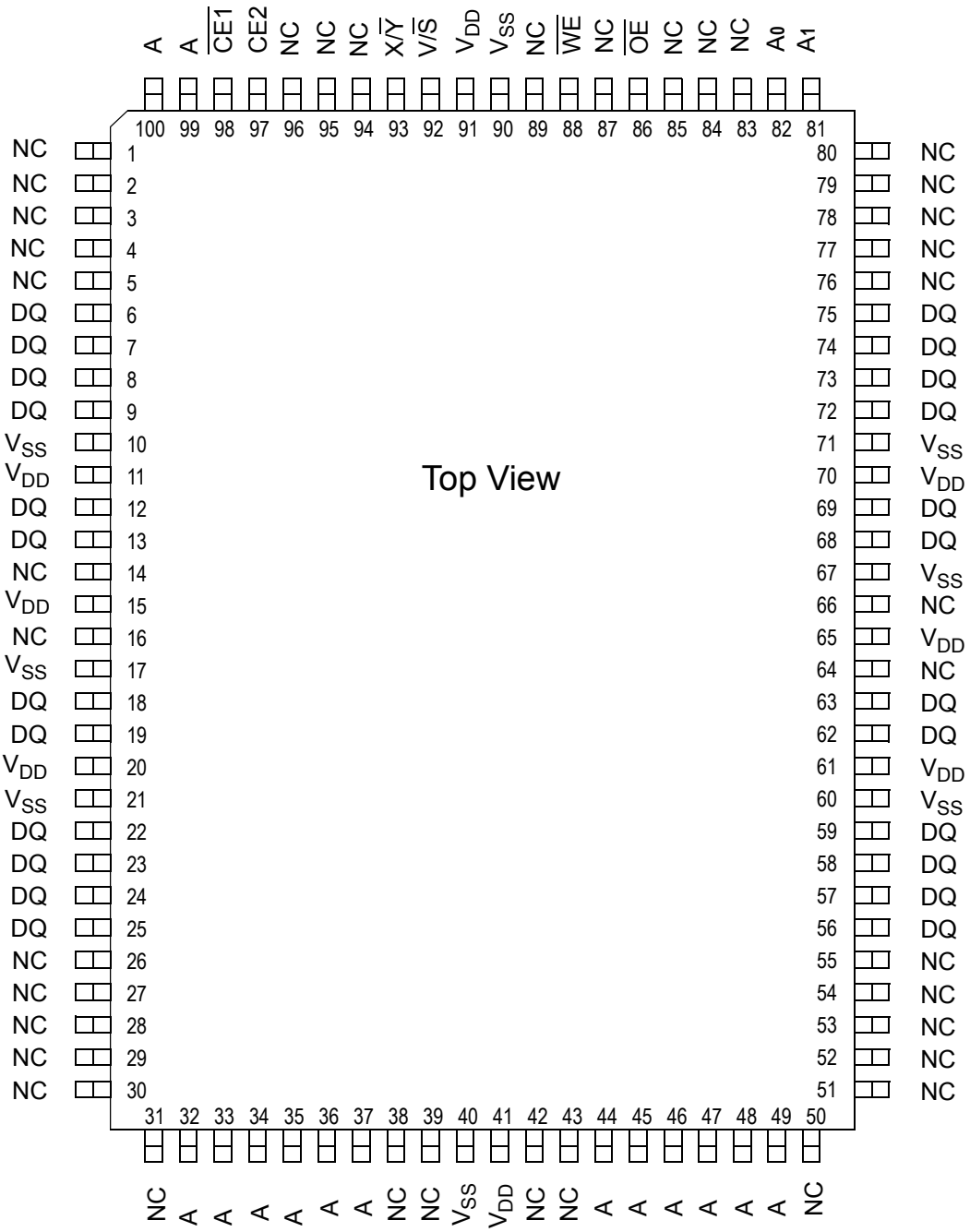
Symbol	Description	Symbol	Description
A_0 to A_{15}	Address input	DQ_1 to DQ_{24}	Data input/output
$X/\overline{Y}$	Vector Input	$V/\overline{S}$	Address Multiplexer Control
$\overline{WE}$	Write enable input	$\overline{OE}$	Output enable input
$\overline{CE1}$, CE2	Chip enable input	—	—
V_{DD}	+3.3 V power supply	V_{SS}	Ground

Block Diagram



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100-Pin TQFP Pinout



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Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	V/$\overline{S}$	Mode	DQ0 to DQ23	V_{DD} Current
H	X	X	X	X	Not selected	High Z	ISB1, ISB2
X	L	X	X	X	Not selected	High Z	
L	H	L	H	H	Read using X/$\overline{Y}$	Data Out	I_{DD}
L	H	L	H	L	Read using A15	Data Out	
L	H	X	L	H	Write using X/$\overline{Y}$	Data In	
L	H	X	L	L	Write using A15	Data In	
L	H	H	H	X	Output disable	High Z	

X: “H” or “L”

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	–0.5 to +4.6	V
Input Voltage	V_{IN}	–0.5 to V_{DD} + 0.5 (≤ 4.6 V max.)	V
Output Voltage	V_{OUT}	–0.5 to V_{DD} + 0.5 (≤ 4.6 V max.)	V
Allowable TQFP power dissipation	PD	1	W
Allowable FPBGA power dissipation	PD	1	W
Storage temperature	T_{STG}	–55 to 150	°C

Note:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

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Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage for -10/12/15	V_{DD}	3.0	3.3	3.6	V
Supply Voltage for -8	V_{DD}	3.135	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V
Ambient Temperature, Commercial Range	T_{Ac}	0	—	70	°C
Ambient Temperature, Industrial Range	T_{Ai}	–40	—	85	°C

Notes:
1. Input overshoot voltage should be less than V_{DD} + 2 V and not exceed 20 ns.
2. Input undershoot voltage should be greater than –2 V and not exceed 20 ns.

Capacitance

Parameter	Symbol	Test Condition	Maximum	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	5	pF
I/O Capacitance	C_{OUT}	V_{OUT} = 0 V	7	pF

Notes:
1. Tested at T_A = 25°C, f = 1 MHz
2. These parameters are sampled and are not 100% tested

DC I/O Pin Characteristics

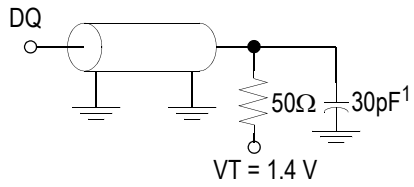
Parameter	Symbol	Test Conditions	Minimum	Maximum
Input Leakage Current	I_{IL}	V_{IN} = 0 to V_{DD}	–1uA	1uA
Output Leakage Current	I_{OL}	Output High Z, V_{OUT} = 0 to V_{DD}	–1uA	1uA
Output High Voltage	V_{OH}	I_{OH} = –4mA	2.4	—
Output Low Voltage	V_{OL}	I_{OL} = +4mA	—	0.4 V

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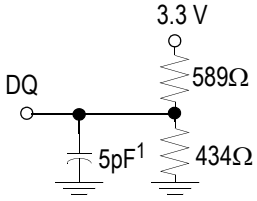
AC Test Conditions

Parameter	Conditions
Input high level	V_{IH} = 2.4 V
Input low level	V_{IL} = 0.4 V
Input rise time	tr = 1 V/ns
Input fall time	tf = 1 V/ns
Input reference level	1.4 V
Output reference level	1.4 V
Output load	**Fig. 1& 2**

Output Load 1



Output Load 2



Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted
3. Output load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}.

Power Supply Currents

Parameter	Symbol	Test Conditions	0 to 70°C					-40 to 85°C		
			8 ns	9 ns	10 ns	12 ns	15 ns	10 ns	12 ns	15 ns
Operating Supply Current	I_{DD}	$\overline{CE} \le V_{IL}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time I_{OUT} = 0 mA	190 mA	170 mA	160 mA	130 mA	110 mA	165 mA	135 mA	115 mA
Standby Current	I_{SB1}	$\overline{CE} \ge V_{IH}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time	45 mA	45 mA	40 mA	35 mA	30 mA	45 mA	40 mA	35 mA
Standby Current	I_{SB2}	$CE \ge V_{DD} - 0.2$ V All other inputs $\ge V_{DD} - 0.2$ V or ≤ 0.2 V	10 mA					15 mA		

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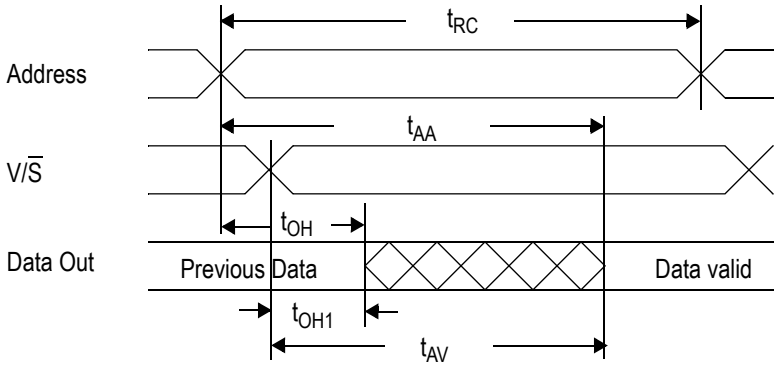
AC Characteristics

Read Cycle

Parameter	Symbol	-8		-9		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	8	—	9	—	10	—	12	—	15	—	ns
Address access time	t_{AA}	—	8	—	9	—	10	—	12	—	15	ns
Chip enable access time ($\overline{CE1}$, CE2)	t_{AC}	—	8	—	9	—	10	—	12	—	15	ns
MUX control to output valid (V/$\overline{S}$)	t_{AV}	—	8	—	9	—	10	—	12	—	15	ns
Output enable to output valid ($\overline{OE}$)	t_{OE}	—	4	—	4.5	—	5	—	6	—	7	ns
Output hold from address change	t_{OH}	3	—	3	—	3	—	3	—	3	—	ns
Output hold from MUX controls change	t_{OH1}	3	—	3	—	3	—	3	—	3	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ}*	3	—	3	—	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	0	—	0	—	ns
Chip disable to output in High Z ($\overline{CE1}$, CE2)	t_{HZ}*	—	4	—	4.5	—	5	—	6	—	7	ns
Output disable to output in High Z ($\overline{OE}$)	t_{OHZ}*	—	4	—	4.5	—	5	—	6	—	7	ns

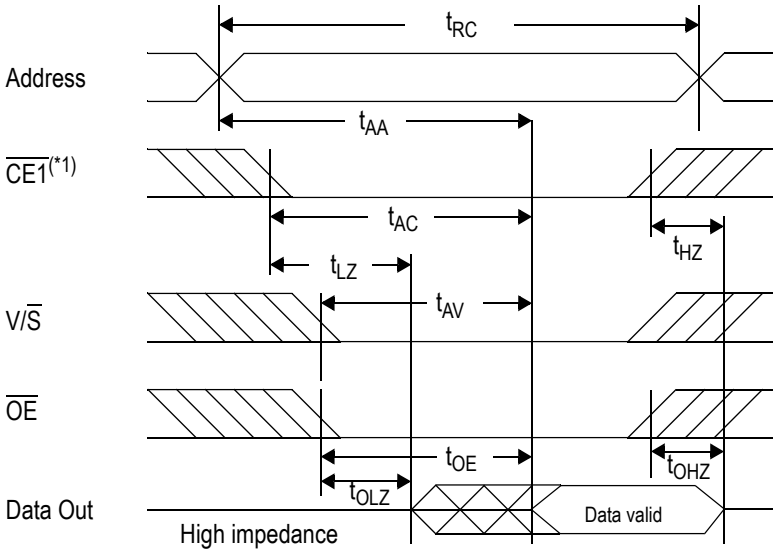
* These parameters are sampled and are not 100% tested

Read Cycle 1: $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}



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Read Cycle 2: $\overline{WE}$ = V_{IH}



*1 CE1 represents both $\overline{CE1}$ low and CE2 high.

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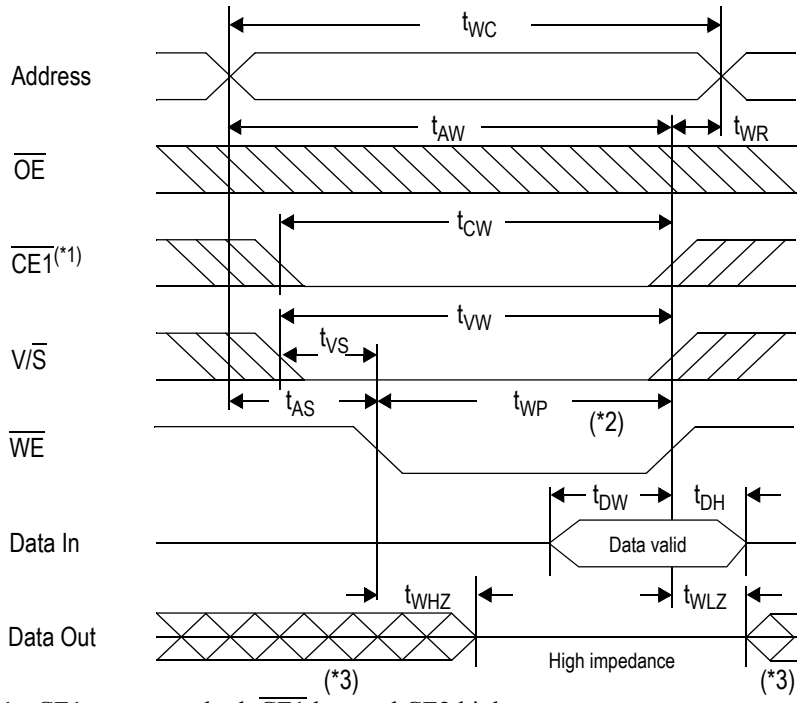
Write Cycle

Parameter	Symbol	-8		-9		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	8	—	9	—	10	—	12	—	15	—	ns
Address valid to end of write	t_{AW}	5.5	—	6.25	—	7	—	8	—	10	—	ns
Chip enable to end of write ($\overline{CE1}$, CE2)	t_{CW}	5.5	—	6.25	—	7	—	8	—	10	—	ns
MUX control to end of write (V/$\overline{S}$)	t_{VW}	5.5	—	6.25	—	7	—	8	—	10	—	ns
Data set up time	t_{DW}	4	—	4.5	—	5	—	6	—	7	—	ns
Data hold time	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	5.5	—	6.25	—	7	—	8	—	10	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns
MUX control set up time	t_{VS}	0	—	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns
Write recovery time (V/$\overline{S}$, $\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	0	—	0	—	ns
Output Low Z from end of write	t_{WLZ}*	2	—	2.5	—	3	—	3	—	3	—	ns
Write to output in High Z	t_{WHZ}*	—	4	—	4.5	—	5	—	6	—	7	ns

* These parameters are sampled and are not 100% tested

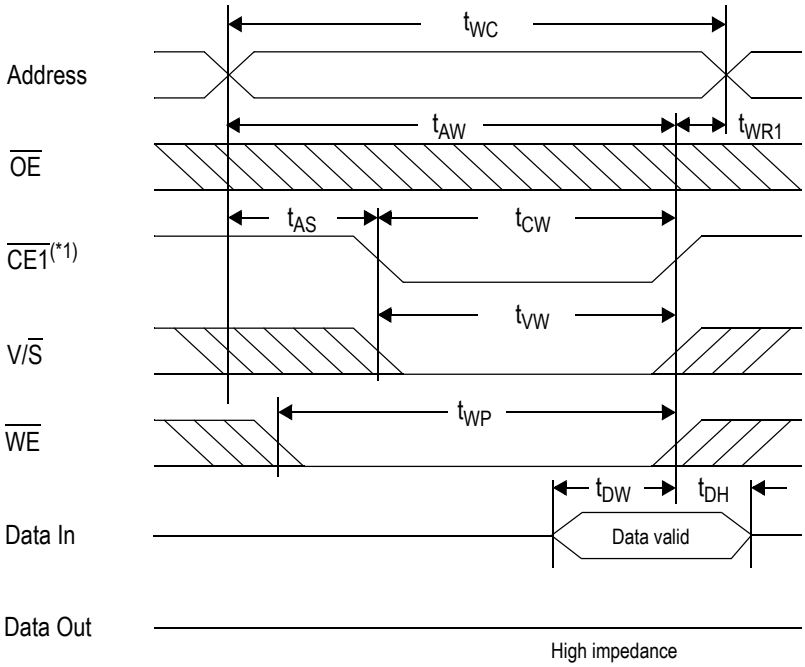
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Write Cycle 1: $\overline{WE}$ control



*1 CE1 represents both $\overline{CE1}$ low and CE2 high.
*2 Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low simultaneously.
*3 Do not apply the data input voltage to the output while DQ pin is in output condition.

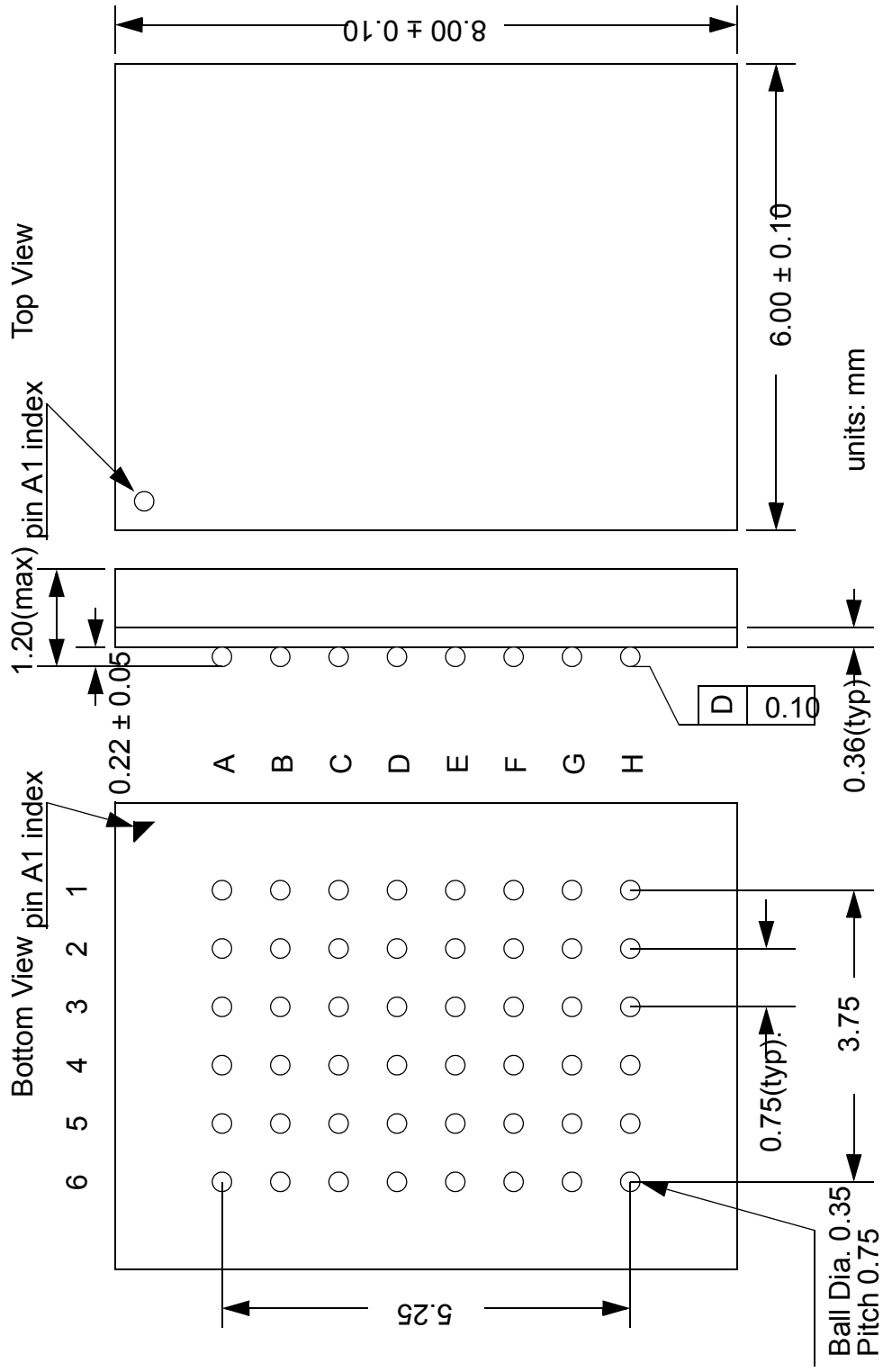
Write Cycle 2: $\overline{CE}$ control



*1 CE1 represents both $\overline{CE1}$ low and CE2 high.

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6 mm x 8 mm Fine Pitch BGA

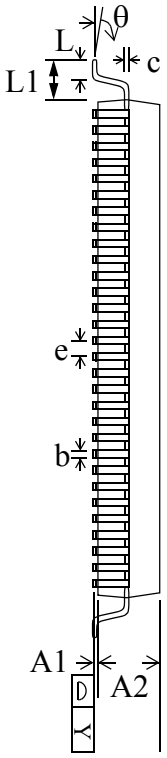


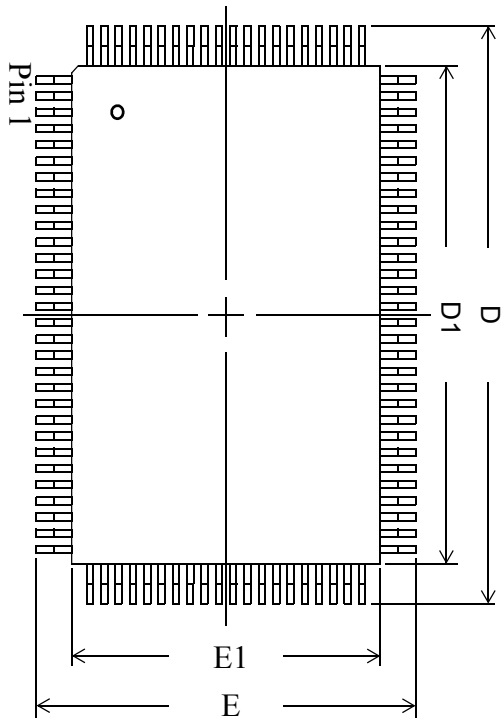
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TQFP Package Drawing

Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09		0.20
D	Terminal Dimension	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch		0.65	
L	Foot Length	0.45	0.60	0.75
L1	Lead Length		1.00	
Y	Coplanarity			0.10
θ	Lead Angle	0°		7°

Notes:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion





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Ordering Information

Part Number	Package	Access Time	Temp. Range	Status
GS71024T-8	100-Pin TQFP	8 ns	Commercial	
GS71024T-9	100-Pin TQFP	9 ns	Commercial	
GS71024T-10	100-Pin TQFP	10 ns	Commercial	
GS71024T-12	100-Pin TQFP	12 ns	Commercial	
GS71024T-15	100-Pin TQFP	15 ns	Commercial	
GS71024T-8I	100-Pin TQFP	8 ns	Industrial	
GS71024T-9I	100-Pin TQFP	9 ns	Industrial	
GS71024T-10I	100-Pin TQFP	10 ns	Industrial	
GS71024T-12I	100-Pin TQFP	12 ns	Industrial	
GS71024T-15I	100-Pin TQFP	15 ns	Industrial	
GS71024GT-8	Pb-free 100-Pin TQFP	8 ns	Commercial	
GS71024GT-9	Pb-free 100-Pin TQFP	9 ns	Commercial	
GS71024GT-10	Pb-free 100-Pin TQFP	10 ns	Commercial	
GS71024GT-12	Pb-free 100-Pin TQFP	12 ns	Commercial	
GS71024GT-15	Pb-free 100-Pin TQFP	15 ns	Commercial	
GS71024GT-8I	Pb-free 100-Pin TQFP	8 ns	Industrial	
GS71024GT-9I	Pb-free 100-Pin TQFP	9 ns	Industrial	
GS71024GT-10I	Pb-free 100-Pin TQFP	10 ns	Industrial	
GS71024GT-12I	Pb-free 100-Pin TQFP	12 ns	Industrial	
GS71024GT-15I	Pb-free 100-Pin TQFP	15 ns	Industrial	
GS71024U-8	6 mm x 8 mm Fine Pitch BGA	8 ns	Commercial	
GS71024U-9	6 mm x 8 mm Fine Pitch BGA	9 ns	Commercial	
GS71024U-10	6 mm x 8 mm Fine Pitch BGA	10 ns	Commercial	
GS71024U-12	6 mm x 8 mm Fine Pitch BGA	12 ns	Commercial	
GS71024U-15	6 mm x 8 mm Fine Pitch BGA	15 ns	Commercial	
GS71024U-8I	6 mm x 8 mm Fine Pitch BGA	8 ns	Industrial	
GS71024U-9I	6 mm x 8 mm Fine Pitch BGA	9 ns	Industrial	
GS71024U-10I	6 mm x 8 mm Fine Pitch BGA	10 ns	Industrial	

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Ordering Information

Part Number	Package	Access Time	Temp. Range	Status
GS71024U-12I	6 mm x 8 mm Fine Pitch BGA	12 ns	Industrial	
GS71024U-15I	6 mm x 8 mm Fine Pitch BGA	15 ns	Industrial	

* Customers requiring Tape and Reel should add the character "T" to the end of the part number. For example: GS71024T/U-12T.

Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page/Revisions/Reason
GS71024Rev 2:17pm, 4/8/1999; 1.00a5/1999	Format/Typos	• Document Changed subscripts to small caps. • 1/Features: Changed TP to T. • Document/Replaced "micro" with "fine pitch".
	Content	• Ordering Information/Added Tape and Reel Note/ Enhancement • Pin Description/Changed A0 - A14 to A0 - A15/Correction • Page 1/Took out "Byte Control" from Features/Correction • 3/Changed pin 97 from NC to CE2/Correction •
GS710241.00a5/1999; 1.01 8/1999B	Content	1. Pin out/Changed Pin 89 from CK to NC/Correction 2. Pin out/Changed Pin 92 from NC to V/$\overline{S}$/Correction 3. Pin out/Changed Pin 93 from V/$\overline{S}$ to X/$\overline{Y}$/Correction 4. Pin out/Changed Pin 94 from X/$\overline{Y}$ to NC/Correction
GS710241.01 8/1999C; 1.02 9/1999C	Content	• Package Diagram/Changed Dimension "D Max" from 20.1 to 22.1/Correction
GS71024Rev1.01 8/ 1999C;Rev1.02 2/2000D	Format	• GSI Logo
Rev1.02 2/2000D; 71024_r1_03	Format and Content	• Updated format to comply with Technical Publications standards • Changed all V_{SSQ} to V_{SS} and all V_{DDQ} to V_{DD} in pinout on page 2 • Updated Revision History (revision notes for 8/1999 incorrect)
71024_r1_03; 71024_r1_04	Content	• Added 9 ns references to entire document
71024_r1_04; 71024_r1_05	Content/Format	• Updated format • Added Pb-free information for TQFP package

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