GS1572 Multi-Rate Serializer with Cable Driver and ClockCleaner™

Key Features

- HD-SDI, SD-SDI, DVB-ASI transmitter
- Integrated SMPTE 292M and 259M-C compliant cable driver
- Integrated ClockCleaner™
- User selectable video processing features, including:
  - Generic ancillary data insertion
  - Support for HVF or EIA/CEA-861 timing input
  - Automatic standard detection and indication
  - Enhanced SMPTE 352M payload identifier generation and insertion
  - TRS, CRC, ANC data checksum, and line number calculation and insertion
  - EDH packet generation and insertion
  - Illegal code remapping
  - SMPTE 292M and SMPTE 259M-C compliant scrambling and NRZ → NRZI encoding
  - Blanking of input HANC and VANC space
- JTAG test interface
- 1.8V core and 3.3V charge pump power supply
- 1.8V and 3.3V digital I/O support
- Low power standby mode
- Operating temperature range: -20°C to +85°C
- Pb-free, RoHS compliant, 11mm x 11mm 100-ball BGA package

Applications

- SMPTE 292M and SMPTE 259M-C Serial Digital Interfaces
- DVB-ASI Serial Digital Interfaces

Description

The GS1572 is the next generation multi-standard serializer with an integrated cable driver. The device provides robust parallel to serial conversion, generating a SMPTE 292M/259M-C compliant serial digital output signal. The integrated cable driver features an output disable (high-impedance) mode and an adjustable signal swing. Data input is accepted in 20-bit parallel format or 10-bit parallel format. An associated parallel clock input must be provided at the appropriate operating frequency - 74.25/74.1758/13.5MHz (20-bit mode) or 148.5/148.352/27MHz (10-bit mode).

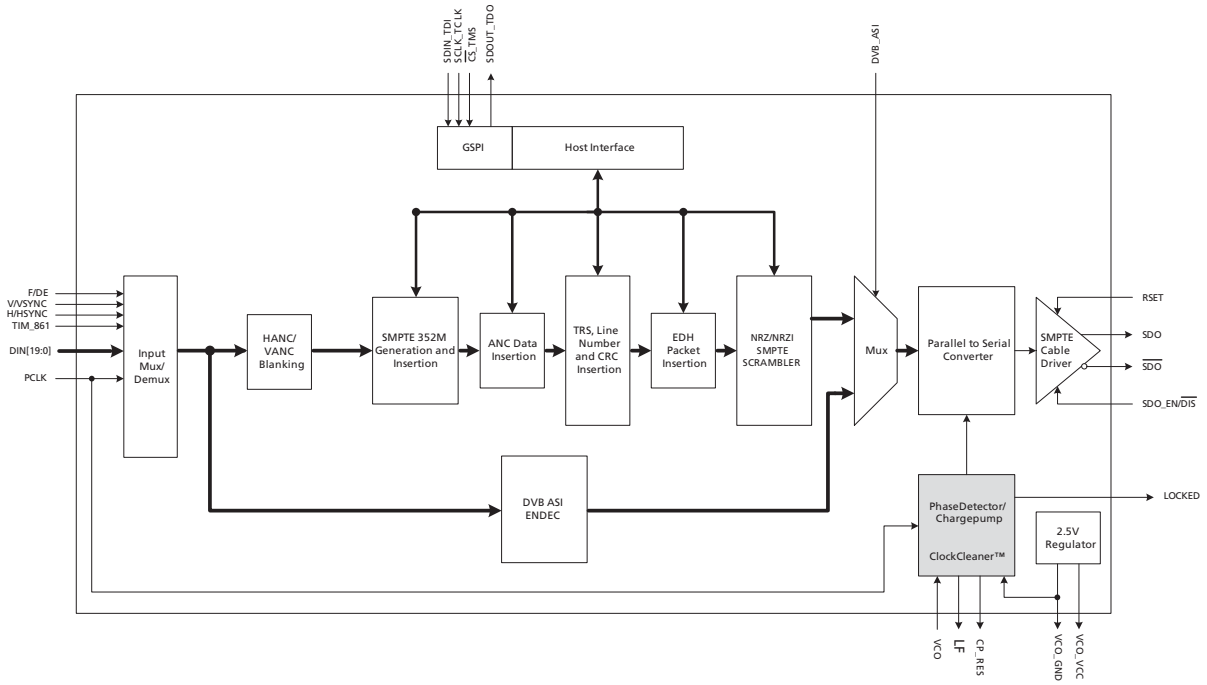
The GS1572 features an internal PLL which, if desired, can be configured for a loop bandwidth below 100kHz. When used in conjunction with the GO1555 Voltage Controlled Oscillator, the GS1572 can tolerate well in excess of 300ps jitter on the input PCLK and still provide output jitter within SMPTE specifications.

In addition to serializing the input, the GS1572 performs NRZ-to-NRZI encoding and scrambling as per SMPTE 292M/259M-C when operating in SMPTE mode. When operating in DVB-ASI mode, the device will insert K28.5 sync characters and 8b/10b encode the data prior to serialization. The device also provides a range of other data processing functions. All processing features are optional and may be enabled/disabled via external control pin(s) and/or host interface programming.

Typical power consumption, including the GO1555 VCO, is 440mW. The standby feature allows the power to be reduced to 125mW. Power may be reduced to less than 10mW by also removing the power to the cable driver and eliminating transitions at the parallel data and clock inputs.

The GS1572 is Pb-free and RoHS compliant.

Functional Block Diagram



GS1572 Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
4	151052	52184	March 2009	Updated document format. Changed Figure 4-14: GSPI Write Mode Timing. Changed Parallel Input Data Hold Time from 2ns to 0.8ns in Table 2-4: AC Electrical Characteristics.
3	148226	–	November 2007	Converted from Preliminary Data Sheet to Data Sheet. Updates to; 2.1 Absolute Maximum Ratings, 4.12 GSPI Host Interface, Table 4-4: Host Interface Description for Raster Structure Registers, 2.3 DC Electrical Characteristics, 4.8.4.4 Ancillary Data Checksum Generation and Insertion, Table 2-4: AC Electrical Characteristics and 4.8.4.1 SMPTE 352M Payload Identifier Packet Insertion.
2	146447	–	July 2007	Updated Typical Application Circuit.
1	146292	–	July 2007	Format change.
0	145654	–	July 2007	Converted from Advance Information Note to Preliminary Data Sheet. Changes were made in the following areas: Pin Descriptions on page 8, Absolute Maximum Ratings on page 16, Recommended Operating Conditions on page 17, DC Electrical Characteristics on page 17, AC Electrical Characteristics on page 18, SMPTE Mode on page 26, HVF Timing on page 26, Standby Mode on page 33, on page 34, VANC Insertion on page 36, SMPTE 352M Payload Identifier Packet Insertion on page 40, EDH Generation and Insertion on page 42, Loop Filter on page 45, Lock Detect Output on page 46, Command Word Description on page 48, Device Reset on page 58, Typical Application Circuit on page 59, Package Dimensions on page 61, Solder Reflow Profiles on page 62, Packaging Data on page 63, Ordering Information on page 63.
A	144897	–	April 2007	New Document.

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1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	DIN17	DIN18	F/DE	H/HSYNC	CORE_VDD	PD_VDD	LF	VCO_VCC	VCO	CP_VDD
B	DIN15	DIN16	DIN19	PCLK	CORE_GND	PD_VDD	CP_RES	VCO_GND	VCO_GND	CP_GND
C	DIN13	DIN14	DIN12	V/VSYNC	CORE_GND	PD_GND	PD_GND	PD_GND	CD_GND	SDO
D	DIN11	DIN10	STANDBY	SDO_EN/$\overline{\text{DIS}}$	CORE_GND	NC	NC	NC	CD_GND	$\overline{\text{SDO}}$
E	CORE_VDD	CORE_GND	SD/$\overline{\text{HD}}$	NC	CORE_GND	CORE_GND	CORE_GND	NC	CD_GND	CD_VDD
F	DIN9	DIN8	DETECT_TRS	CORE_GND	CORE_GND	CORE_GND	CORE_GND	NC	CD_GND	RSET
G	IO_VDD	IO_GND	TIM 861	20bit/$\overline{\text{10bit}}$	DVB_ASI	$\overline{\text{SMPTE_BYPASS}}$	IOPROC_EN/$\overline{\text{DIS}}$	$\overline{\text{RESET}}$	CORE_GND	CORE_VDD
H	DIN7	DIN6	$\overline{\text{ANC_BLANK}}$	LOCKED	RSV	RSV	RSV	JTAG/$\overline{\text{HOST}}$	IO_GND	IO_VDD
J	DIN5	DIN4	DIN1	RSV	RSV	RSV	RSV	CORE_GND	SDOUT_TDO	SCLK_TCLK
K	DIN3	DIN2	DIN0	RSV	RSV	RSV	RSV	CORE_VDD	$\overline{\text{CS}}$_TMS	SDIN_TDI

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description	
A1, A2, B1, B2, B3, C1, C2, C3, D1, D2	DIN[19:10]	Synchronous with PCLK	Input	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible. DIN19 is the MSB and DIN10 is the LSB.	
				HD 20-bit mode SD/$\overline{HD}$ = LOW 20bit/$\overline{10bit}$ = HIGH	Luma data input in SMPTE mode $\overline{SMPTE_BYPASS}$ = HIGH DVB_ASI = LOW Data input in Data-Through mode $\overline{SMPTE_BYPASS}$ = LOW DVB_ASI = LOW
				HD 10-bit mode SD/$\overline{HD}$ = LOW 20bit/$\overline{10bit}$ = LOW	Multiplexed Luma and Chroma data input in SMPTE mode $\overline{SMPTE_BYPASS}$ = HIGH DVB_ASI = LOW Data input in Data-Through mode $\overline{SMPTE_BYPASS}$ = LOW DVB_ASI = LOW
				SD 20-bit mode SD/$\overline{HD}$ = HIGH 20bit/$\overline{10bit}$ = HIGH	Luma data input in SMPTE mode $\overline{SMPTE_BYPASS}$ = HIGH DVB_ASI = LOW Data input in Data-Through mode $\overline{SMPTE_BYPASS}$ = LOW DVB_ASI = LOW DVB-ASI data input in DVB-ASI mode $\overline{SMPTE_BYPASS}$ = LOW DVB_ASI = HIGH
				SD 10-bit mode SD/$\overline{HD}$ = HIGH 20bit/$\overline{10bit}$ = LOW	Multiplexed Luma and Chroma data input in SMPTE mode $\overline{SMPTE_BYPASS}$ = HIGH DVB_ASI = LOW Data input in data through mode $\overline{SMPTE_BYPASS}$ = LOW DVB_ASI = LOW DVB-ASI data input in DVB-ASI mode $\overline{SMPTE_BYPASS}$ = LOW DVB_ASI = HIGH

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
A3	F/DE	Synchronous with PCLK	Input	PARALLEL DATA TIMING Signal levels are LVCMOS/LVTTL compatible. TIM_861 = LOW: Used to indicate the ODD / EVEN field of the video signal when DETECT_TRS is set LOW. The device will set the F bit in all outgoing TRS signals for the entire period that the F input signal is HIGH (IOPROC_EN/$\overline{DIS}$ must also be HIGH). The F signal should be set HIGH for the entire period of field 2 and should be set LOW for all lines in field 1 and for all lines in progressive scan systems. The F signal is ignored when DETECT_TRS = HIGH. TIM_861 = HIGH: The DE signal is used to indicate the active video period. DE is HIGH for active data and LOW for blanking. See Section 4.3.1 and Section 4.3.2 for timing details. The DE signal is ignored when DETECT_TRS = HIGH.
A4	H/HSYNC	Synchronous with PCLK	Input	PARALLEL DATA TIMING Signal levels are LVCMOS/LVTTL compatible. TIM_861 = LOW: The H signal is used to indicate the portion of the video line containing active video data, when DETECT_TRS is set LOW. Active Line Blanking The H signal should be set HIGH for the entire horizontal blanking period, including the EAV and SAV TRS words, and LOW otherwise. This is the default setting. TRS Based Blanking (H_CONFIG = 1_h) The H signal should be set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS ID words, and LOW otherwise. The H signal is ignored when DETECT_TRS = HIGH. TIM_861 = HIGH: The HSYNC signal indicates horizontal timing. See Section 4.3.1 for timing details. The HSYNC signal is ignored when DETECT_TRS = HIGH.
A5, E1, G10, K8	CORE_VDD	Non Synchronous	Input Power	Power supply connection for the digital core logic. Connect to +1.8V DC digital.
A6, B6	PD_VDD	Analog	Input Power	Power supply connection for the phase detector. Connect to +1.8V DC analog.
A7	LF	Analog	Input	PLL loop filter connection.
A8	VCO_VCC	Analog	Output Power	Power supply for the external voltage controlled oscillator. 2.5V DC supplied by the device to the external VCO.
A9	VCO	Analog	Input	Input from external VCO.
A10	CP_VDD	Analog	Input Power	Power supply connection for the charge pump and on chip VCO regulator. Connect to +3.3V DC analog.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description	
B4	PCLK	–	Input	PARALLEL DATA BUS CLOCK Signal levels are LVCMOS/LVTTL compatible.	
				HD 20-bit mode	PCLK = 74.25MHz or 74.25/1.001MHz
				HD 10-bit mode	PCLK = 148.5MHz or 148.5/1.001MHz
				SD 20-bit mode	PCLK = 13.5MHz
				SD 10-bit mode	PCLK = 27MHz
B5, C5, D5, E2, E5, E6, E7, F4, F5, F6, F7, G9, J8	CORE_GND	Non Synchronous	Input Power	Ground connection for the digital core logic. Connect to digital GND.	
C6, C7, C8	PD_GND	Analog	Input Power	Ground connection for the phase detector. Connect to analog GND.	
B7	CP_RES	–	Input	Charge pump current setting resistor.	
B8, B9	VCO_GND	Analog	Output Power	Ground pins for the VCO.	
B10	CP_GND	Analog	Input Power	Ground pin for the charge pump and PLL.	
C4	V/VSYNC	Synchronous with PCLK	Input	PARALLEL DATA TIMING Signal levels are LVCMOS/LVTTL compatible. TIM_861 = LOW: The V signal is used to indicate the portion of the video field/frame that is used for vertical blanking, when DETECT_TRS is set LOW. The V signal should be set HIGH for the entire vertical blanking period and should be set LOW for all lines outside of the vertical blanking interval. The V signal is ignored when DETECT_TRS = HIGH. TIM_861 = HIGH: The VSYNC signal indicates vertical timing. See Section 4.3.1 for timing details. The VSYNC signal is ignored when DETECT_TRS = HIGH.	
C9, D9, E9, F9	CD_GND	Analog	Input Power	Ground connection for the serial digital cable driver. Connect to analog GND.	
C10, D10	SDO, $\overline{\text{SDO}}$	Analog	Output	Serial digital output signal operating at 1.485Gb/s, 1.485/1.001Gb/s, or 270Mb/s. The slew rate of these outputs is automatically controlled to meet SMPTE 292M and 259M requirements according to the setting of the SD/$\overline{\text{HD}}$ pin. Serial digital output signal from the internal cable driver. NOTE: The SDO/$\overline{\text{SDO}}$ output signals will be set to high impedance when $\overline{\text{RESET}}$ = LOW.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
D3	STANDBY	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Power down input. When set HIGH, the device will be in standby mode.
D4	SDO_EN/$\overline{\text{DIS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable the serial digital output stage. When set LOW, the serial digital output signals SDO and $\overline{\text{SDO}}$ are disabled and become high impedance. When set HIGH, the serial digital output signals SDO and $\overline{\text{SDO}}$ are enabled. The SDO and $\overline{\text{SDO}}$ outputs will also be high impedance when the $\overline{\text{RESET}}$ pin is LOW.
D6, D7, D8, E4, E8, F8	NC	–	–	No connect. Not connected internally.
E3	SD/$\overline{\text{HD}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When set LOW, the device will be configured to transmit signals of 1.485Gb/s - 1.485/1.001Gb/s rates only. When set HIGH, the device will be configured to transmit signals of a 270Mb/s rate only.
E10	CD_VDD	Analog	Input Power	Power supply connection for the serial digital cable driver. Connect to +3.3V DC analog.
F1, F2, H1, H2, J1, J2, J3, K1, K2, K3	DIN[9:0]	Synchronous with PCLK	Input	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible. DIN9 is the MSB and DIN0 is the LSB.
				HD 20-bit mode SD/$\overline{\text{HD}}$ = LOW 20bit/$\overline{\text{10bit}}$ = HIGH — Chroma data input in SMPTE mode $\overline{\text{SMPTE_BYPASS}}$ =HIGH DVB_ASI = LOW Data input in Data-Through mode $\overline{\text{SMPTE_BYPASS}}$ = LOW DVB_ASI = LOW
				HD 10-bit mode SD/$\overline{\text{HD}}$ = LOW 20bit/$\overline{\text{10bit}}$ = LOW — High impedance in all modes.
				SD 20-bit mode SD/$\overline{\text{HD}}$ = HIGH 20bit/$\overline{\text{10bit}}$ = HIGH — Chroma data input in SMPTE mode $\overline{\text{SMPTE_BYPASS}}$ = HIGH DVB_ASI = LOW Data input in Data-Through mode $\overline{\text{SMPTE_BYPASS}}$ = LOW DVB_ASI = LOW Forced low in DVB-ASI mode $\overline{\text{SMPTE_BYPASS}}$ = LOW DVB_ASI = HIGH
				SD 10-bit mode SD/$\overline{\text{HD}}$ = HIGH 20bit/$\overline{\text{10bit}}$ = LOW — High impedance in all modes.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
F3	DETECT_TRS	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select external HVF timing mode or TRS Extraction timing mode. When DETECT_TRS = LOW, the device will use timing from the externally supplied H:V:F or CEA-861 timing signals, dependent on the state of the TIM_861 pin. When DETECT_TRS = HIGH, the device will extract timing from TRS signals embedded in the supplied video stream.
F10	RSET	Analog	Input	An external 1% resistor connected to this input is used to set the SDO/$\overline{\text{SDO}}$ output amplitude.
G1, H10	IO_VDD	Non Synchronous	Input Power	Power supply connection for digital I/O buffers. Connect to +3.3V or +1.8V DC digital.
G2, H9	IO_GND	Non Synchronous	Input Power	Ground connection for digital I/O buffers. Connect to digital GND.
G3	TIM_861	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select external CEA-861 timing mode. When DETECT_TRS = LOW and TIM_861 = LOW, the device will use externally supplied H:V:F timing signals. When DETECT_TRS = LOW and TIM_861 = HIGH, the device will use externally supplied HSYNC, VSYNC, DE timing signals. When DETECT_TRS = HIGH, the device will extract timing from TRS signals embedded in the supplied video stream.
G4	20bit/$\overline{\text{10bit}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select the input data bus width.
G5	DVB_ASI	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When set HIGH, the device is configured for the transmission of DVB-ASI data in SD mode (SD/$\overline{\text{HD}}$ = HIGH). When set LOW, the device will not support the encoding of DVB-ASI data. NOTE: When operating in DVB-ASI mode the SD/$\overline{\text{HD}}$ pin must be set HIGH and $\overline{\text{SMPTE_BYPASS}}$ must be set LOW.
G6	$\overline{\text{SMPTE_BYPASS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable/disable all forms of encoding/decoding, scrambling and EDH insertion. When set LOW, the device will operate in data through mode (DVB_ASI = LOW), or in DVB-ASI mode (DVB_ASI = HIGH). No SMPTE scrambling will take place and none of the I/O processing features of the device will be available when $\overline{\text{SMPTE_BYPASS}}$ is set LOW. When set HIGH, the device will perform SMPTE scrambling and I/O processing.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
G7	IOPROC_EN/$\overline{\text{DIS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable I/O processing features. When set HIGH, the following I/O processing features of the device are enabled: • EDH Packet Generation and Insertion (SD-only) • SMPTE 352M Packet Generation and Insertion • ANC Data Checksum Calculation • ANC Data Insertion • Line-based CRC Generation and Insertion (HD-only) • Line Number Generation and Insertion (HD-only) • TRS Generation and Insertion • Illegal Code Remapping To enable a subset of these features, set IOPROC_EN/$\overline{\text{DIS}}$ = HIGH and disable the individual feature(s) in the IOPROC_DISABLE register accessible via the host interface. When set LOW, the I/O processing features of the device are disabled, and can not be enabled by changing the settings in the IOPROC_DISABLE register.
G8	$\overline{\text{RESET}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to reset the internal operating conditions to default settings and to reset the JTAG test sequence. Normal Mode (JTAG/$\overline{\text{HOST}}$ = LOW) When set LOW, all functional blocks will be set to default conditions and all input and output signals become high impedance including the serial digital outputs SDO and $\overline{\text{SDO}}$. When set HIGH, normal operation of the device resumes 10usec after the low to high transition of the $\overline{\text{RESET}}$ signal. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) When set LOW, all functional blocks will be set to default and the JTAG test sequence will be held in reset. When set HIGH, normal operation of the JTAG test sequence resumes.
H3	$\overline{\text{ANC_BLANK}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable ANC data blanking. When set LOW, the HANC and VANC data is mapped to the appropriate blanking levels.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
H4	LOCKED	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. This signal is set HIGH by the device when the internal PLL has achieved lock to the supplied PCLK signal. This pin is set LOW by the device under all other conditions. IO_VDD = 3.3V Drive Strength = 8mA IO_VDD = 1.8V Drive Strength = 4mA
H5, H6, H7, J4, J5, J6, J7, K4, K5, K6, K7	RSV	Non Synchronous	Input	Reserved. Do not connect.
H8	JTAG/$\overline{\text{HOST}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select JTAG Test Mode or Host Interface Mode. When set HIGH, $\overline{\text{CS}}$_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK are configured for JTAG boundary scan testing. When set LOW, $\overline{\text{CS}}$_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK are configured as Gennum Serial Peripheral Interface (GSPI) pins for normal host interface operation.
J9	SDOUT_TDO	Synchronous with SCLK_TCK	Output	COMMUNICATION SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Output / Test Data Output Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) This pin operates as the host interface serial output, used to read status and configuration information from the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) This pin is used to shift test results and operates as the JTAG test data output, TDO. NOTE: If the host interface is not being used leave this pin unconnected. Drive Strength: IO_VDD = 3.3V = 12mA IO_VDD = 1.8V = 4mA
J10	SCLK_TCK	Non Synchronous	Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Clock / Test Clock. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) SCLK_TCK operates as the host interface burst clock, SCLK. Command and data read/write words are clocked into the device synchronously with this clock. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) This pin is the TEST MODE START pin, used to control the operation of the JTAG test clock, TCK. NOTE: If the host interface is not being used, tie this pin HIGH.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
K9	CS_TMS	Synchronous with SCLK_TCK	Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Chip Select / Test Mode Start. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) $\overline{\text{CS}}$_TMS operates as the host interface chip select, $\overline{\text{CS}}$, and is active LOW. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) $\overline{\text{CS}}$_TMS operates as the JTAG test mode start, TMS, used to control the operation of the JTAG test, and is active HIGH. NOTE: If the host interface is not being used, tie this pin HIGH.
K10	SDIN_TDI	Synchronous with SCLK_TCK	Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data In / Test Data Input Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) This pin operates as the host interface serial input, SDIN, used to write address and configuration information to the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) This pin is used to shift and operates as the JTAG test data input, TDI. NOTE: If the host interface is not being used, tie this pin HIGH.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Core (CORE_VDD)	-0.3V to +2.1V
Supply Voltage, Analog 1.8V (PD_VDD)	-0.3V to +2.1V
Supply Voltage, I/O (IO_VDD)	-0.3V to +3.6V
Supply Voltage, Analog 3.3V (CP_VDD, CD_VDD)	-0.3V to +3.6V
Input Voltage Range (PCLK, DIN)	-0.5V to IO_VDD+0.25V
Input Voltage Range (VCO, CP_RES, LF, RSET)	-0.5V to +3.6V
Input Voltage Range (All other pins)	-0.5V to +5.25V
Ambient Operating Temperature	$-40°C \leq T_A \leq 95°C$
Storage Temperature	$-40°C \leq T_{STG} \leq 125°C$
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	4000V
ESD Sensitivity, MM (JESD22-A115)	200V

NOTES:

1. Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Operating Temperature Range, Ambient	T_A	–	-20	25	85	°C	
Supply Voltage, Digital Core	CORE_VDD	–	1.71	1.8	1.89	V	
Supply Voltage, Phase Detector	PD_VDD	–	1.71	1.8	1.89	V	
Supply Voltage, Charge Pump	CP_VDD	–	3.13	3.3	3.47	V	
Supply Voltage, Cable Driver	CD_VDD	–	3.13	3.3	3.47	V	
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	
Supply Voltage, Digital I/O	IO_VDD	3.3V mode	3.13	3.3	3.47	V	

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
External VCO Power Supply Voltage (VCO_VDD)			2.375	2.5	2.625	V	1
+1.8V Supply Current	I_{1V8}	10/20bit HD	–	109	130	mA	2,4
		10/20bit SD	–	104	120	mA	2,4
		DVB_ASI	–	100	120	mA	2,4
+3.3V Supply Current	I_{3V3}	10/20bit HD	–	74	86	mA	3,4
		10/20bit SD	–	74	86	mA	3,4
		DVB_ASI	–	74	86	mA	3,4
Total Device Power	P_D	10/20bit HD	–	440	540	mW	4
		10/20bit SD	–	430	530	mW	4
		DVB_ASI	–	424	510	mW	4
		Reset	–	310	–	mW	–
		Standby	10	125	–	mW	5

Table 2-3: DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Digital I/O							
Input Logic LOW	V_{IL}	3.3V or 1.8V operation	–	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V_{IH}	3.3V or 1.8V operation	0.7 x IO_VDD	–	–	V	–
Output Logic LOW	V_{OL}	1.8V mode	–	–	0.3	V	–
		3.3V mode	–	–	0.4	V	–
Output Logic HIGH	V_{OH}	1.8V mode	1.4	–	–	V	–
		3.3V mode	2.4	–	–	V	–
Output							
Output Common Mode Voltage	V_{CMOUT}	75Ω load, RSET=750Ω SD and HD mode	–	CD_VDD - ΔV_{SDD}	–	V	–

NOTES

1. VCO_VDD guaranteed only when GO1555 is connected.
2. Sum of all 1.8V supplies.
3. Sum of all 3.3V supplies.
4. IO_VDD = 3.3V. When IO_VDD = 1.8V, the current/power consumption is lower by up to 5mA/10mW.
5. See 4.6 Standby Mode for details.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Device Latency	–	–	–	–	27	PCLK	–
	–	DVB-ASI	–	–	15	PCLK	–
Reset Pulse Width	t_{reset}	–	10	–	–	ms	1
Parallel Input							
Parallel Clock Frequency	f_{PCLK}	–	13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC_{PCLK}	–	40	–	60	%	–
Input Data Setup Time	t_{su}	50% levels; 3.3V or 1.8V operation	2	–	–	ns	4
Input Data Hold Time	t_{ih}		0.8	–	–	ns	4
Serial Digital Output							
Serial Output Data Rate	DR_{SDO}	–	–	1.485	–	Gb/s	–
		–	–	1.485/1.001	–	Gb/s	–
		–	–	270	–	Mb/s	–
Serial Output Swing	V_{SDD}	RSET = 750Ω 75Ω load	750	800	850	mVp-p	–

Table 2-4: AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Output Rise/Fall Time 20% ~ 80%	trf_{SDO}	HD mode	–	120	270	ps	–
	trf_{SDO}	SD mode	400	660	800	ps	–
Mismatch in rise/fall time	$\Delta t_r, \Delta t_f$	–	–	–	35	ps	–
Duty Cycle Distortion	–	–	–	1	5	%	5
Overshoot	–	SD/$\overline{HD}$=0	–	5	10	%	5
	–	SD/$\overline{HD}$=1	–	3	8	%	5
Output Return Loss	ORL	5 MHz - 1.485 GHz	–	18	–	dB	6
Serial Output Intrinsic Jitter	t_{OJ}	Pseudorandom and SMPTE Colour Bars HD signal	–	35	80	ps	2
	t_{OJ}	Pseudorandom and SMPTE Colour Bars SD signal	–	100	200	ps	3
GSPI							
GSPI Input Clock Frequency	f_{SCLK}	50% levels 3.3V or 1.8V operation	–	–	10	MHz	–
GSPI Input Clock Duty Cycle	DC_{SCLK}		40	50	60	%	–
GSPI Input Data Setup Time	–		1.5	–	–	ns	–
GSPI Input Data Hold Time	–		1.5	–	–	ns	–
GSPI Output Data Hold Time	–	15pF load	1.5	–	–	ns	–
CS low before SCLK rising edge	–	50% levels 3.3V or 1.8V operation	1.5	–	–	ns	–
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	–	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	–
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	–	50% levels 3.3V or 1.8V operation	148.4	–	–	ns	–
CS high after SCLK rising edge	–	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	–

NOTES:

1. See 'Device Reset' on page 58, Figure 4-17.
2. Alignment Jitter = measured from 100kHz to 148.5MHz
3. Alignment Jitter = measured from 1kHz to 27MHz
4. Input setup and hold time is dependent on the rise and fall time on the parallel input. Parallel clock and data with rise time or fall time greater than 500ps require larger setup and hold times.
5. Single Ended into 75Ω external load.
6. ORL depends on board design. The GS1572 achieves this specification on Gennum's evaluation boards.

3. Input/Output Circuits

All resistors in ohms, all capacitors in farads, unless otherwise shown.

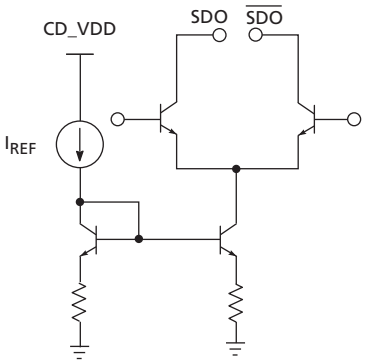


Figure 3-1: Differential Output Stage (SDO/$\overline{\text{SDO}}$)

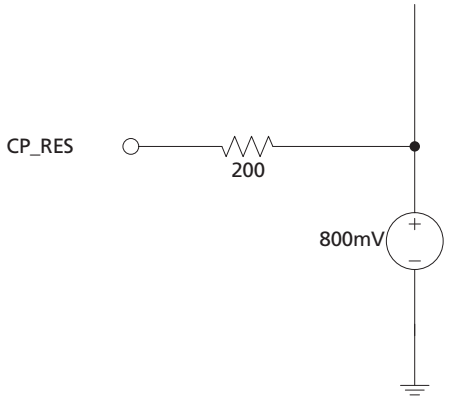


Figure 3-2: Charge Pump Current Setting Resistor (CP_RES)

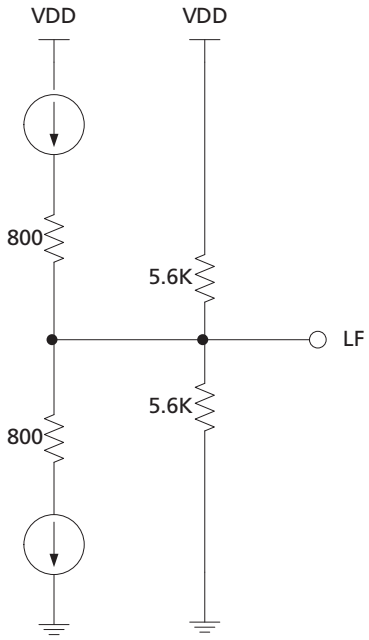


Figure 3-3: PLL Loop Filter

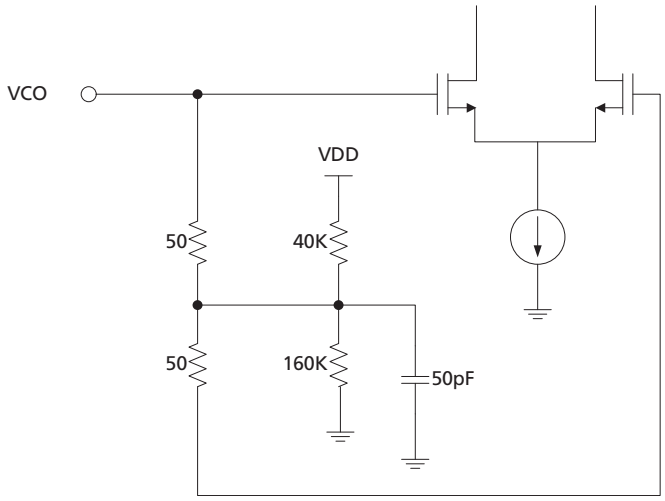


Figure 3-4: VCO Input

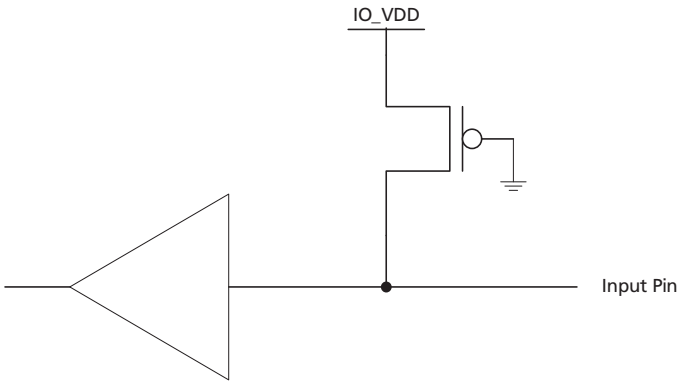


Figure 3-5: Digital Input Pin with Weak Pull Up(>33kΩ)
(PCLK, DIN[19:0])

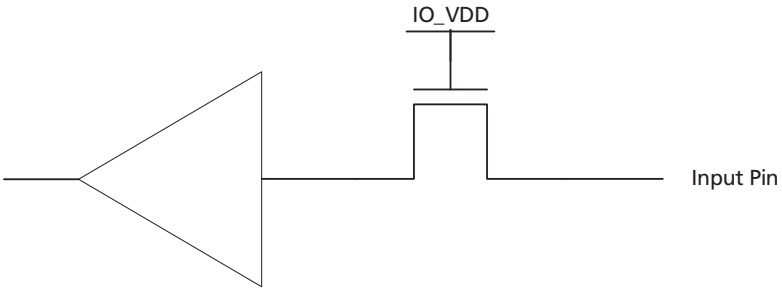


Figure 3-6: 5V Tolerant Input Pin (All Other Input Pins)

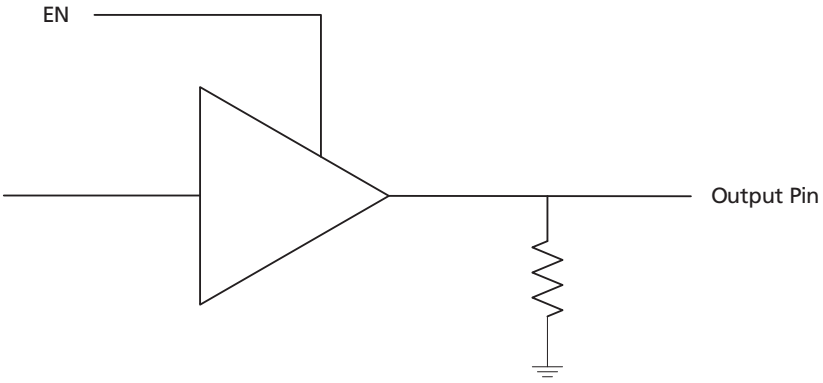


Figure 3-7: Digital Output Pin with High Impedance Mode
(LOCKED, SDOUT_TDO)

4. Detailed Description

4.1 Functional Overview

The GS1572 is a multi-rate Serializer with an Integrated Cable Driver. When used in conjunction with the external GO1555 Voltage Controlled Oscillator, a transmit solution at 1.485Gb/s, 1.485/1.001Gb/s or 270Mb/s is realized.

The device has three basic modes of operation that must be set through external device pins: SMPTE mode, DVB-ASI mode and Data-Through mode.

In SMPTE mode, the device will accept 10-bit multiplexed or 20-bit demultiplexed SMPTE compliant data at both HD and SD signal rates. By default, the device's additional processing features will be enabled in this mode.

In DVB-ASI mode, the GS1572 will accept an 8-bit parallel DVB-ASI compliant transport stream on DIN[17:10]. The serial output data stream will be 8b/10b encoded with stuffing characters added as per the standard.

Data-Through mode allows for the serializing of data not conforming to SMPTE or DVB-ASI streams. No additional processing will be done in this mode.

In Standby mode, the device power consumption will be reduced.

The Serial Digital Output features a high-impedance mode and adjustable signal swing. The output slew rate is automatically set by the SD/$\overline{\text{HD}}$ pin setting.

GS1572 provides several data processing functions including generic ANC insertion, SMPTE 352M and EDH data packet generation and insertion, automatic video standards detection, and TRS, CRC, ANC data checksum, and line number calculation and insertion. These features are all enabled/disabled collectively by using the external IO processing pin, but may be individually disabled via internal registers accessible through the GSPI Host Interface.

Finally, the GS1572 contains a JTAG interface for boundary scan test implementations.

4.2 Parallel Data Inputs

Data is clocked into the device on the rising edge of PCLK as shown in Figure 4-1.

The input data format is defined by the setting of the external SD/$\overline{\text{HD}}$, $\overline{\text{SMPTE_BYPASS}}$, and DVB_ASI pins and may be presented in 10-bit or 20-bit format. The input data bus width is controlled by the 20bit/$\overline{\text{10bit}}$ input pin.

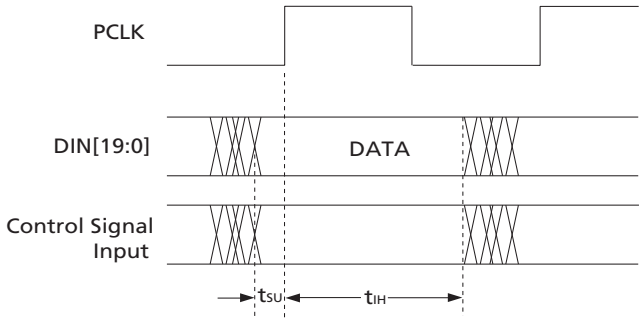


Figure 4-1: PCLK to Data Timing

4.2.1 Parallel Input in SMPTE Mode

When the device is operating in SMPTE mode, see SMPTE Mode on page 26, both SD and HD data may be presented to the input bus in either multiplexed or demultiplexed form depending on the setting of the 20bit/$\overline{10bit}$ input pin.

In 20-bit mode, (20bit/$\overline{10bit}$ = HIGH), the input data format should be word aligned, demultiplexed Luma and Chroma data. Luma words should be presented on DIN[19:10] while Chroma words should be presented on DIN[9:0].

In 10-bit mode, (20bit/$\overline{10bit}$ = LOW), the input data format should be word aligned, multiplexed Luma and Chroma data. The data should be presented on DIN[19:10]. DIN[9:0] will be high-impedance in this mode.

4.2.2 Parallel Input in DVB-ASI Mode

When operating in DVB-ASI mode, see DVB-ASI mode on page 32, the GS1572 must be set to 10-bit operation mode by setting the 20bit/$\overline{10bit}$ pin LOW.

The device will accept 8-bit data words on DIN[17:10] such that DIN17 = HIN is the most significant bit of the encoded transport stream data and DIN10 = AIN is the least significant bit.

In addition, DIN19 and DIN18 will be configured as the DVB-ASI control signals INSSYNCIN and KIN respectively. See DVB-ASI mode on page 32 for a description of these DVB-ASI specific input signals.

DIN[9:0] will have a logic level HIGH in DVB-ASI mode.

4.2.3 Parallel Input in Data-Through Mode

When operating in Data-Through mode, see Data-Through Mode on page 33, the GS1572 passes data from the parallel input bus to the serial output without performing any encoding or scrambling. The input data bus width is controlled by the setting of the 20bit/$\overline{10bit}$ pin.

4.2.4 Parallel Input Clock (PCLK)

The frequency of the PCLK input signal required by the GS1572 is determined by the input data format. Table 4-1 below lists the possible input signal formats and their corresponding parallel clock rates. Note that DVB-ASI input will only be in 10-bit format, when setting the 20bit/$\overline{10bit}$ pin LOW.

Table 4-1: Parallel Data Input Format

Input Data Format	DIN [19:10]	DIN [9:0]	PCLK	Control Signals			
				20bit/ $\overline{10bit}$	SD/ $\overline{HD}$	$\overline{SMPTE_BYPASS}$	DVB_ASI
SMPTE MODE							
20-bit DEMULTIPLEXED SD	LUMA	CHROMA	13.5MHz	HIGH	HIGH	HIGH	LOW
10-bit MULTIPLEXED SD	LUMA/ CHROMA	HIGH IMPEDANCE	27MHz	LOW	HIGH	HIGH	LOW
20-bit DEMULTIPLEXED HD	LUMA	CHROMA	74.25 or 74.25/ 1.001MHz	HIGH	LOW	HIGH	LOW
10-bit MULTIPLEXED HD	LUMA/ CHROMA	HIGH IMPEDANCE	148.5 or 148.5/ 1.001MHz	LOW	LOW	HIGH	LOW
DVB-ASI MODE							
10-bit DVB-ASI	DVB-ASI DATA	HIGH IMPEDANCE	27MHz	LOW	HIGH	LOW	HIGH
				LOW	HIGH	LOW	HIGH
DATA-THROUGH MODE							
20-bit SD	DATA	DATA	13.5MHz	HIGH	HIGH	LOW	LOW
10-bit SD	DATA	HIGH IMPEDANCE	27MHz	LOW	HIGH	LOW	LOW
20-bit HD	DATA	DATA	74.25 or 74.25/ 1.001MHz	HIGH	LOW	LOW	LOW
10-bit HD	DATA	HIGH IMPEDANCE	148.5 or 148.5/ 1.001MHz	LOW	LOW	LOW	LOW

4.3 SMPTE Mode

The GS1572 operates in SMPTE mode when the $\overline{\text{SMPTE_BYPASS}}$ pin is set HIGH and the DVB_ASI pin is set LOW.

In this mode, the parallel data will be scrambled according to SMPTE 259M or 292M, and NRZ-to-NRZI encoded prior to serialization.

4.3.1 HVF Timing

In SMPTE mode, the GS1572 can automatically detect the video standard and generate all internal timing signals. The total line length, active line length, total number of lines per field/frame and total active lines per field/frame are calculated for the received parallel video.

When DETECT_TRS is LOW, the video standard and timing signals are based on the externally supplied H_Blanking, V_Blanking, and F_Digital signals. These signals go to the H/HSYNC, V/VSYNC, and F/DE pins respectively. When DETECT_TRS is HIGH, the video standard timing signals will be extracted from the embedded TRS ID words in the parallel input data. Both 8-bit and 10-bit TRS code words will be identified by the device.

NOTE: I/O processing must be enabled for the device to remap 8-bit TRS words to the corresponding 10-bit value for transmission. See Section 4.8.4.2 for more information.

The GS1572 determines the video standard by timing the Horizontal and Vertical reference information supplied at the H/HSYNC, V/VSYNC, and F/DE input pins, or contained in the TRS ID words of the received video data. Therefore, full synchronization to the received video standard requires one complete video frame. Once synchronization has been achieved, the GS1572 will continue to monitor the received TRS timing or the supplied H, V, and F timing information to maintain synchronization. GS1572 will lose all timing information immediately following loss of H, V and F.

The H signal timing should also be configured via the H_CONFIG bit of the internal IOPROC_DISABLE register as either active line based blanking or TRS based blanking. See Packet Generation and Insertion on page 39.

Active line based blanking is enabled when the H_CONFIG bit is set LOW. In this mode, the H input should be HIGH for the entire horizontal blanking period, including the EAV and SAV TRS words. This is the default H timing used by the device.

The timing of these signals is shown in Figure 4-2.

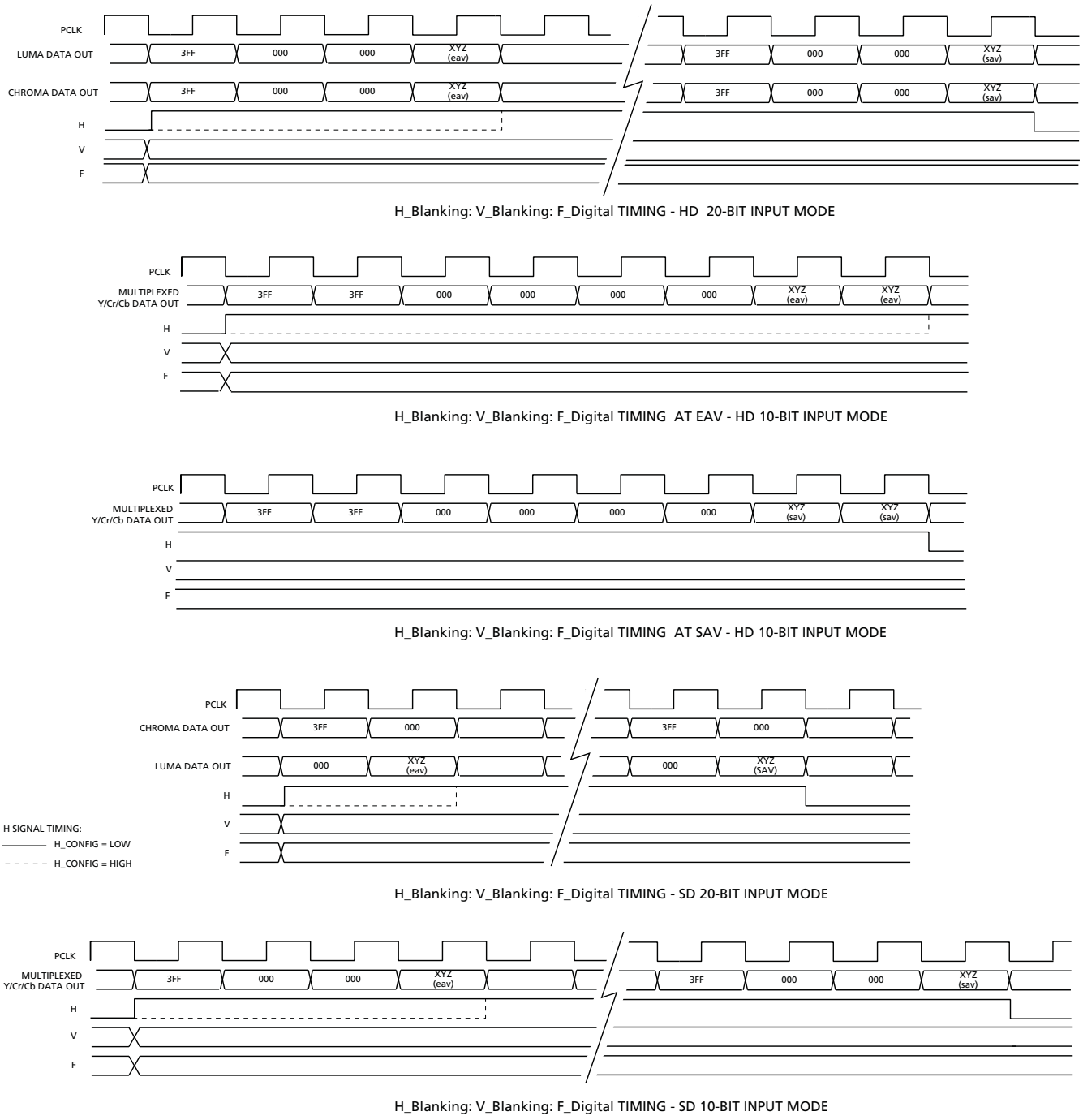


Figure 4-2: H_Blanking, V_Blanking, F_Digital Timing

4.3.2 CEA 861 Timing

The GS1572 extracts timing information from externally provided HSYNC, VSYNC, and DE signals when CEA 861 timing mode is selected by setting DETECT_TRS = LOW and TIM_861 = HIGH.

Horizontal sync (H), Vertical sync (V), and Data Enable (DE) timing must be provided via the H/HSYNC, V/VSYNC and F/DE input pins. The Host Interface register bit H_CONFIG will be ignored in the CEA 861 input timing mode.

The GS1572 will determine the EIA/CEA-861 standard and embed EAV and SAV TRS words in the output serial video stream.

Video standard detection is not dependent on the HSYNC pulse width or the VSYNC pulse width and therefore the GS1572 will tolerate non-standard pulse widths. In addition, the device can compensate for up to ±1 PCLK cycle of jitter on VSYNC with respect to HSYNC and sample VSYNC correctly.

NOTE 1: The period between the leading edge of the HSYNC pulse and the leading edge of Data Enable (DE) must follow the timing requirements described in the EIA/CEA-861 specification. The GS1572 embeds TRS words according to this timing relationship to maintain compatibility with the corresponding SMPTE standard.

NOTE 2: When CEA 861 standards 6 & 7 [720(1440)x480i] are presented to the GS1572, the device will embed TRS words corresponding to the timing defined in SMPTE 125M to maintain SMPTE compatibility.

CEA 861 standards 6 & 7 [720(1440)x480i] define the active area on lines 22 to 261 and 285 to 524 inclusive (240 active lines per field). SMPTE 125M defines the active area on lines 20 to 263 and 283 to 525 inclusive (244 lines on field 1; 243 lines on field 2).

Therefore, in the first field, the GS1572 adds two active lines above and two active lines below the original active image. In the second field it adds two lines above and one line below the original active image.

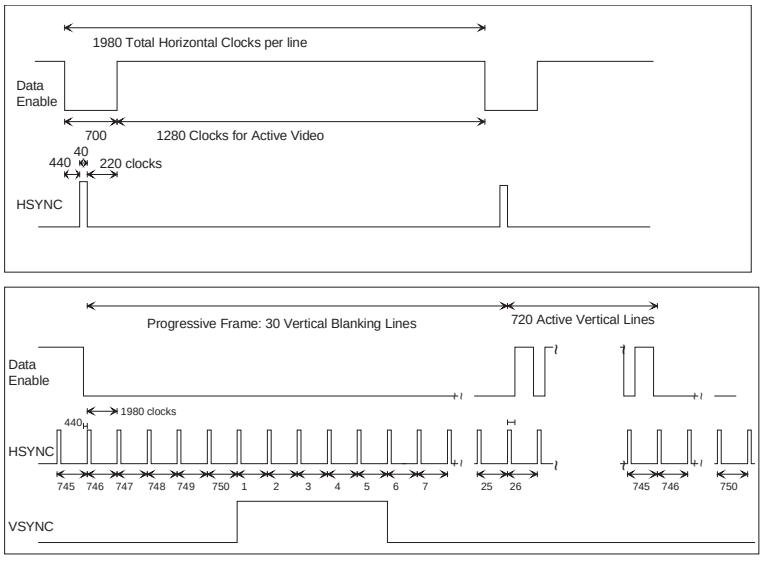


Figure 4-3: HSYNC:VSYNC:DE Input Timing 1280 x 720p @ 59.94/60

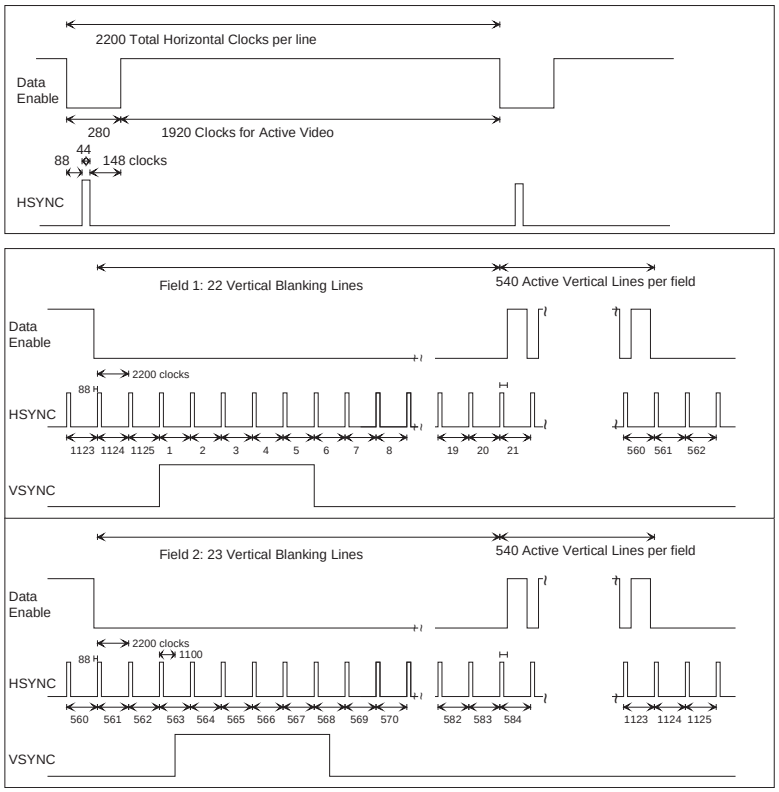


Figure 4-4: HSYNC:VSYNC:DE Input Timing 1920 x 1080i @ 59.94/60

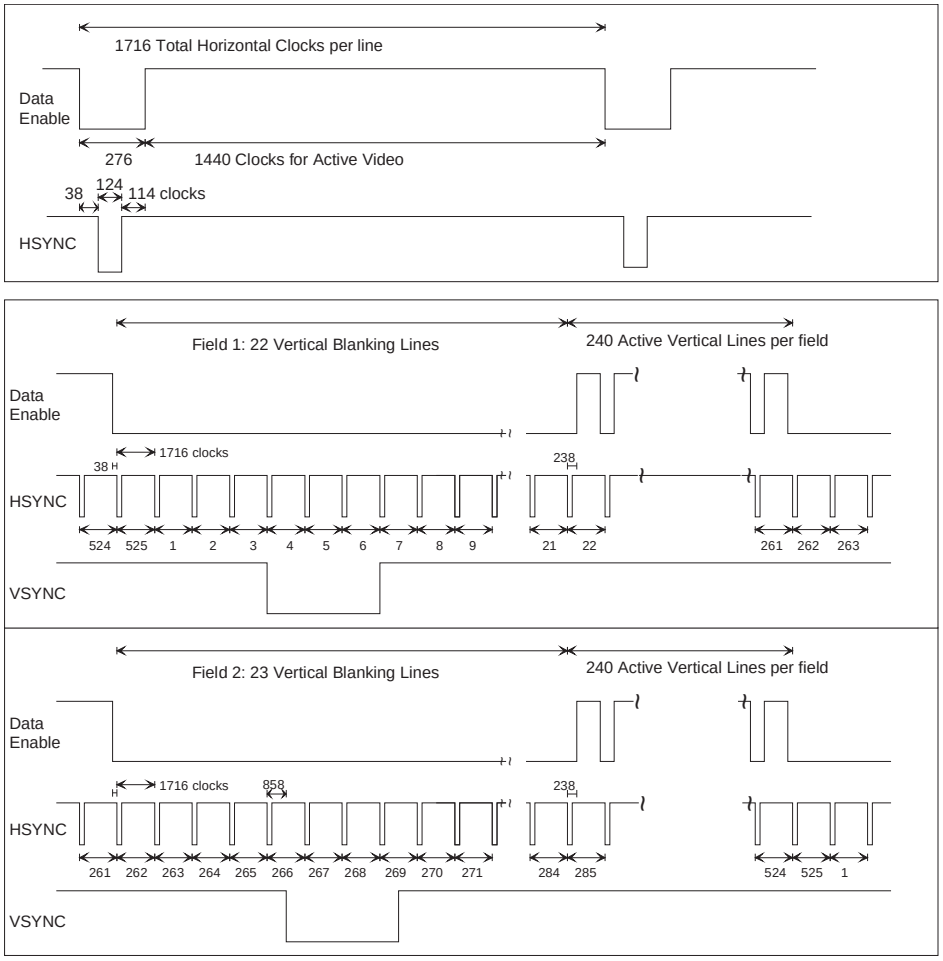


Figure 4-5: HSYNC:VSYNC:DE Input Timing 720 (1440) x 480i @ 59.94/60

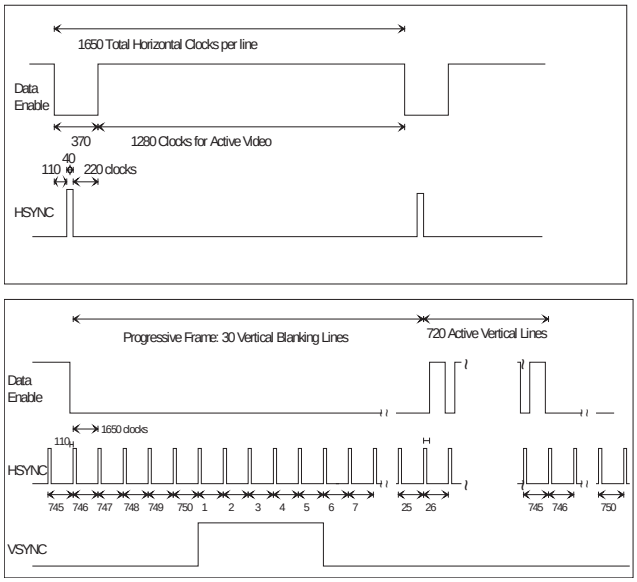


Figure 4-6: HSYNC:VSYNC:DE Input Timing 1280 x 720p @ 50

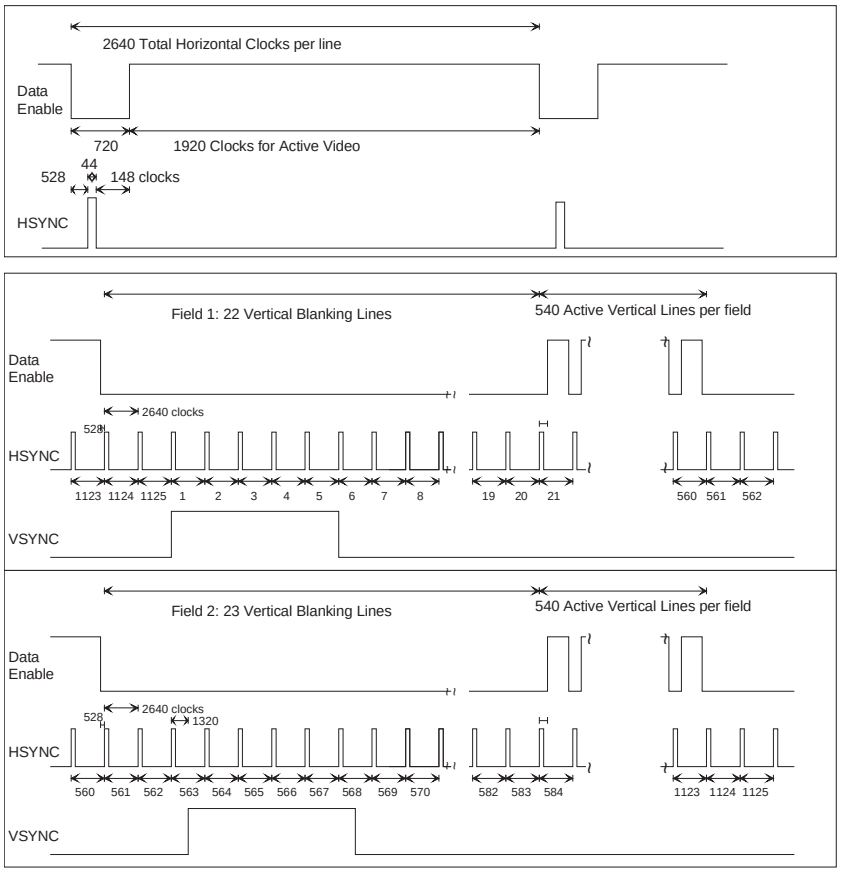


Figure 4-7: HSYNC:VSYNC:DE Input Timing 1920 x 1080i @ 50

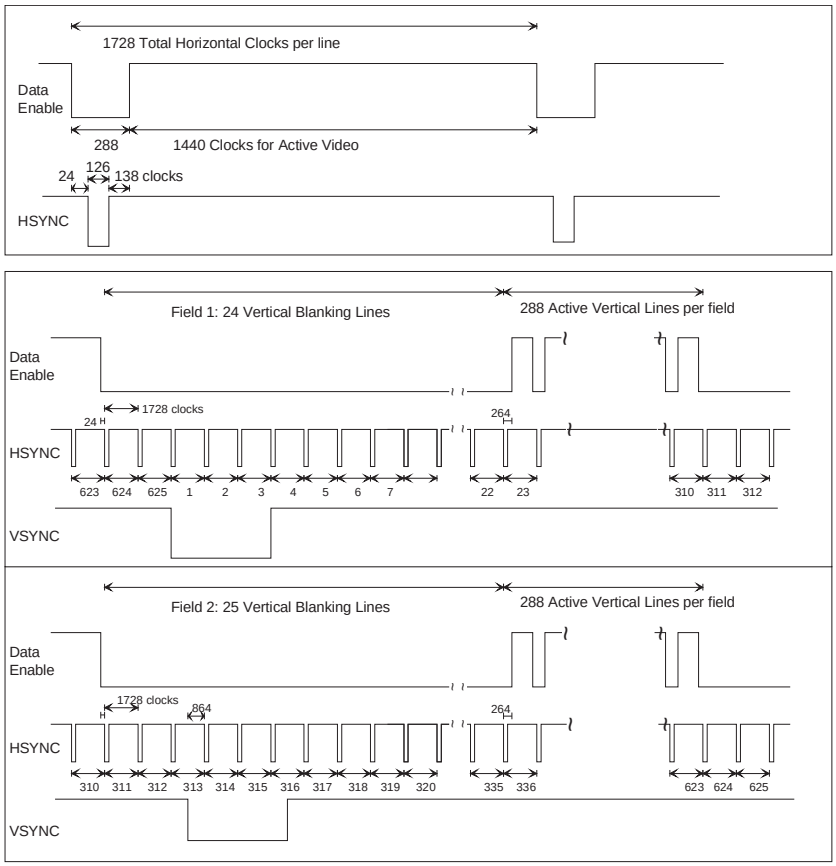


Figure 4-8: HSYNC:VSYNC:DE Input Timing 720 (1440) x 576 @ 50

4.4 DVB-ASI mode

The GS1572 operates in DVB-ASI mode when the $\overline{\text{SMPTE_BYPASS}}$ pin is set LOW and the DVB_ASI and SD/$\overline{\text{HD}}$ pins are set HIGH.

In this mode, all SMPTE processing functions are disabled, and the 8-bit transport stream data will be 8b/10b encoded prior to serialization.

4.4.1 Control Signal Inputs

In DVB-ASI mode, the DIN19 and DIN18 pins are configured as DVB-ASI control signals INSSYNCIN and KIN respectively.

When INSSYNCIN is set HIGH, the device will insert K28.5 sync characters into the data stream. This function is used in system implementations where the GS1572 is preceded by an external data FIFO. Parallel DVB-ASI data may be clocked into the FIFO at some rate less than 27MHz. The INSSYNCIN input may then be connected to the FIFO empty signal, providing a means of padding the data transmission rate to 27MHz. See Figure 4-9.

NOTE: 8b/10b encoding will take place after K28.5 sync character insertion.

KIN should be set HIGH whenever the parallel data input is to be interpreted as any special character defined by the DVB-ASI standard (including the K28.5 sync character). This pin should be set LOW when the input is to be interpreted as data.

NOTE: When operating in DVB-ASI mode, DIN[9:0] will have a Logic Level HIGH.

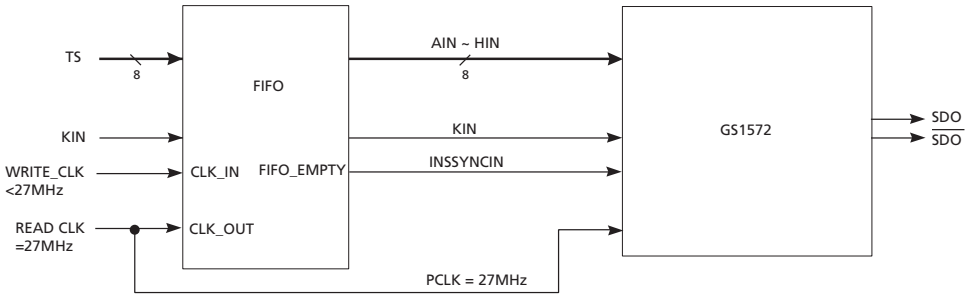


Figure 4-9: DVB-ASI FIFO Implementation using the GS1572

4.5 Data-Through Mode

The GS1572 may be configured to operate as a simple parallel-to-serial converter. In this mode, the device passes data to the serial output without performing any scrambling or encoding.

Data-through mode is enabled only when both the $\overline{\text{SMPTE_BYPASS}}$ and DVB_ASI pins are set LOW.

4.6 Standby Mode

In standby mode, the power consumption of the GS1572 is reduced to 125mW. Standby mode is enabled when the STANDBY pin is set HIGH. Once the STANDBY pin is set HIGH, it may take up to 50ms for power reduction to take place.

In this mode, the serial output pins are set to high-impedance and the GS1572 loses lock to the reference input PCLK. While in Standby mode, the programmed register values are retained. However, no registers can be accessed for reading or writing via the GSPI port. No write bits will be captured and all read functions will return a value of zero.

The power in standby mode can be further reduced through two means:

1. Eliminate activity on all parallel data and clock inputs. This can be achieved by setting the parallel data and clock HIGH or not driving them. Setting the parallel inputs to LOW is not recommended, as it will result in a smaller power saving.
2. Remove the 3.3V supply to the CD_VDD pin of the device.

The standby power consumption under various conditions is shown in Table 4-2: Standby Power Consumption.

In order to return to normal operation from standby mode, the STANDBY pin must be set to LOW. Once normal operation mode is resumed, the GS1572 will re-lock to the

reference PCLK. The recovery time from standby mode is the same as initial power-up but no reset is required. Once GS1572 re-locks to the reference PCLK, operation is resumed according to the configuration held before entering standby mode.

Table 4-2: Standby Power Consumption

Standby Condition	Typical Power Consumption (mW)
STANDBY asserted	125
STANDBY asserted Parallel data and clock inactive	100
STANDBY asserted 3.3V supply removed from CD_VDD	35
STANDBY asserted Parallel data and clock inactive 3.3V supply removed from CD_VDD	<10

4.7 Ancillary Data Insertion

Horizontal or vertical ancillary data words may be inserted on up to four different lines per video frame. In order to insert HANC data, the ANC_TYPE bit in the Host Interface, must be set LOW. VANC data can be inserted by setting the ANC_TYPE bit in the Host Interface HIGH. By default, at power up, HANC data insertion is selected.

The user must write the ancillary data words to be inserted, the line number for the insertion, and the total number of words to be inserted to the designated registers in the host interface. At power up, or after system reset, all ANC data insertion line numbers and total number of words default to zero.

All data words including the ancillary packet ADF, DBN, DC, DID, SDID, and CHECKSUM (placeholder) must be provided. The user provided CHECKSUM word is a placeholder. The correct value will be calculated and inserted automatically.

Two modes of operation are provided; Separate Line mode and Concatenated mode. By default, at power up or after system reset, Separate Line operating mode is selected.

The GS1572 ancillary data insertion provides no error checking or correction. The provided ancillary data must be fully SMPTE compliant.

The PACKET_MISSED bit in the Host Interface is set if:

- An ancillary data packet is only partially inserted because there is no more free space in the HANC or VANC region of the selected line
- An ancillary data packet is not inserted at all because there is no free space in the HANC or VANC region of the selected line
- The number of words to insert programmed through the Host Interface is greater than the maximum allowed for the operating mode (128 in separate line mode or 512 in concatenated line mode). Under this condition, the bit will be set once the maximum number has been reached

This bit is cleared once per frame on the rising edge of V or when it is read through the Host Interface.

In SD mode, the ancillary data packets are inserted into the multiplexed YCbCr video stream. In HD mode, by default ancillary data packets will be inserted into the Luma channel. Insertion in the Chroma channel may be selected via the Host Interface. Ancillary data insertion in the Luma and Chroma channels can be selected on a per line basis.

Ancillary data insertion only takes place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is set HIGH, $\overline{\text{SMPTE_BYPASS}}$ is set HIGH, and the ANC_INS bit in the IOPROC_DISABLE register is set LOW.

NOTE 1: It is good practice to program the ancillary data words prior to programming the line number and number of words. Ancillary data insertion only begins once the line number and number of words are set to a non-zero value. Therefore, this practice ensures that no data is written to the ANC space before the programming is complete. As such, no unintended data is written to the ANC space even if the programmed line number is reached before the programming is complete. Also, read/write conflicts are avoided. It is recommended to finish programming all the data at least 1 line prior to where ancillary data insertion is to begin.

NOTE 2: In both Separate Line mode and Concatenated mode, more than one ancillary data packet may be inserted per line. The user provided ancillary data packets must contain a checksum place holder word. The correct checksum for each packet will then be re-calculated and inserted by GS1572. The total number of words for all the provided ancillary data packets with checksum should not exceed 128 in Separate Line mode and 512 in Concatenated mode.

4.7.1 Ancillary Data Insertion Operating Mode

4.7.1.1 Separate Line Mode

In Separate Line mode, it is possible to insert horizontal or vertical ancillary data on up to four lines per video frame. For each of the four video lines, up to 128 8-bit HANC or VANC data words can be inserted. Separate Line mode is selected by setting the ANC_INS_MODE bit in the Host Interface LOW. By default, at power up, Separate Line mode is selected.

The non-zero video line numbers on which to insert the ancillary data, the ancillary data type (HANC or VANC), and the total number of words to insert per line must be provided via the Host Interface. At power up, or after system reset, all ancillary data insertion line numbers and total number of words default to zero.

If the total number of data words specified per line exceeds 128 only the first 128 data words will be inserted.

The device automatically converts the provided 8-bit data words into the 10-bit data, formatted according to SMPTE 291M prior to insertion.

4.7.1.2 Concatenated Mode

In Concatenated mode, it is possible to insert up to 512 8-bit horizontal or vertical ancillary data words on one line per video frame. Concatenated line mode can be selected by setting the ANC_INS_MODE bit in the host interface HIGH. By default, at power up, Separate Line mode is selected.

The non-zero video line number on which to insert the ancillary data, the ancillary data type (HANC or VANC), and the total number of words to insert must be provided via the Host Interface. At power up, or after system reset, the ancillary data insertion line number and total number of words default to zero.

If the total number of data words specified exceeds 512 only the first 512 data words will be inserted.

The device automatically converts the provided 8-bit data words into the 10-bit data formatted according to SMPTE 291M prior to insertion.

4.7.2 HANC Insertion

By default, at power up or after system reset, all ancillary data is inserted in the HANC space. Data is inserted contiguously starting at the TRS EAV or the first available location following any pre-existing ancillary data packets. Data insertion terminates when all provided data words have been inserted or at the start of the TRS SAV code, whichever occurs first. If termination occurs before all words have been inserted, the PACKET_MISSED bit will be set in the host interface.

NOTE 1: EDH packet insertion in SD mode occurs following ancillary data insertion. Thus, any HANC data inserted on the same line as the EDH packet may be overwritten during EDH insertion. When HANC data is inserted on an EDH line, the PACKET_MISSED bit may be erroneously set, even though the ancillary data packet has been inserted correctly.

NOTE 2: HANC space ancillary data headers undergo 8-bit to 10-bit remapping. This means that when the 8 MSBs are all zero, the value gets mapped to 000 and when the 8 MSBs are all 1, the value gets mapped to 3FF. (i.e. 000, 001, 002, 003 –—> 000 and 3FE, 3FD, 3FC –—> 3FF)

4.7.3 VANC Insertion

Ancillary data insertion into the VANC space can be selected via the Host Interface. Data is inserted contiguously starting at the TRS SAV or the first available location following any pre-existing ancillary data packets. Data insertion terminates when all provided data words have been inserted or at the start of the TRS EAV code, whichever occurs first. If termination occurs before all words have been inserted, the PACKET_MISSED bit will be set in the host interface.

NOTE: When ancillary data is inserted into the active region of the video raster using the VANC feature, if the ILLEGAL_REMAP in the IOPROC_DISABLE register bit is set to zero, then the ADFs are remapped to '004 | 3FB | 3FB' and the downstream devices will not detect the ancillary data packets.

4.8 Additional Processing Functions

The GS1572 incorporates additional data processing which is available in SMPTE mode only, see SMPTE Mode on page 26.

4.8.1 ANC Data Blanking

The horizontal and vertical ancillary spaces of the input video may be 'blanked' by the GS1572. In this mode, the TRS words and active video will be preserved. Any additional processing functions, including ancillary data insertion, occur after blanking and will be present in the output video stream.

This function is enabled by setting the $\overline{\text{ANC_BLANK}}$ pin LOW.

4.8.2 Automatic Video Standard Detection

The GS1572 can detect the input video standard by using the timing parameters extracted from the received TRS ID words, the supplied H_Blanking, V_Blanking, and F_Digital timing signals, or the CEA 861 timing signals, see HVF Timing on page 26and CEA 861 Timing on page 28. This information is presented in the VIDEO_STANDARD register (Table 4-3).

Total samples per line, active samples per line, total lines per field/frame and active lines per field/frame are also calculated and available via the RASTER_STRUCTURE registers (Table 4-4). These line and sample count registers are updated once per frame at the end of line 12.

After device reset, the four RASTER_STRUCTURE registers default to zero.

Table 4-3: Host Interface Description for Video Standard Register

Register Name	Bit	Name	Description	R/W	Default
VIDEO_STANDARD Address: 004h	15	–	Not Used.	–	–
	14-10	VD_STD[4:0]	Video Data Standard (see Table 4-5).	R	0
	9	INT_$\overline{\text{PROG}}$	Interlace/Progressive: Set LOW if detected video standard is PROGRESSIVE and is set HIGH if it is INTERLACED.	R	0
	8	STD_LOCK	Standard Lock: Set HIGH when the device has achieved full synchronization.	R	0
	7-0	–	Not Used.	–	–

Table 4-4: Host Interface Description for Raster Structure Registers

Register Name	Bit	Name	Description	R/W	Default
RASTER_STRUCTURE1 Address: 00Eh	15-12	–	Not Used.	–	–
	11-0	RASTER_STRUCTURE_1[11:0]	Words Per Active Line	R	0
RASTER_STRUCTURE2 Address: 00Fh	15-13	–	Not Used.	–	–
	12-0	RASTER_STRUCTURE_2[12:0]	Words Per Total Line.	R	0

Table 4-4: Host Interface Description for Raster Structure Registers

Register Name	Bit	Name	Description	R/W	Default
RASTER_STRUCTURE3 Address: 010h	15-11	–	Not Used.	–	–
	10-0	RASTER_STRUCTURE_3[10:0]	Total Lines Per Frame	R	0
RASTER_STRUCTURE4 Address: 011h	15-11	–	Not Used.	–	–
	10-0	RASTER_STRUCTURE_4[10:0]	Active Lines Per Field	R	0

4.8.3 Video Standard Indication

The value reported in the VD_STD[4:0] bits of the VIDEO_STANDARD register corresponds to the SMPTE standards as shown in Table 4-5.

In addition to the 5-bit video standard code word, the VIDEO_STANDARD register also contains two status bits. The STD_LOCK bit will be set HIGH whenever the device has achieved full synchronization. The INT_$\overline{\text{PROG}}$ bit will be set LOW if the detected video standard is progressive and HIGH if the detected video standard is interlaced.

The VD_STD[4:0], STD_LOCK and INT_$\overline{\text{PROG}}$ bits of the VIDEO_STANDARD register will default to zero after device reset. The VD_STD[4:0] and INT_$\overline{\text{PROG}}$ bits will also default to zero if the $\overline{\text{SMPTE_BYPASS}}$ pin is asserted LOW. The STD_LOCK bit will retain its previous value if the PCLK is removed.

Table 4-5: Supported Video Standards

VD_STD[4:0]	SMPTE Standard	Video Format	Length of HANC	Length of Active Video	Total Samples	SMPTE352M Lines
00h	296M (HD)	1280x720/60 (1:1)	358	1280	1650	13
01h	296M (HD)	1280x720/60 (1:1) - EM	198	1440	1650	13
02h	296M (HD)	1280x720/30 (1:1)	2008	1280	3300	13
03h	296M (HD)	1280x720/30 (1:1) - EM	408	2880	3300	13
04h	296M (HD)	1280x720/50 (1:1)	688	1280	1980	13
05h	296M (HD)	1280x720/50 (1:1) - EM	240	1728	1980	13
06h	296M (HD)	1280x720/25 (1:1)	2668	1280	3960	13
07h	296M (HD)	1280x720/25 (1:1) - EM	492	3456	3960	13
08h	296M (HD)	1280x720/24 (1:1)	2833	1280	4125	13
09h	296M (HD)	1280x720/24 (1:1) - EM	513	3600	4125	13
0Ah	274M (HD)	1920x1080/60 (2:1) or 1920x1080/30 (PsF)	268	1920	2200	10, 572
0Bh	274M (HD)	1920x1080/30 (1:1)	268	1920	2200	18
0Ch	274M (HD)	1920x1080/50 (2:1) or 1920x1080/25 (PsF)	708	1920	2640	10, 572
0Dh	274M (HD)	1920x1080/25 (1:1)	708	1920	2640	18

Table 4-5: Supported Video Standards (Continued)

VD_STD[4:0]	SMPTE Standard	Video Format	Length of HANC	Length of Active Video	Total Samples	SMPTE352M Lines
0Eh	274M (HD)	1920x1080/25 (1:1) - EM	324	2304	2640	18
0Fh	274M (HD)	1920x1080/25 (PsF) - EM	324	2304	2640	10, 572
10h	274M (HD)	1920x1080/24 (1:1)	818	1920	2750	18
11h	274M (HD)	1920x1080/24 (PsF)	818	1920	2750	10, 572
12h	274M (HD)	1920x1080/24 (1:1) - EM	338	2400	2750	18
13h	274M (HD)	1920x1080/24 (PsF) - EM	338	2400	2750	10, 572
14h	295M (HD)	1920x1080/50 (2:1)	444	1920	2376	10, 572
15h	260M (HD)	1920x1035/60 (2:1)	268	1920	2200	10, 572
16h	125M (SD)	1440x487/60 (2:1) (Or dual link progressive)	268	1440	1716	13, 276
17h	125M (SD)	1440x507/60 (2:1)	268	1440	1716	13, 276
19h	125M (SD)	525-line 487 generic	–	–	1716	13, 276
1Bh	125M (SD)	525-line 507 generic	–	–	1716	13, 276
18h	ITU-R BT.656 (SD)	1440x576/50 (2:1) (Or dual link progressive)	280	1440	1728	9, 322
1Ah	ITU-R BT.656 (SD)	625-line generic (EM)	–	–	1728	9, 322
1Dh	Unknown HD	–	–	–	–	–
1Eh	Unknown SD	–	–	–	–	–
1Ch, 1Fh	Reserved	–	–	–	–	–

NOTE: Though the GS1572 will work correctly on and serialize both 59.94Hz and 60Hz formats, it will not distinguish between them.

4.8.4 Packet Generation and Insertion

The GS1572 can calculate, assemble and insert TRS ID words and various types of ancillary data packets.

These features are only available when the IOPROC_EN/$\overline{\text{DIS}}$ pin is set HIGH. Individual insertion features may be enabled or disabled via the IOPROC_DISABLE register (Table 4-6).

All of the IOPROC_DISABLE register bits default to 'zero' after device reset, enabling all of the processing features. To disable any individual error correction feature, set the corresponding bit HIGH in this register.

Table 4-6: Host Interface Description for Internal Processing Disable Register

Register Name	Bit	Name	Description	R/W	Default
IOPROC_DISABLE Address: 000h	15-13	–	Not Used. Set to zero.	–	0
	12	–	Setting this bit LOW allows the timing mode to be selectable through the CEA_861 bit. Setting this bit HIGH allows the timing mode to be selectable through the CEA_861 bit, regardless of the pin setting.	–	0
	11	ANC_INS	Enable or disable ancillary data insertion. Set LOW for enable. Set HIGH for disable.	R/W	0
	10	–	Not Used. Set to zero.	–	0
	9	CEA_861	CEA_861 pin override bit. Active when TIM_861_PIN_EN bit is set HIGH. Set CEA_861 bit LOW to enable CEA 861 timing. Set this bit HIGH to disable CEA 861 timing.	R/W	0
	8	H_CONFIG	Horizontal blanking timing configuration. Set LOW when the H/HSYNC input timing is based on active line blanking (default). Set HIGH when the H input timing is based on the H bit of the TRS words. See Figure 4-2.	R/W	0
	7	–	Not Used. Set to zero.	–	0
	6	352M_INS	SMPTE352M packet insertion. In HD mode, 352M packets are inserted in the luma channel only when one of the bytes in the VIDEO_FORMAT_A or VIDEO_FORMAT_B registers are programmed with non-zero values. Set HIGH to disable.	R/W	0
	5	ILLEGAL_REMAP	Illegal Code Remapping. Detection and correction of illegal code words within the active picture area (AP). Set HIGH to disable.	R/W	0
	4	EDH_CRC_INS	Error Detection & Handling (EDH) Cyclical Redundancy Check (CRC) error correction. In SD mode the GS1572 will generate and insert EDH packets. Set HIGH to disable.	R/W	0
	3	ANC_CSUM_INS	Ancillary Data Checksum insertion. Set HIGH to disable.	R/W	0
	2	CRC_INS	Luma and chroma line-based CRC insertion. In HD mode, line-based CRC words are inserted in both the luma and chroma channels. Set HIGH to disable	R/W	0
	1	LNUM_INS	Luma and chroma line number insertion - HD mode only. Set HIGH to disable.	R/W	0
	0	TRS_INS	Timing Reference Signal Insertion. Set HIGH to disable.	R/W	0

4.8.4.1 SMPTE 352M Payload Identifier Packet Insertion

The GS1572 can generate and insert SMPTE 352M Payload Identifier Ancillary Data Packets.

When this feature is enabled, the device will automatically generate the ancillary data preambles, (DID, SDID, DBN, DC), and calculate the checksum. The SMPTE 352M packet

will be inserted into the data stream according to the line numbers programmed in the LINE_352M_f1 and LINE_352M_f2 registers (Table 4-7).

Packet insertion will only take place if at least one of the bytes in the VIDEO_FORMAT_A or VIDEO_FORMAT_B registers are programmed with a non-zero value (Table 4-8). In addition, the 352M_INS bit must be set LOW (Table 4-6).

The GS1572 will differentiate between PsF and interlaced formats based on bits 14 and 15 of the VIDEO_FORMAT_A register.

The packets will be inserted immediately after the EAV word in SD video streams and immediately after the line-based CRC word in the luma channel of HD video streams. If other ancillary packets exist in the horizontal ancillary space 352M packets will be inserted immediately following these packets. SMPTE 352M packets will not be inserted if there is insufficient room in the HANC space.

NOTE: If there are existing 352M packets in the input stream, and $\overline{\text{ANC_BLANK}}$ is set HIGH (disabled), then the existing data is preserved and new 352M is inserted. GS1572 does not overwrite existing 352M data.

Table 4-7: Host Interface Description for SMPTE 352M Packet Line Number Insertion Registers

Register Name	Bit	Name	Description	R/W	Default
LINE_0_352M Address: 01Bh	15-11	–	Not Used.	–	–
	10-0	LINE_0_352M[10:0]	Line number where SMPTE352M packet is inserted in field 1.	R/W	0
LINE_1_352M Address: 01Ch	15-11	–	Not Used.	–	–
	10-0	LINE_1_352M[10:0]	Line number where SMPTE352M packet is inserted in field 2.	R/W	0

Table 4-8: Host Interface Description for SMPTE 352M Payload Identifier Registers

Register Name	Bit	Name	Description	R/W	Default
VIDEO_FORMAT_B Address: 00Bh	15-8	Video_Format[2] [7:0]	SMPTE352M Byte 4 information must be programmed in this register when 352M_INS = LOW.	R/W	0
	7-0	Video_Format[1] [7:0]	SMPTE352M Byte 3information must be programmed in this register when 352M_INS = LOW.	R/W	0
VIDEO_FORMAT_A Address: 00Ah	15-8	Video_Format[4] [7:0]	SMPTE352M Byte 2information must be programmed in this register when 352M_INS = LOW.	R/W	0
	7-0	Video_Format[3] [7:0]	SMPTE352M Byte 1information must be programmed in this register when 352M_INS = LOW.	R/W	0

4.8.4.2 Illegal Code Remapping

If the ILLEGAL_REMAP bit of the IOPROC_DISABLE register is set LOW, the GS1572 will remap all codes within the active picture between the values of 3FCh and 3FFh to 3FBh. All codes within the active picture area between the values of 000h and 003h will be remapped to 004h.

In addition, 8-bit TRS and ancillary data preambles will be remapped to 10-bit values.

4.8.4.3 EDH Generation and Insertion

When operating in SD mode, (SD/$\overline{HD}$ = HIGH), the GS1572 will generate and insert complete EDH packets. Packet generation and insertion will only take place if the EDH_CRC_INS bit of the IOPROC_DISABLE register is set LOW.

The GS1572 will generate all of the required EDH packet data, including all ancillary data preambles DID, DBN, DC, reserved code words, and the checksum. Calculation of both Full Field (FF) and Active Picture (AP) CRC's will be carried out by the device.

SMPTE RP165 specifies the calculation ranges and scope of EDH data for standard 525 and 625 component digital interfaces. The GS1572 uses these standard ranges by default.

If the received video format does not correspond to 525 or 625 digital component video standards, then the ranges will be determined from the received TRS ID words or supplied H_Blanking, V_Blanking, and F_Digital timing signals; or HSYNC, VSYNC and DE CEA 861 timing signals. See 'HVF Timing' on page 26, and 'CEA 861 Timing' on page 28,.

The First Active and Full Field pixel will always be the first pixel after the SAV TRS code word. The Last Active and Full Field pixel will always be the last pixel before the start of the EAV TRS code words.

EDH error flags (EDH, EDA, IDH, IDA and UES) for ancillary data, full field and active picture will also be inserted when the corresponding bit of the EDH_FLAG register is set HIGH. (Table 4-9).

NOTE 1: The EDH flag registers must be updated once per field. The prepared EDH packet will be inserted at the appropriate line according to SMPTE RP165. The start pixel position of the inserted packet will be based on the SAV position of that line such that the last byte of the EDH packet (the checksum) will be placed in the sample immediately preceding the start of the SAV TRS word.

NOTE 2: EDH packets will not be inserted if there is insufficient room in the HANC space.

Table 4-9: Host Interface Description for EDH Flag Register (SD Mode Only)

Register Name	Bit	Name	Description	R/W	Default
EDH_FLAG Address: 002h	15	–	Not Used.	–	–
	14	ANC-UES	Ancillary Unknown Error Status flag will be generated and inserted.	R/W	0
	13	ANC-IDA	Ancillary Internal device error Detected Already flag will be generated and inserted.	R/W	0
	12	ANC-IDH	Ancillary Internal device error Detected Here flag will be generated and inserted.	R/W	0
	11	ANC-EDA	Ancillary Error Detected Already flag will be generated and inserted.	R/W	0
	10	ANC-EDH	Ancillary Error Detected Here flag will be generated and inserted.	R/W	0
	9	FF-UES	Full Field Unknown Error flag will be generated and inserted.	R/W	0
	8	FF-IDA	Full Field Internal device error Detected Already flag will be generated and inserted.	R/W	0
	7	FF-IDH	Full Field Internal device error Detected flag will be generated and inserted.	R/W	0
	6	FF-EDA	Full Field Error Detected Already flag will be generated and inserted.	R/W	0
	5	FF-EDH	Full Field Error Detected Here flag will be generated and inserted.	R/W	0
	4	AP-UES	Active Picture Unknown Error Status flag will be generated and inserted.	R/W	0
	3	AP-IDA	Active Picture Internal device error Detected Already flag will be generated and inserted.	R/W	0
	2	AP-IDH	Active Picture Internal device error Detected Here flag will be generated and inserted.	R/W	0
	1	AP-EDA	Active Picture Error Detected Already flag will be generated and inserted.	R/W	0
	0	AP-EDH	Active Picture Error Detected Here flag will be generated and inserted.	R/W	0

4.8.4.4 Ancillary Data Checksum Generation and Insertion

The GS1572 will calculate checksums for all detected ancillary data packets presented to the device. These calculated checksum values are inserted into the data stream prior to serialization.

Ancillary data checksum generation and insertion will only take place if the ANC_CSUM_INS bit of the IOPROC_DISABLE register is set LOW.

NOTE: The GS1572 will recalculate the checksum and, if incorrect, will re-insert the correct value. However, the GS1572 does not check the correctness of the parity bit. That is, if all the bits from 0 to 8 in the checksum word are correct and only bit 9 (the parity

bit, which is the inverse of bit 8) is incorrect, then the checksum word is not re-calculated. If even one of bit 0 to bit 8 has an incorrect value, then the checksum word is re-calculated and re-inserted.

4.8.4.5 Line Based CRC Generation and Insertion

The GS1572 will generate and insert line based CRC words into both the Luma and Chroma channels of the data stream. This feature is only available in HD mode and is enabled by setting the CRC_INS bit of the IOPROC_DISABLE register LOW.

4.8.4.6 HD Line Number Generation and Insertion

In HD mode, the GS1572 will calculate and insert line numbers into the Luma and Chroma channels of the output data stream.

Line number generation is in accordance with the relevant HD video standard as determined by the device, see Automatic Video Standard Detection on page 37.

This feature is enabled when SD/$\overline{\text{HD}}$ = LOW, and the LNUM_INS bit of the IOPROC_DISABLE register is set LOW.

4.8.4.7 TRS Generation and Insertion

The GS1572 can generate and insert 10-bit TRS code words into the data stream as required. This feature is enabled by setting the TRS_INS bit of the IOPROC_DISABLE register LOW.

TRS word generation will be performed in accordance with the timing parameters extracted from either the received TRS ID words, the supplied H_Blanking, V_Blanking, and F_Digital timing signals, or the CEA 861 timing signals, see HVF Timing on page 26 and CEA 861 Timing on page 28.

4.9 Parallel to Serial Conversion

The GS1572 can accept either 10-bit or 20-bit parallel data in both SD and HD modes. The supplied PCLK rate must correspond to the settings of the SD/$\overline{\text{HD}}$ and 20bit/$\overline{\text{10bit}}$ pins as shown in Table 4-10.

Table 4-10: Serial Digital Output Rates

Supplied PCLK Rate	Serial Digital Output Rate	Pin Settings	
		SD/$\overline{\text{HD}}$	20bit/$\overline{\text{10bit}}$
74.25 or 74.25/1.001MHz	1.485 or 1.485/1.001Gb/s	LOW	HIGH
148.5 or 148.5/1.001MHz	1.485 or 1.485/1.001Gb/s	LOW	LOW
13.5MHz	270Mb/s	HIGH	HIGH
27MHz	270Mb/s	HIGH	LOW

4.10 Internal ClockCleaner™ PLL

To obtain a clean clock signal for serialization and transmission, an external VCO signal is locked to the input PCLK via the GS1572's integrated Phase-Locked Loop. This high quality analog PLL has a bang-bang implementation, which automatically narrows the loop bandwidth in the presence of jitter, allowing the GS1572 to significantly attenuate jitter on the incoming PCLK.

4.10.1 External VCO

The GS1572 requires the GO1555 external Voltage Controlled Oscillator as part of its internal PLL.

Power for the external VCO is generated by the GS1572 from an integrated voltage regulator. The internal regulator uses +3.3V supplied on the CP_VDD/CP_GND pins to provide +2.5V on the VCO_VCC/VCO_GND pins.

The external VCO produces a 1.485GHz signal for the PLL, input on the VCO pin of the device. See Typical Application Circuit on page 59.

NOTE: The VCO_VCC output voltage is guaranteed to be 2.5V only when supplying power to the GO1555. The VCO_VCC pin should not be shorted to GND under any circumstances.

4.10.2 Loop Filter

The GS1572 PLL Loop Filter is an external first order filter formed by a series RC connection as shown in the Typical Application Circuit on page 59. The loop filter resistor value sets the bandwidth of the PLL and the capacitor value controls its stability and lock time. A loop filter resistor value between 1Ω to 20Ω and a loop filter capacitor value between 1µF to 33µF are recommended.

The GS1572 uses a non-linear, bang-bang, PLL, therefore its bandwidth scales with the input jitter amplitude - greater input jitter results in a smaller loop bandwidth causing more of the input jitter to be rejected. For a given input jitter amplitude, a smaller loop filter resistor produces a narrower loop bandwidth. With an input jitter amplitude of 300ps, for example, the PLL bandwidth can be adjusted from 2KHz to 40KHz by varying the loop filter resistor, as shown in Table 4-11: Loop Filter Component Values. For use with GEN-CLOCKS™ timing generators, a narrow loop bandwidth is recommended.

Increasing the loop filter capacitor value increases the stability of the PLL, but results in a longer lock time. For loop filter resistors smaller than 7Ω, a capacitor value of 33µF is recommended, while larger resistor values can accommodate smaller capacitors. Sample combinations of the loop filter resistor and capacitor values are shown in Table 4-11: Loop Filter Component Values, along with the resulting loop bandwidth. Additional loop bandwidths can be achieved by using different loop filter resistor values.

Table 4-11: Loop Filter Component Values

Loop Filter Resistor Value	Typical Loop Bandwidth*	Recommended Loop Filter Capacitor Value	Comments
1Ω	2kHz	33µF	Narrow bandwidth - provides maximum jitter reduction. Long lock-time.
7Ω	8kHz	10µF	
20Ω	40kHz	1µF	Wide bandwidth. Fast lock-time.

* Measured with 300ps pk-pk input jitter on PCLK

4.10.3 Lock Detect Output

The LOCKED output will be asserted HIGH when the internal PLL has locked to the input PCLK signal. In the absence of the PCLK, when frequency lock has not been achieved, and during device reset, the LOCKED output will be LOW.

Lock time, the time it takes for the internal PLL to frequency-lock to the reference PCLK following power-up or standby, is determined by the loop filter capacitor value chosen. A 1µF loop filter capacitor, for example, will result in lock times of less than 500µs. A 33µF loop filter capacitor, on the other hand, will result in a lock time of greater than 5s.

NOTE 1: When the PLL is in the process of locking to the reference PCLK, the LOCKED pin may generate LOW and HIGH pulses. The durations of these pulses are dependent on the loop filter capacitor value, but do not exceed 30ms. Once the PLL has achieved frequency lock, the LOCKED pin will remain HIGH and not change state.

NOTE 2: When the GS1572 is placed in standby mode, the value of LOCKED is maintained although the PLL does lose lock to the reference PCLK. When STANDBY is released, the PLL will re-lock. During this time, if the LOCKED pin was previously HIGH, it will de-assert approximately 6µs later, and re-assert once the PLL has re-locked to the input PCLK.

4.11 Serial Digital Output

The GS1572 includes a SMPTE compliant current mode differential serial digital Cable Driver with automatic slew rate control. The serial output has improved eye quality, exceptional ORL performance, and reduced duty cycle distortion.

The Cable Driver uses a separate +3.3V DC power supply provided via the CD_VDD and CD_GND pins.

To enable the output, SDO_EN/$\overline{\text{DIS}}$ must be set HIGH. Setting the SDO_EN/$\overline{\text{DIS}}$ signal LOW will set the SDO and $\overline{\text{SDO}}$ output pins to high-impedance, resulting in reduced device power consumption.

4.11.1 Output Swing

Nominally, the voltage swing of the serial digital output is 800mVp-p single-ended into a 75Ω load. This is set externally by connecting the RSET pin to CD_VDD through a 750Ω ±1% resistor.

4.12 GSPI Host Interface

The GS1572 Host Interface, also called the Gennum Serial Peripheral Interface (GSPI), provides access to configuration/status registers for the video processing functions of the chip.

By default, the device will be "live at power up", with all major functional blocks active in the defined default operating conditions described below.

Dedicated configuration pins are provided for basic configuration of the device.

The Host Interface is provided to allow optional configuration of some of the more advanced functions and operating modes of the device.

To simplify Host Interface access to the configuration and status registers, a single contiguous register map is provided for the video functions.

Registers are grouped by like function and wherever possible functional configuration will not be spread across multiple registers.

The GSPI is comprised of a Serial Data Input Signal (SDIN), Serial Data Output Signal (SDOUT), an active low Chip Select ($\overline{CS}$), and a Burst Clock (SCLK). The Burst Clock must have a duty cycle between 40% and 60% while active.

Because these pins are shared with the JTAG interface port, an additional control signal pin JTAG/$\overline{HOST}$ is provided. When JTAG/$\overline{HOST}$ is LOW, the GSPI interface is enabled.

When operating in GSPI mode, the SCLK, SDIN, and $\overline{CS}$ are inputs to the device. The SDOUT loops the SDIN back out when the GSPI is in write mode, or when $\overline{CS}$ is HIGH, allowing multiple devices to be connected in series. During reset, SDOUT is held in high-impedance mode. The interface is illustrated in the Figure 4-10.

Each GSPI access begins with a 16-bit command word on SDIN indicating the address of the register of interest. This is followed by a 16-bit data word on SDIN in write mode, or a 16-bit data word on SDOUT in read mode.

NOTE 1: When the device is in standby mode (STANDBY = HIGH) no Host Interface register can be read back or written to. Attempting a read or write will not damage the device. However, all reads will return a value of zero, and no writes will take effect.

NOTE 2: In the Configuration and Status Registers, there are several registers that have been designated as Reserved. If possible, writing to these registers should be avoided. If writing a value to these registers is not avoidable, then only a value of 'zero' should be written to these registers. Writing a value of 'one' may alter the functional behaviour of GS1572, but will not permanently damage the device.

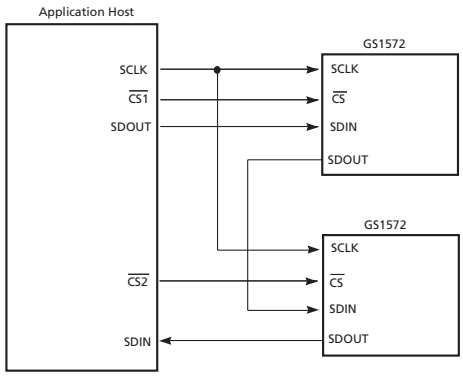


Figure 4-10: Gennum Serial Peripheral Interface (GSPI)

4.12.1 Command Word Description

The Command Word consists of a 16-bit word transmitted MSB first and contains a Read/Write bit, an Auto-Increment bit and a 12-bit address. Figure 4-11 shows the Command Word format and bit configurations. Command Words are clocked into the GS1572 on the rising edge of the serial clock SCLK, which operates in a burst fashion.

When the Auto-Increment bit is set LOW, each Command Word must be followed by only one Data Word to ensure proper operation. If the Auto-Increment bit is set HIGH, the following Data Word will be written into the address specified in the Command Word, and subsequent Data Words will be written into incremental addresses from the previous Data Word. This facilitates multiple address writes without sending a Command Word for each Data Word.

NOTE: All registers can be written to through single address access or through the auto-increment feature. However, the LSB of the video registers cannot be read through single address read-back. Single address read-back will return a 'zero' value for the LSB. If auto-increment is used to read back the values from at least two registers, the LSB value read will always be correct. Therefore, for register read-back, it is recommended that auto-increment be used and that at least two registers be read back at a time.

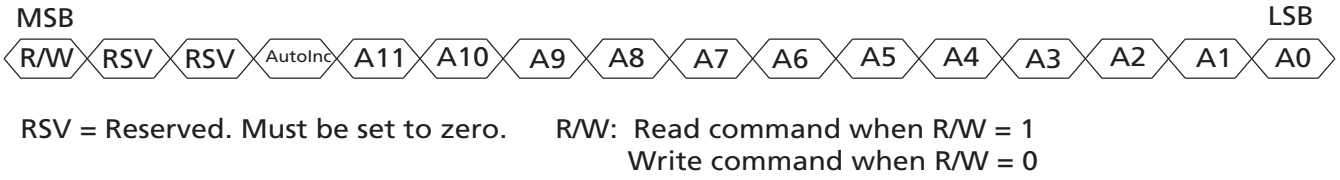


Figure 4-11: Command Word

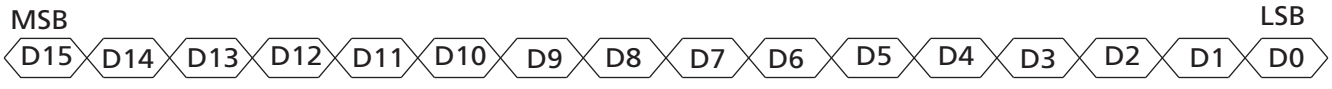


Figure 4-12: Data Word

4.12.2 Data Read and Write Timing

Read and Write mode timing for the GSPI interface is shown in Figure 4-13 and Figure 4-14 respectively. The timing parameters are defined in Table 4-12.

When several devices are connected to the GSPI chain, only one $\overline{CS}$ must be set LOW during a Read sequence.

During the write sequence, all Command and subsequent Data Words are looped through from SDIN to SDOUT. When several devices are connected to the GSPI chain, data can be written simultaneously to all the devices that have $\overline{CS}$ set LOW.

Table 4-12: GSPI Timing Parameters

Parameter	Definition	Specification
t_0	The minimum duration of time chip select, $\overline{CS}$, must be LOW before the first SCLK rising edge.	1.5 ns
t_1	The minimum SCLK period.	100 ns
t_2	Duty cycle tolerated by SCLK.	40% to 60%
t_3	Minimum input setup time.	1.5 ns
t_4	Write Cycle: the minimum duration of time between the last SCLK command (or data word if the Auto-Increment bit is HIGH) and the first SCLK of the data word.	37.1 ns
t_5	Read Cycle: the minimum duration of time between the last SCLK command (or data word if the Auto-Increment bit is HIGH) and the first SCLK of the data word.	148.4 ns
t_6	Minimum output hold time.	1.5 ns
t_7	The minimum duration of time between the last SCLK of the GSPI transaction and when $\overline{CS}$ can be set HIGH.	37.1 ns
t_8	Minimum input hold time.	1.5 ns

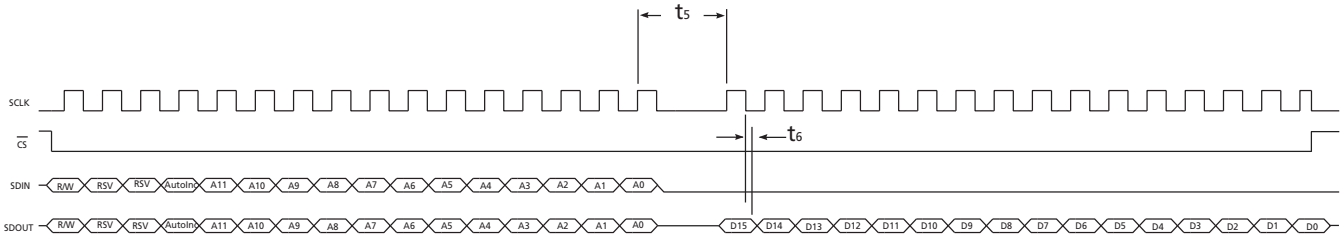


Figure 4-13: GSPI Read Mode Timing

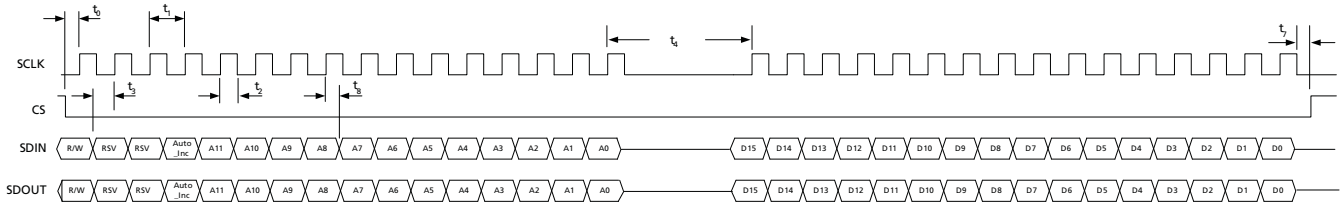


Figure 4-14: GSPI Write Mode Timing

4.12.3 Configuration and Status Registers

Table 4-13 summarizes the GS1572's internal status and configuration registers.

Table 4-14 summarizes the video core status and configuration registers.

All bits are available to the host via the GSPI.

Table 4-13: GS1572 Internal Registers

Address	Register Name	See Section
000h	IOPROC_DISABLE	Section 4.8.4
002h	EDH_FLAG	Section 4.8.4.3
004h	VIDEO_STANDARD	Section 4.8.2
005h - 009h	ANC_DATA_TYPE	–
00Ah - 00Bh	VIDEO_FORMAT	Section 4.8.4.1
00Eh - 011h	RASTER_STRUCTURE	Section 4.8.2
01Ah	GLOBAL_ERROR_MASK_VECTOR	–
01Bh - 01Ch	LINE_352M	Section 4.8.4.1

4.12.3.1 Configuration and Status Registers

Table 4-14: Configuration and Status Registers

Address	Register Name	Bit	Description	R/W	Default
000h	Reserved	15-13	Reserved.	R	000b
	TIM_861_PIN_EN	12	Selects pin for control for 861 timing converter. Reference: Section 4.3.2 on page 28.	R/W	0
	ANC_INS	11	Disable for ancillary data insertion feature. Reference: Section 4.7 on page 34.	R/W	0
	Reserved	10	Reserved.	R	0
	CEA_861	9	Disable 861 timing converter. Reference: Section 4.3.2 on page 28.	R/W	0
	H_CONFIG	8	Horizontal sync timing input configuration. Set LOW when the H input timing is based on active line blanking (default). Set HIGH when the H input timing is based on the H bit of the TRS words. Reference: Section 4.3.1 on page 26.	R/W	0
	Reserved	7	Reserved.	R	0
	352M_INS	6	SMPTE352M packet insertion. In HD mode, 352M packets are inserted in the luma channel only when one of the bytes in the VIDEO_FORMAT_A or VIDEO_FORMAT_B registers are programmed with non-zero values. Set HIGH to disable. Reference: Section 4.8.4.1 on page 40.	R/W	0
	ILLEGAL_REMAP	5	Illegal Code Remapping. Detection and correction of illegal code words within the active picture area (AP). Set HIGH to disable. Reference: Section 4.8.4.2 on page 42.	R/W	0
	EDH_CRC_INS	4	Error Detection & Handling (EDH) Cyclical Redundancy Check (CRC) error correction. In SD mode the GS1572 will generate and insert EDH packets. Set HIGH to disable. Reference: Section 4.8.4.3 on page 42.	R/W	0
	ANC_CSUM_INS	3	Ancillary Data Checksum insertion. Set HIGH to disable. Reference: Section 4.8.4.4 on page 43.	R/W	0
	CRC_INS	2	Luma and chroma line-based CRC insertion. In HD mode, line-based CRC words are inserted in both the luma and chroma channels. Set HIGH to disable Reference: Section 4.8.4.5 on page 44.	R/W	0
	LNUM_INS	1	Luma and chroma line number insertion - HD mode only. Set HIGH to disable. Reference: Section 4.8.4.6 on page 44.	R/W	0
	TRS_INS	0	Timing Reference Signal Insertion. Set HIGH to disable. Reference: Section 4.8.4.7 on page 44.	R/W	0

Table 4-14: Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
001h	Reserved	15-0	Reserved.	R	N/A
002h	Reserved	15	Reserved.	R/W	0
	ANC-UES	14	Ancillary Unknown Error Status flag will be generated and inserted. SD mode only. Reference: Section 4.8.4.3 on page 42.	R/W	0
	ANC-IDA	13	Ancillary Internal device error Detected Already flag will be generated and inserted. SD mode only. Reference: Section 4.8.4.3 on page 42.	R/W	
	ANC-IDH	12	Ancillary Internal device error Detected Here flag will be generated and inserted. SD mode only. Reference: Section 4.8.4.3 on page 42.	R/W	0
	ANC-EDA	11	Ancillary Error Detected Already flag will be generated and inserted. SD mode only. Reference: Section 4.8.4.3 on page 42.	R/W	0
	ANC-EDH	10	Ancillary Error Detected Here flag will be generated and inserted. SD mode only. Reference: Section 4.8.4.3 on page 42.	R/W	0
	FF-UES	9	Full Field Unknown Error flag will be generated and inserted. SD mode only. Reference: Section 4.8.4.3 on page 42.	R/W	0
	FF-IDA	8	Full Field Internal device error Detected Already flag will be generated and inserted. SD mode only. Reference: Section 4.8.4.3 on page 42.	R/W	0
	FF-IDH	7	Full Field Internal device error Detected flag will be generated and inserted. SD mode only. Reference: Section 4.8.4.3 on page 42.	R/W	0
	FF-EDA	6	Full Field Error Detected Already flag will be generated and inserted. SD mode only. Reference: Section 4.8.4.3 on page 42.	R/W	0
	FF-EDH	5	Full Field Error Detected Here flag will be generated and inserted. SD mode only. Reference: Section 4.8.4.3 on page 42.	R/W	0
	AP-UES	4	Active Picture Unknown Error Status flag will be generated and inserted. SD mode only.	R/W	0
	AP-IDA	3	Active Picture Internal device error Detected Already flag will be generated and inserted. SD mode only.	R/W	0
	AP-IDH	2	Active Picture Internal device error Detected Here flag will be generated and inserted. SD mode only.	R/W	0
	AP-EDA	1	Active Picture Error Detected Already flag will be generated and inserted. SD mode only.	R/W	0
	AP-EDH	0	Active Picture Error Detected Here flag will be generated and inserted. SD mode only.	R/W	0

Table 4-14: Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
003h	Reserved	15-0	Reserved.	R	N/A
004h	Reserved	15	Reserved	R	0
	VID_STD[4:0]	14-10	Reports the detected video standard. Reference: Section 4.8.3 on page 38.	R	00000b
	INT_$\overline{\text{PROG}}$	9	Interlace/Progressive: Set LOW if detected video standard is PROGRESSIVE and is set HIGH if it is INTERLACED. Reference: Section 4.8.3 on page 38.	R	0
	STD_LOCK	8	Standard Lock: Set HIGH when the device has achieved full synchronization. Reference: Section 4.8.3 on page 38.	R	0
	Reserved	7-0	Reserved.	R	N/A
005h-009h	Reserved	15-0	Reserved.	R	N/A
00Ah	Video_Format_A[15:8]	15-8	SMPTE 352M Byte 2 information must be programmed in this register when 352M_INS = LOW. Reference: Section 4.8.4.1 on page 40.	R/W	0
	Video_Format_A[7:0]	7-0	SMPTE 352M Byte 1 information must be programmed in this register when 352M_INS = LOW. Reference: Section 4.8.4.1 on page 40.	R/W	0
00Bh	Video_Format_B[15:8]	15-8	SMPTE 352M Byte 4 information must be programmed in this register when 352M_INS = LOW. Reference: Section 4.8.4.1 on page 40.	R/W	0
	Video_Format_B[7:0]	7-0	SMPTE 352M Byte 3 information must be programmed in this register when 352M_INS = LOW. Reference: Section 4.8.4.1 on page 40.	R/W	0
00Ch-00Dh	Reserved	15-0	Reserved.	R	N/A
00Eh	Reserved	15-12	Reserved.	–	–
	RASTER_STRUCTURE_1	11-0	Words Per Active Line Reference: Section 4.8.2 on page 37.	R	0
00Fh	Reserved	15-13	Reserved.	–	–
	RASTER_STRUCTURE_2	12-0	Words Per Total Line. Reference: Section 4.8.2 on page 37.	R	0
010h	Reserved	15-11	Reserved.	–	–
	RASTER_STRUCTURE_3	10-0	Total Lines Per Frame Reference: Section 4.8.2 on page 37.	R	0
011h	Reserved	15-11	Reserved.	–	–
	RASTER_STRUCTURE_4	10-0	Active Lines Per Field Reference: Section 4.8.2 on page 37.	R	0
012h	Reserved	15-0	Reserved.	–	0

Table 4-14: Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
013h	Reserved	15-0	Reserved.	–	–
014h	Reserved	15-0	Reserved.	–	–
015h	Reserved	15-0	Reserved.	–	–
016h	Reserved	15-0	Reserved.	–	–
017h	Reserved	15-0	Reserved.	–	–
018h	Reserved	15-0	Reserved.	–	–
019h	Reserved	15-0	Reserved.	–	–
01Ah	Reserved	15-0	Reserved.	R	N/A
01Bh	Reserved	15-11	Reserved.	–	–
	LINE_0_352M[10:0]	10-0	Line number where SMPTE352M packet is inserted in field 1. Reference: Section 4.8.4.1 on page 40.	R/W	0
01Ch	Reserved	15-11	Reserved.	–	–
	LINE_1_352M[10:0]	10-0	Line number where SMPTE352M packet is inserted in field 2. Reference: Section 4.8.4.1 on page 40.	R/W	0
01Dh-01Eh	Reserved	15-0	Reserved.	R	N/A
01Fh	FORMAT_ERR	15	861 timing format error flag.	R	0
	Reserved	14-9	Reserved.	R	0
	LINE_OFFSET	8-6	Shifts the timing of the output 861 timing signal by up to +/-3 lines.	R/W	0
	PIXEL_OFFSET	5-3	Shifts the timing of the output 861 timing signal by up to +/-3 pixels.	R/W	0
	Reserved	2-1	Reserved.	R	0
	FSYNC_INVERT	0	Inverts the polarity of the detected field.	R/W	0
020h	ANC_INS_MODE	15	Selects the ANC data insertion operating mode. 0 Separate line mode 1 Concatenated mode Reference: Section 4.7.1 on page 35.	R/W	0
	PACKET_MISSED	14	Flag to indicate ancillary data packet could not be inserted in its entirety. Reference: Section on page 34.	R	0
	RW_CONFLICT	13	Flag to indicate the same RAM address was read and written at the same time.	R	0
	Reserved	12-11	Reserved	R/W	0000b
	FIRST_LINE_NUMBER	10-0	Defines the line number for the first line in separate line mode or the single line for concatenated mode.	R/W	0

Table 4-14: Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
021h	ANC_TYPE	15	Selects the ANC data type as HANC or VANC. 0 HANC 1 VANC Reference: Section 4.7.2 & Section 4.7.3	R/W	0
	STREAM_TYPE	14	Selects the luma or chroma stream for ANC insertion. 0 Luma stream 1 Chroma stream This field is ignored in SD mode. Reference: Section 4.7.2 & Section 4.7.3	R/W	0
	Reserved	13-10	Reserved	R/W	0000b
	FIRST_LINE_NUMBER_OF_WORDS	9-0	Defines the total number of data words to insert on the first line in separate line mode or single line in the concatenated mode.	R/W	0
022h	Reserved	15-11	Reserved	R/W	00000b
	SECOND_LINE_NUMBER	10-0	Defines the line number for ANC data insertion for the 2nd line in separate line mode.	R/W	0
023h	ANC_TYPE	15	Selects the ANC data type as HANC or VANC. 0 HANC 1 VANC Reference: Section 4.7.2 & Section 4.7.3	R/W	0
	STREAM_TYPE	14	Selects the luma or chroma stream for ANC insertion. 0 Luma stream 1 Chroma stream This field is ignored in SD mode. Reference: Section 4.7.2 & Section 4.7.3	R/W	0
	Reserved	13-10	Reserved	R/W	0000b
	SECOND_LINE_NUMBER_OF_WORDS	9-0	Defines the total number of data words to insert on the 2nd line in separate line mode.	R/W	0
024h	Reserved	15-11	Reserved	R/W	00000b
	THIRD_LINE_NUMBER	10-0	Defines the line number for ANC data insertion for the 3rd line in separate line mode.	R/W	0
025h	ANC_TYPE	15	Selects the ANC data type as HANC or VANC. 0 HANC 1 VANC Reference: Section 4.7.2 & Section 4.7.3	R/W	0
	STREAM_TYPE	14	Selects the luma or chroma stream for ANC insertion. 0 Luma stream 1 Chroma stream This field is ignored in SD mode. Reference: Section 4.7.2 & Section 4.7.3	R/W	0
	Reserved	13-10	Reserved.	R/W	0000b
	THIRD_LINE_NUMBER_OF_WORDS	9-0	Defines the total number of data words to insert on the 3rd line in separate line mode.	R/W	0

Table 4-14: Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
026	Reserved	15-11	Reserved	R/W	00000b
	FOURTH_LINE_NUMBER	10-0	Defines the line number for ANC data insertion for the 4th line in separate line mode.	R/W	0
027h	ANC_TYPE	15	Selects the ANC data type as HANC or VANC. 0 HANC 1 VANC Reference: Section 4.7.2 & Section 4.7.3	R/W	0
	STREAM_TYPE	14	Selects the luma or chroma stream for ANC insertion. 0 Luma stream 1 Chroma stream This field is ignored in SD mode. Reference: Section 4.7.2 & Section 4.7.3	R/W	0
	Reserved	13-10	Reserved	R/W	0000b
	FOURTH_LINE_NUMBER_OF_WORDS	9-0	Defines the total number of data words to insert on the 4th line in separate line mode.	R/W	0
040h-07Fh	ANC_DATA_BANK1	15-0	First bank of user defined 8 bit words. 15-8: High order byte 7-0: Low order byte	W	0
080h-0BFh	ANC_DATA_BANK2	15-0	Second bank of user defined 8 bit words. 15-8: High order byte 7-0: Low order byte	W	0
0C0h-0FFh	ANC_DATA_BANK3	15-0	Third bank of user defined 8 bit words. 15-8: High order byte 7-0: Low order byte	W	0
100h-13Fh	ANC_DATA_BANK4	15-0	Fourth bank of user defined 8 bit words. 15-8: High order byte 7-0: Low order byte	W	0

4.13 JTAG Test Operation

When the JTAG/$\overline{\text{HOST}}$ input pin of the GS1572 is set HIGH, the Host Interface port will be configured for JTAG test operation. In this mode, pins J9, J10, K9, and K10 become TDO, TCK, TMS, and TDI. In addition, the $\overline{\text{RESET_TRST}}$ pin will operate as the test reset pin.

Boundary scan testing using the JTAG interface will be enabled in this mode.

There are two ways in which JTAG can be used on the GS1572:

1. As a stand-alone JTAG interface to be used at in-circuit ATE (Automatic Test Equipment) during PCB assembly; *or*
2. Under control of a host processor for applications such as system power on self tests.

When the JTAG tests are applied by ATE, care must be taken to disable any other devices driving the digital I/O pins. If the tests are to be applied only at ATE, this can be

accomplished with tri-state buffers used in conjunction with the JTAG/$\overline{\text{HOST}}$ input signal. This is shown in Figure 4-15.

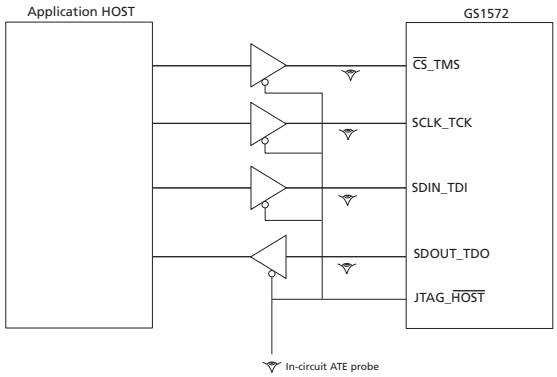


Figure 4-15: In-Circuit JTAG

Alternatively, if the test capabilities are to be used in the system, the Host Processor may still control the JTAG/$\overline{\text{HOST}}$ input signal, but some means for tri-stating the Host must exist in order to use the interface at ATE. This is represented in Figure 4-16.

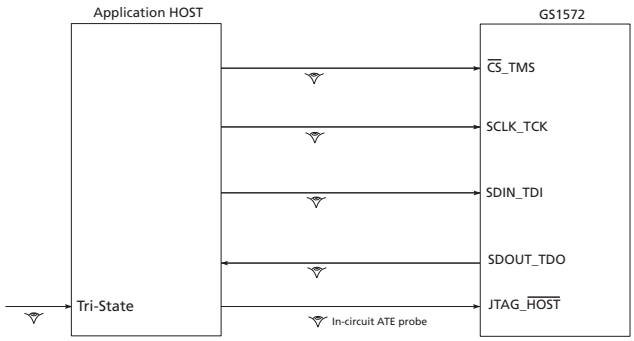


Figure 4-16: System JTAG

NOTE: Scan coverage is limited to digital pins only. There is no scan coverage for analog pins VCO, SDO/$\overline{\text{SDO}}$, RSET, LF, and CP_RES.

NOTE: The SD/$\overline{\text{HD}}$ pin must be held LOW during scan and therefore has no scan coverage.

Please contact your Gennum representative to obtain the BSDL model for the GS1572.

4.14 Device Reset

In order to initialize all internal operating conditions to their default states, hold the $\overline{\text{RESET_TRST}}$ signal LOW for a minimum of t_{reset} = 10ms after all power supplies are stable. There are no requirements for power supply sequencing.

When held in reset, all device outputs will be driven to a high-impedance state.

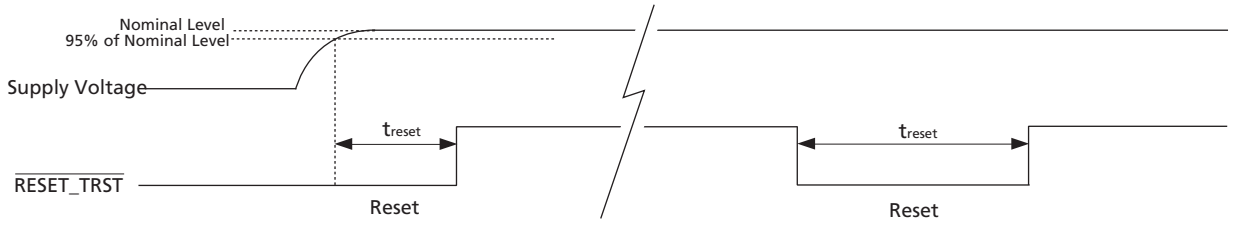
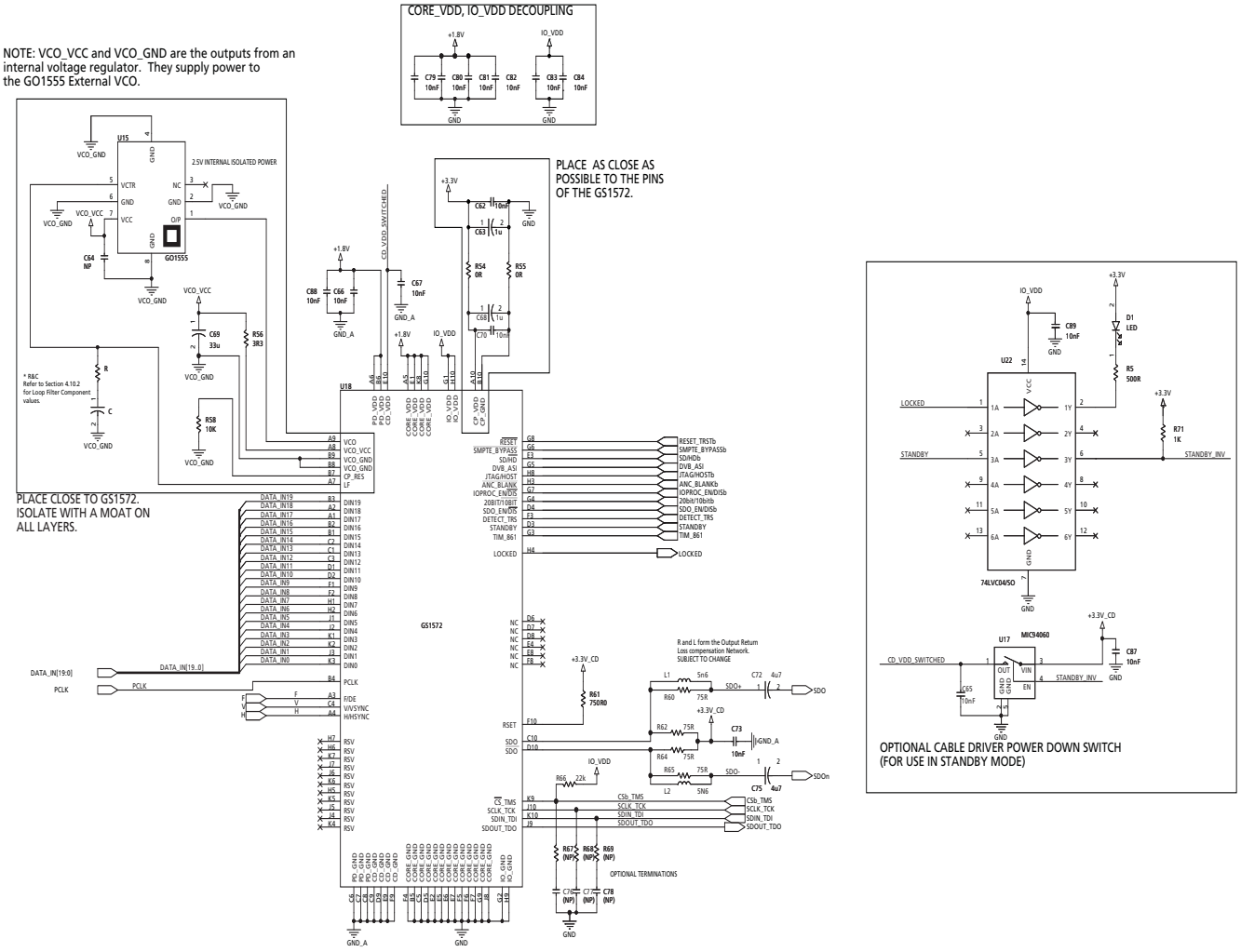


Figure 4-17: Reset Pulse

5. Application Reference Design

5.1 Typical Application Circuit

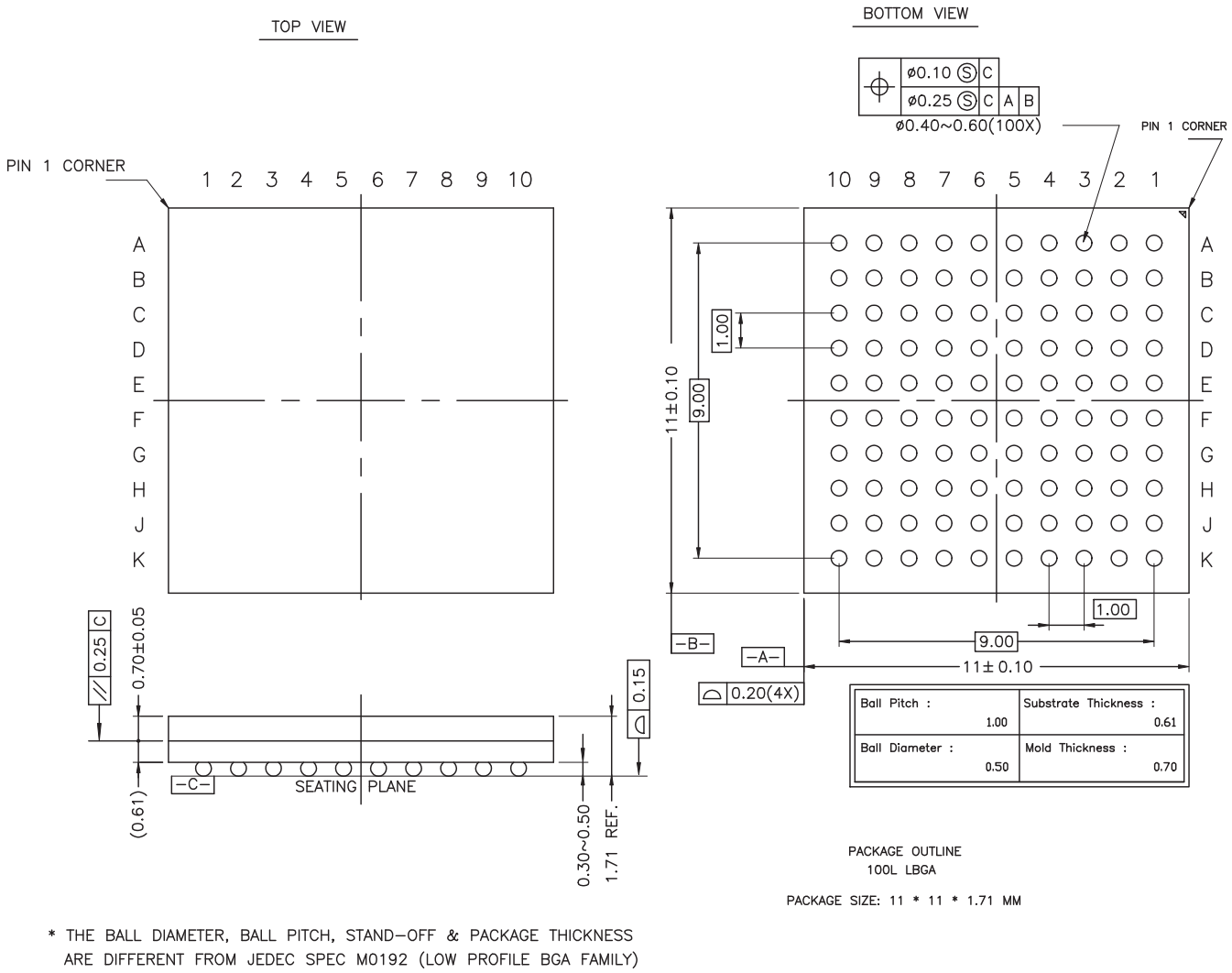


6. References & Relevant Standards

SMPTE 125M	Component video signal 4:2:2 – bit parallel interface
SMPTE 259M	10-bit 4:2:2 Component and 4fsc Composite Digital Signals - Serial Digital Interface
SMPTE 260M	1125 / 60 high definition production system – digital representation and bit parallel interface
SMPTE 267M	Bit parallel digital interface – component video signal 4:2:2 16 x 9 aspect ratio
SMPTE 274M	1920 x 1080 scanning analog and parallel digital interfaces for multiple picture rates
SMPTE 291M	Ancillary Data Packet and Space Formatting
SMPTE 292M	Bit-Serial Digital Interface for High-Definition Television Systems
SMPTE 293M	720 x 483 active line at 59.94 Hz progressive scan production – digital representation
SMPTE 296M	1280 x 720 scanning, analog and digital representation and analog interface
SMPTE 352M	Video Payload Identification for Digital Television Interfaces
SMPTE RP165	Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television
SMPTE RP168	Definition of Vertical Interval Switching Point for Synchronous Video Switching

7. Package & Ordering Information

7.1 Package Dimensions



PACKAGE OUTLINE
100L LBGA

PACKAGE SIZE: 11 * 11 * 1.71 MM

* THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC M0192 (LOW PROFILE BGA FAMILY)

7.2 Solder Reflow Profiles

The GS1572 is available in a Pb-free package. It is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 7-1.

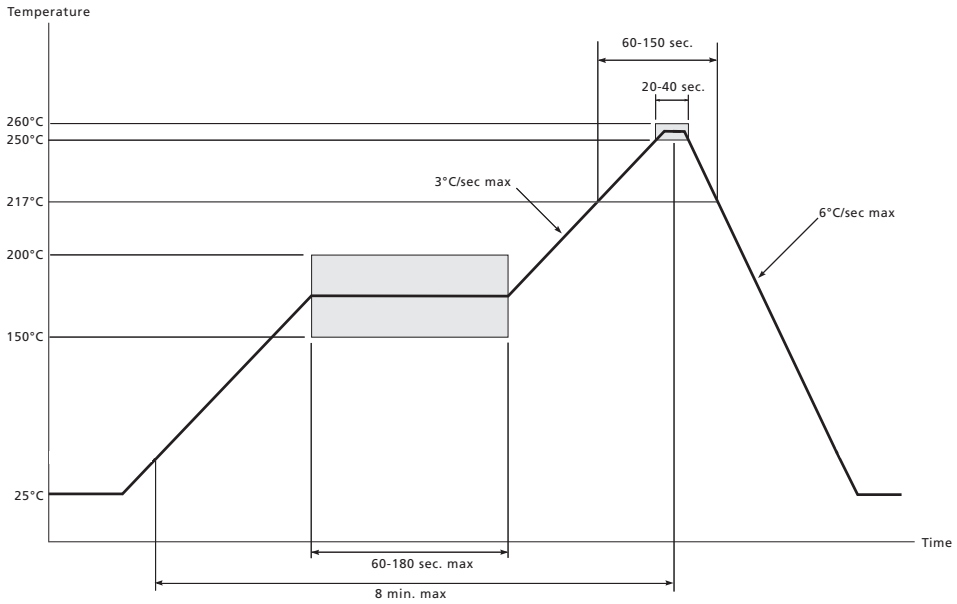


Figure 7-1: Maximum Pb-free Solder Reflow Profile

7.3 Marking Diagram



7.4 Packaging Data

Parameter	Value
Package Type	11mm x 11mm 100-ball LBGA
Package Drawing Reference	JEDEC M0192 (with exceptions noted in Package Dimensions on page 61).
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	15.4°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	37.1°C/W
Junction to Board Thermal Resistance, θ_{j-b}	26.4°C/W
Psi, ψ	0.4°C/W
Pb-free and RoHS Compliant	Yes

7.5 Ordering Information

Part Number	Package	Pb-free	Temperature Range
GS1572-IBE3	100-ball BGA	Yes	-20°C to 85°C

DOCUMENT IDENTIFICATION
DATA SHEET
The product is in production. Gennum reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION



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