DATA SHEET

GPCE040A

16-bit Sound Controller with 24K x 16 ROM

OCT. 01, 2013

Version 1.4

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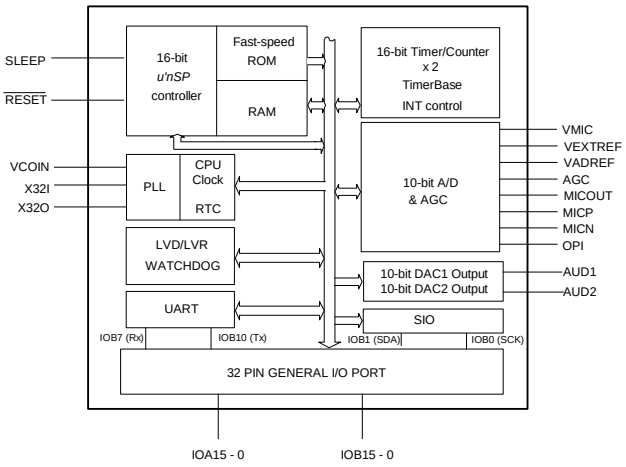
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16-BIT SOUND CONTROLLER WITH 24K X 16 ROM

1. GENERAL DESCRIPTION

The GPCE040A, a 16-bit architecture product, carries the newest 16-bit microprocessor, μ'nSP™ (pronounced as micro-n-SP), developed by Sunplus Technology. This high processing speed assures the μ'nSP™ is capable of handling complex digital signal processes easily and rapidly. Therefore, the GPCE040A is applicable to the areas of digital sound process and voice recognition. The operating voltage of 2.4V through 3.6V and speed of 0.32MHz through 49.152MHz yield the GPCE040A to be easily used in varieties of applications. The memory capacity includes 24K-word fast-speed ROM plus a 2K-word working SRAM. Other features include 32 programmable multi-functional I/Os, two 16-bit timers/counters, 32768Hz Real Time Clock, Low Voltage Reset/Detection, eight channels 10-bit ADC (one channel built-in MIC amplifier with auto gain controller), 10-bit DAC output and many others.

2. BLOCK DIAGRAM



3. FEATURES

- 16-bit *μ'nSP*™ microprocessor
- CPU clock: 0.32MHz - 49.152MHz
- Operating voltage: 3.0V - 3.6V @CPU clock = 49.152Mhz
  Operating voltage: 2.4V - 3.6V @CPU clock <=40.96Mhz
- IO PortA & B operating voltage: 2.4V - 5.5V
- 24K-word fast-speed ROM
- 2K-word working SRAM
- Software-based audio processing
- Crystal Resonator
- Standby mode (Clock Stop mode) for power savings,
  Max. 2.0μA @ VDD = 3.6V
- Two 16-bit timers/counters
- Two 10-bit DAC outputs
- 32 general I/Os (bit programmable)
- 14 INT sources with two priority levels
- Key wakeup function (IOA0 - 7)
- PLL feature for system clock
- 32768Hz Real Time Clock (RTC)
- Eight channels 10-bit AD converter
- ADC external top reference voltage
- 2.0V voltage regulator output, 5mA of driving capability
- Serial interface I/O (SIO)
- Built-in microphone amplifier and AGC function
- UART receiver and transmitter (full duplex)
- Low voltage reset and low voltage detection
- Watchdog enable (bonding option)

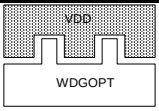
4. APPLICATION FIELD

- Voice recognition products
- Intelligent interactive talking toys
- Advanced educational toys
- Kids learning products
- Kids storybook
- General speech synthesizer
- Long duration audio products
- Recording / playback products

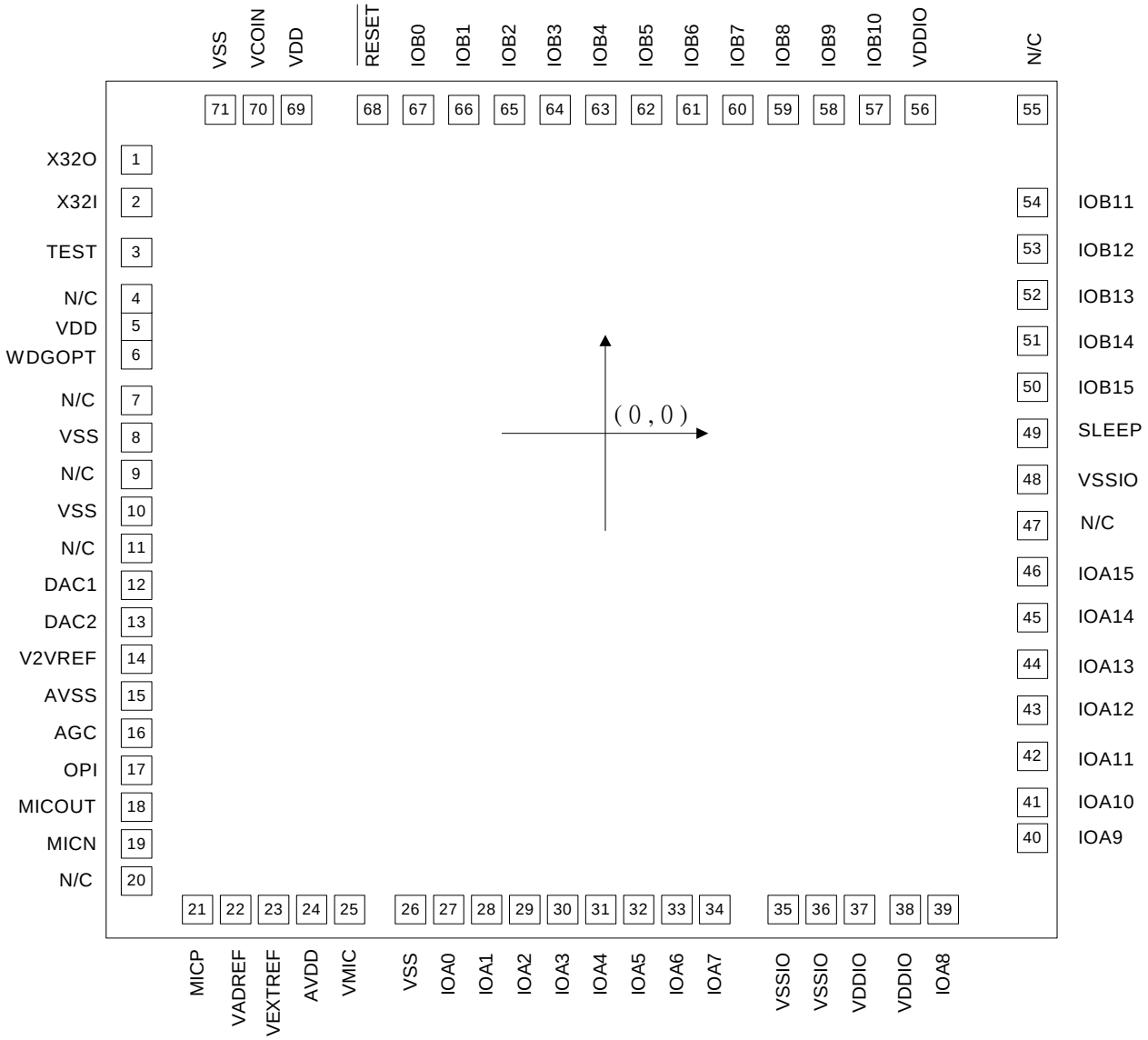
5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
IOA [15:8]	46 - 39	I/O	IOA [15:8]: bi-directional I/O ports.
IOA [7:0]	34 - 27	I/O	IOA [7:0] can be software programmed to wakeup I/O pins. IOA [6:0] can be optioned as ADC Line-in input.
IOB [15:11]	50 - 54	I/O	IOB [15:11]: bi-directional I/O ports.
IOB 10	57	I/O	IOB10 can also be selected as UART Transmitter (Tx).
IOB 9	58	I/O	IOB9 can also be Multi-duty cycle output of TimerB (BPWMO).
IOB 8	59	I/O	IOB8 can also be Multi-duty cycle output of TimerA (APWMO).
IOB 7	60	I/O	IOB7 can also be selected as UART receiver (Rx).
IOB 6	61	I/O	IOB6 is a bi-directional I/O ports.
IOB 5	62	I/O	IOB5 can also be selected as feedback signal with EXT2.
IOB 4	63	I/O	IOB4 can also be selected as feedback signal with EXT1.
IOB 3	64	I/O	IOB3 can also be selected as an external interrupt input pin (EXT2)(Negative-edge Triggered).
IOB 2	65	I/O	IOB2 can also be selected as an external interrupt input pin (EXT1)(Negative-edge Triggered).
IOB 1	66	I/O	IOB1 can also be selected as a serial interface data.(SDA).
IOB 0	67	I/O	IOB0 can also be selected as a serial interface clock (SCK).
DAC1	12	O	Audio DAC1 output.
DAC2	13	O	Audio DAC2 output.
X32I	2	I	Oscillator Crystal input.
X32O	1	O	Oscillator Crystal output.
VCOIN	70	I	RC filter connection for PLL.
AGC	16	I	AGC control pin.
MICN	19	I	Microphone differential input (negative).
MICP	21	I	Microphone differential input (positive).
V2VREF	14	O	2.0V output voltage, 5.0mA of driving capability (can be used as external ADC Line_IN top reference voltage).
MICOUT	18	O	Microphone 1st amplifier output.
OPI	17	I	Microphone 2nd amplifier input.
VEXTREF	23	I	ADC Line_IN top external reference voltage input pin.
VMIC	25	O	Microphone power supply.
VADREF	22	O	AD reference voltage (generated by internal AD converter).
VDD	5, 69	I	Positive supply for logic.
VSS	8, 10, 26, 71	I	Ground reference for logic and I/O pins.
VDDIO	37, 38, 56	I	Positive supply for I/O pins.
VSSIO	35, 36, 48	I	Ground reference for I/O pins.
AVDD	24	I	Positive supply for analog circuit including ADC, DAC and 2.0V regulator.
AVSS	15	I	Ground reference for analog circuit including ADC, DAC and 2.0V regulator.
$\overline{\text{RESET}}$	68	I	An active low reset to the chip.
SLEEP	49	O	Sleep mode (active high).
TEST	3	I	Connected to high for test mode, normally connected to GND (test mode disabled) or unconnected.
N/C	7, 9, 11, 20, 47, 55	I	Not used.
N/C	4	I	Do NOT bonding and connect this pin, if user binding this pin, IC will not work.
WDGOPT*	6	I	Bonded for watchdog disabled, unbonded for watchdog enabled.

Note*: WDGOPT is the watchdog option pin, selected by bonding option. Remain WDGOPT unbonded to enable the watchdog. In contrast, bonding this pad will disable watchdog. The reason of placing WDTOPT adjacent to VDD is to facilitate connection between VDD and WDGOPT when disabling watchdog is necessary. The layout of WDOGPT option pin is drawn in the right.



5.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: To ensure the IC functions properly, please bond all of VDD and VSS pins.
Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as closed as possible

6.FUNCTIONAL DESCRIPTIONS

6.1. CPU

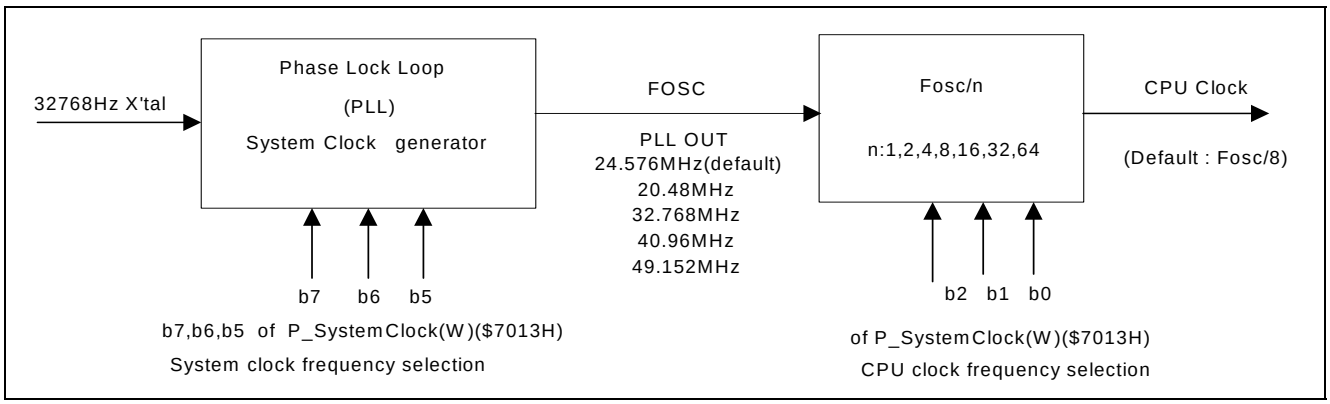
The GPCE040A is equipped with a 16-bit μ'nSP™, the newest 16-bit microprocessor by Sunplus and pronounced as micro-n-SP. Eight registers are involved in μ'nSP™: R1 - R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP) and SR (Segment Register). The interrupts include three FIQs (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software-interrupt, BREAK.

Moreover, a high performance hardware multiplier with the capability of FIR filter is also built in to reduce the software multiplication loading.

6.2. Memory

6.2.1. SRAM

The amount of SRAM is 2K-word (including Stack), ranged from $0000 through $07FF with access speed of two CPU clock cycles.



6.2.2. ROM

The GPCE040A provides a 24K-word fast-speed ROM with access speed of two CPU clock cycles.

6.3. PLL, Clock, Power Mode

6.3.1. PLL (Phase Lock Loop)

The purpose of PLL is to provide a base frequency (32768Hz) and to pump the frequency from 20.48MHz to 49.152MHz for system clock (F_{OSC}). The default PLL frequency is 24.576MHz.

6.3.1.1. System clock

Basically, the system clock is provided by PLL and programmed by the Port_SystemClock (W) to determine the frequency of clock for system. The default system clock F_{OSC} = 24.576MHz and CPU clock is Fosc/8 if not specified. The initial CPU clock is Fosc/8 after system wakes up and to be adjusted to desired CPU clock by programming the Port_SystemClock (W).

6.3.1.2. 32768Hz RTC

The Real Time Clock (RTC) is normally used in watch, clock or other time related products. A 2Hz-RTC (1/2 second) function is loaded in GPCE040A. The RTC counts the timing as well as to wake CPU up whenever RTC occurs. Since the RTC is generated in every 0.5 seconds, time can be traced by the numbers of RTC occurrence. In addition, GPCE040A supports 32768Hz oscillator in normal mode and auto-power-saving mode. In normal mode, 32768Hz OSC always runs at the highest power consumption. In auto-power-saving mode, however, it runs in normal mode for the first 7.5 seconds and changes back to power-saving mode automatically to save powers.

6.4. Standby Mode

The GPCE040A also offers a standby mode for low power application needs. To enter standby mode, the desired key wakeup port(IOA[7:0]) must be configured to input first. And read the Port_IOA_Latch(R) to latch the IOA state before entering the standby mode. Also remember to enable the corresponding interrupt source(s) for wakeup. After that, stop the CPU clock by writing the STOP CLOCK Register (b0~b2 of Port_SystemClock (W)) to enter standby mode. In such mode, SRAM and I/Os remain in the previous states till CPU being awoken. The wakeup sources in GPCE040A include Port IOA7 - 0 and IRQ1 - IRQ6. After GPCE040A is awoken, the CPU will continue to execute the program. Programmer can also enable or disable the 32768Hz OSC when CPU is in standby mode.

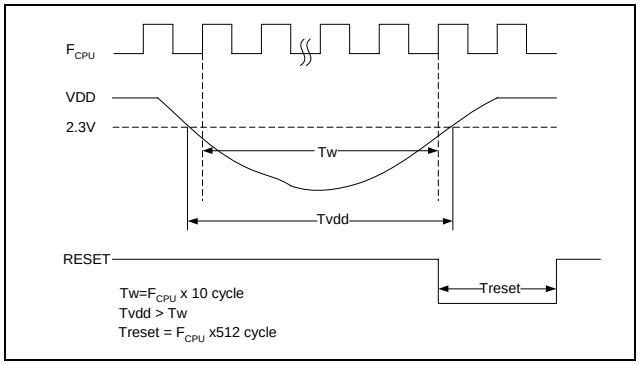
6.5. Low Voltage Detection and Low Voltage Reset

6.5.1. Low voltage detection (LVD)

The Low Voltage Detection (LVD) reports the circumstance of present voltage. There are three LVD levels to be selected: 2.5V, 2.9V, and 3.3V. These levels can be programmed via Port_LVD_Ctrl (W). As an example, suppose LVD is given to 2.9V. When the voltage drops below 2.9V, the b15 of Port_LVD_Ctrl is read as HIGH. In such state, program can be designed to react to this condition.

6.5.2. Low voltage reset

In addition to the LVD, the GPCE040A has another important function, Low Voltage Reset (LVR). With the LVR function, a reset signal is generated to reset system when the operating voltage drops below 2.3V for 10 consecutive CPU clock cycles. Without LVR, the CPU becomes unstable and malfunctions when the operating voltage drops below 2.3V. The LVR will reset all functions to the initial operational (stable) states when the voltage drops below 2.3V. A LVR timing diagram is given as follows:



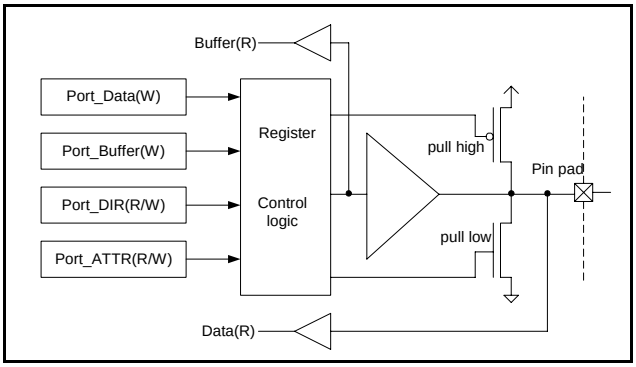
6.6. Interrupt

The GPCE040A has 14 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. FIQ is the high-priority interrupt while IRQ is the low-priority one. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources.

Interrupt Source	Interrupt Name	Priority
Fosc/1024	FIQ_PWM/IRQ0_PWM	High(FIQ)
Timer A	FIQ_TMA/ IRQ1_TMA	High(FIQ)
Timer B	FIQ_TMB/ IRQ2_TMB	High(FIQ)
EXT2	IRQ3_EXT2	Low
EXT1	IRQ3_EXT1	Low
Key change wakeup	IRQ3_KEY	Low
4096Hz	IRQ4_4KHz	Low
2048Hz	IRQ4_2KHZ	Low
1024Hz	IRQ4_1KHz	Low
4Hz	IRQ5_4Hz	Low
2Hz	IRQ5_2Hz	Low
Time-base 1	IRQ6_TMB1	Low
Time-base 2	IRQ6_TMB2	Low
UART (TxRDY or RxRDY)	UART IRQ	Low

6.7. I/O

Two I/O ports are built in GPCE040A, PortA and PortB. The PortA is an ordinary I/O with programmable wakeup capability. In addition to the regular IO function, the PortB can also perform some special functions in certain pins. Suppose operating voltage is running at 3.6V (VDD) and VDDIO (power for I/O) operates from 3.6V (VDD) to 5.5V. In such condition, the I/O pad is capable of operating from 0V through VDDIO. The following diagram is an I/O schematic.



Although data can be written into the same register through Port_Data and Port_Buffer, they can be read from different places, Buffer (R) and Data (R). The IOA [7:0] is the key wakeup port. To activate key wakeup function, latch data on PORT_IOA_Latch and enable the key wakeup function. Wakeup is triggered when the PortA state is different from at the time latched. In addition to an ordinary I/O port, PortB carries some special functions. A summary of PortB special functions is listed as follows:

Special function in PortB

PortB	Special Function	Function Description	Note
IOB0	SCK	Serial interface clock	Refer to see SIO section
IOB1	SDA	Serial interface data	Refer to see SIO section
IOB2	EXT1	External interrupt source 1(Negative-edge Triggered)	IOB2 set as input mode
	Feedback Output1	Works with IOB4 by adding a RC circuit between them to get an OSC to EXT1 interrupt	IOB2 set as inverted output
IOB3	EXT2	External interrupt source 2(Negative-edge Triggered)	IOB3 set as input mode
	Feedback Output2	Works with IOB5 by adding a RC circuit between them to get an OSC to EXT2 interrupt	IOB3 set as inverted output
IOB4	Feedback Input1	-	-
IOB5	Feedback Input2	-	-
IOB7	Rx	UART Receiver	Refer to see UART section
IOB8	APWMO	TimerA PWM output	Refer to Timer/Counter section
IOB9	BPWMO	TimerB PWM output	Refer to Timer/Counter section
IOB10	Tx	UART Transmitter	Refer to UART section

Default state: Pull Low
PWM: Pulse Width Modulation

Refer to the above table, the configuration of IOB2, IOB3, IOB4, and IOB5 involves feedback function in which an OSC frequency can be obtained from EXT1 (EXT2) by simply adding a RC circuit between IOB2 (IOB3) and IOB4 (IOB5).

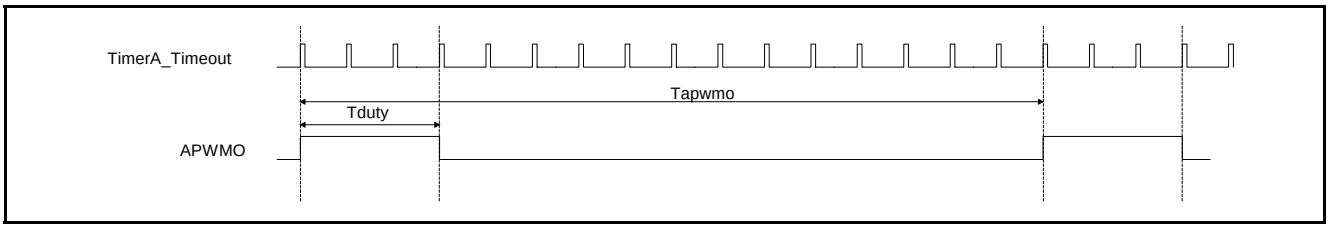
6.8. Timer/Counter

The GPCE040A provides two 16-bit timers/counters, TimerA and TimerB. The TimerA is called a universal counter. TimerB is a general-purpose counter. The clock source of TimerA comes from the combination of clock source A and clock source B. In TimerB, the clock source is given from source C. When timer overflows, an INT signal is sent to CPU to generate a time-out signal.

Clock of Source A	Clock of Source B	Clock of Source C
Fosc/2	2048Hz	Fosc/2
Fosc/256	1024Hz	Fosc/256
32768Hz	256Hz	32768Hz
8192Hz	TMB1	8192Hz
4096Hz	4Hz	4096Hz
1	2Hz	1
0	1	0
EXT1	EXT2	EXT1

Initially, write a value of N into a timer and select a desired clock source, timer will start counting from N, N+1, N+2,... through FFFF. An INT (TimerA/TimerB) signal is generated at the next clock after reaching “FFFF” and the INT signal is transmitted to INT controller for further processing. At the same time, N will be reloaded into timer and start all over again. The clock source A is a high frequency source and clock source B is a low frequency source. The combination of clock source A and B provides a variety of speeds to TimerA. A “1” represents pass signal and not gating. In contrast, “0” indicates deactivating timer. The EXT1 and EXT2 are the external clock sources. Moreover, counter can generate time-out signal for input clock source to a four bits (16 levels) PWM pulse width counter. A variety of clock duration can be generated and exported from IOB8 (APWMO) and IOB9 (BPWMO).

The following example is a 3/16-duration cycle. The APWMO waveform is made by selecting a pulse width through Port_TimerA_Ctrl (W) [9:6]. As a result, each 16 cycles will generate a pulse width defined in control port. These PWM signals can be applied for controlling the speed of motor or other devices.



Generally speaking, the clock source A and C are fast clock sources and source B comes from RTC system (32768Hz). Therefore, clock source B can be utilized as a precise counter for time counting, e.g., the 2Hz clock can be used for real time counting.

6.8.1. Timebase

Timebase, generated by 32768Hz, is a combination of frequency selections. The outputs of timebase block are named to TMB1 and TMB2. TMB1 is frequency for TimerA (Clock source B). The TMB1 and TMB2 are the sources for Interrupt (IRQ6). Furthermore, timebases generates additional 2Hz to 4096Hz interrupt sources (IRQ4 and IRQ5) for Real-Time-Clock (RTC).

TMB2	TMB1
128Hz	8Hz
256Hz	16Hz
512Hz	32Hz
1024Hz	64Hz
Default: 128Hz	Default: 8Hz

6.9. Sleep, Wakeup and Watchdog

6.9.1. Wakeup and sleep

1). Sleep: After power-on reset, IC starts running until a sleep command occurs. When a sleep command is accepted, IC will turn the system clock (PLL) off. After all, it enters sleep mode.

2). Wakeup: CPU waking up from sleep mode requires a wakeup signal to turn the system clock (PLL) on. The IRQ signal makes CPU to complete the wakeup process and initialization. The key wakeup and interrupt sources (IRQ1 - IRQ6) can be used for wakeup sources.

6.9.2. Watchdog

The purpose of watchdog is to monitor if the system operates normally. Within a certain period, watchdog must be cleared. If watchdog is not cleared, CPU assumes the program has been running in an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again. The watchdog function can be removed by bonding option. In GPCE040A, the clear period is 0.75 seconds. If watchdog is cleared within each 0.75 seconds, the system will not be reset. To clear watchdog, simply write “xxxx xxxx xxxx xx01B” to Port_Watchdog_Clear(W). The content written to Port_Watchdog_Clear (W) for watchdog clearance must be exactly the same as the one illustrated above (xxxx xxxx xxxx xx01B). Other values given to the Port_Watchdog_Clear (W) for watchdog clearance may end up with system reset. The watchdog function remains enabled during standby mode if the 32768Hz is turned on.

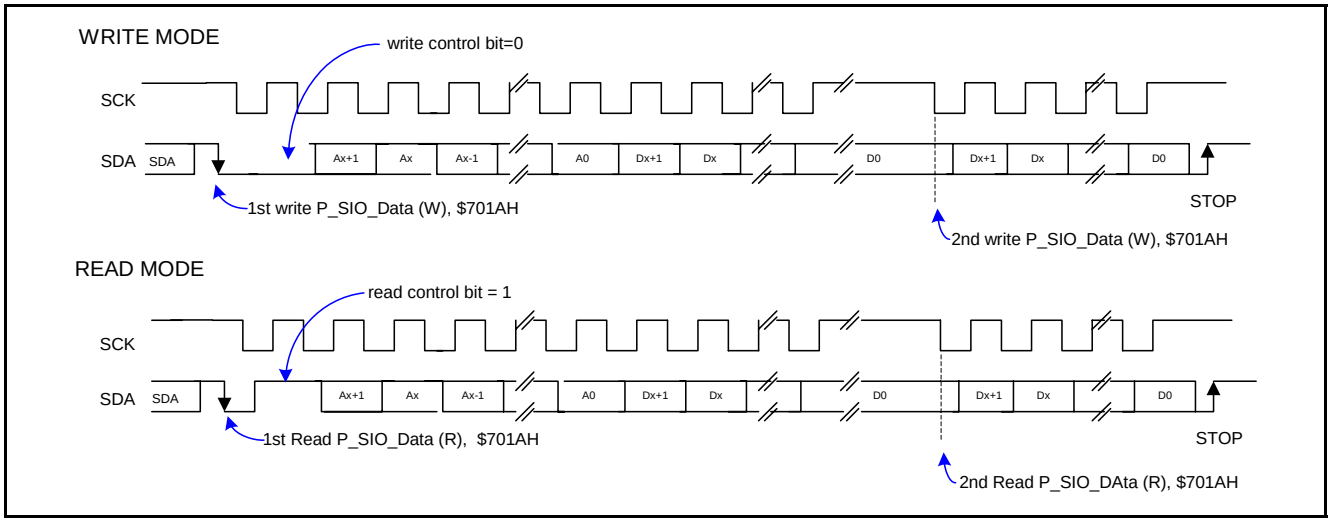
6.10. ADC (Analog to Digital Converter) / DAC

The GPCE040A has eight channels 10-bit ADC (Analog to Digital Converter). The function of an ADC is to convert analog signal to digital signal, e.g. a voltage level into a digital word. The eight channels of ADC can be seven channels of line-in from IOA [6:0] or one channel microphone (MIC) input through amplifier and AGC controller. The MIC amplifier circuit is capable of reducing common mode noise by transmitting signals through differential MIC Inputs (MICN, MICP). Moreover, an external resistor can be applied to adjust microphone gain and time of AGC operating. The AD needs to select source of line-in before conversion. The ADC is able to choose the external or internal (=AVDD) top reference voltage. If constant voltage source is unavailable, GPCE040A offers a constant voltage 2.0V with 5.0mA driving ability with a capacitor connected.

The GPCE040A has two 10-bit D/A with 2.0mA or 3.0mA driving current for audio outputs, DAC1 and DAC2.

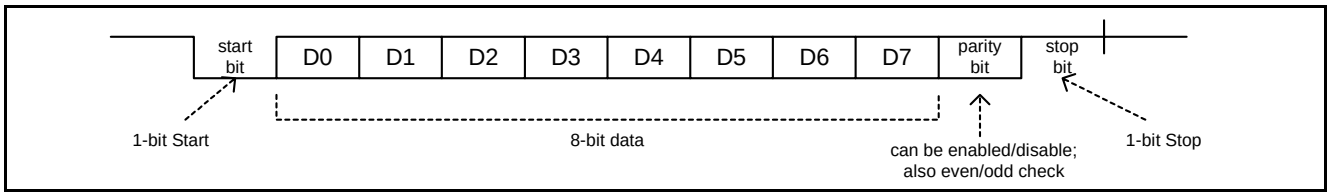
6.11. Serial interface I/O (SIO)

Serial interface I/O offers a one-bit serial interface for communication. This serial interface is capable of transmitting or receiving data via two I/O pins, IOB0 (SCK) and IOB1 (SDA).



6.12. UART

UART block provides a full-duplex standard interface that facilitates the communication with other devices. With this interface, GPCE can transmit and receive simultaneously. The maximum baud-rate can be up to 115200bps. This function can be accomplished by using PortB and Interrupt (UART IRQ). The Rx and Tx of UART are shared with IOB7 and IOB10. When GPCE040A receives and/or transmits a frame of data, the b7 (RxRDY) and/or b6 (TxRDY) in Port_UART_Command2(R) will be set to “1” and the UART IRQ is activated at the same time.



6.13. Audio Algorithm

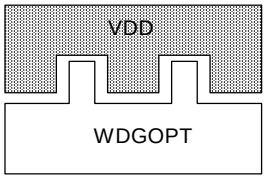
The following speech types can be used in GPCE040A: PCM, SACM_S200, SACM_S480, SACM_S530, SACM_S720, SACM_A1600, SACM_A1601, SACM_A3600, SACM_DVR520, SACM_DVR1600, SACM_DVR3200, and SACM_DVR4800. For melody synthesis, the GPCE040A supports SACM_MS01 (FM) and SACM_MS02 (wave-table) synthesizers.

6.14. Bonding Option Summary

The GPCE040A has the following bonding option:

6.14.1. Watchdog function

WDGOPT is the optional pin for watchdog by bonding option. The shape looks as the figure given below. When watchdog is selected, WDGOPT is unbonded. If watchdog is not selected, WDGOPT is bonded. The reason for WDGOPT adjacent to VDD is that when watchdog is not selected, it is easy to make the connection between VDD and WDGOPT.



7.ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 4.0V
PortA/B Pad Supply Voltage	V_{IO}	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to + 60℃
Storage Temperature	T_{STO}	-50℃ to + 150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see DC Electrical Characteristics.

7.2. DC Characteristics (VDD = 3.3V, VDD_{IO} = 5.5V (PortA & B), T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	3.3	3.6	V	-
Operating Current	I_{OP}	-	26	-	mA	F_{OSC} = 49.152MHz, AD, DAC disable, no loading
Standby Current	I_{STB}	-	-	2.0	μA	Disable 32KHz crystal
Input High Level	V_{IH}	$0.7VDD_{IO}$	-	-	V	-
Input Low Level	V_{IL}	-	-	$0.3VDD_{IO}$	V	-
Output High Current	I_{OH}	-	-5.0	-	mA	V_{OH} = 4.0V
Output Low Current	I_{OL}	-	12	-	mA	V_{OL} = 1.0V
Input Pull-Low Resister (PA15 :0, PB15 :0)	R_{PL}	-	110	-	KΩ	V_{IN} = VDD_{IO}
Input Pull-High Resister (PA15 :0, PB15 :0)	R_{PH}	-	150	-	KΩ	V_{IN} = VSS

7.3. DC Characteristics (VDD = 3.3V, VDD_{IO} = 3.3V (PortA & B), T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	3.3	3.6	V	-
Operating Current	I_{OP}	-	26	-	mA	F_{OSC} = 49.152MHz, AD, DAC disable, no loading
Standby Current	I_{STB}	-	-	2.0	μA	Disable 32KHz crystal
Input High Level	V_{IH}	$0.7VDD_{IO}$	-	-	V	-
Input Low Level	V_{IL}	-	-	$0.3VDD_{IO}$	V	-
Output High Current	I_{OH}	-	-2.9	-	mA	V_{OH} = 2.6V
Output Low Current	I_{OL}	-	6.7	-	mA	V_{OL} = 0.7V
Input Pull-Low Resister (PA15 :0, PB15 :0)	R_{PL}	-	175	-	KΩ	V_{IN} = VDD_{IO}
Input Pull-High Resister (PA15 :0, PB15 :0)	R_{PH}	-	242	-	KΩ	V_{IN} = VSS

7.4. DC Characteristics (VDD = 2.7V, VDD_{IO} = 2.7V (PortA & B) , T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	2.7	3.6	V	-
Operating Current	I_{OP}	-	17	-	mA	F_{OSC} = 49.152MHz, AD, DAC disable, no loading
Standby Current	I_{STB}	-	-	2.0	μA	Disable 32KHz crystal
Input High Level	V_{IH}	$0.7VDD_{IO}$	-	-	V	-
Input Low Level	V_{IL}	-	-	$0.3VDD_{IO}$	V	-
Output High Current	I_{OH}	-	-1.9	-	mA	V_{OH} = 2.1V
Output Low Current	I_{OL}	-	4.4	-	mA	V_{OL} = 0.5V
Input Pull-Low Resister (PA15 :0, PB15 :0)	R_{PL}	-	230	-	KΩ	V_{IN} = VDD_{IO}
Input Pull-High Resister (PA15 :0, PB15 :0)	R_{PH}	-	325	-	KΩ	V_{IN} = VSS

7.5. DC Characteristics (VDD = 2.4V, VDD_{IO} = 2.4V (PortA & B) ,T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	2.4	3.6	V	-
Operating Current	I_{OP}	-	14	-	mA	F_{OSC} = 49.152MHz, AD, DAC disable, no loading
Standby Current	I_{STB}	-	-	2.0	μA	Disable 32KHz crystal
Input High Level	V_{IH}	$0.7VDD_{IO}$	-	-	V	-
Input Low Level	V_{IL}	-	-	$0.3VDD_{IO}$	V	-
Output High Current	I_{OH}	-	-1.5	-	mA	V_{OH} = 1.92V
Output Low Current	I_{OL}	-	3.5	-	mA	V_{OL} = 0.48V
Input Pull-Low Resister (PA15 :0, PB15 :0)	R_{PL}	-	275	-	KΩ	V_{IN} = VDD_{IO}
Input Pull-High Resister (PA15 :0, PB15 :0)	R_{PH}	-	395	-	KΩ	V_{IN} = VSS

7.6. ADC Characteristics (VDD = 3.3V, T_A = 25℃)

Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
ADC Power Dissipation for LINE_IN	IADC	-	1.0	-	mA
ADC Power Dissipation For MIC_IN	-	-	1.9	-	mA
ADC LINE_IN Input Voltage Range from IOA[6:0]	VINL (Note 1)	VSS-0.3	-	VDD+0.3	V
ADC Microphone Input Voltage Range	VINM	VSS-0.3	-	VDD+0.3	V
External ADC Top Voltage	VEXTREF (Note 2)	2.0	-	VDD+0.3	V
Resolution of ADC	RESO	-	-	10	bits
Signal-to-Noise Plus Distortion of ADC from Line In	SINAD (Note 4)	-	56	-	dB
Effective Number of Bit	ENOB (Note 5)	8.0	9.0	-	bits
Integral Non-Linearity of ADC	INL	-	±4.0	-	LSB (Note 3)
Differential Non-Linearity of ADC	DNL (Note 6)	-	±0.5	-	LSB
AD Conversion Rate	F_{CONV}	-	-	Fcpu/512	Hz
Microphone Amplifier Gain (Note 7)	A_{MIC}	-	-	42	dB

Note1: Internal protection diodes clamp the analog input to VDD and VSS. These diodes allow the analog input to swing from (VSS-0.3V) to (VDD+0.3V) without causing damages to the devices.

Note2: The ADC performance is limited by the system noise level and therefore, the GPCE040A only guarantees to the 8-bit accuracy when VEXTREF is 2.0V.

Note3: The LSB means Least Significant Bit. VINL = 2.0V, 1LSB = 2.0V/2^10 = 1.953mV.

Note4: The SINAD testing condition at VINLp-p = 0.8*VDD, F_{CONV} = Fcpu/512 = 49MHz/512 = 95KHz, Fin=1.0KHz Sine waves at VDD = 3.0V from the IOA [6:0] input.

Note5: ENOB = (SINAD-1.76)/6.02.

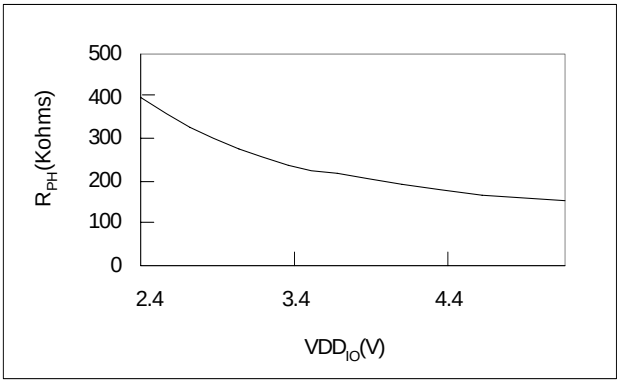
Note6: The ADC of GPCE040A guarantees no data missed during conversion.

Note7: The microphone amplifier maximum gain = 15 * (60K/(1.5K+REXT) V/V. The REXT is external resistor between OPI and MICOUT. The gain is 132V/V (=42dB) when REXT is 5.1K.

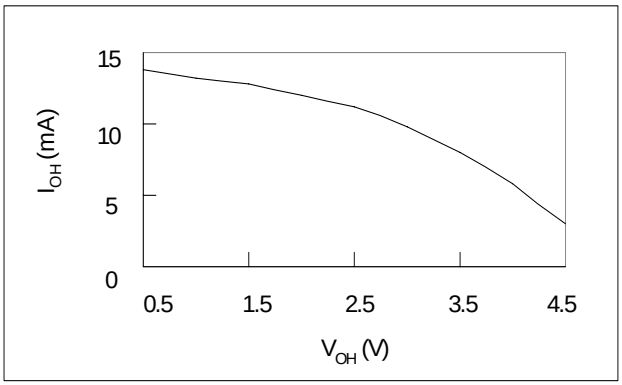
7.7. DAC Characteristics (T_A = 25℃)

Characteristics	Test condition	Symbol	Unit			Unit
			Min.	Typ.	Max.	
DAC resolution	VDD = 3.3V	RESO	-	-	10	bit
Signal to Noise Ratio of DAC	VDD = 3.3V	SNR	-	54	-	dB
Sample Rate	VDD = 3.3V	F_S	-	-	100K	Hz
Output DAC current (AUD1, AUD2)	VDD = 3.3V (2.0mA mode)	I_{AUD}	-	2.0	-	mA
	VDD = 3.3V (3.0mA mode)		-	3.0	-	

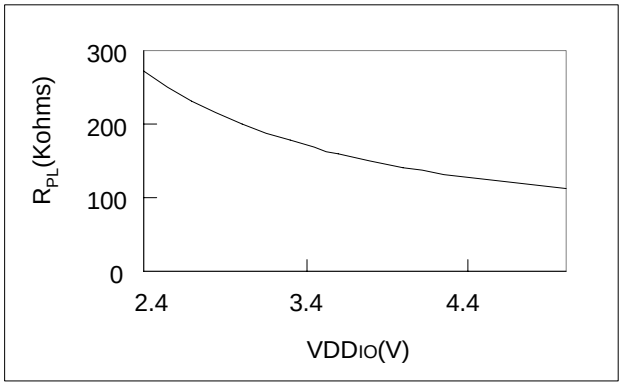
7.8. Pull High Resister and VDD_{IO}



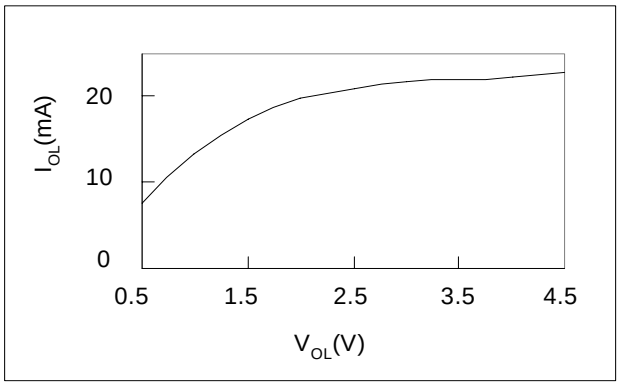
7.9. I/O Output High Current I_{OH} and V_{OH}



7.10. Pull Low Resister and VDD_{IO}

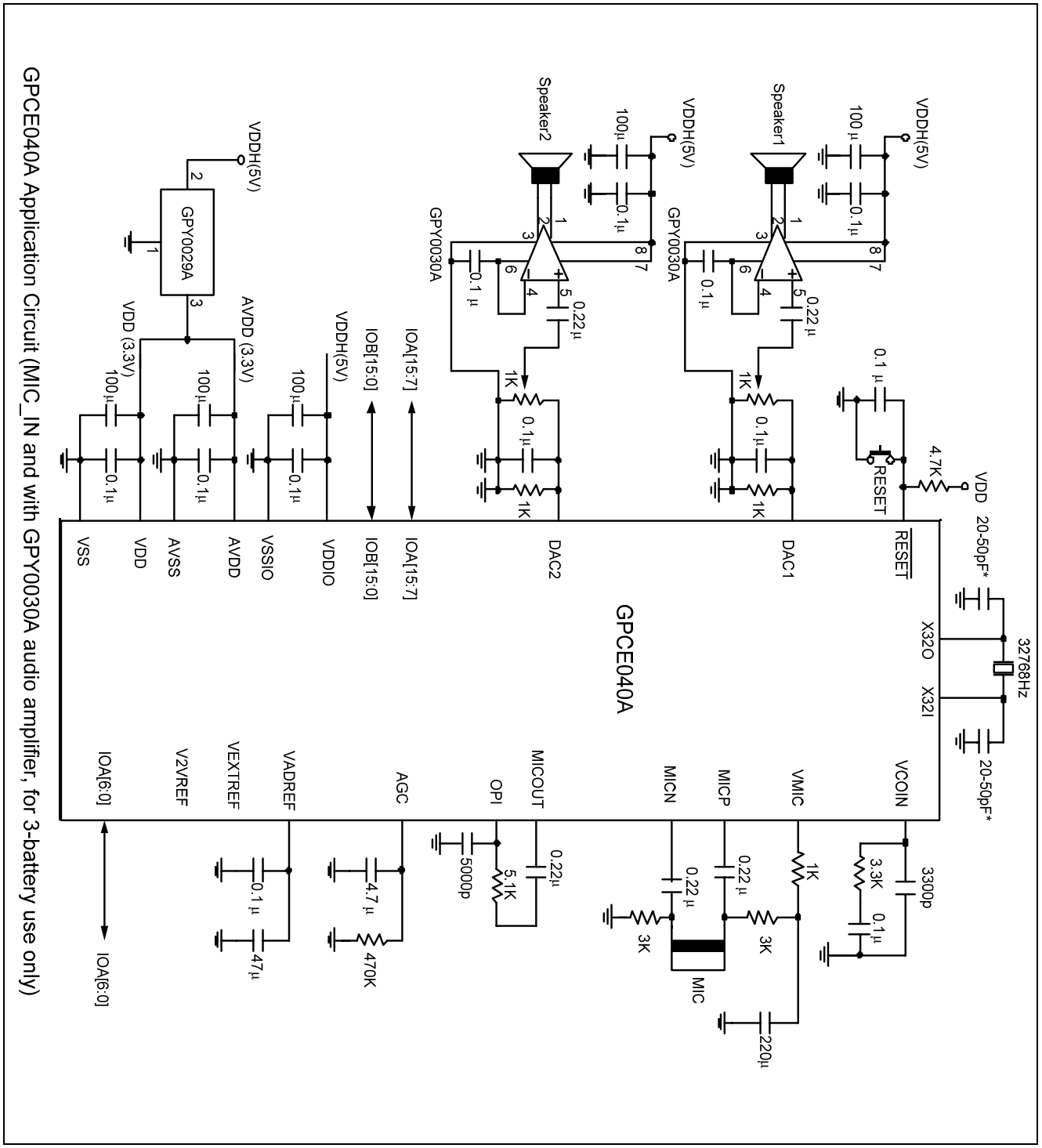


7.11. I/O Output Low Current I_{OL} and V_{OL}



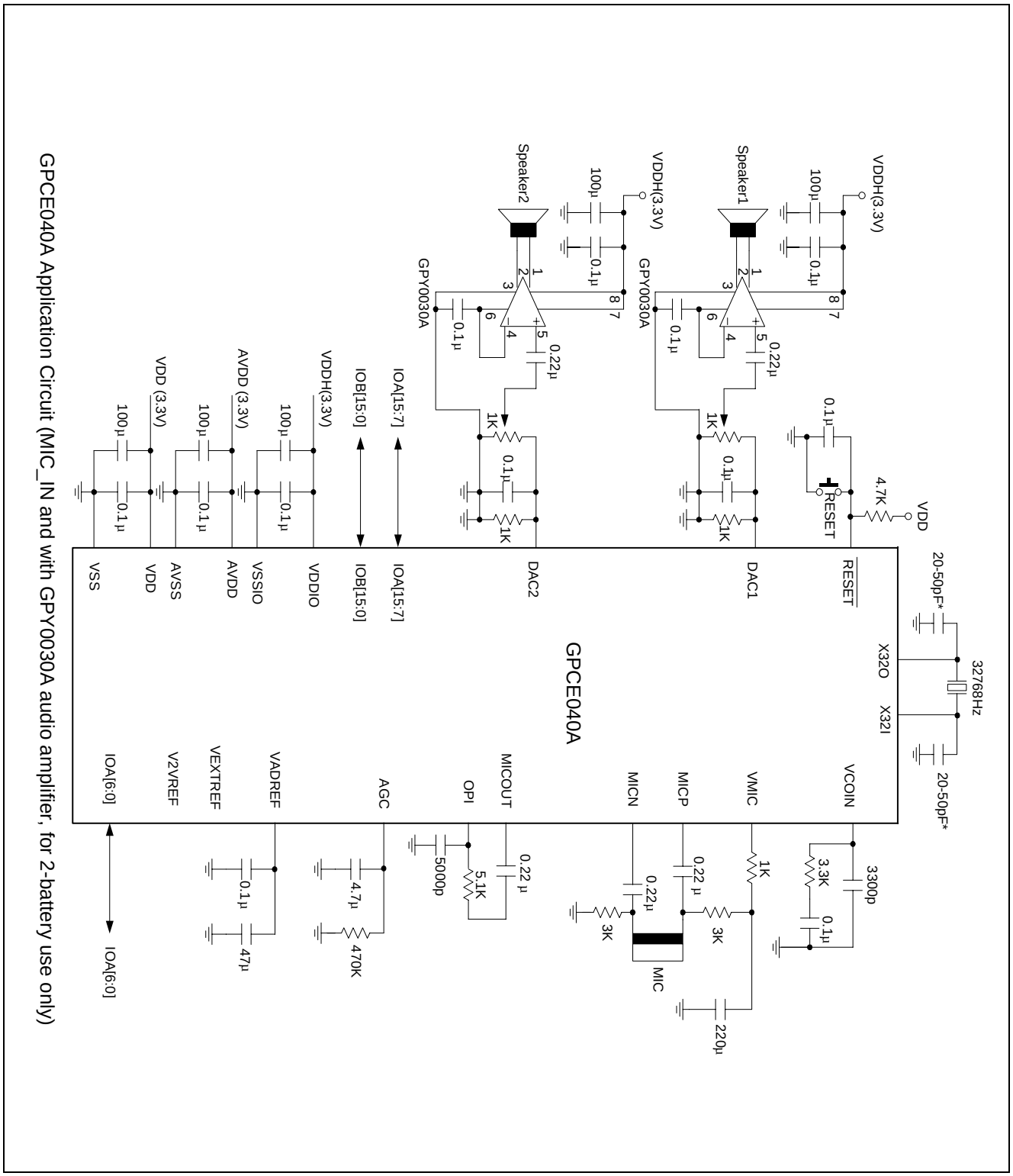
8.APPLICATION CIRCUITS

8.1. Application Circuit - (1)



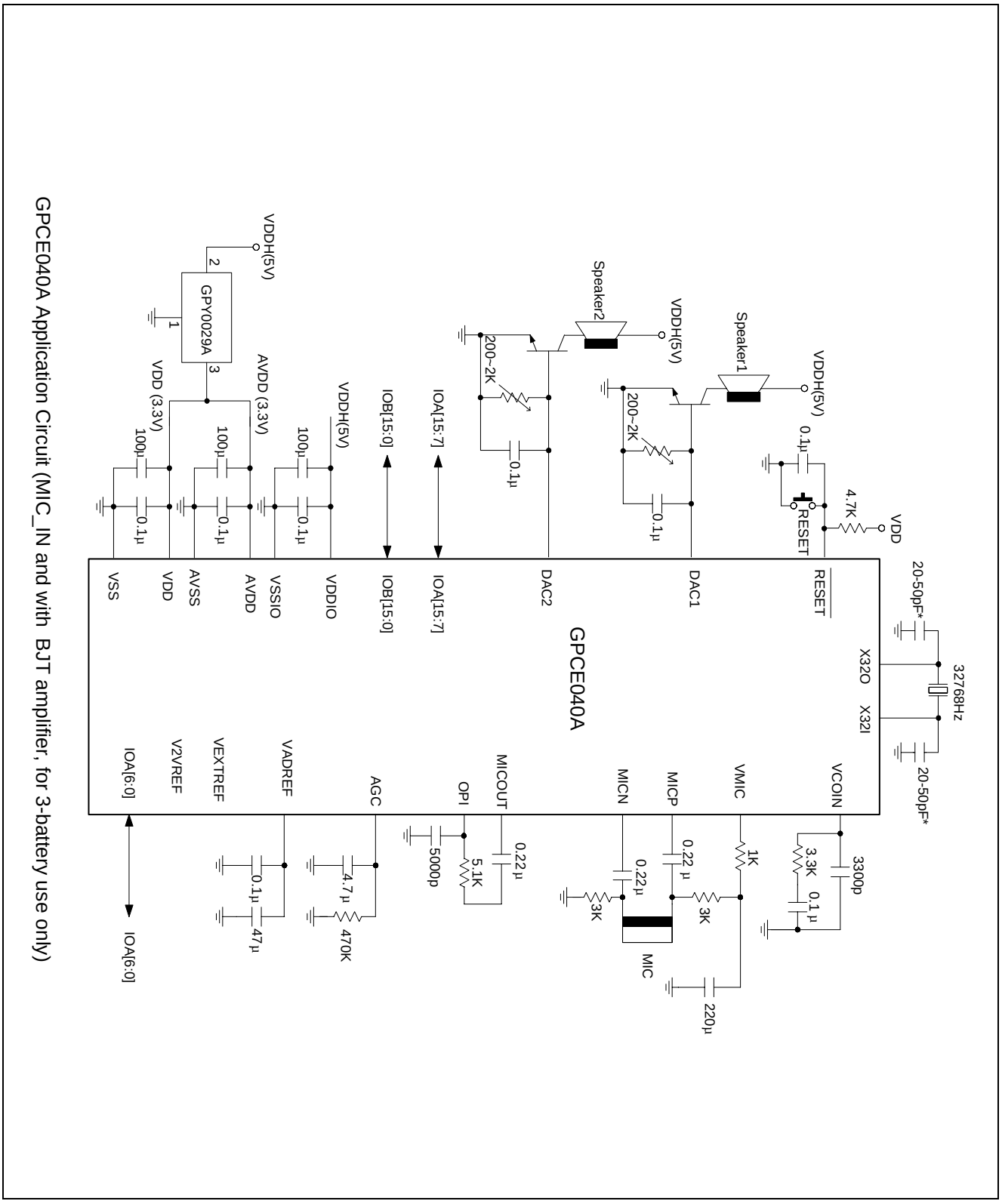
Note*: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8.2. Application Circuit - (2)



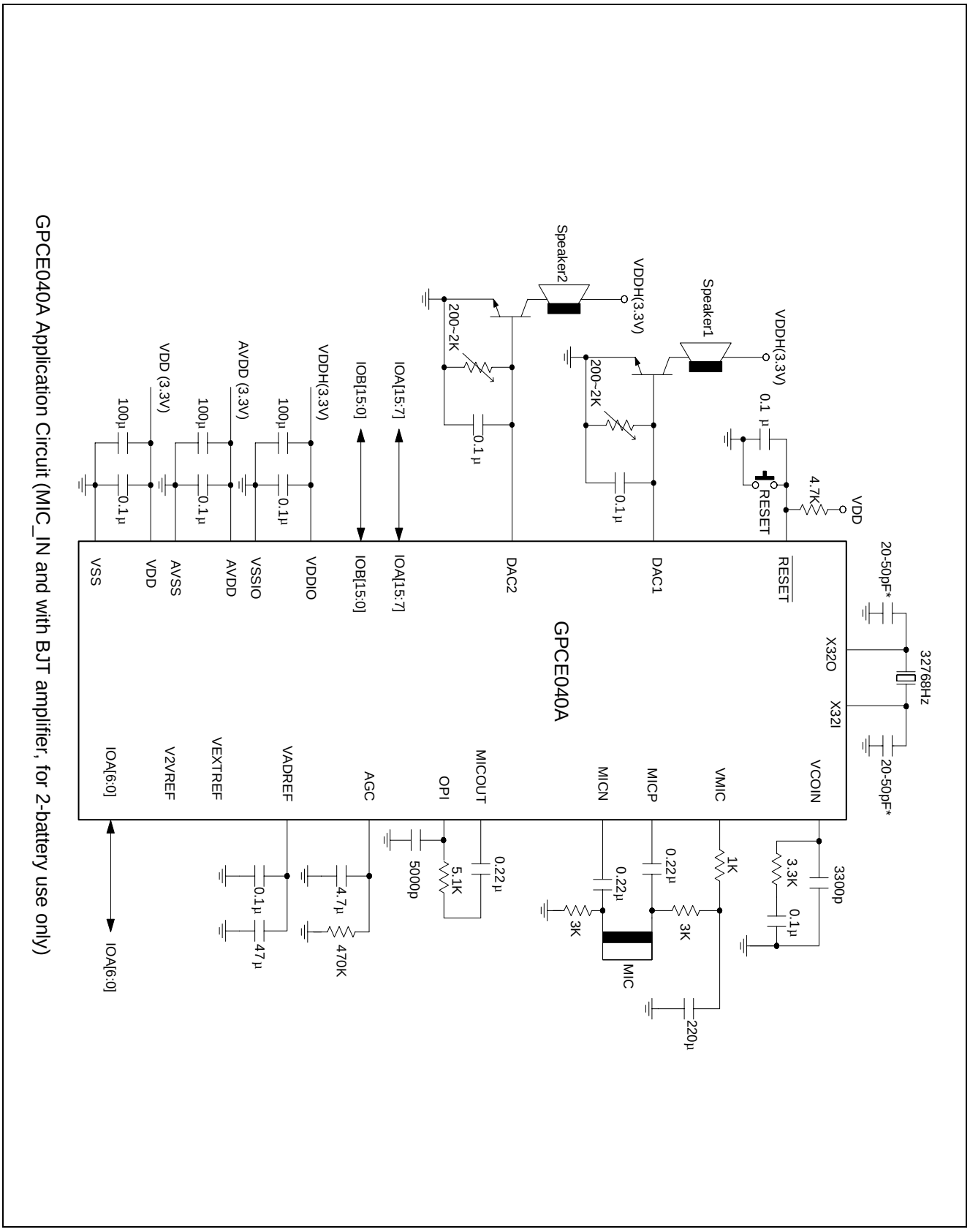
Note*: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8.3. Application Circuit - (3)



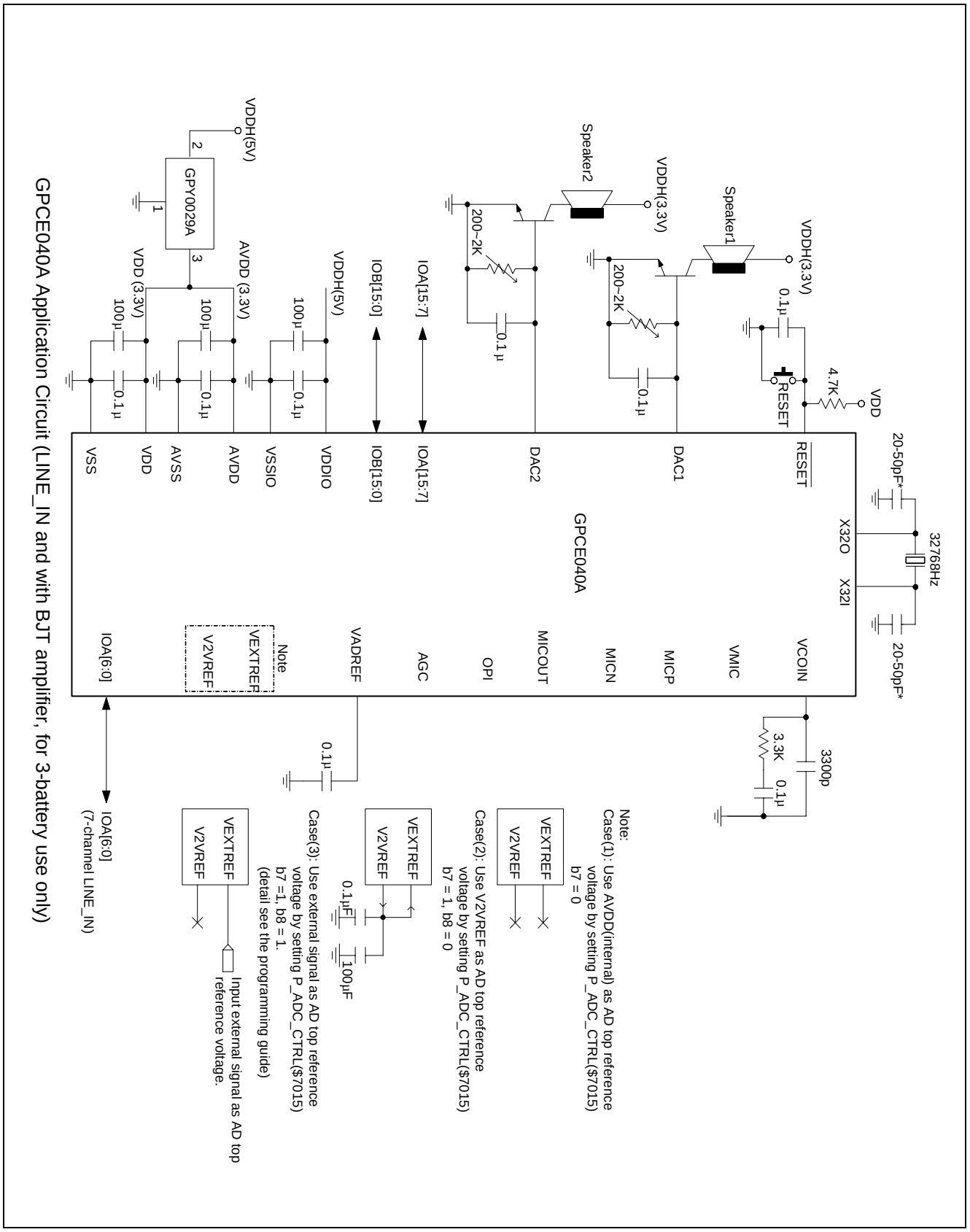
Note*: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8.4. Application Circuit - (4)



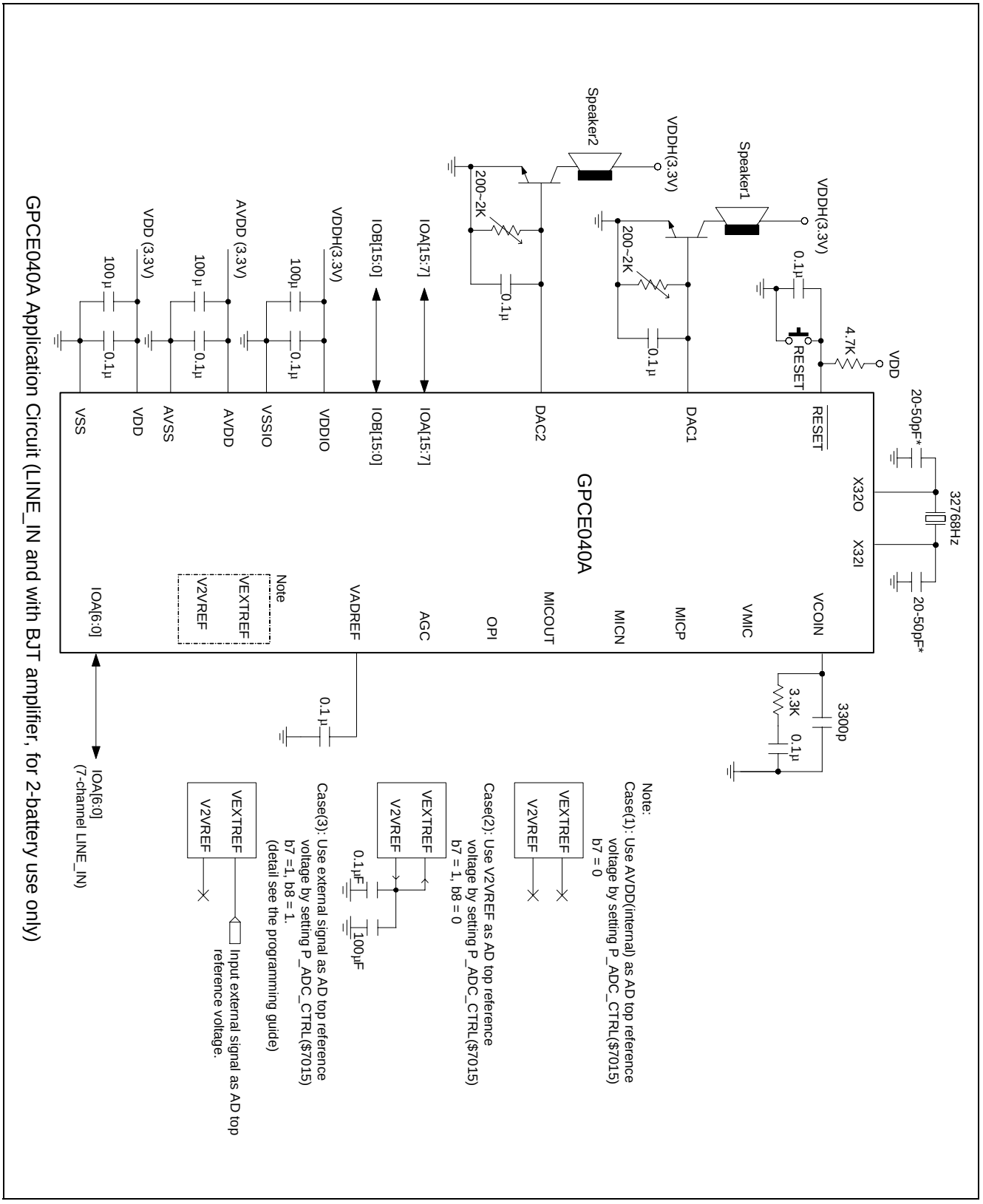
Note*: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8.5. Application Circuit - (5)



Note*: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8.6. Application Circuit - (6)



Note*: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPCE040A-NnnV-C	Chip form
GPCE040A-NnnV-HL04n-W	Green Package form - LQFP 80

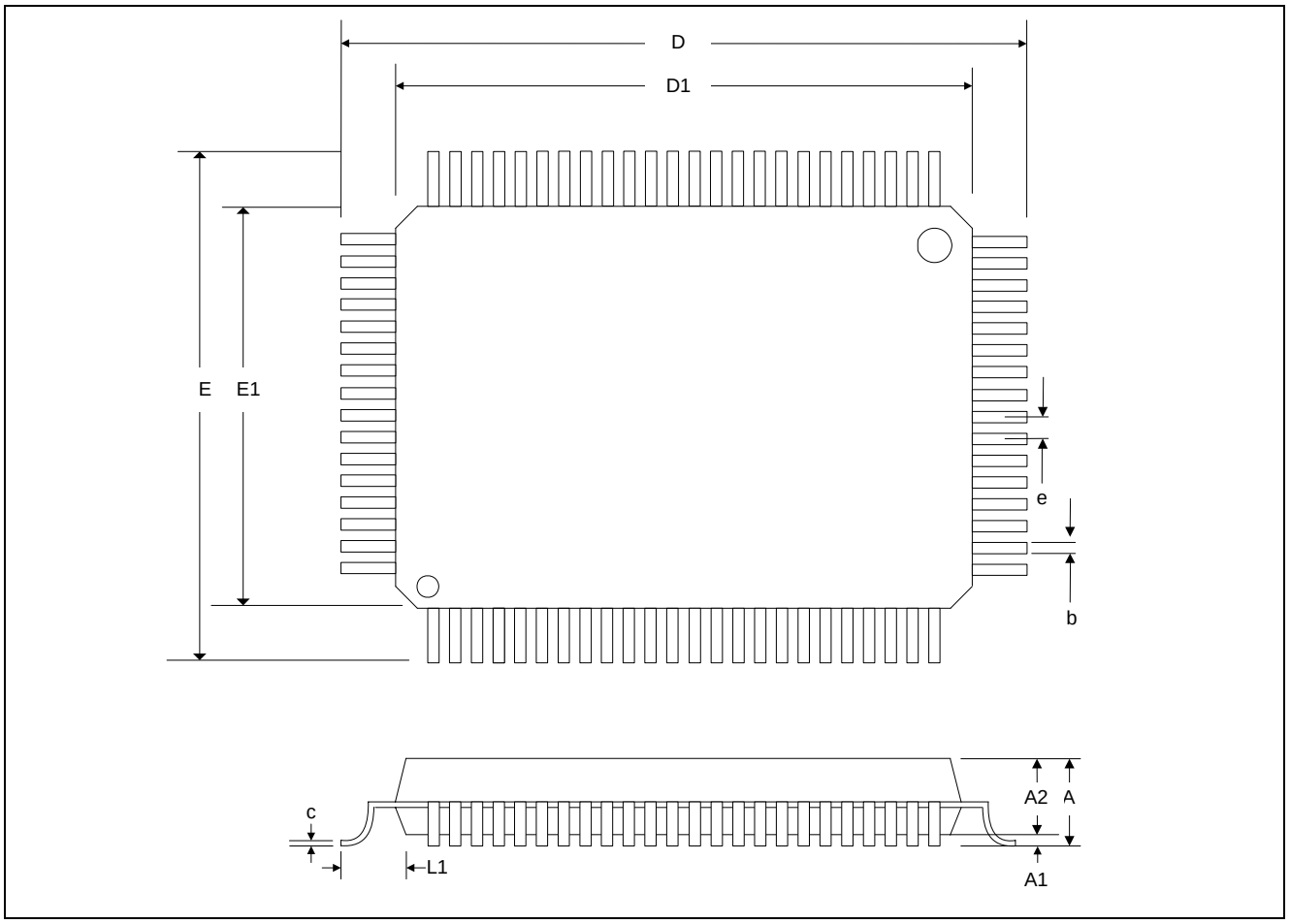
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: HL04n-W, HL04 is assign for LQFP80, n is assign for customer, W is watch dog bonding option (W=0 enable, W=1 disable).

9.2. Package information

9.2.1. LQFP 80



Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	-	-	0.063
A1	0.002	-	0.006
A2	0.053	0.055	0.057
b	0.007	0.009	0.011
c	0.004	-	0.008
D	0.551 BSC.		
D1	0.472 BSC.		

Symbol	Dimension in inch		
	Min.	Typ.	Max.
E		0.551 BSC.	
E1		0.472 BSC.	
e		0.020 BSC.	
L1		0.039 REF	

PAD No.	PAD Name	PAD No.	PAD Name
1	X32O	38	VDDIO
2	X32I	39	VDDIO
3	TEST	40	IOA8
4	N/C	41	N/C
5	VDD	42	N/C
6	N/C	43	IOA9
7	N/C	44	IOA10
8	VSS	45	IOA11
9	N/C	46	IOA12
10	VSS	47	IOA13
11	N/C	48	IOA14
12	DAC1	49	IOA15
13	DAC2	50	N/C
14	V2VREF	51	N/C
15	AVSS	52	VSSIO
16	AGC	53	N/C
17	OPI	54	SLEEP
18	MICOUT	55	IOB15
19	MICN	56	IOB14
20	N/C	57	IOB13
21	MICP	58	IOB12
22	VADREF	59	IOB11
23	VEXTREF	60	NC
24	AVDD	61	N/C
25	VMIC	62	N/C
26	N/C	63	IN/C
27	VSS	64	VDDIO
28	IOA0	65	IOB10
29	IOA1	66	IOB9
30	IOA2	67	IOB8
31	IOA3	68	IOB7
32	IOA4	69	IOB6
33	IOA5	70	IOB5
34	IOA6	71	IOB4
35	IOA7	72	IOB3
36	VSSIO	73	IOB2
37	VSSIO	74	IOB1

PAD No.	PAD Name	PAD No.	PAD Name
75	IOB0	78	VDD
76	$\overline{\text{RESET}}$	79	VCOIN
77	N/C	80	VSS

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
OCT. 01, 2013	1.4	Add COMAIR logo to the cover page	
OCT. 12, 2010	1.3	Modify 3. FEATURES	4
MAY 23, 2008	1.2	Modify 8. APPLICATION CIRCUITS.	16-21
JUL. 04,2006	1.1	1. Modify the 9.2 Ordering Information. 2. Delete the 9.3.2 PLCC84. 3. Modify the 8. APPLICATION CIRCUITS.	21 24 15-20
DEC. 14, 2005	1.0	Original Note: The GPCE040A data sheet v1.0 is a continued version of SPCE040A data sheet v0.4.	27