DATA SHEET

GPBA01B

Bus Extender

MAY 28, 2007

Version 1.1

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BUS EXTENDER

1. GENERAL DESCRIPTION

GPBA01B, a low cost 8-bit bus extender (BEX) by GENERALPLUS, manipulates two pins, MC0 and MC1, to receive the multiplexed 8-bit address/data bus from main processor, e.g. GENERALPLUS GPL13x and GPLB3x and…etc. GPBA01B is able to facilitate the expansion of memory capacity up to 4M bytes of RAM/ROM/EPROM/FLASH, or 25 I/O pins. Users may concatenate numbers of GPBA01B (up to 7) to fit application needs. Plus, GPBA01B equips a Clock divider to easily generate clock for IR application or any other applications. As compared with GPBA01A, majority of functions are identical, but AC characteristics have better performance and DVP mode is phased out.

2. FEATURES

- Fully compatible with GPBA01A expect DVP mode
- A speed-up version of bus extender*:
- One GPBA01B Expansible up to 4M bytes or 25I/Os.
- Daisy chain logic concatenates up to 7 extenders
- Supports varieties of memory types: SRAM, ROM, EPROM, EEPROM and FLASH

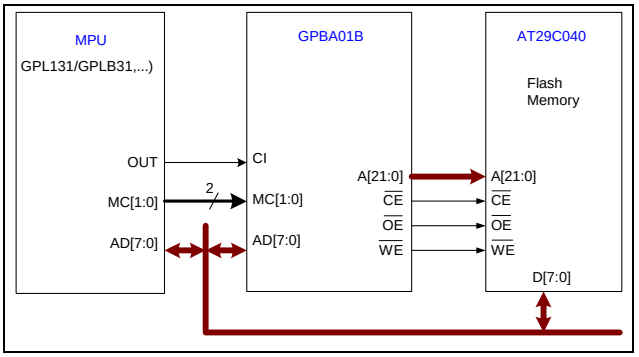
Note: when co-work with Generalplus controller, e.g. GPL13X or GPLB3X series and GPR23LXXX Mask ROM series, it is applicable to 4MHz@2.4V 6MHz@3.6V.

3. APPLICATION FIELD

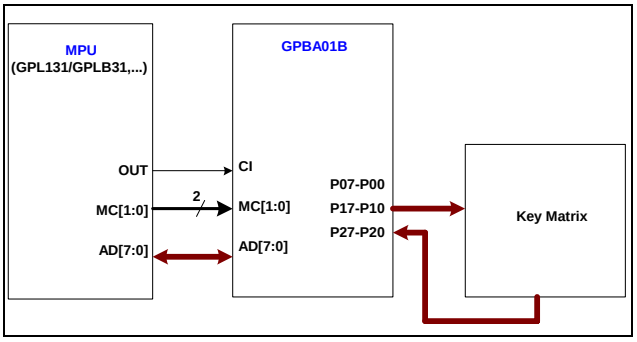
Memory extension, I/O extension for data bank and any others.

4. BLOCK DIAGRAM

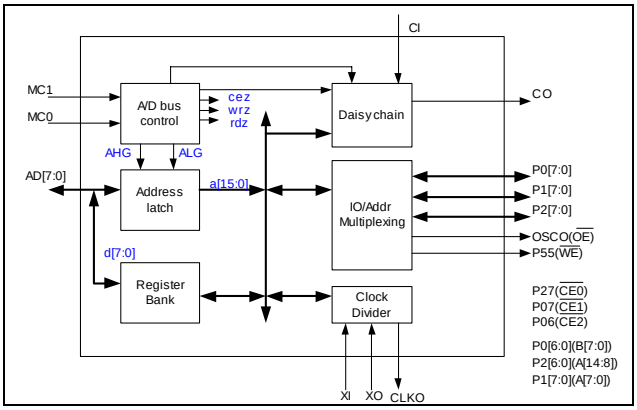
4.1. Work as Memory Extender



4.2. Work as I/O Extender



4.3. GPBA01B Block Diagram



5. SIGNAL DESCRIPTIONS

Mnemonic	History alias	PIN No.	Type	Description
CI	PCI	17	I	Cascade in for daisy chain
CO	PCO	16	O	Cascade out for daisy chain
AD7 - AD0	PD7 - PD0	4 - 11	I/O	Multiplexing Address/Data bus(AD BUS)
MC1, MC0	PMC1, PMC0	1, 2	I	Input pins to indicate AD bus status
P27($\overline{CE0}$) P26 - P20	XP27 - XP20	27 26 - 20	I/O	P2 are short for P27-P20. **Memory extender** P27($\overline{CE0}$): Memory-0 chip-enable pin P26-P20: Memory offset address A[14:8]. **I/O extender** Input Mode: Pull-low internal Output Mode: Pure
P17 - P10	XP17 - XP10	37 - 44	I/O	P1 are short for P17-P10. **Memory extender** P17-P10: Memory offset address A[7:0]. **I/O extender** Input Mode: Pull-low internal Output Mode: Pure
P07($\overline{CE1}$) P06($\overline{CE2}$) P05 - P00	XP07 - XP00	28 29 30 - 35	I/O	P0 are short for P07-P00. **Memory extender** P07($\overline{CE1}$): Memory-1 chip-enable pin P06/($\overline{CE2}$): Memory-2 chip-enable pin P06-P00: Memory bank address B[6:0], GPBA01B support up to 128 banks, each bank is 32K bytes. **I/O extender** Input Mode: Pull-low internal Output Mode: Pure
OSCO($\overline{OE}$)	PRDZ	18	O	**Memory extender** OSCO($\overline{OE}$): External memories output-enable signal **I/O extender** Output only: 1.84MHz oscillator output
P55($\overline{WE}$)	PWRZ	19	O	**Memory extender** P55($\overline{WE}$): External memories write-enable signal **I/O extender** Output only control by B5 of $0023
XI	XTAL1	12	I	1.84 MHz crystal input (20p capacitor required)
XO	XTAL2	13	O	1.84 MHz crystal output (20p capacitor required)
CLKO	ICLK	15	O	Clock divider output
VDD		36	I	Positive supply
VSS		3	I	Ground reference
DVP		14	I	Test mode, please leave it open. Pull-low internal.

Note1: Fully compatible with GPBA01A, expect DVP mode is discarded.

Note2: There are built-in pull low resistors at all input and bi-direction pins except AD [7:0], MC0, MC1, CI. The pull low resistors of bi-direction pin are disabled when working in output mode.

Note3: Internal pull-low resistor with value of approx. 37K Ohms @ VDD = 5.0V; 78K Ohms @ VDD = 3.0V.

Note4: Generalplus strongly recommend user use **Mnemonic** name instead of **History alias** for easy understanding.

Note5: Physical addresses are concatenated from {B [6:0], A [14:8], A [7:0]}.

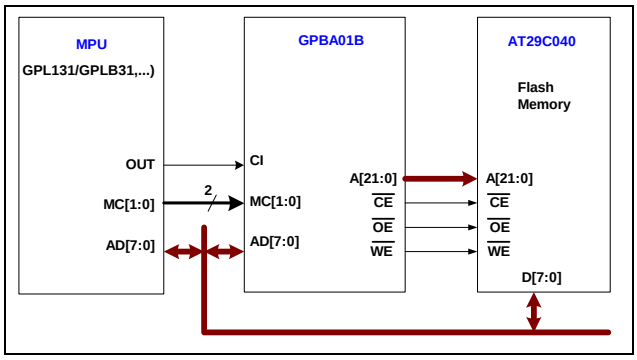
6. FUNCTIONAL DESCRIPTIONS

6.1. The Easiest System

Bus extender (BEX) plays a role as an interface between MPU (GPLB31, GPL131…) and general-purposed (third-party) memory products. In fact, the BEX is a bus translator that translates the AD bus of BMI[tm] to the general-purposed memory bus.

Below figure show the easiest way to use GPBA01B, the MPU send 11 signals to GPBA01B, GPBA01B latch the address and then send it to AT29C040 flash memory, GPBA01B also have responsibility to generate $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ to the memory. On read cycle, the memory output the data at the common bus (AD7-AD0); while write cycle, GPL131 drive the written-data to AD7-AD0.

The AD bus (AD7-AD0) may Address High-Byte (AH), Address-Low-Byte (AL) and 8-bit bi-direction data. Also, the AD bus is common for MPU, GPBA01B, and memory. All of these may drive the bus depending on MC1, MC0 status.



6.2. Address/Data Bus Control

The GPBA01B (Bus extender) is a bridge between MPU (GPL130A, GPLB31A…) and general-purposed (third-party) memory products. The MC1 and MC0 are the control signals for AD7-AD0, which can be three states: Address High-Byte (AH), Address-Low-Byte (AL) and 8-bit bi-direction data.

When MC1 is high, AD [7:0] functions as an address-bus, otherwise the AD [7:0] becomes a data-bus. In address-bus mode, AD [7:0] signifies high-address, A [15:8], when MC0 is high; in contrast, AD [7:0] expresses low-address, A [7:0], when MC0 is low. In data-bus mode, AD [7:0] represents data, D [7:0], which will be read from CPU when MC0 is high and CPU writes data to AD [7:0] when MC0 is low.

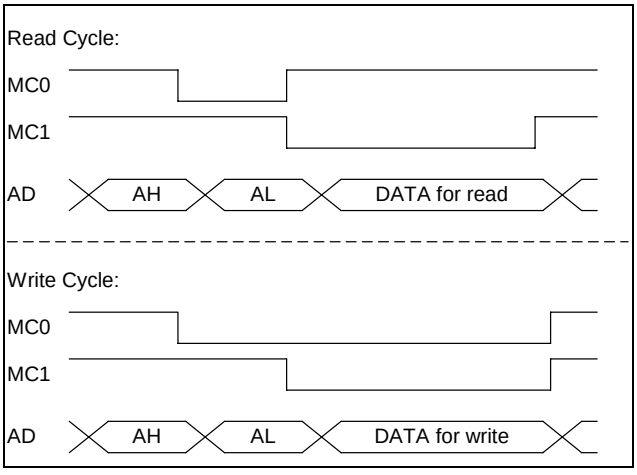
P0, P1, P2, $\overline{WE}$, $\overline{OE}$ can be utilized as address-line, chip-enable, output-enable or write-enable for addressing external memory chip (please refer to ***Bus Extender Pin Assignment for 8 configurations***). The number of pins needed for addressing depends on configuration and the remaining pins used for I/O port. When used as memory extender, chip-enable ($\overline{CE}$), output-enable ($\overline{OE}$) and write-enable ($\overline{WE}$) operate in negative logic (voltage low stands for active, and voltage high stands for inactive). The address lines include A [14:0] (presenting CPU address) and B [6:0] (presenting bank register).

6.2.1. Decode table

MC1 decides AD bus to be address or data bus, and MC0 decides operation mode (Read or Write).

MC1	MC0	AD BUS
H	H	AH
H	L	AL
L	H	Data for Read
L	L	Data for Write

6.2.2. Timing relations between control signals, AH, AL and data.



6.3. Example on Address Mapping

```
1. CI=0
2. CI=1
3. %MOV   P_0DH_BMIVolumeID,#%00000001
4. %MOV   P_23H_BEXConfig,#%1100-0000        ; set CFG=6(B[7:5]), three 1MB memory enable
5. %MOV   P_00H_BankSelect,#%1010-0000       ; select MEM1's bank0,(i.e. CE1 will active when access)
6. %MOV   0x8000, 0x1111                     ; write 0x1111 to MEM0[0x00000]
7. %MOV   0xBFFF, 0x2222                     ; write 0x2222 to MEM0[0x03fff]
8. %MOV   0x4000, 0x3333                     ; write 0x3333 to MEM0[0x04000]
9. %MOV   0x7fff, 0x4444                     ; write 0x4444 to MEM0[0x7ffff]
10.%MOV   P_00H_BankSelect,#%1010-0001       ; select MEM1's bank1
11.%MOV   0x8000, 0x5555                     ; write 0x5555 to MEM0[0x08000]
12.%MOV   0xBFFF, 0x6666                     ; write 0x6666 to MEM0[0x0bfff]
13.%MOV   0x4000, 0x7777                     ; write 0x7777 to MEM0[0x0c000]
14.%MOV   0x7fff, 0x8888                     ; write 0x8888 to MEM0[0xfffff]
```

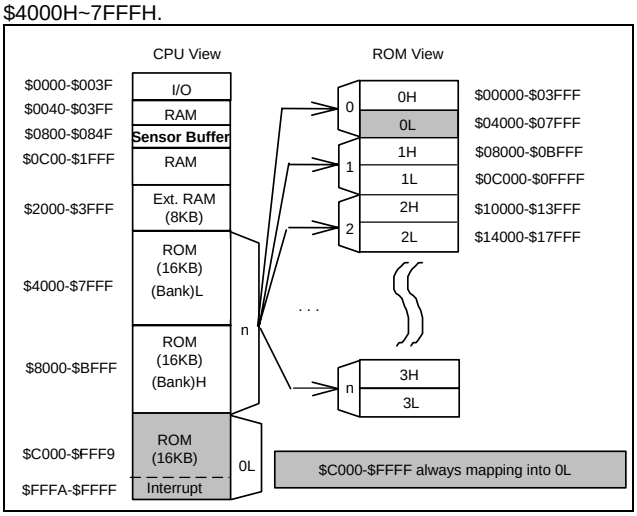
After consecutive 8 write

ADDRESS	DATA	Memo
00000H	1111H	BANK0, 32KB per bank
…	…	
03FFFH	2222H	
04000H	3333H	
…	…	
07FFFH	4444H	
08000H	5555H	BANK1
…	…	
0BFFFH	6666H	
0C000H	7777H	
…	…	
0FFFFH	8888H	
10000H	…	BANK2
…	…	…

6.4. Address Mapping on a System

Bus extender usually use $4000~$BFFF for memory extension, while $0000~003f for register setting.

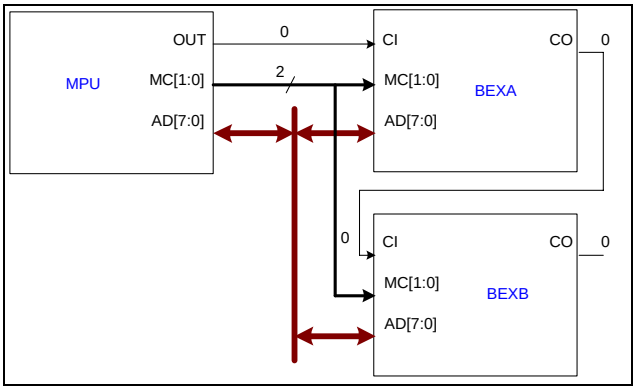
Each bank are 32K bytes, $8000H~$BFFFH are mapped to $0000H~$3FFFH; $4000H~$7FFFH are mapped to $4000H~7FFFH.



6.5. Daisy Chain

There are 11 pins connecting from MPU to BEX, except MC0, MC1, and AD bus. In addition, there is another pin, named CI, the Cascade-In of BEX. When CI goes from low to high, the VID/SID of BEX will be reset and must be setup. When accessing BEX, the CI pin must keep in logical high level.

Both CI and CO provide the circuitry to concatenate up to seven BEX. In such case, the CO (Cascade-Out) of the former BEX is connected to the CI of next BEX to form a daisy-chain. After CI of 1st BEX goes from low to high, the 1st setting of Volume ID, VID, (setting $000DH) will apply to the 1st BEX. After the 1st BEX is configured, it will raise its CO. The CO of the 1st BEX is connected with the CI of the 2nd BEX; as a result, the configuration will apply to the 2nd BEX, and…etc.



For correction operation, if there are 5 BEXs on the system, issue exactly five unique VID.

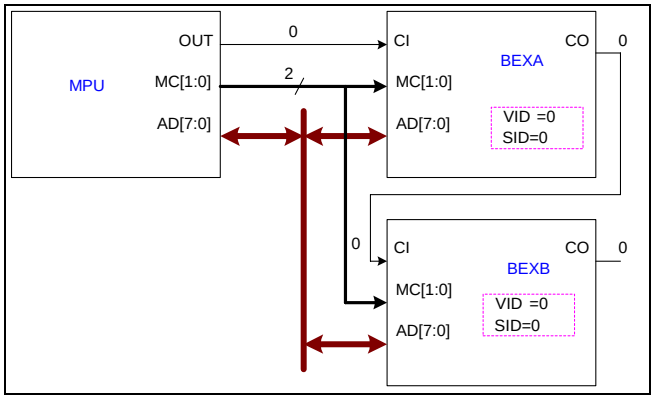
After all VID have been set, any writing activity to $000D will be taken as "selecting". For example, after setting the VID of the BEXs as 1, 2, 3... up to 7, simply write 3 to $000DH to select and access it when MPU intends to access BEX of ID 3.

Note that the sequence of ID is not necessary of 1, 2, 3...7. The user is allowed to set the IDs as 3, 2, 1... or 7,2,4... Just keep in mind that the 1st ID is applied to the 1st BEX in the daisy chain. The 0 is not a valid ID.

Because we want all BEXs to share the same BMI, every BEX needs two variables, Volume-ID (VID) and Select-ID (SID) inside. We must send unique VID to every BEX and then we should choose one of these BEX by setting SID. **At any time, only one BEX can operate**. Which BEX will be activated depending on which BEX has VID=SID (but VID cannot be 0). $000DH register is used for set both VID and SID, but VID can be written once only. When MPU sends OUT=0, CI of BEXA=0 causes VID, SID, CO of BEXA=0, too; CO of BEXA always causes VID, SID, CO of BEXB=0. Finally, all functions in these two GPBA01B are disabled and all registers remain at the previous states, except volume-id (**VID**) and select-id (**SID**), which are reset to zero.

6.5.1. Example

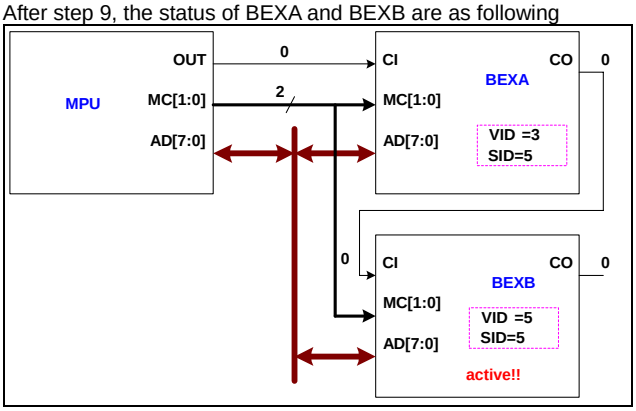
We will describe the action of two BEX on the daisy chain as follows. It's important that MPU shares bus with BEXs. How can we identify BEX and send a unique VID to each BEX? It is achieved by CI and CO.



$000DH register works for setting a unique VID for each BEXs, and then acts as SID only. VID are write-once register. The first step is accessing BEXA and then accessing BEXB as follows:

1. MPU's OUT=0
2. MPU's OUT=1
3. Send_addr_data($000d,$03)
   ; Set 3 to **VID** of BEXA(VID write once)
4. Send_addr_data($000d,$05)
   ; Set 5 to **VID** of BEXB(VID write once)
5. Send_addr_data($000d,$03)
   ; Set 3 to **SID** of BEXA and BEXB
   (**BEXA active**, BEXB inactive)
6. Send_addr_data($0023,$XX)
   ; Configure BEXA as 'Memory extender' or 'I/O extender'
7. (**Access BEXA….**)
8. …..
9. Send_addr_data($000d,$05)
   ; Set 5 to **SID** of BEXA and BEXB
   (BEXA inactive, **BEXB active**)
10. Send_addr_data($0023,$XX)
    ; Configure BEXB as 'Memory extender' or 'I/O extender'
11. (**Access BEXB…..**)

After step 9, the status of BEXA and BEXB are as following



6.5.2. Configuration

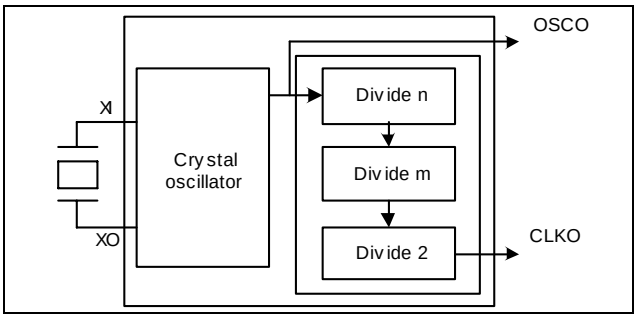
BEX has two modes: memory extender (major mode), and I/O extender. As we use the BEX, we need to set configuration register immediately after volume-id is given. Writing to B[7:5] of $0023H establishes the GPBA01B configurations. .

When GPBA01B works as memory extender, it can extend from 1 to 3 memories, depending configuration. Please refer to ***Register description*** chapter.

When using as I/O extender, P0, P1 and P2 are bi-directional pins. The value written to B[4:0] of $0023H defines directions. Logical "1" stands for output and logical "0" stands for input. Specially, P55 ($\overline{WE}$) and OSCO ($\overline{OE}$) cannot operate in input direction.

6.6. Clock Divider

Writing to PS [1:0] (B [5:4] of register $0021H) and CDP [7:0] (register $0022H) sets the frequency of CLKO out. Writing a logical one to OSCE (B7 of register $0021H) makes the crystal oscillator enable. Writing a logical zero to OSCE makes the crystal oscillator disable, and reduces power consumption. When both OSCE and CLKOE are logical one, CLKO is enabled.



OSCE	CLKOE	OSCO	CLKO
0	X	H	L
1	0	Freq1	L
1	1	Freq1	Freq2

Freq1 is dependent on crystal.

Freq2 = freq1/ (m*n*2), where n=2^PS [1:0],

m=256-(CDP [7:0] value)

OSCO is available in CFG0 and CFG1

7. REGISTER DESCRIPTION

7.1. P_00H_BMIBank ($0000) (W)

Bank Selection Register

	B7	B6	B5	B4	B3	B2	B1	B0
W	**must be1**	BANK6	BANK5	BANK4	BANK3	BANK2	BANK1	BANK0

B6 - B0 are BANK6-BANK0. The extended memory is dividing into banks, 32K bytes per bank. Each AD BUS cycle can only address up to 32KB. To access another bank, you should issue P_00H_BMIBank ($0000) command. When GPBA01B connects to one 4MB memory, B6 - B0 are bank selections for total of 128 banks. In CFG=6 mode, one GPBA01B can support up to three memory; thus, B6 - B5 act as memory selections while B4 - B0 act as bank selection.

7.1.1. CFG=3 Example

CFG=3, one 4MB is configured and B6 - B0 are all for 128-bank selections.

B6-B0	Description
B6	A21
B5	A20
B4	A19
B3	A18
B2	A17
B1	A16
B0	A15

7.1.2. CFG=6 Example

CFG=6, three 1MB are configured and B4 - B0 are for 32-bank selections.

B6-B5	Description
00	$\overline{CE2}$ will be asserted
01	$\overline{CE1}$ will be asserted
1X	$\overline{CE0}$ will be asserted

B6-B0	Description
B4	A19
B3	A18
B2	A17
B1	A16
B0	A15

7.2. P_0DH_BMIVolumeID ($000D) (W)

Bus memory Volume ID Setup & Selection

	B7	B6	B5	B4	B3	B2	B1	B0
Write-once	-	-	-	-	-	VID2	VID1	VID0
W	-	-	-	-	-	SID2	SID1	SID0

VID [2:0]: Volume-ID for unique identify the GPBA01B on the daisy-chain, write once only.

SID [2:0]: Select-ID for selection one of GPBA01Bs on the daisy-chain.

7.3. P_20H_BEXPort0 ($0020)(R/W)

Extender Port0

	B7	B6	B5	B4	B3	B2	B1	B0
W/R	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

I/O extender: P07-P00: bi-direction port to communication with external device. The direction is set by B [2:0] of $0023.

Memory extender: No function.

7.4. P_21H_BEXPort1 ($0021) (R/W)

Extender Port1 & Function Control (W)

	B7	B6	B5	B4	B3	B2	B1	B0
W/R	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
W	OSCE	CLKOE	PS1	PS0	**1**	X	X	X

I/O extender: P17-P10: bi-direction port to communicate with external device. The direction is set by B3 of $0023.

Memory extender: OSCE: Oscillator Enable

CLKOE: Clock Output Enable

PS [1..0]: Pre-scalar Counter

B3: Must be 1.

7.5. P_22H_BEXPort2 ($0022) (R/W)

Extender Port2 & ClockDividerPreload (W)

	B7	B6	B5	B4	B3	B2	B1	B0
W/R	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
W	CDP7	CDP 6	CDP 5	CDP 4	CDP 3	CDP 2	CDP 1	CDP 0

I/O extender: P27-P20: bi-direction port to communication with external device. The direction is set by B4 of $0023.

Memory extender: CDP [7:0]: Clock divider preload value.

7.6. P_23H_BEXConfig ($0023)(W)

Bus Extender Configuration

	B7	B6	B5	B4	B3	B2	B1	B0
W	CFG2	CFG1	CFG0 P55	DIR2	DIR1	DIR03	DIR01	DIR00

CFG [2..0]: Bus Extender Configuration Number (0~7)

P55: ExterndPort55 Output Bit (P55 is output pin only)

DIR2: ExtendPort2 Control (1: Output, 0: Input)

DIR1: ExtendPort1 Control (1: Output, 0: Input)

DIR03: ExtendPort0 [7..3] Control (1:Output, 0: Input)

DIR01: ExtendPort0 [2..1] Control (1:Output, 0: Input)

DIR00: ExtendPort0.0 Control (1: Output, 0: Input)

Note 1: P55 is available for output only if CFG=0 or 1

Note 2: If the extend port is configured as input, there will be an internal pull-low resistor (37K Ohms @ VDD=5V or 78K Ohms @ VDD=3V).

7.6.1. Bus extender pin assignment for 8 configurations

PINs Name	Configuration Register $0023[7:5]							
	000(I/O)	001(I/O)	010(32KB)	011(4MB)	100(1MB)	101(4MB)	110(1MB)	111(2MB)
P00	I/O	I/O	I/O	B0	B0	B0	B0	B0
P01	I/O	I/O	I/O	B1	B1	B1	B1	B1
P02	I/O	I/O	I/O	B2	B2	B2	B2	B2
P03	I/O	I/O	I/O	B3	B3	B3	B3	B3
P04	I/O	I/O	I/O	B4	B4	B4	B4	B4
P05	I/O	I/O	I/O	B5	I/O	B5	I/O	B5
P06	I/O	I/O	I/O	B6	I/O	B6	$\overline{CE2}$	$\overline{CE2}$
P07	I/O	I/O	I/O	I/O	$\overline{CE1}$	$\overline{CE1}$	$\overline{CE1}$	$\overline{CE1}$
P10	I/O	I/O	A0	A0	A0	A0	A0	A0
P11	I/O	I/O	A1	A1	A1	A1	A1	A1
P12	I/O	I/O	A2	A2	A2	A2	A2	A2
P13	I/O	I/O	A3	A3	A3	A3	A3	A3
P14	I/O	I/O	A4	A4	A4	A4	A4	A4
P15	I/O	I/O	A5	A5	A5	A5	A5	A5
P16	I/O	I/O	A6	A6	A6	A6	A6	A6
P17	I/O	I/O	A7	A7	A7	A7	A7	A7
P20	I/O	I/O	A8	A8	A8	A8	A8	A8
P21	I/O	I/O	A9	A9	A9	A9	A9	A9
P22	I/O	I/O	A10	A10	A10	A10	A10	A10
P23	I/O	I/O	A11	A11	A11	A11	A11	A11
P24	I/O	I/O	A12	A12	A12	A12	A12	A12
P25	I/O	I/O	A13	A13	A13	A13	A13	A13
P26	I/O	I/O	A14	A14	A14	A14	A14	A14
P27	I/O	I/O	$\overline{CE0}$	$\overline{CE0}$	$\overline{CE0}$	X	$\overline{CE0}$	X
OSCO/ $\overline{OE}$	OSCO	OSCO	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
P55/ $\overline{WE}$	LOW	HIGH	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$
Total I/O Available	25	25	8	1	2	0	1	0
No. of Memories available	0	0	1	1	2	1	3	2
Total memory size	0	0	32KB	4MB	2MB	4MB	3MB	4MB

The memory is divided into banks, 32KB per bank. banks are address by B6-B0, while A14-A0 are offset address of bank.

ITEM	Description	Memo
B6-B0	**Memory extender:** Bank selection pin	
A14-A0	**Memory extender:** Address pin to access 32KB memory in a bank	
$\overline{CE2}$, $\overline{CE1}$, $\overline{CE0}$	**Memory extender:** Chip enable pin	
X	**Memory extender:** Don't use.	
I/O	**I/O extender:** Pins can be configured as input or output	
O	**I/O extender:** Output pin only	
OSCO	**I/O extender:** Crystal output	
P55	**I/O extender:** When CFG=0 output Low, when CFG=1 output High	

7.6.2. Memory Mapping Summary with Configuration 2~7

Mapping Address	Bank Select Value($0000)	Mode	Chip Selection
$2000~$3FFF (8K)		CFG=2	Asserting $\overline{CE0}$ to select last 8KB memory
		CFG=4	Bank, with b[4:0] become 11111.
		CFG=5	
		CFG=6	
		CFG=7	
$8000~$BFFF $4000~$7FFF (32K each bank, mainly used for memory extension)	1XXXXXXX	CFG=2	Access 32KB Memory with $\overline{CE0}$
	1BBBBBBB	CFG=3	Access 4MB Memory with $\overline{CE0}$
	10XBBBBB	CFG=4	Access 1MB Memory with $\overline{CE1}$
	11XBBBBB	CFG=4	Access 1MB Memory with $\overline{CE0}$
	1BBBBBBB	CFG=5	Access 4MB Memory with $\overline{CE1}$
	100BBBBB	CFG=6	Access 1MB Memory with $\overline{CE2}$
	101BBBBB	CFG=6	Access 1MB Memory with $\overline{CE1}$
	11XBBBBB	CFG=6	Access 1MB Memory with $\overline{CE0}$
	10BBBBBB	CFG=7	Access 2MB Memory with $\overline{CE2}$
	11BBBBBB	CFG=7	Access 2MB Memory with $\overline{CE1}$

Note1: “B” is for extender memory bank selection; “KB” means K-byte and “MB” for M-byte.

Note2: “X” means “don’t care” which has no effect on bank selection.

8. STANDBY CONDITION

Item	Description
CI	VDD VSS
MC1-MC0	VDD
AD7-AD0	VDD or VSS
P0, P1, P2	Memory extender: Leave open I/O extender: Output mode: inhibit any pull-low or pull-up Input mode: leave open or VSS
DVP	Leave open or VSS
Register OSCE(B7 of $0021)	**Must be set to 0**

9. PCB LAYOUT CONSIDERATION

Due to MC0 and Mc1 are edge triggering signal, the trace must be as short as possible; shielding with ground signal is better.

10. ELECTRICAL SPECIFICATIONS

10.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +70℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Ratings table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

10.2. DC Characteristics (VDD = 2.4V - 5.5V, T_A = 0℃ to 70℃)

Characteristics	Symbols	Limits			Units	Test conditions
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	5.5	V	-
Operating Current	I_{CC}	-	0.32	0.6	mA/MHz	VDD = 2.4V, C_L = 10pF
		-	0.55	1.0	mA/MHz	VDD = 3.6V, C_L = 10pF
		-	0.88	2.0	mA/MHz	VDD = 5.5V, C_L = 10pF
Operating Current	I_{CC2}	-	1.4	3.0	mA/MHz	VDD = 2.4V, C_L = 50pF
		-	2.3	4.0	mA/MHz	VDD = 3.6V, C_L = 50pF
		-	3.6	6.0	mA/MHz	VDD = 5.5V, C_L= 50pF
Standby Current	I_{STBY}	-	-	1.0	μA	All signal un-toggle, ***T_A = 25℃***
Input High Voltage	V_{IH}	0.7VDD	-	VDD	V	-
Input Low Voltage	V_{IL}	-0.3V	-	0.2 VDD	V	-
Output High Voltage	V_{OH}	0.75 VDD	-	-	V	I_{OH} = 1.0mA @ 2.4V I_{OH} = 1.5mA @ 3.0V I_{OH} = 4mA @ 5.0V
Output Low Voltage	V_{OL}	-	-	0.15VDD	V	I_{OL} = 0.8mA @ 2.4V I_{OL} = 1.2mA @ 3.0V I_{OL} = 3mA @ 5.0V
Pull-low MOS Current	I_{PL3}	-	38	-	μA	VDD = 3.0V, V_{IN} = VDD
Pull-low MOS Current	I_{PL3}	-	157	-	μA	VDD = 5.0V, V_{IN} = VDD

10.3. AC Characteristics (VDD = 2.4V - 5.5V, T_A = 0℃ to 70℃)

Test Condition V_{IH} = VDD, V_{IL} = 0V, Input Rise and Fall Times = 1ns, I/O Timing Reference Level = VDD/2, Output Load: C_{LOAD} = 100pF

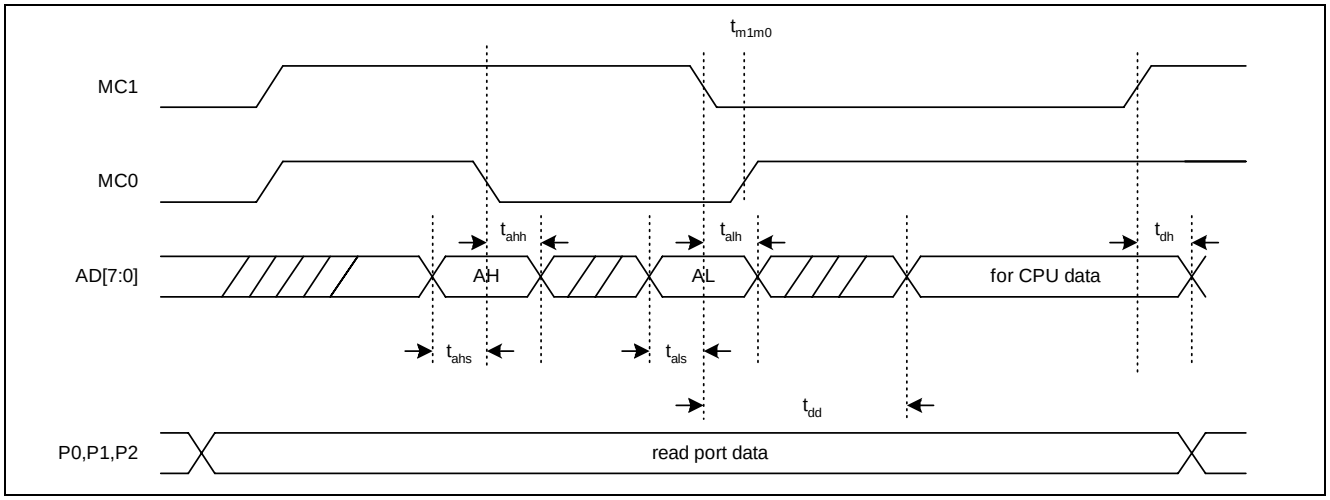
Characteristics	Symbols	Limits			Units	Test conditions
		Min.	Typ.	Max.		
AH Setup Time	T_{ahs}	10	-	-	ns	-
AH Hold Time	T_{ahh}	10	-	-	ns	-
AL Setup Time	T_{als}	10	-	-	ns	-
AL Hold Time[1]	T_{alh}	10	-	25	ns	VDD = 2.4V
		10	-	15	ns	VDD = 3.6V
		10	-	10	ns	VDD = 5.5V
Data Setup Time	T_{ds}	10	-	-	ns	-
Data Hold Time[2]	T_{dh}	10	-	-	ns	-
MC1 Falling to MC0 Rising	T_{m1m0}	-	-	15	ns	VDD = 2.4V
		-	-	9	ns	VDD = 3.6V
		-	-	4	ns	VDD = 5.5V
Address High Delay	T_{ahd}	-	31	49	ns	VDD = 2.4V
		-	21	30	ns	VDD = 3.6V
		-	16	22	ns	VDD = 5.5V
Address Low Delay[3]	T_{ald}	-	32	58	ns	VDD = 2.4V @ ah hold time = 10n
		-	20	31	ns	VDD = 3.6V @ ah hold time = 10n
		-	17	23	ns	VDD = 5.5V @ ah hold time = 10n
MC1 Rising to Chip-enable Falling	T_{cezf}	-	46	69	ns	VDD = 2.4V
		-	28	40	ns	VDD = 3.6V
		-	22	30	ns	VDD = 5.5V
MC1 Rising to Chip-enable Rising	T_{cezr}	-	29	46	ns	VDD = 2.4V
		-	19	28	ns	VDD = 3.6V
		-	14	20	ns	VDD = 5.5V
MC1 Falling to Write-enable Falling	T_{wrzf}	-	36	52	ns	VDD = 2.4V
		-	23	34	ns	VDD = 3.6V
		-	18	23	ns	VDD = 5.5V
MC1 Falling to Write-enable Rising	T_{wrzr}	-	19	25	ns	VDD = 2.4V
		-	13	20	ns	VDD = 3.6V
		-	10	15	ns	VDD = 5.5V
MC1 Falling to Read-enable Falling	T_{rdzf}	-	37	54	ns	VDD = 2.4V
		-	24	35	ns	VDD = 3.6V
		-	18	25	ns	VDD = 5.5V
MC1 Rising to Read-enable Rising	T_{rdzr}	-	24	39	ns	VDD = 2.3V
		-	16	24	ns	VDD = 3.6V
		-	12	17	ns	VDD = 5.5V
Read Port Data Delay Time	T_{dd}	-	54	90	ns	VDD = 2.3V
		-	34	54	ns	VDD = 3.6V
		-	25	37	ns	VDD = 5.5V

Note1: T_{alh} Max value prevent bus fighting.

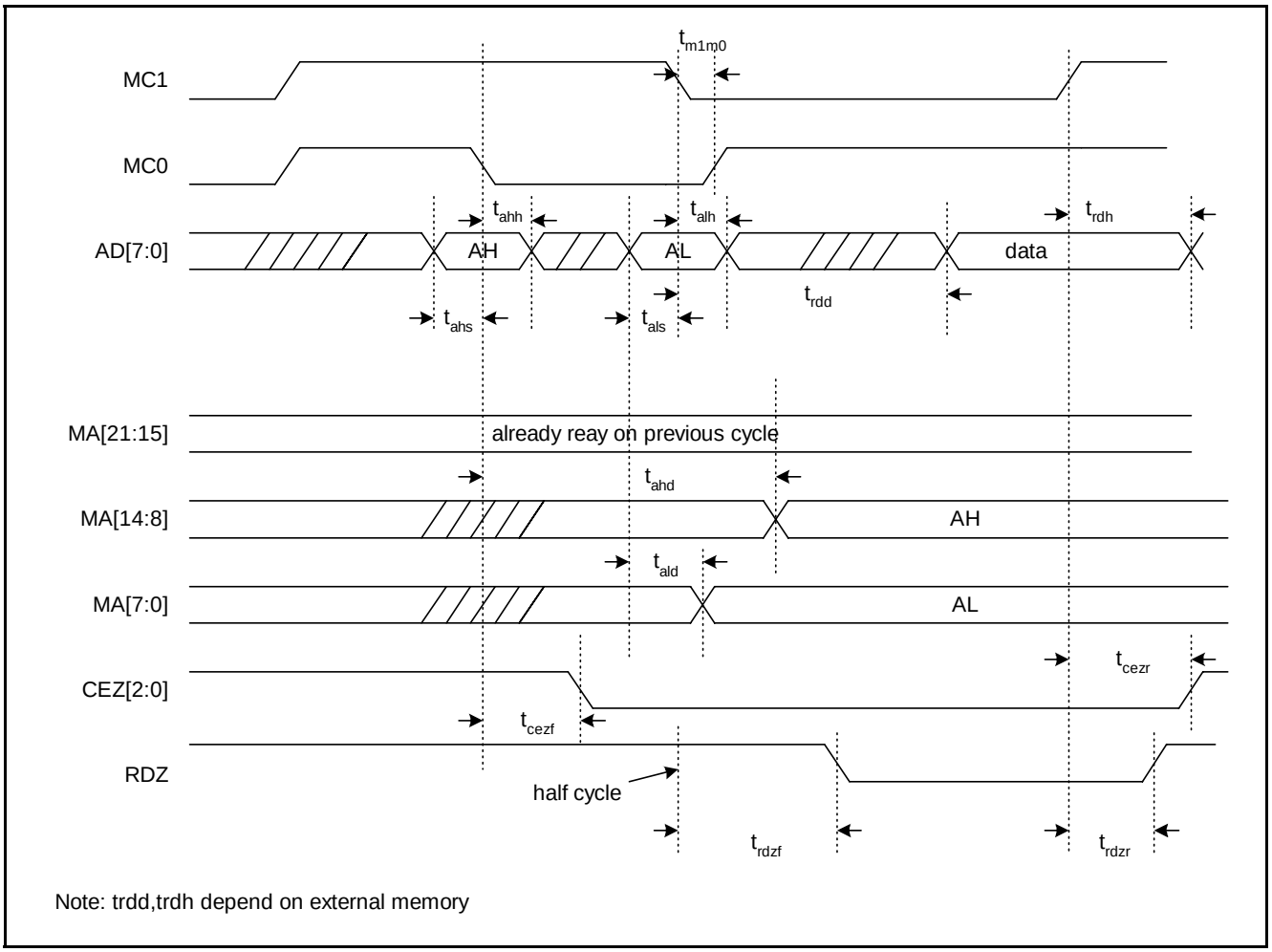
Note2: When write memory cycle, please refer to accompany memory.

Note3: Measure from al_in to al_out.

10.4. Read Port Cycle

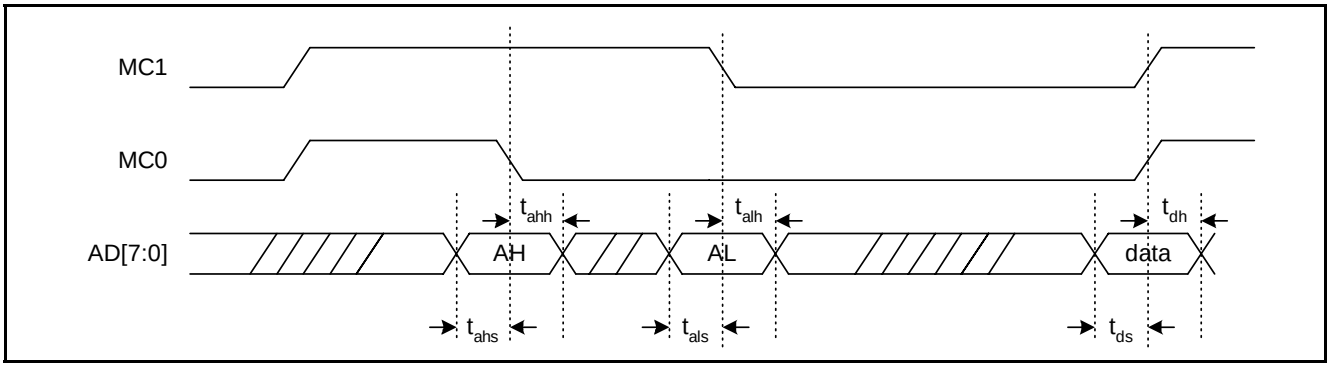


10.5. Read Memory Cycle

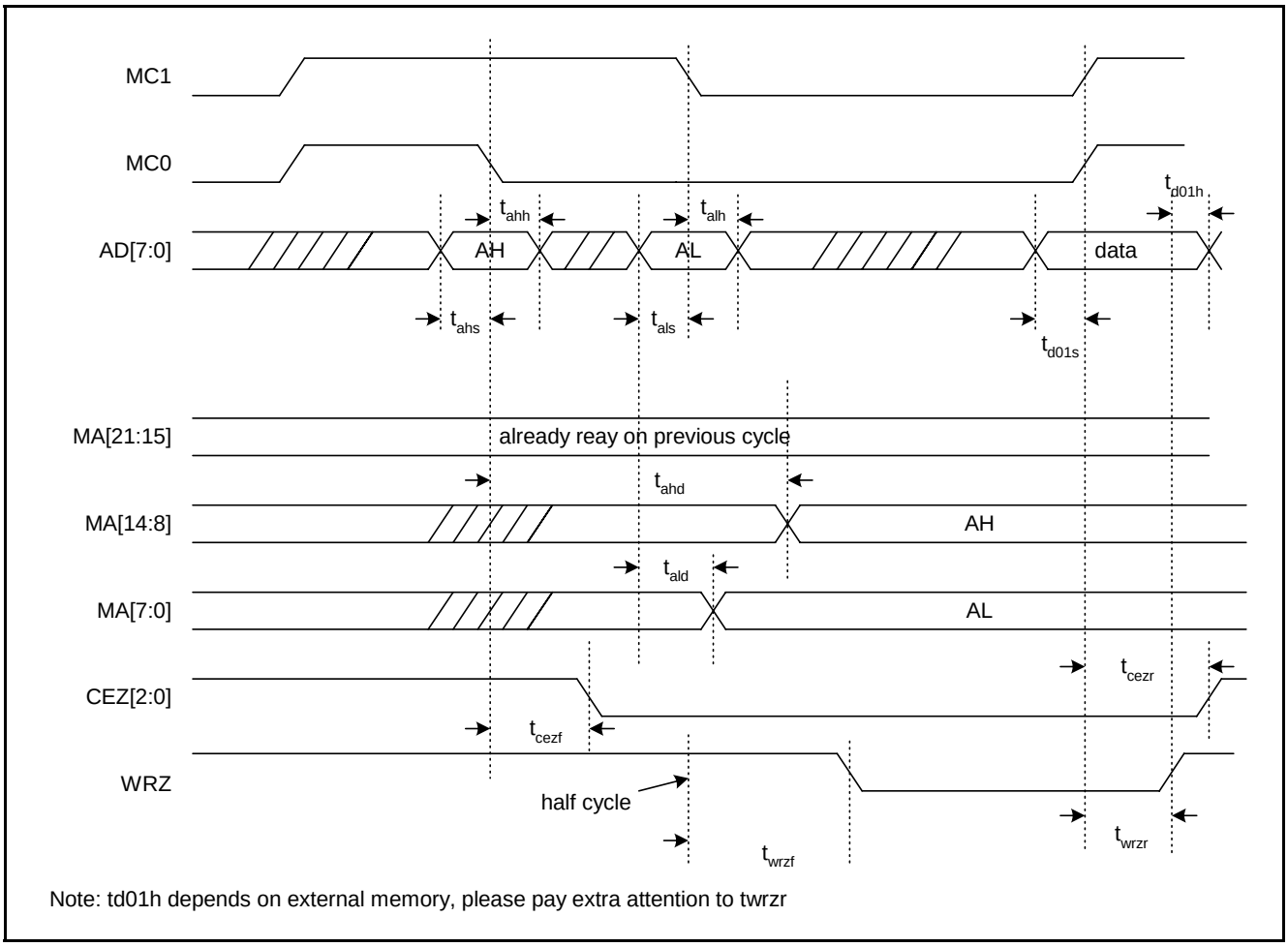


Note: trdd,trdh depend on external memory

10.6. Write Port Cycle



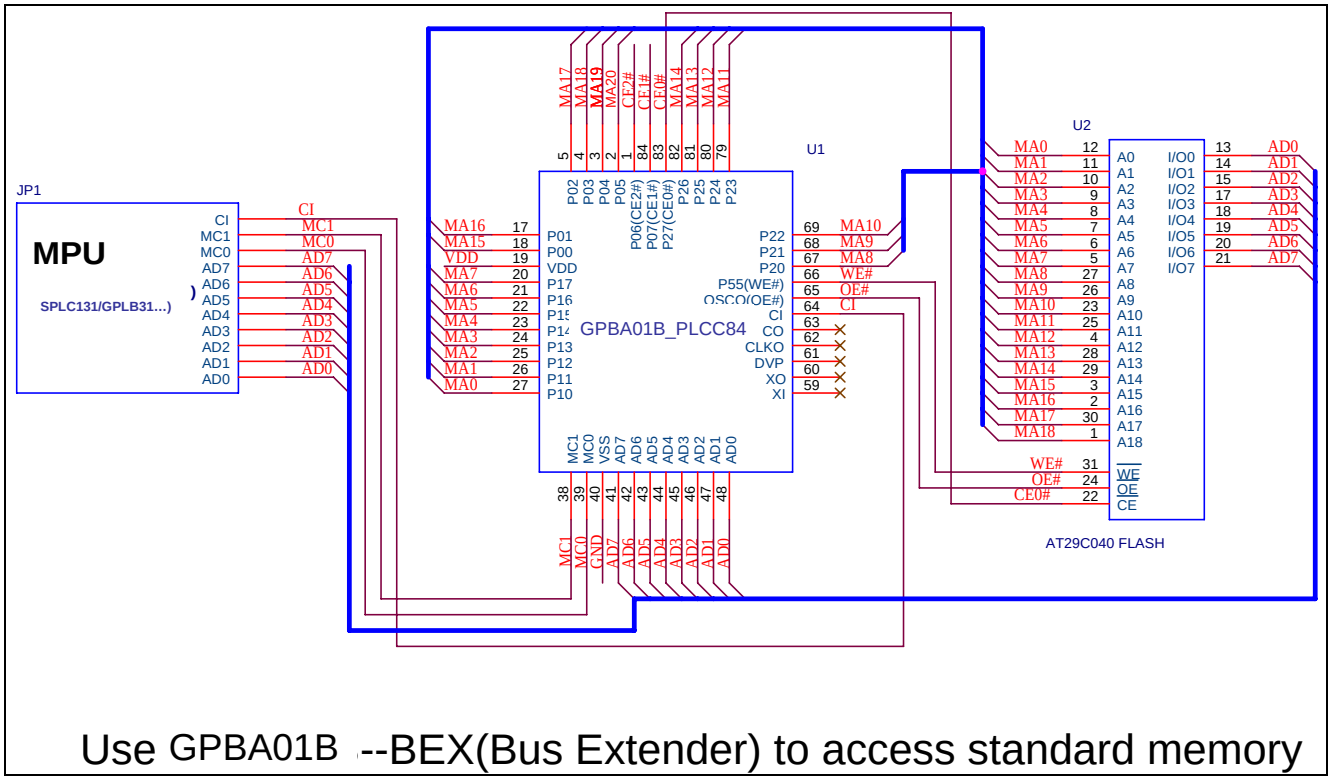
10.7. Write Cycle



Note: td01h depends on external memory, please pay extra attention to twrzr

11. APPLICATION CIRCUITS & EXAMPLE PROGRAM

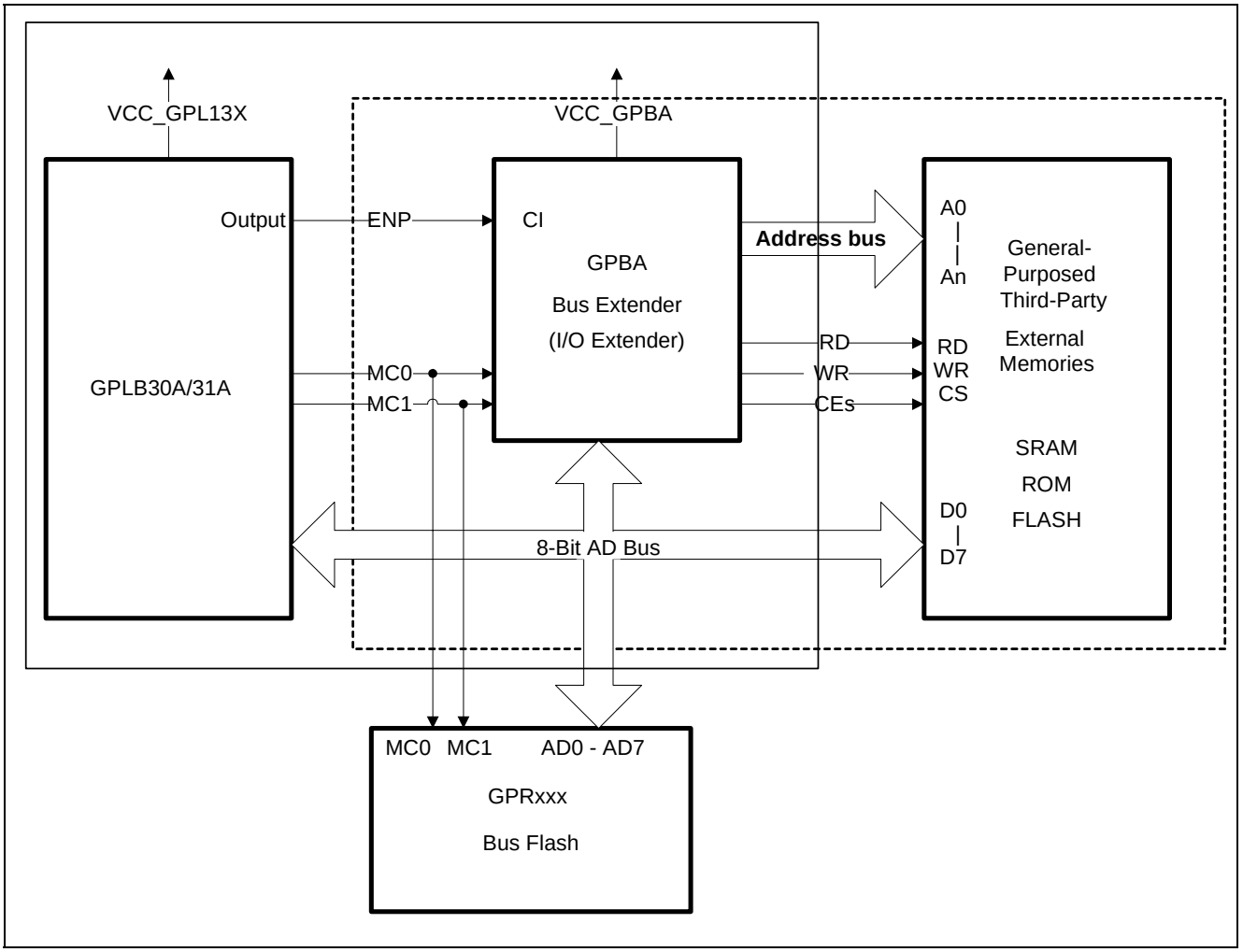
11.1. Simplest Application--One Flash Memory Extension




```
%PullBEXENLow                       ; Set CI to 0
%PullBEXENHigh                      ; Set CI to 1
LDA   #1                            ; Set Volume-ID and Select-IDto 1
STA   P_0DH_BexVolID
LDA   #%011XXXXX                    ; Set CFG=3 for 4MB configuration
STA   P_23H_BEXConfig               ; 128 banks in total(bank0~bank127)
LDA   #%1000-0010                   ; Set bank to 2,
STA   P_00H_BexBank                 ; mapping $8000-$BFFF to $010000-$013FFF
                                    ; mapping $4000-$7FFF to $014000-$017FFF
(access bank 2)
...
LDA   #%1000-0000                   ; Set bank to 0,
STA   P_00H_BexBank                 ; mapping $8000-$BFFF to $000000-$003FFF
                                    ; mapping $4000-$7FFF to $004000-$007FFF
(access bank 0)
...
LDA   #%1111-1111                   ; Set bank to 127,
STA   P_00H_BexBank                 ; mapping $8000-$BFFF to $3F8000-$3FBFFF
                                    ; mapping $4000-$7FFF to $3FC000-$3FFFFF
(access bank 127)
...
```

Note: %PullBEXENLow and %PullBEXENHigh are macros that control the high or low for GPBA01B's CI.

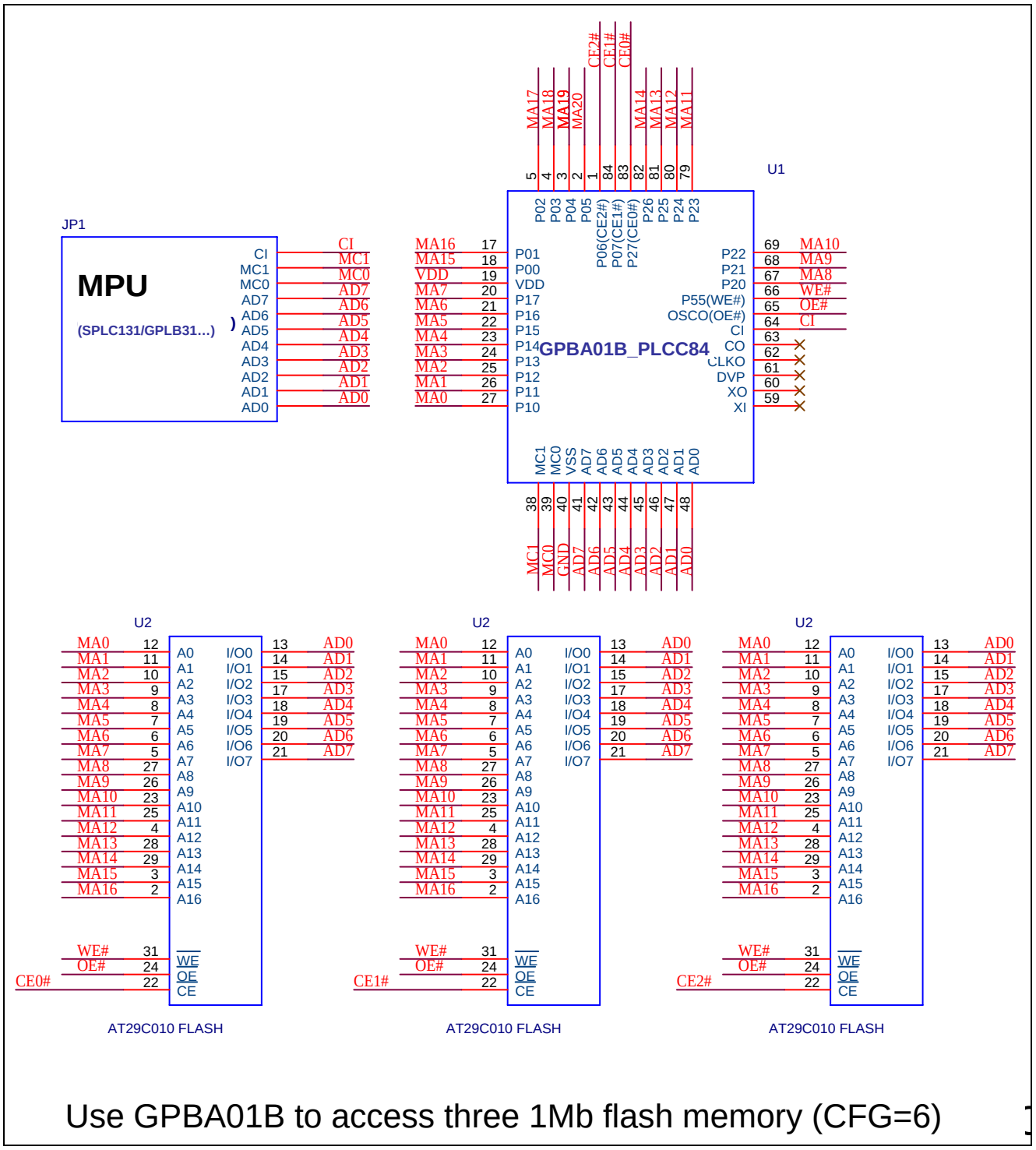
11.2. GPLB30A/31A with Bus Extender and Bus Flash



The area in solid line can be viewed as a micro-controller with address bus.

The area in dash line can be viewed as the memory within the bus extender.

11.3. One BEX with Three Memory

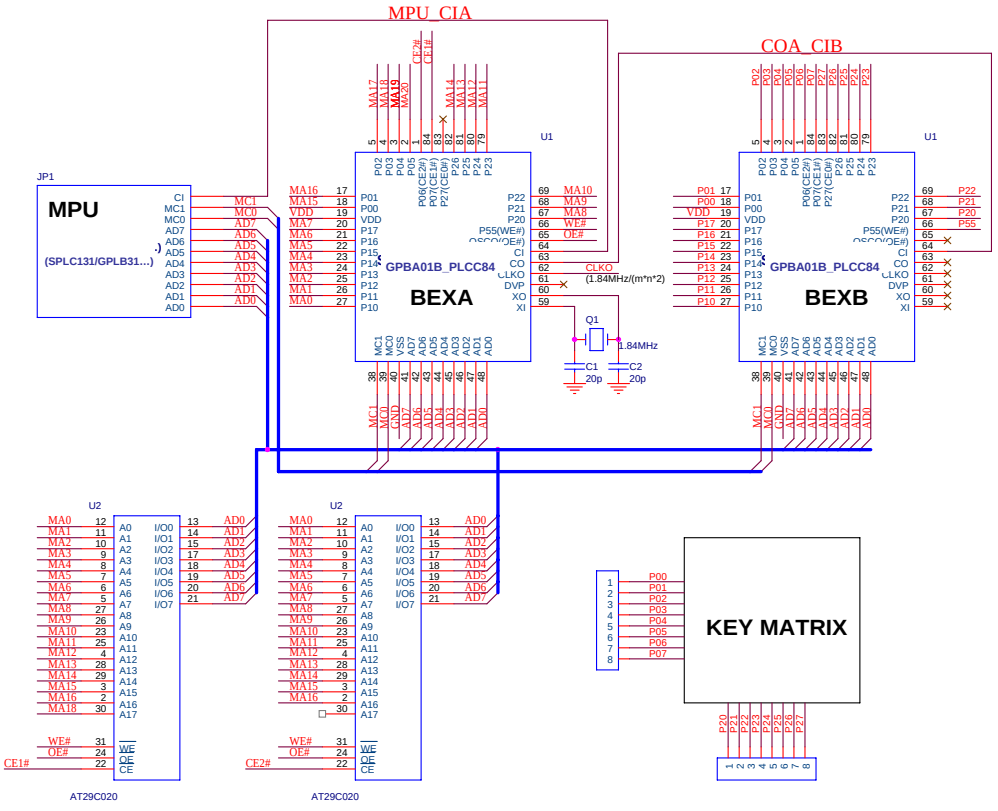


Use GPBA01B to access three 1Mb flash memory (CFG=6)

```
%PullBEXENLow                          ; Set CI to 0
%PullBEXENHigh                         ; Set CI to 1
 LDA    #1                             ; Set Volume-ID and Select-IDto 1
 STA    P_0DH_BexVolID
 LDA    #%110XXXXX                     ; Set CFG=6 for three 1MB configuration
 STA    P_23H_BEXConfig                ; 128 banks in total( bank0~bank127)
 LDA    #%1100-0010                    ; Select memory0, set bank to 2
```

```
STA    P_00H_BexBank
(access memory0 bank 2)
...
LDA    #%101 0-0000                    ; Select memory1, set bank to 0
STA    P_00H_BexBank
(access memory2 bank 3)
...
LDA    #%100 1-1111                    ; Select memory2, set bank to 31
STA    P_00H_BexBank
(access bank 127)
...
```

11.4. Two BEXs form Daisy-Chain



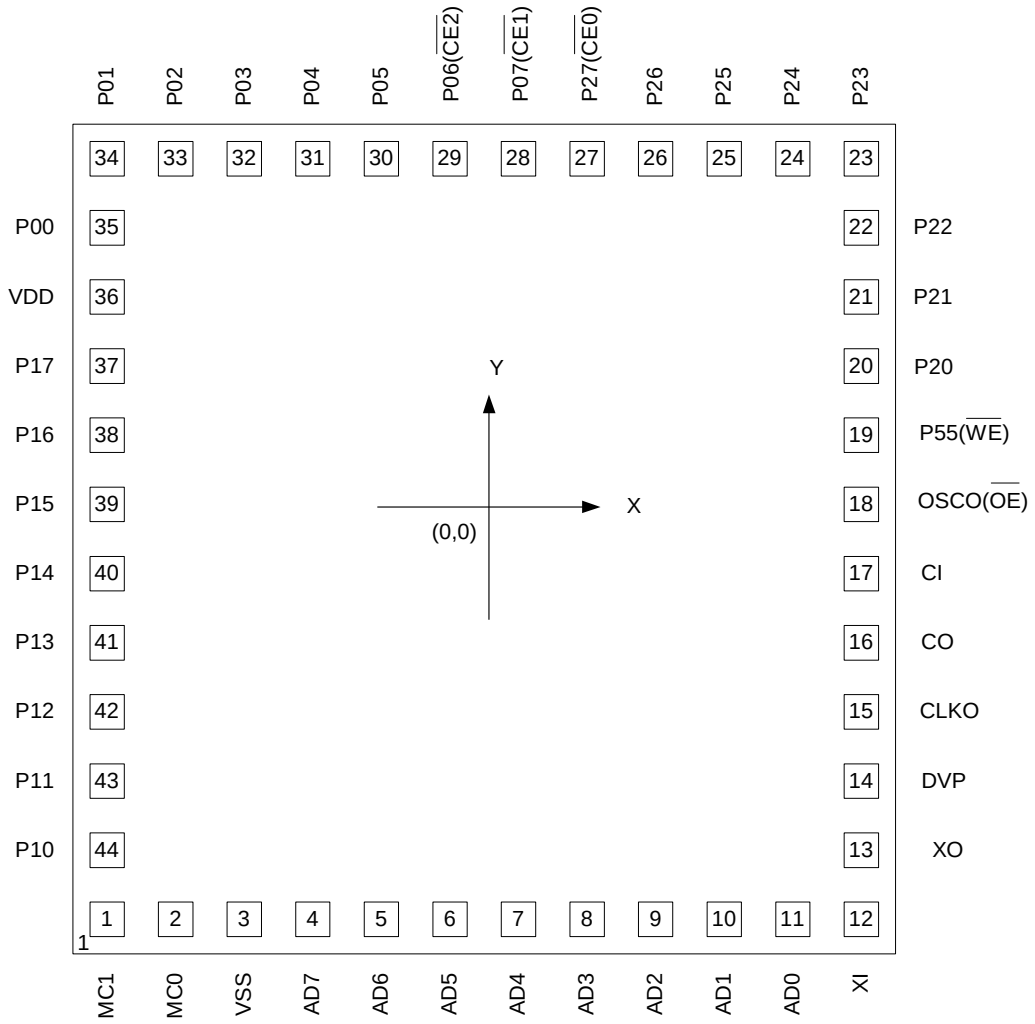
BEXA is memory extender, BEXB is IO extender and clock divider
BEXA CFG=7; BEXB CFG=0

```
%PullBEXENLow                          ; Set CI to 0
%PullBEXENHigh                         ; Set CI to 1
 LDA    #1                             ; Set BEXA Volume-ID to 1, BEXA Select-ID=1
 STA    P_0DH_BexVolID
 LDA    #3                             ; Set BEXB Volume-ID to 3
 STA    P_0DH_BexVolID                 ; BEXA VID=1, SID=3(inactive)
                                       ; BEXB VID=3, SID=3(active)
 LDA    #%000 11111                    ; Set CFG=0 ; BEXB act as IO extender, all port are output
 STA    P_23H_BEXConfig
 LDA    #%10101010                     ; BEXB: P0=AAH
```

```
STA    P_20H_BEXPort0
LDA    #%01010101                    ; BEXB: P2=55H
STA    P_22H_BEXPort2
LDA    #1                            ; BEXA: VID=1, SID=1(active)
STA    P_0DH_BexVolID                ; BEXB: VID=3, SID=1(inactive)
LDA    #%1100-0010                   ; BEXA: Select memory1, set bank to 2
STA    P_00H_BexBank
LDA    #%1110-1000                   ; BEXA: oscillator enable, CLKO enable, pre-scale = 2
STA    P_21H_BEXPort1
LDA    #%0011-1100                   ; BEXA: CDP[7:0]=60, CLKO=1.84MHz/(2^2)/60/2=3.83KHz
STA    P_22H_BEXPort2
(access memory0 bank 2)              ; Access BEXA memory1
...
```

12. PACKAGE/PAD LOCATIONS

12.1. PAD Assignment and Locations



This IC substrate should be connected to VSS

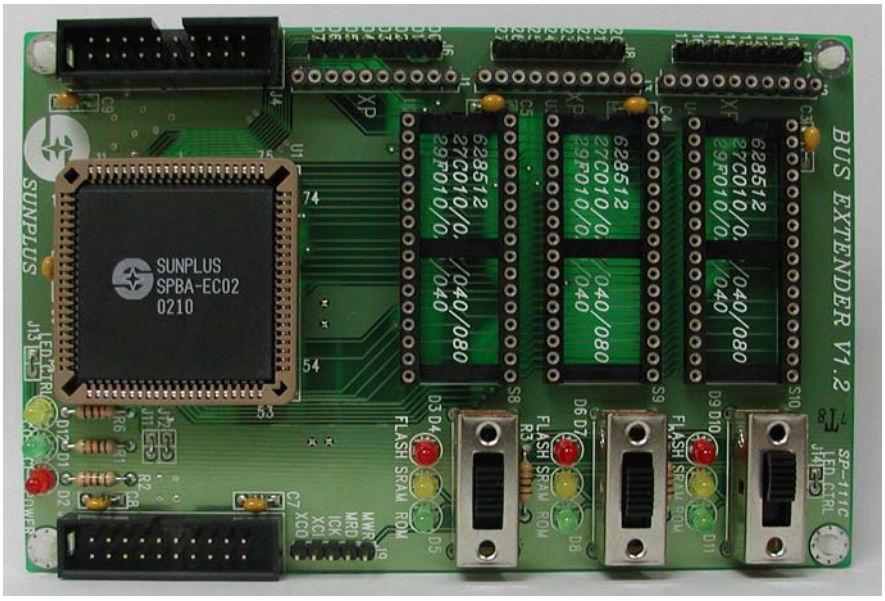
Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.
Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

12.2. Ordering Information

Product Number	Package Type
GPBA01B - C	Chip form

13. GPBA01B EVALUATION BOARD

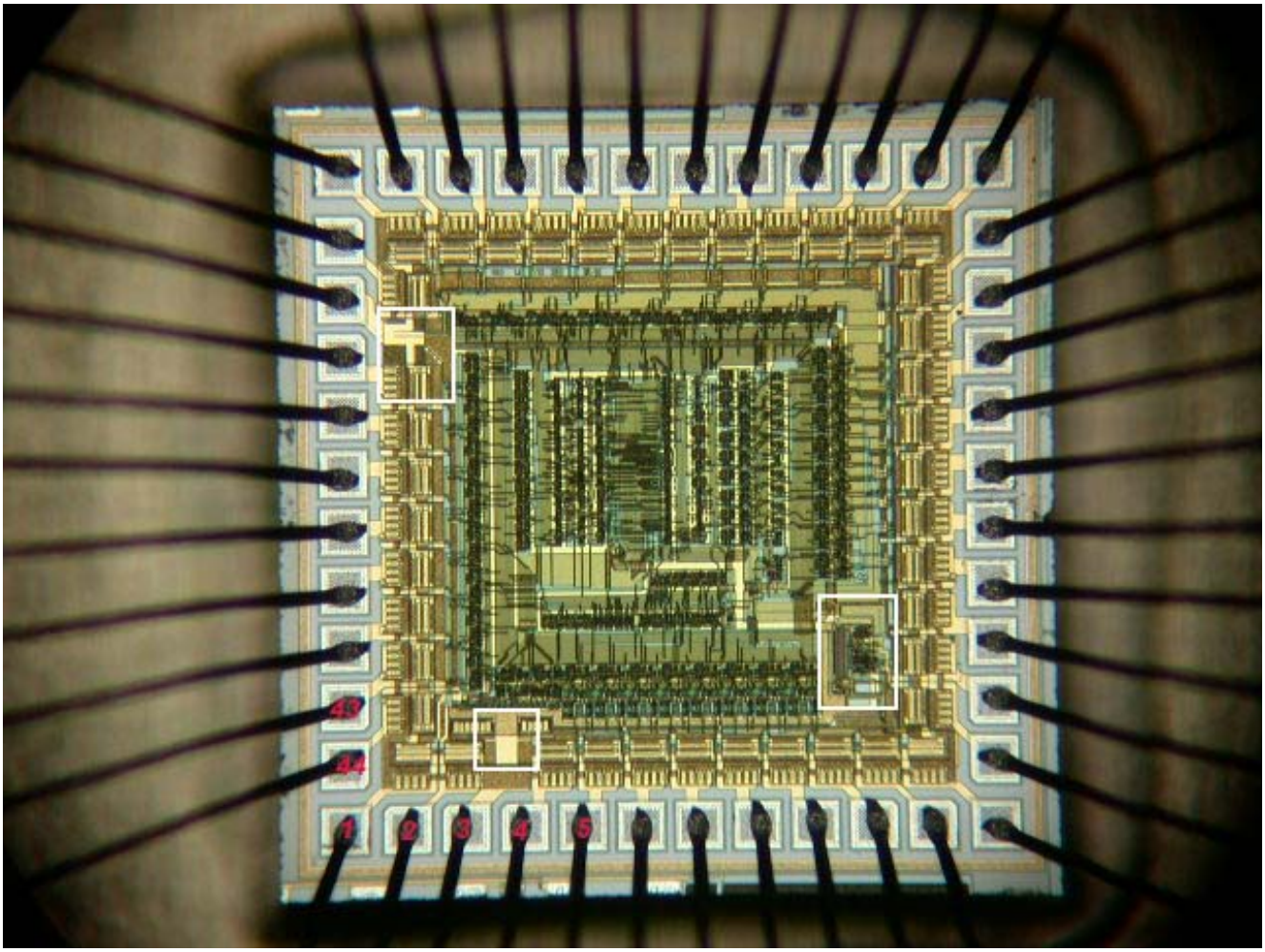
13.1. Evaluation Board—one BEX with Three Memory Extension



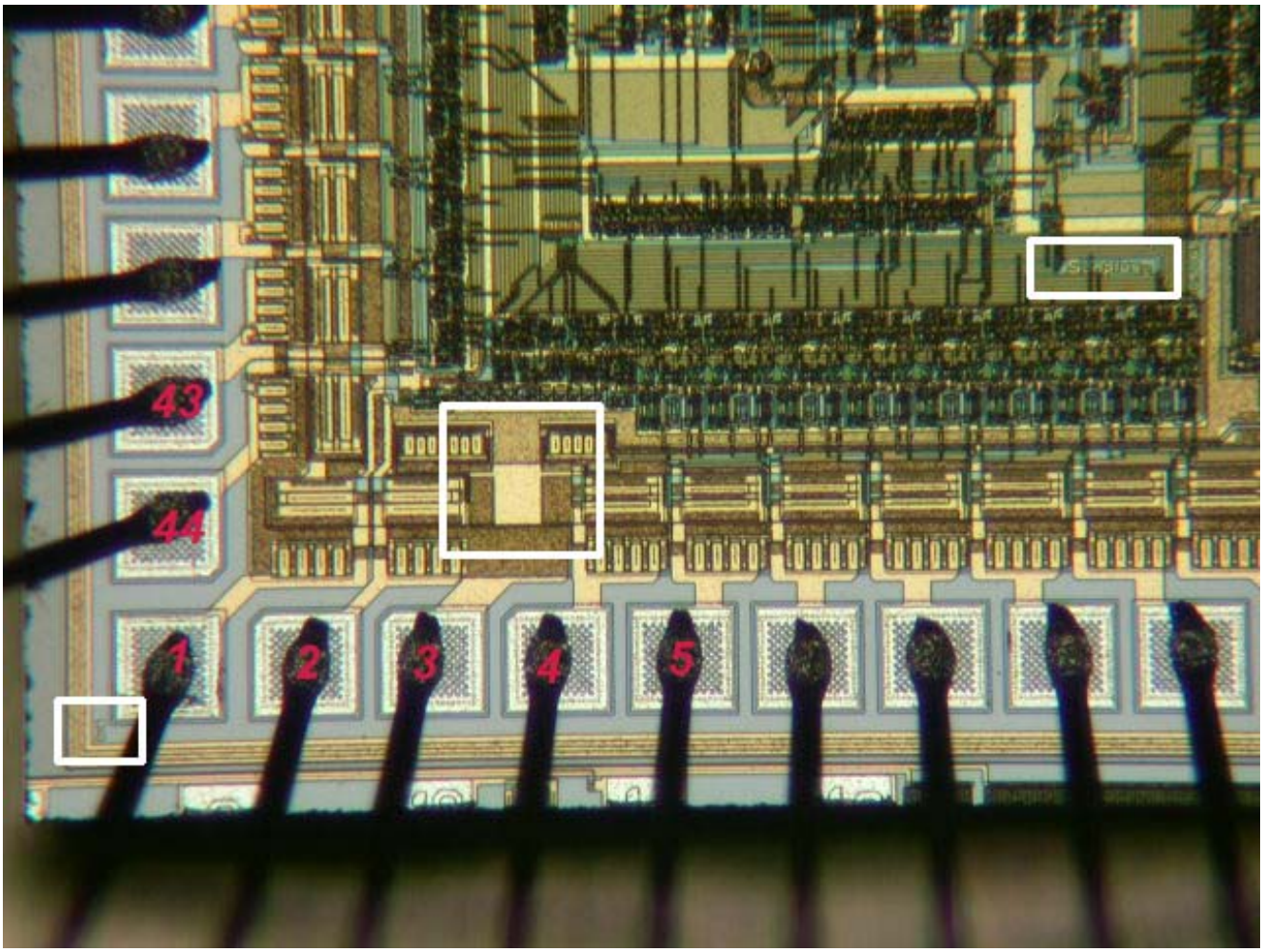
14. LAYOUT IMAGES/ DIE PHOTOS

14.1. Die Photo

14.1.1. Characteristic marks (whole chip)



14.1.2. Characteristic marks (left-bottom corner)



15. DISCLAIMER

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16. REVISION HISTORY

Date	Revision #	Description	Page
May 28, 2007	1.1	1. Modify “FEATURES” in section 2. 2. Modify “CFG=3 Example” in section 7.1.1.	4 10
JUN. 05, 2006	1.0	Original Note: The GPBA01B data sheet v1.0 is a continued version of SPBA01B data sheet v1.0.	29