GLT440L16

256K X 16 CMOS DYNAMIC RAM WITH EXTENDED DATA OUTPUT

Aug. 2000 (Rev.1.1)

Features :

* 262,144 words by 16 bits organization.
* Fast access time and cycle time.
* Dual $\overline{CAS}$ Input.
* Low power dissipation.
* Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, Hidden Refresh and Test Mode Capability.
* 512 refresh cycles per 8ms.
* Available in 40-Pin 400 mil SOJ and 40/44 Pin TSOP(II)
* Single +3.3V±10% Power Supply.
* All inputs and Outputs are TTL compatible.
* Extended Data-Out(EDO) Page Mode operation.

Description :

The GLT440L16 is a 262,144 x 16 bit high-performance CMOS dynamic random access memory. The GLT44016 offers Fast Page mode with Extended Data Output, and has both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins. The GLT440L16 has symmetric address and accepts 512-cycle refresh in 8ms interval.

All inputs are TTL compatible. EDO Page Mode operation allows random access up to 512 x 16 bits within a page, with cycle time as short as 14ns.

The GLT440L16 is best suited for graphics, and DSP applications requiring high performance memories.

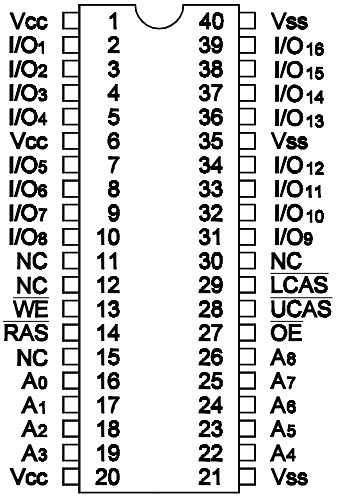
HIGH PERFORMANCE	35	40	50
Max. $\overline{RAS}$ Access Time, (t_{RAC})	35 ns	40 ns	50 ns
Max. Column Address Access Time, (t_{CAA})	13 ns	20 ns	25 ns
Min. Extended Data Out Page Mode Cycle Time, (t_{PC})	14 ns	15 ns	19 ns
Min. Read/Write Cycle Time, (t_{RC})	45 ns	75 ns	90 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	11 ns	12 ns	13 ns

G-Link Technology Corporation
2701Northwestern Parkway
Santa Clara, CA 95051, U.S.A.

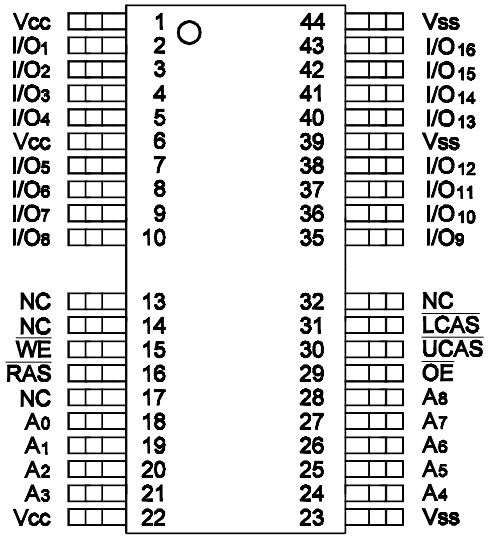
G-Link Technology Corporation,Taiwan
6F, No. 24-2, Industry E, RD, IV, Science Based
Industrial Park, Hsin Chu, Taiwan.

Pin Configuration :

GLT440L16
SOJ Top View



TSOP(Type II)
Top View



Pin Descriptions:

Name	Function
A_0 - A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe/Upper Byte Control
$\overline{LCAS}$	Column Address Strobe/Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
DQ_1 - DQ_{16}	Data Inputs / Outputs
V_{CC}	+3.3V Power Supply
V_{SS}	0V Supply
NC	No Connection

Absolute Maximum Ratings*

Operating Temperature, T_A (ambient)
.....-10°C to +70°C
Storage Temperature(plastic)....-55°C to +150°C
Voltage Relative to V_{SS}.....-1.0V to + 4.6V
Short Circuit Output Current.....50mA
Power Dissipation.....1.0W

*Note:Operation above Absolute Maximum Ratings can abversely affect device reliability.

Capacitance*

T_A=25°C, V_{CC}=3.3V±10%, V_{SS}=0V

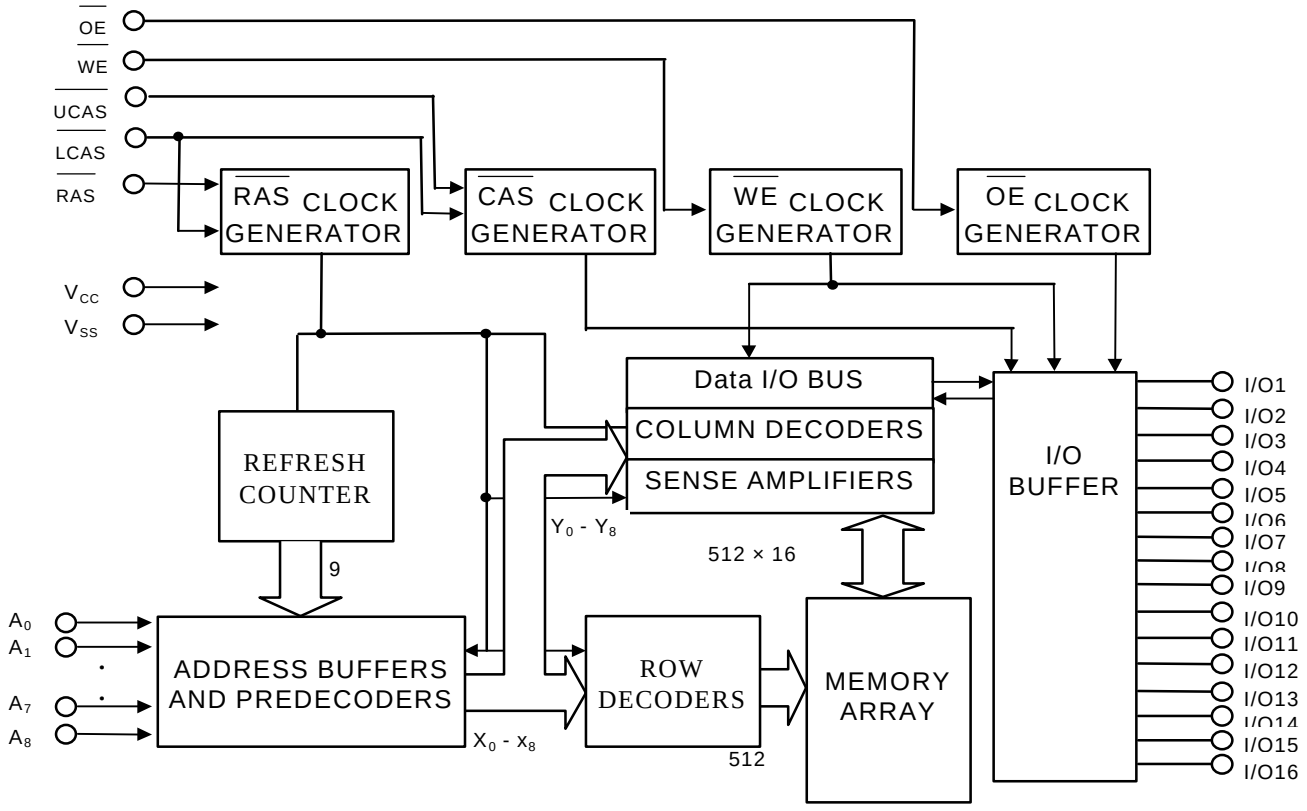
Symbol	Parameter	Typ	Max.	Unit
C_{IN1}	Address Input	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$	4	5	pF
C_{OUT}	Data Input/Output	5	7	pF

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up, wait more than 100µs and then, execute eight $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycles as dummy cycles to initialize internal circuit.

Block Diagram :



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Truth Table: GLT440L16

Function		$\overline{RAS}$	$\overline{CASL}$	$\overline{CASH}$	$\overline{WE}$	$\overline{OE}$	ADDRESS	DQs	Notes
Stanby		H	H	H	X	X		High-Z	
Read: Word		L	L	L	H	L	ROW/COL	Data Out	
Read: Lower Byte		L	L	H	H	L	ROW/COL	Lower Byte,Data-Out Upper Byte,High-Z	
Read: Upper Byte		L	H	L	H	L	ROW/COL	Lower Byte,High-Z Upper Byte,Data-Out	
Write: Word(Early Write)		L	L	L	L	X	ROW/COL	Data-In	
Write: Lower Byte (Early)		L	L	H	L	X	ROW/COL	Lower Byte,Data-In Upper Byte,High-Z	
Write: Upper Byte (Early)		L	H	L	L	X	ROW/COL	Lower Byte,High-Z Upper Byte,Data-In	
Read Write		L	L	L	H→L	L→H	ROW/COL	Data-Out,Data-In	1,2
EDO-Page-Mode Read	1st Cycle	L	H→L	H→L	H	L	ROW/COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	COL	Data-Out	2
EDO-Page-Mode Write	1st Cycle	L	H→L	H→L	L	X	ROW/COL	Data-In	2
	2nd Cycle	L	H→L	H→L	L	X	COL	Data-In	2
EDO-Page-Mode Read-Write	1st Cycle	L	H→L	H→L	H→L	L→H	ROW/COL	Data-Out,Data-In	1,2
	2nd Cycle	L	H→L	H→L	H→L	L→H	COL	Data-Out,Data-In	1,2
Hidden Refresh	Read	L→H→L	L	L	H	L	ROW/COL	Data-Out	2
	Write	L→H→L	L	L	H	L	ROW/COL	Data-In	2
$\overline{RAS}$-Only Refresh		L	H	H	X	X	ROW	High-Z	
CBR Refresh		H→L	L	L	X	X		High-Z	3

Notes:

1. These READ cycles may also be BYTE READ cycles (either $\overline{UCAS}$ or $\overline{LCAS}$ active).
2. These WRITE cycles may also be BYTE READ cycles (either $\overline{UCAS}$ or $\overline{LCAS}$ active).
3. EARLY WRITE only.
4. At least one of the two CAS signals must be active ($\overline{UCAS}$ or $\overline{LCAS}$).

DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V, unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I_{LI}	Input Leakage Current (any input pin)	0V ≤ V_{IN} ≤ 5.5V (All other pins not under test=0V)		-10		+10	µA	
I_{LO}	Output Leakage Current (for High-Z State)	0V ≤ V_{out} ≤ 5.5V Output is disabled (Hiz)		-10		+10	µA	
I_{CC1}	Operating Current, Random READ/WRITE	t_{RC} = t_{RC} (min.)	t_{RAC} = 35ns t_{RAC} = 40ns t_{RAC} = 50ns			160 145 125	mA	1,2
I_{CC2}	Standby Current,(TTL)	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ at V_{IH} other inputs ≥V_{SS}				4	mA	
I_{CC3}	Refresh Current, $\overline{RAS}$-Only	$\overline{RAS}$ cycling, $\overline{UCAS}$, $\overline{LCAS}$ at V_{IH} t_{RC} = t_{RC} (min.)	t_{RAC} = 35ns t_{RAC} = 40ns t_{RAC} = 50ns			160 145 125	mA	2
I_{CC4}	Operating Current, EDO Page Mode	$\overline{RAS}$ at V_{IL}, $\overline{UCAS}$, $\overline{LCAS}$ address cycling:t_{PC}=t_{PC}(min.)	t_{RAC} = 35ns t_{RAC} = 40ns t_{RAC} = 50ns			160 145 125	mA	1,2
I_{CC5}	Refresh Current, $\overline{CAS}$ Before $\overline{RAS}$	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ address cycling: t_{RC}=t_{RC} (min.)	t_{RAC} = 35ns t_{RAC} = 40ns t_{RAC} = 50ns			160 145 125	mA	1
I_{CC6}	Standby Current, (CMOS)	$\overline{RAS}$ ≥V_{CC}-0.2V, $\overline{UCAS}$ ≥V_{CC}-0.2V, $\overline{LCAS}$ ≥V_{CC}-0.2V, All other inputs V_{SS}				1	mA	
V_{CC}	Supply Voltage			3.0		3.6	V	
V_{IL}	Input Low Voltage			-0.3		0.8	V	3
V_{IH}	Input High Voltage			2.0V		V_{CC}+0.3	V	3
V_{OL}	Output Low Voltage	I_{OL} = 2mA				0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -2mA		2.4			V	

Notes:

1. I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC}(max.) is measured with the output open.
2. I_{CC} is dependent upon the number of address transitions specified I_{CC}(max.) is measured with a maximum of one transition per address cycle in random Read/Write and EDO Fast Page Mode.
3. Specified V_{IL}(min.) is steady state operation. During transitions V_{IL}(min.) may undershoot to –0.3V for a period not to exceed 20ns. All AC parameters are measured with V_{IL}(min.)≥V_{SS} and V_{IH}(max.)≤V_{CC}.

AC Characteristics

T_A = 0°C to 70°C , V_{CC} = 3.3 V ± 10% V_{IH}/V_{IL} = 2.0/0.8V , V_{OH}/V_{OL} = 2.0/0.8V

An initial pause of 100 µs and 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycles are required after power-up.

Parameter	Symbol	35		40		50		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read or Write Cycle Time	t_{RC}	70		75		90		ns	
Read Modify write Cycle Time	t_{RWC}	90		93		109		ns	
$\overline{RAS}$ Precharge Time	t_{RP}	25		25		30		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	35	75k	40	100k	50	100k	ns	
Access Time from $\overline{RAS}$	t_{RAC}		35		40		50	ns	1,2,3
Access Time from $\overline{CAS}$	t_{CAC}		11		12		13	ns	1,5,10
Access Time from Column Address	t_{AA}		18		20		25	ns	1,5,6
$\overline{CAS}$ to Output Low-Z	t_{CLZ}	0		0		0		ns	
$\overline{CAS}$ to Output High-Z	t_{CEZ}	3	8	3	8	3	8	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	10		12		14		ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	t_{ROH}	7		8		9		ns	
$\overline{CAS}$ Hold Time	t_{CSH}	34		34		45		ns	
$\overline{CAS}$ Pulse width	t_{CAS}	6		6		8		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	13	24	18	28	19	37	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	10	17	13	20	14	25	ns	7
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	
Row Address Set-Up Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	6		8		9		ns	
Column Address Set-Up Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	5		6		7		ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	18		20		25		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	25		34		44		ns	
Read Command Set-Up Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	4
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	4
Write Command Set-Up Time	t_{WCS}	0		0		0		ns	8,9
Write Command Hold Time	t_{WCH}	5		6		7		ns	
Write Command Pulse Width	t_{WP}	5		6		7		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	10		12		13		ns	

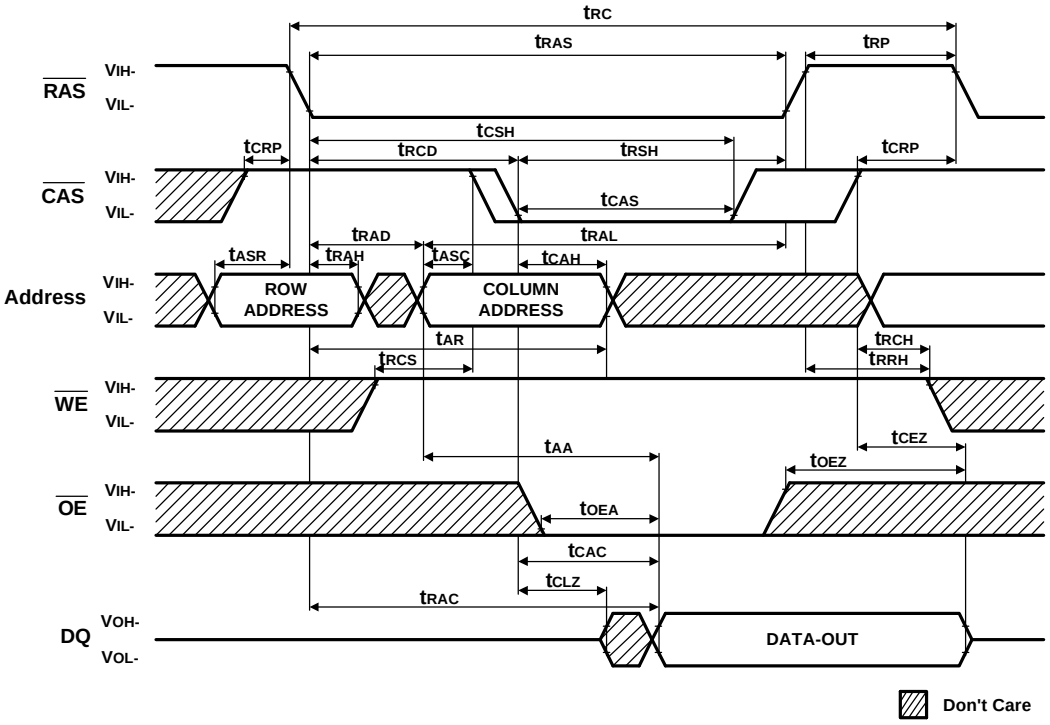
AC Characteristics

Parameter	Symbol	35		40		50		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	8		12		13		ns	
Data Set-Up Time	t_{DS}	0		0		0		ns	
Data Hold Time	t_{DH}	5		8		9		ns	
Data Hold Time Referenced to $\overline{RAS}$	t_{DHR}	25		36		46		ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	46		54		64		ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	23		24		25		ns	
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	29		32		37		ns	
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	t_{RPC}	0		0		0		ns	
Access Time from $\overline{CAS}$ Precharge	t_{CPA}		20		22		30	ns	
EDO Page Mode Cycle Time	t_{PC}	14		15		20		ns	
EDO Page Mode Read-Modify-write Cycle Time	t_{PRWC}	45		50		59		ns	
$\overline{CAS}$ Precharge Time (EDO Page Mode)	t_{CP}	4		5		8		ns	
$\overline{RAS}$ Pulse Width (EDO Page Mode Only)	t_{RASP}	35	100k	40	100k	50	100k	ns	
Access Time from $\overline{OE}$	t_{OEA}		11		12		13	ns	
$\overline{OE}$ to Data Delay Time	t_{OED}	5		8		8		ns	
$\overline{OE}$ to Output High-Z	t_{OEZ}	3	8	3	8	3	8	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	5		7		7		ns	
Data Output Hold after $\overline{CAS}$ Low	t_{DOH}	3		3		5		ns	
$\overline{RAS}$ to Output High-Z	t_{REZ}	3	8	3	8	3	8	ns	
$\overline{WE}$ to Output High-Z	t_{WEZ}	3	10	3	10	3	12	ns	
$\overline{OE}$ to $\overline{CAS}$ Hold Time	t_{OCH}	8		8		8		ns	
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	8		8		8		ns	
$\overline{OE}$ Precharge Time	t_{OEP}	8		8		8		ns	
$\overline{CAS}$ Set-Up Time for $\overline{CAS}$–before-$\overline{RAS}$ Cycle	t_{CSR}	8		10		10		ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$–before-$\overline{RAS}$ Cycle	t_{CHR}	8		10		10		ns	
Transition Time	t_T	2	50	2	50	2	50	ns	
Refresh Period	t_{REF}		8		8		8	ms	

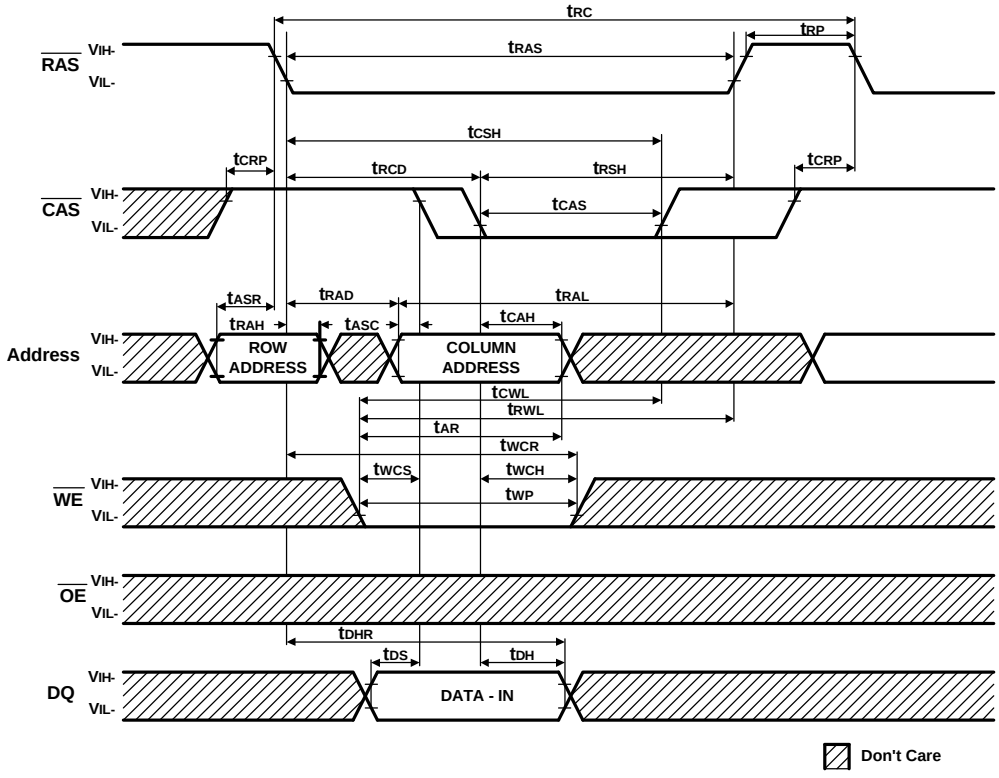
Notes:

1. Measure with a load equivalent to one TTL inputs and 50 pF.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), access time will be t_{AA} dominant.
3. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RCD} (max.), access time will be controlled by t_{CAC}.
4. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle.
5. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CPA}.
6. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
7. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
8. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
9. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ of $\overline{WE}$.
    t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 1.5 ns.

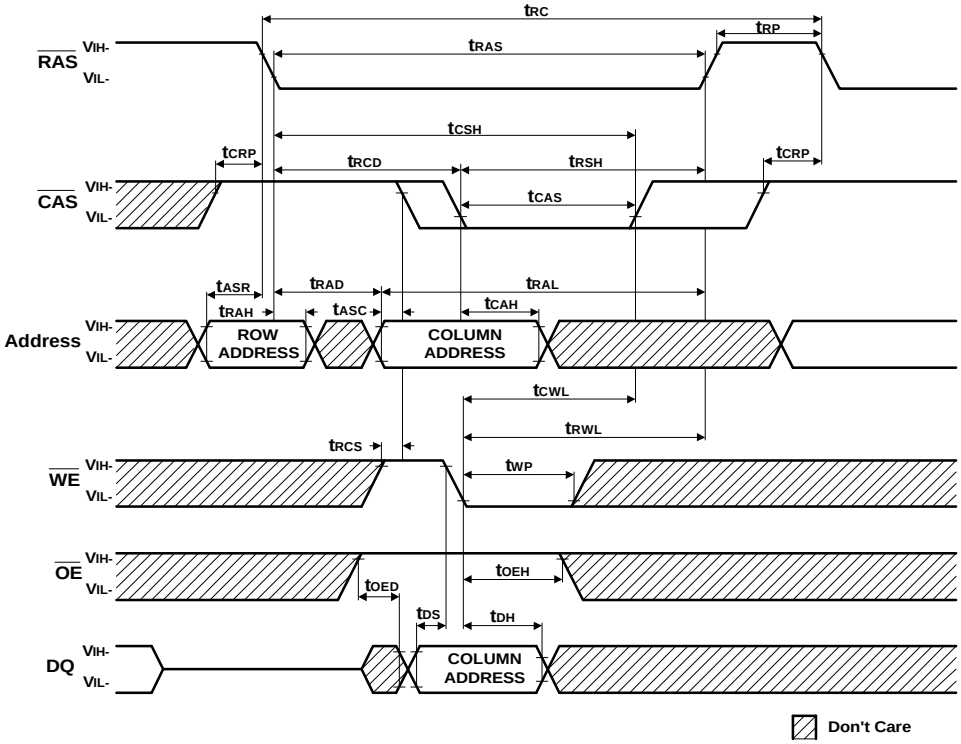
Read Cycle



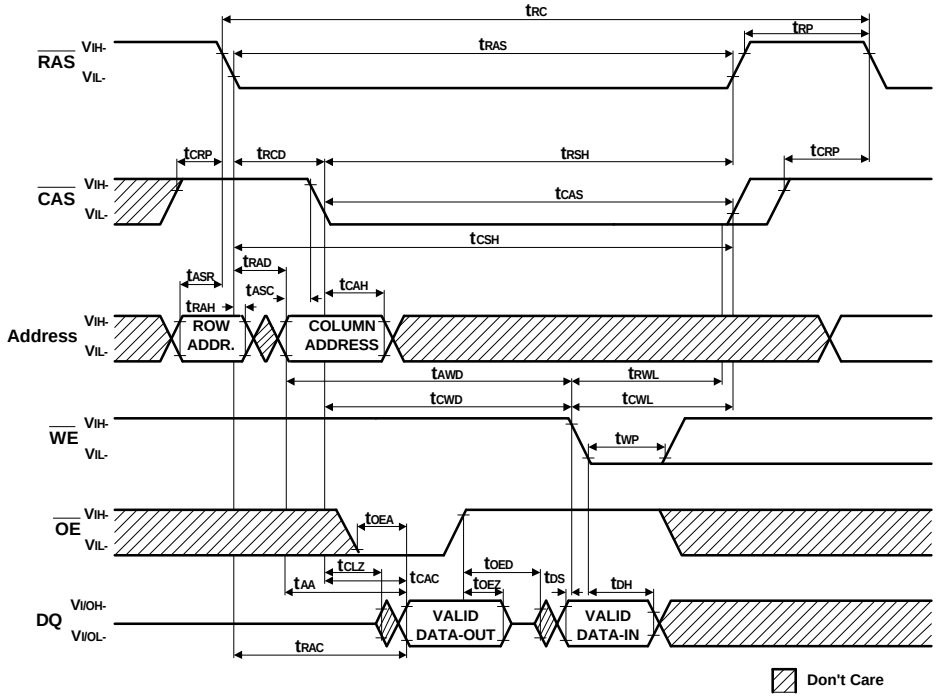
Early Write Cycle NOTE : D_{OUT} = Open



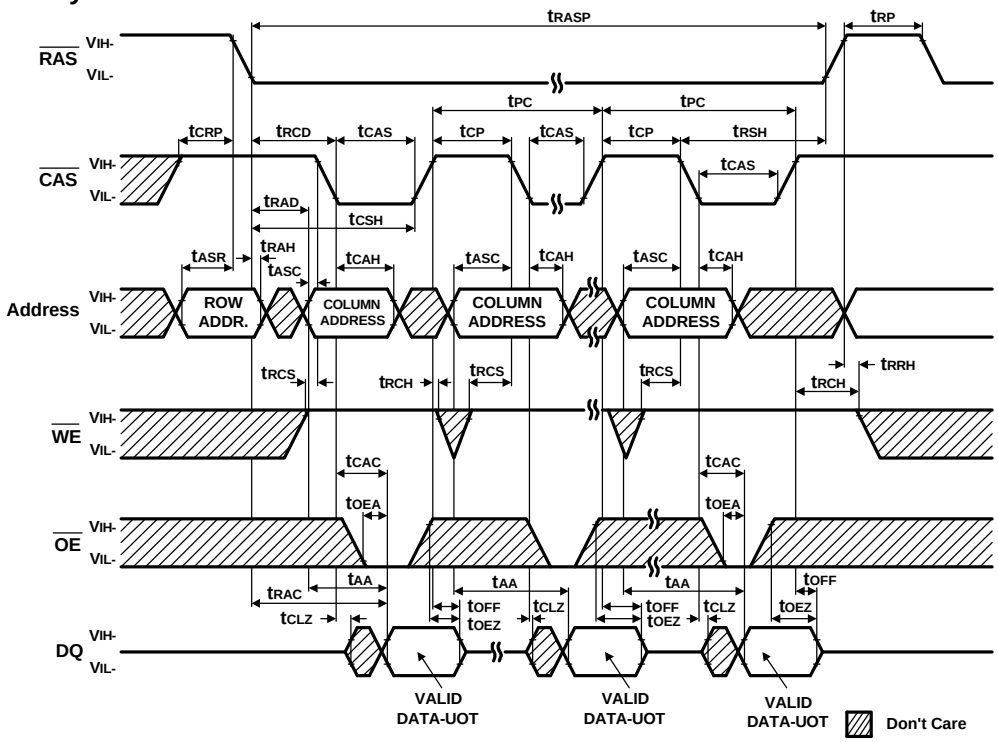
Late Write Cycle ($\overline{OE}$ Controlled Write) NOTE : D_{OUT} = Open



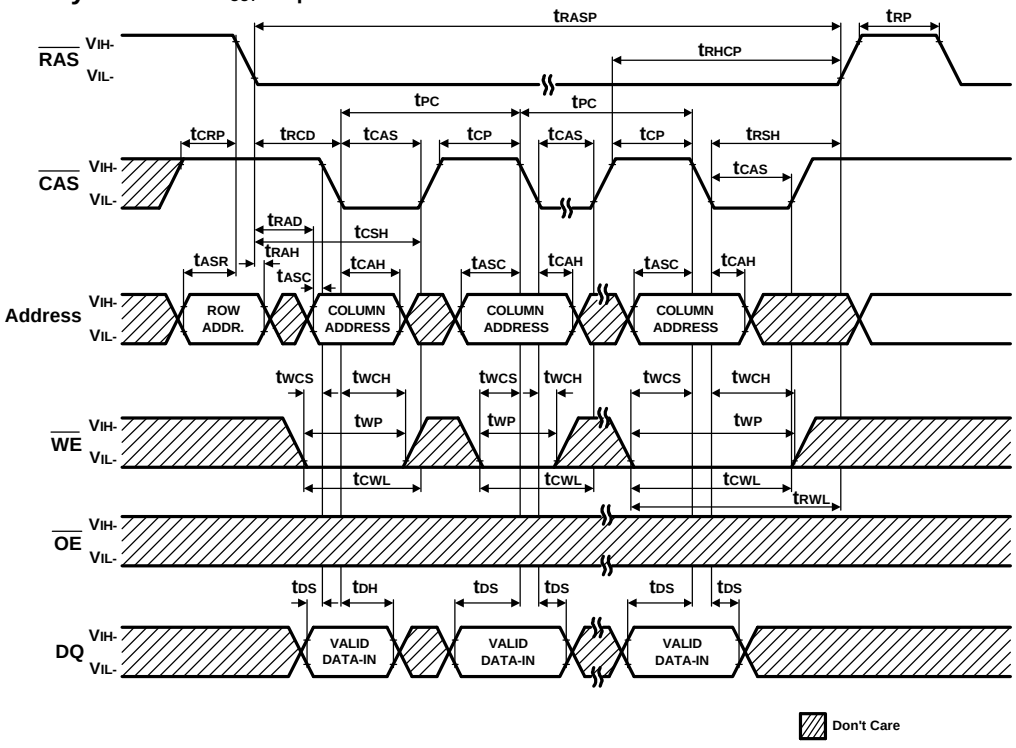
Read - Modify - Write Cycle



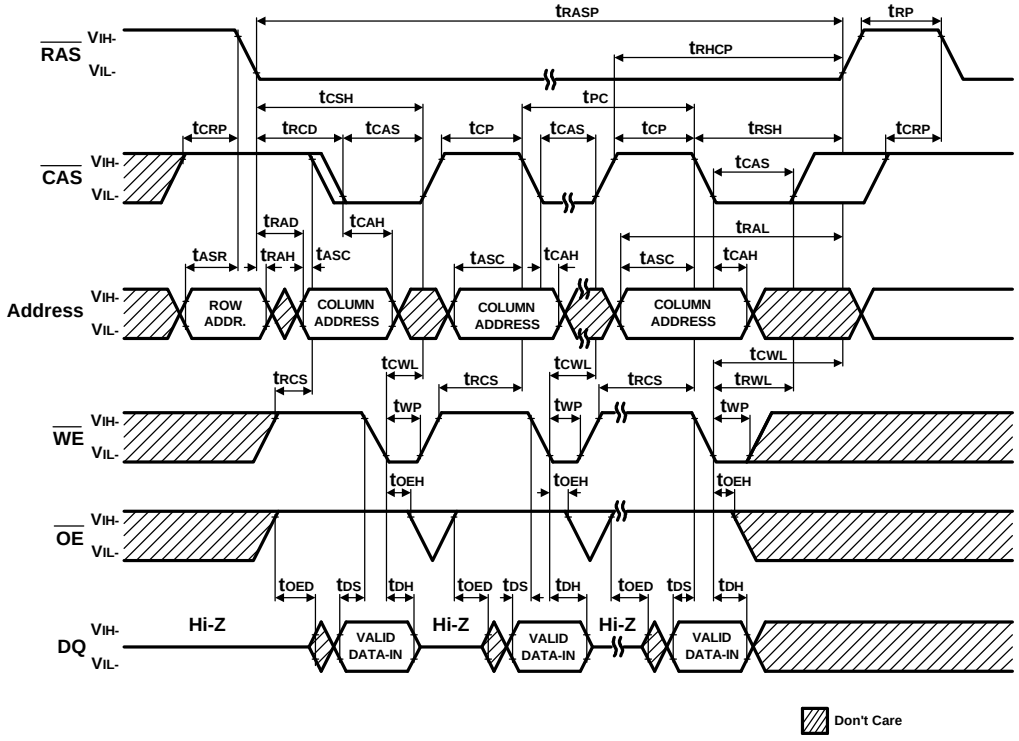
Fast Page Read Cycle



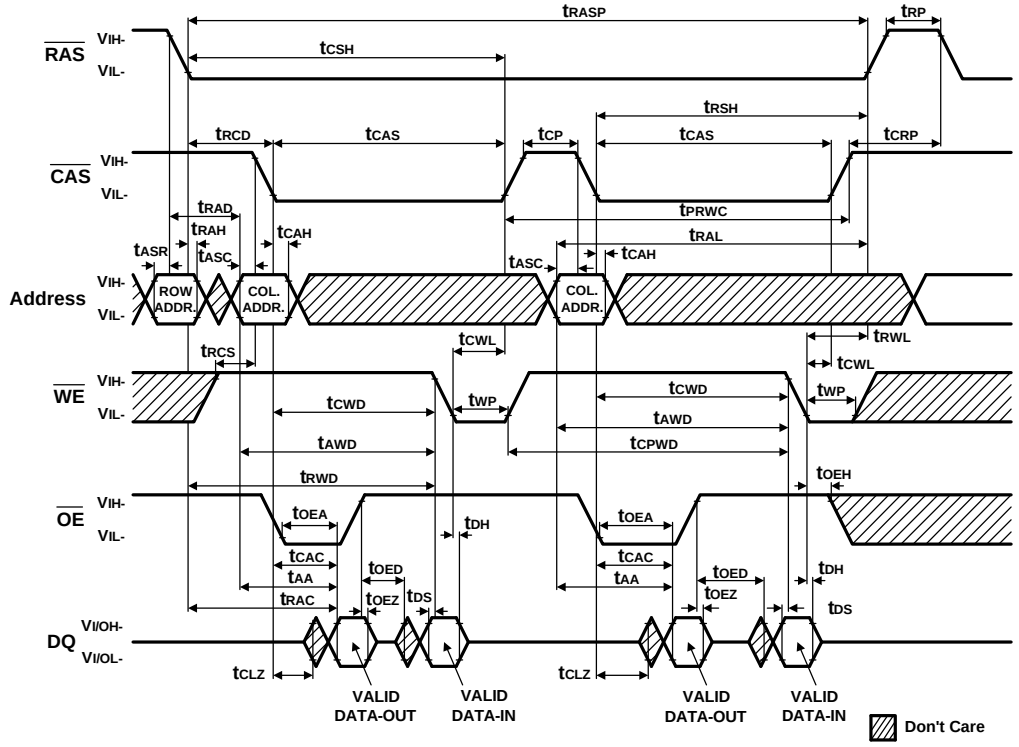
Fast Page Write Cycle NOTE : D_{OUT} = Open



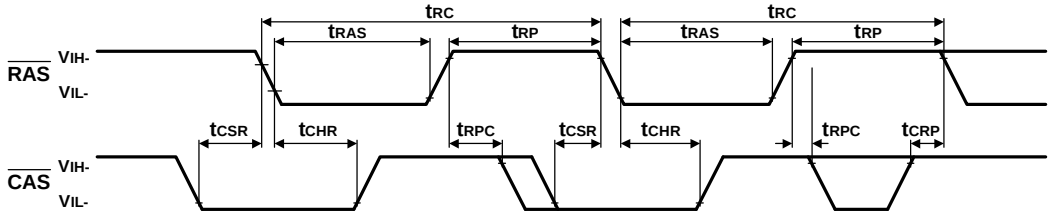
Fast Page Mode Late Write Cycle



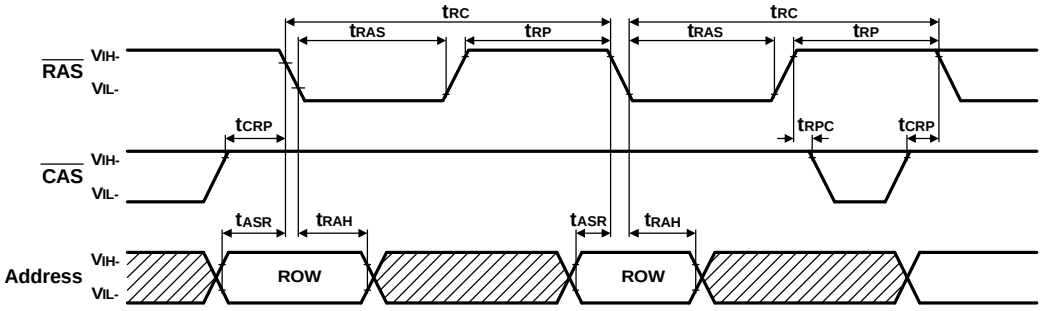
Fast Page Read - Modify - Write Cycle



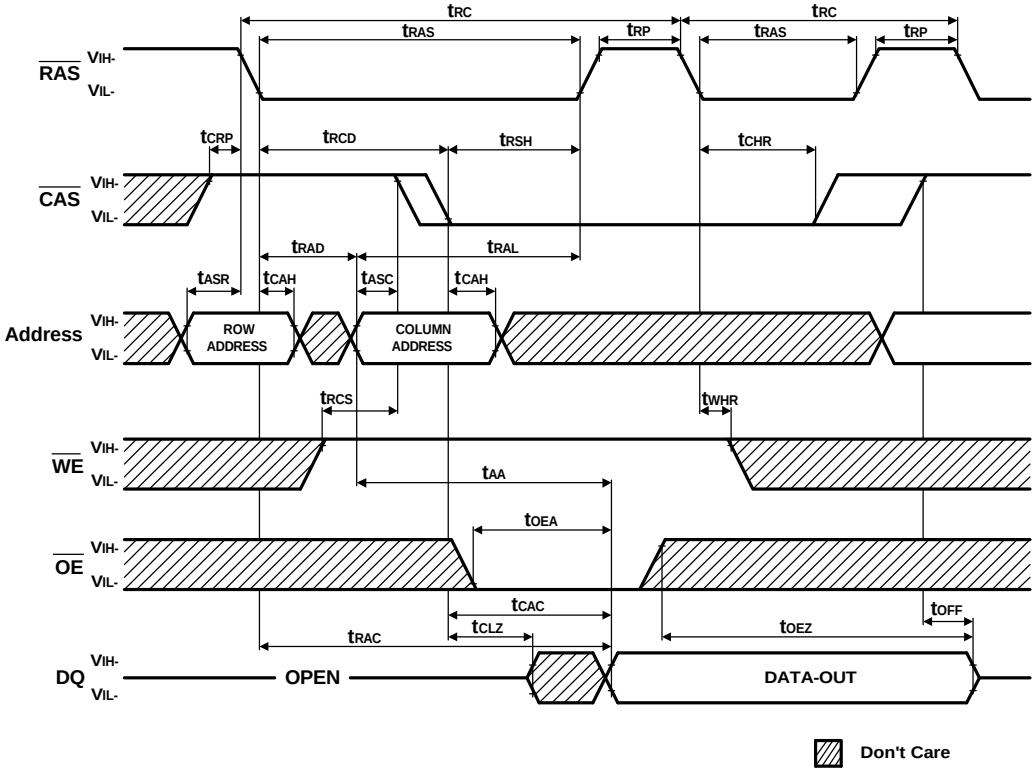
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



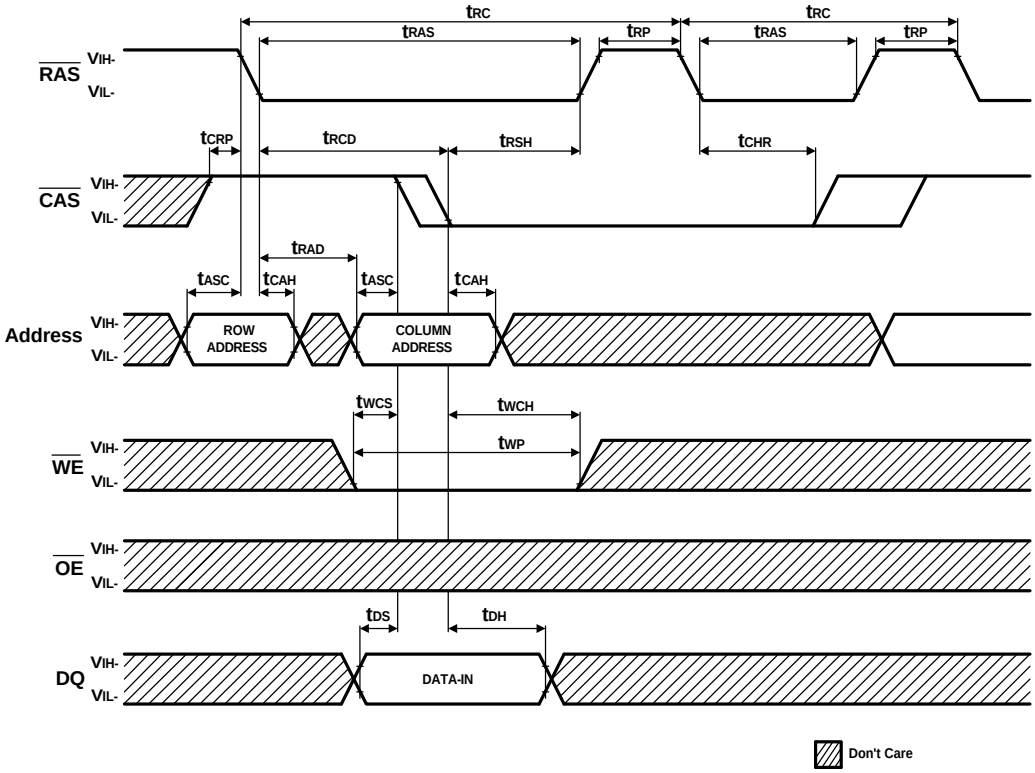
$\overline{RAS}$ -Only Refresh Cycle



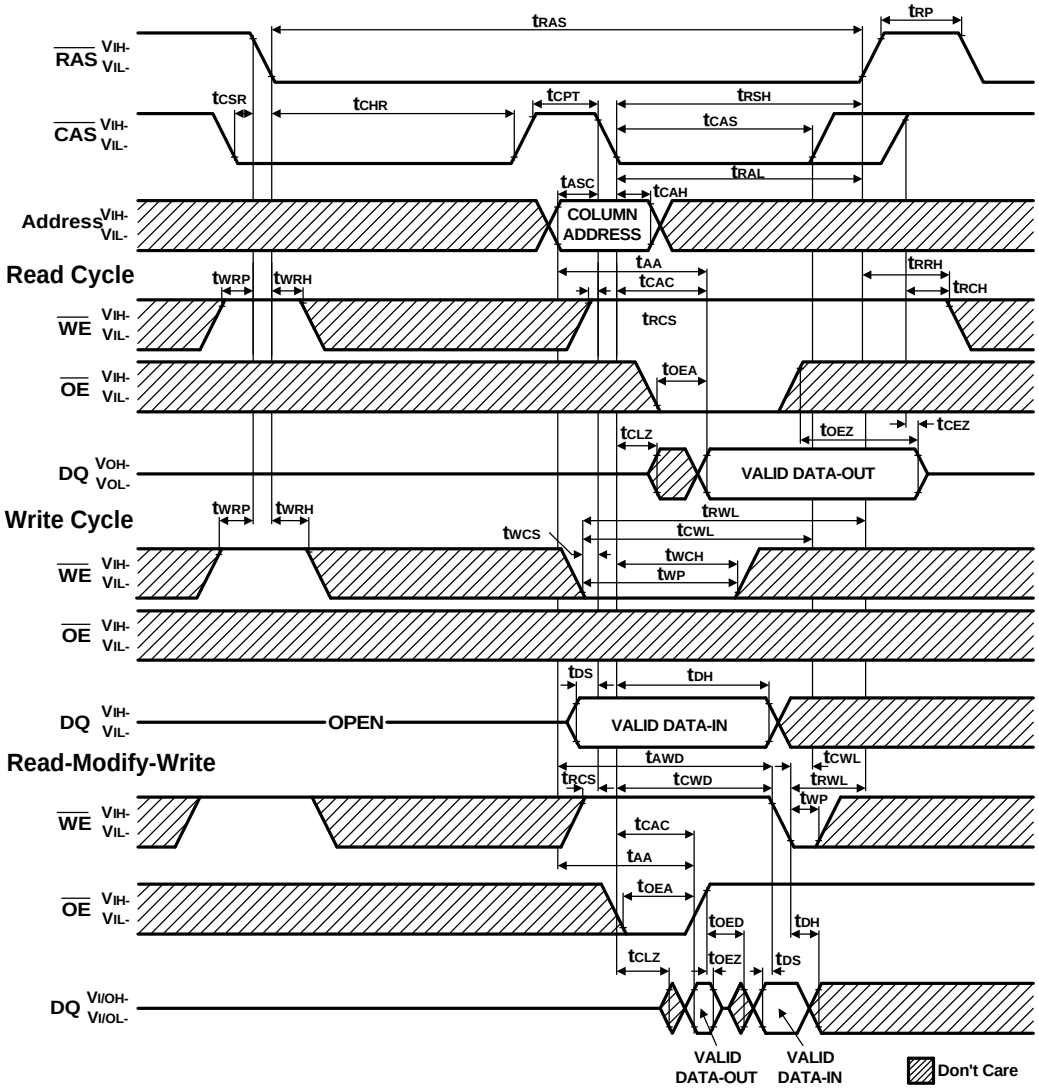
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write) NOTE : D_{OUT} =Open



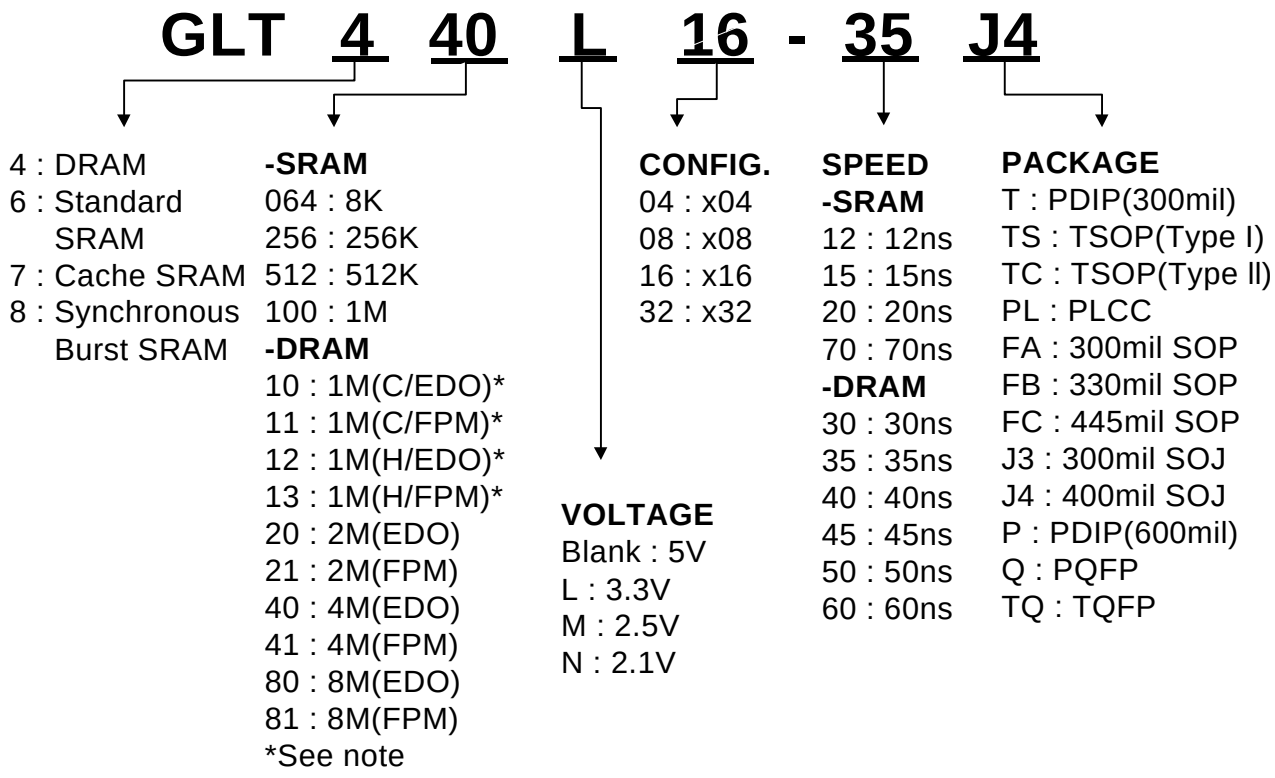
$\overline{CAS}$ - Before $\overline{RAS}$ Refresh Counter Test Cycle



Ordering Information

Part Number	SPEED	POWER	FEATURE	PACKAGE
GLT440L16-35J4	35ns	Normal	EDO	40L 400mil SOJ
GLT440L16-40J4	40ns	Normal	EDO	40L 400mil SOJ
GLT440L16-50J4	50ns	Normal	EDO	40L 400mil SOJ
GLT440L16-35TC	35ns	Normal	EDO	44L 400mil TSOP
GLT440L16-40TC	40ns	Normal	EDO	44L 400mil TSOP
GLT440L16-50TC	50ns	Normal	EDO	44L 400mil TSOP

Parts Numbers (Top Mark) Definition :



Note : C→CDROM , H→HDD.

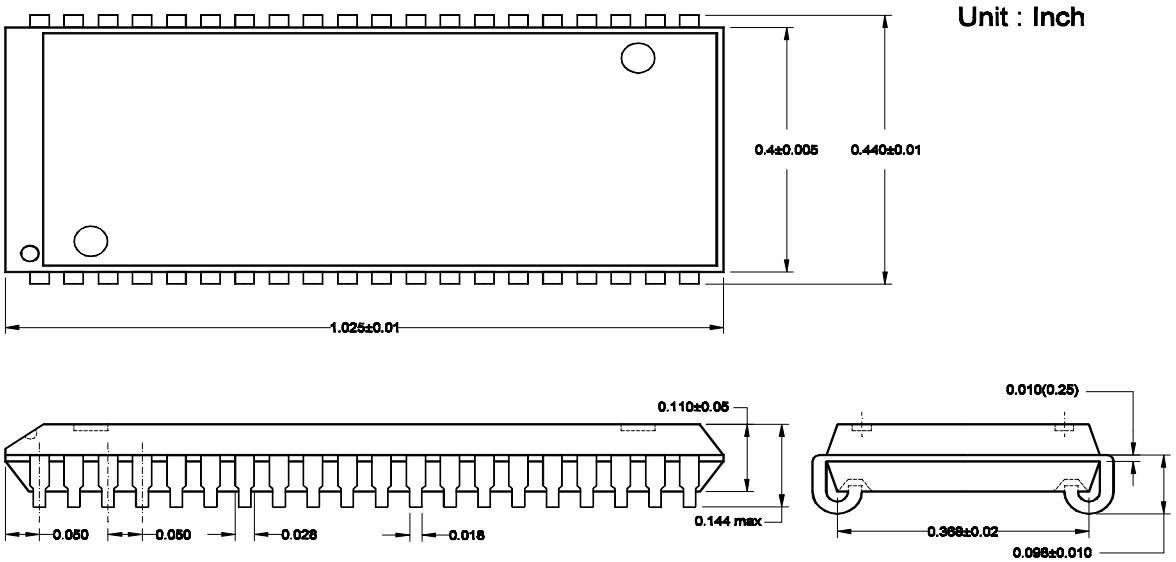
Example :

1.GLT710008-15T 1Mbit(128Kx8)15ns 5V SRAM PDIP(300mil)Package type.

2.GLT44016-40J4 4Mbit(256Kx16)40ns 5V DRAM SOJ(400mil)Package type.

Package Information

40/44 Lead Thin Small Outline Package SOJ



40/44 Lead Thin Small Outline Package TSOP(Type II)

