GeneScan™II

GL646USB

Three-in-one Scanner Controller for USB and 1394

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1. GENERAL DESCRIPTION

Genesys Logic's single-chip GeneScan™II, GL646USB, is a high speed, high performance, low cost and rich scalability controller for scanner. It successfully integrates AFE (16 bits Analog Front End), featured scanner function ASIC and USB 1.1 interface controller into one single-chip. With it's high performance design architecture, GeneScan™II is not only ready for supporting CIS or CCD image sensors (600dpi or 1200dpi resolution) which is used in flatbed or transparency scanners, but also can co-work with uni-polar or bi-polar stepping motors. Advanced features of GeneScan™II includes loseless image data compression, dual motor acceleration/ deceleration curve table for high speed motor moving, industrial standard auto suspend mode and bus-power supporting.

Except the build-in USB 1.1 interface, the capability of cooperating with USB 2.0 and IEEE 1394 interface controller also expand the scalability of GeneScan™II to fit customer's further requirement of supporting high speed interface standards.

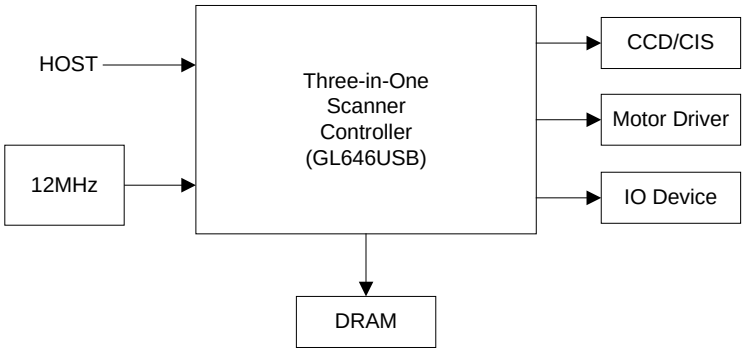
2. FEATURES

- Design for sheetfed, flatbed and transparency scanner.
- Programmable 600,1200 or 2400 DPI color CCD or CIS timing
- Support fast scan for low DPI such as pre-view
- Support three scanning type :pixel by pixel(pixel rate), line by line(line rate) and RGB line by turns(line rate)
- Programmable dummy lines to resolve start/stop (discontinuous) problem.
- 48-Bits true color (16-Bits gray level) scan
- Support color , fine Gray , fast gray and fast B/W scan for CCD
- Support color , gray , true gray and B/W scan for CIS
- Built-in 16 bits Front End
- 16 Bits white shading , dark shading and 12/14 Bits GAMMA correction
- Programming threshold level for B/W
- Exposure time is adjustable (max.524ms , 1 pixel time increment step)
- Scan width(scan area) control for horizontal line(1 pixel increment step)
- Built-in USB(1.1) , external USB(2.0) and external IEEE1394 interface
- Support 4M bits x 1 or x2 (256K x 16) EDO DRAM
- Support digital average for DPI (non-deletion type)
- Support hardware deletion type for DPI (2400 to 1 DPI ,1 DPI decrement)
- Acceleration/ Deceleration double table for high speed motor moving
- Stepping motor phase control ports for bi-polar or uni-polar motor
- Full, half and quarter steps for motor control
- Build-in Uni-polar phase PWM control
- Watch-Dog protection circuit for motor, lamp and ASIC system
- 2 Output ports for lamp (include flatbed and transparency with PWM) control
- Input port for home sensor
- 9 GPIO ports
- Lamp timeout (sleeping) control

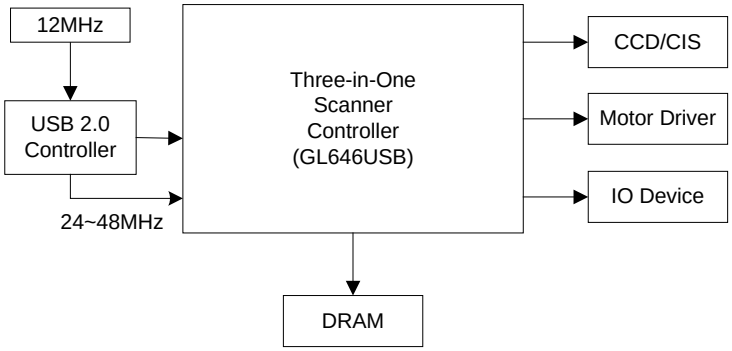
- Support 8/16 bits image data type.
- Build-in lossless 8 bits image data compression.
- Output motor trigger signal under scanning for ADF
- Power on check status
- DMA image read.
- DMA DRAM data read/write

3. SYSTEM BLOCK DIAGRAM

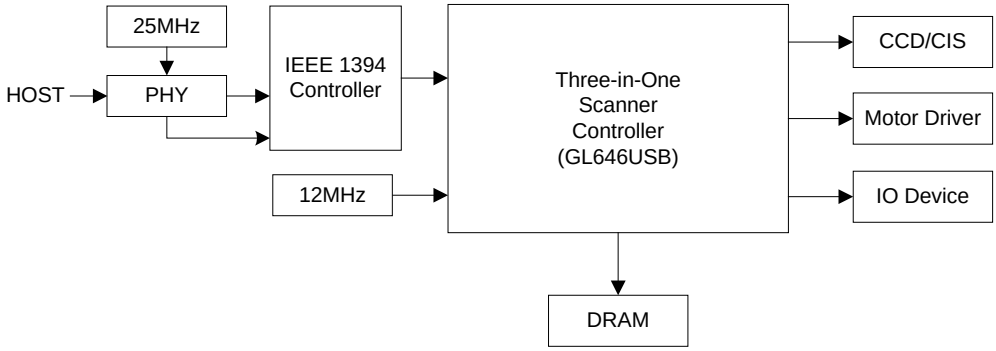
3.1 USB 1.1 System Block Diagram



3.2 USB 2.0 System Block Diagram

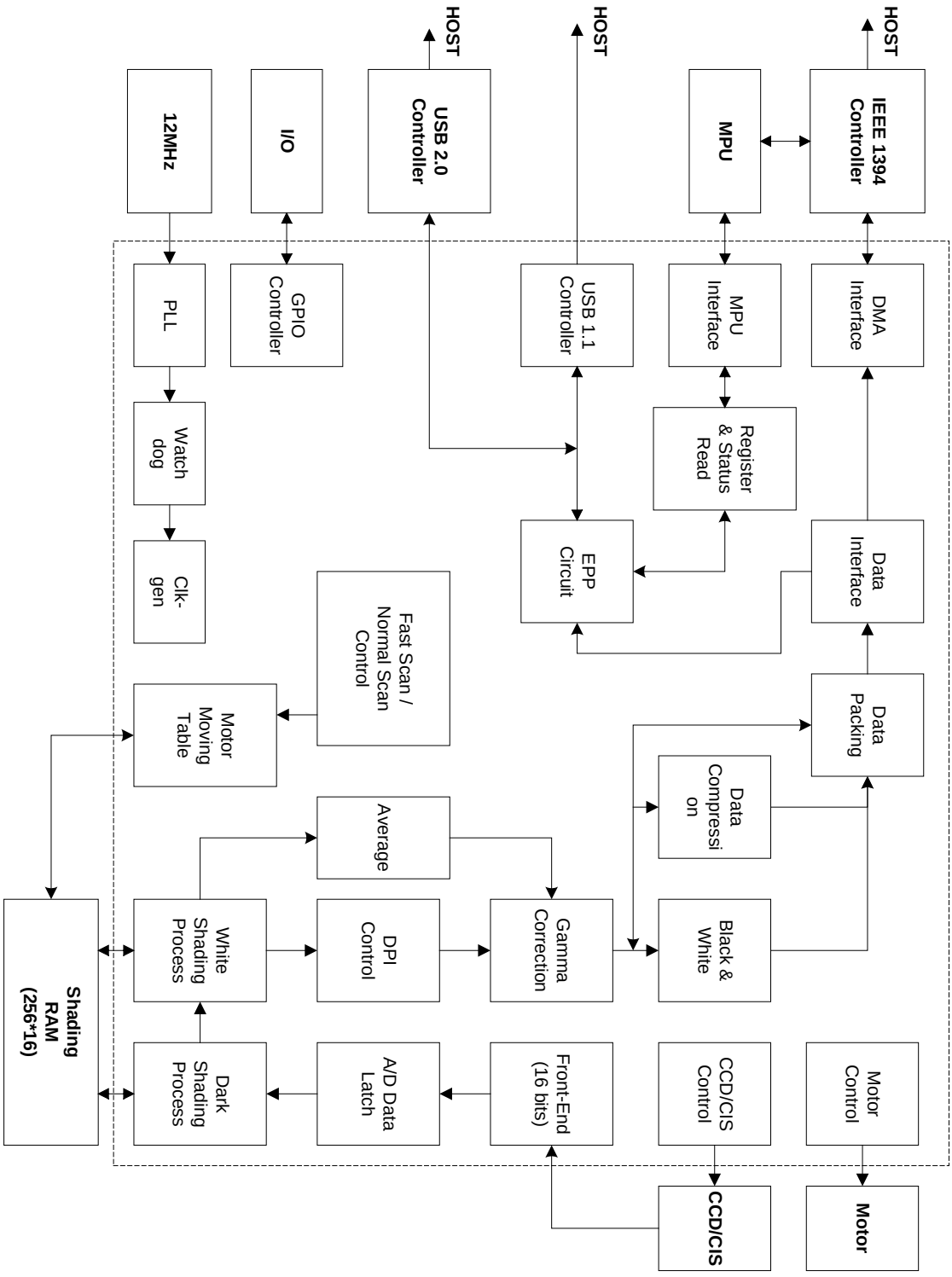


3.3 IEEE 1394 System Block Diagram



Note: 1.The pins assignment and package of GL646 USB is the same as GL643USB.
2.The connection of GL646USB is the same as GL643USB.
3.GL643USB is 14 bits solution; GL646USB is 16 bits solution.

4. FUNCTION BLOCK DIAGRAM



5. HARDWARE DESCRIPTION

5.1 Pins Assignment & Mode Definition:

	Mode 1 SC+ AFE+ USB1.1		Mode 2 SC+ USB1.1		Mode 3 SC+ AFE (For 1394)		Mode 4 SC+ AFE (For USB2.0)		Mode 5 SC+ AFE+ USB1.1 (TEST PLL & DEBUG)		Mode 6 TEST SC		Mode 7 TEST USB1.1		Mode 8 TEST AFE		ASIC I/O Cell
No.	TSTMOD=0 TSTSEL0=0 TSTSEL1=0 MPUSEL=0	I/O	TSTMOD=0 TSTSEL0=1 TSTSEL1=0 MPUSEL=0	I/O	TSTMOD=0 TSTSEL0=0 TSTSEL1=1 MPUSEL=1	I/O	TSTMOD=0 TSTSEL0=0 TSTSEL1=1 MPUSEL=0	I/O	TSTMOD=0 TSTSEL0=1 TSTSEL1=1 MPUSEL=0	I/O	TSTMOD=1 TSTSEL0=0 TSTSEL1=0	I/O	TSTMOD=1 TSTSEL0=1 TSTSEL1=0	I/O	TSTMOD=1 TSTSEL0=0 TSTSEL1=1	I/O	
1		I		I	HSLCTIN	I	HSLCTIN	I	ASTRBO_	O	HSLCTIN	I	ASTRBO_	O		I	bd4rtu
2		I		I	HI_INIT	I	HI_INIT	I	MIARSTB	O	HI_INIT	I		I		I	bd4rtu
3		I		I	HAFXTIN	I	HAFXTIN	I	DSTRBO_	O	HAFXTIN	I	DSTRBO_	O		I	bd4rtu
4		I		I	HSTBIN	I	HSTBIN	I	WRO_	O	HSTBIN	I	WRO_	O		I	bd4rtu
5		I		I	H_BUSY	O	H_BUSY	O	WAITI_	O	H_BUSY	O	WAITI_	I		I	bd4rtu
6		I		I	H_ACK	O	H_ACK	O	PLLOUT	O	H_ACK	O		I		I	bd4rtu
7		I		I	H_PE	O	H_PE	O	OSCENB	O	H_PE	O	OSCENB	O		I	bd4rtu
8	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	
9	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	
10	CKSEL	I	CKSEL	I	H_ERR	I	H_ERR	O	CKSEL	I	H_ERR	I/O	CKSEL	I		I	bd4rtu
11		I		I	HD0	I/O	HD0	I/O	IODAT0	O	HD0	I/O	EPPD0	I/O		I	bd4rt
12		I		I	HD1	I/O	HD1	I/O	IODAT1	O	HD1	I/O	EPPD1	I/O		I	bd4rt
13		I		I	HD2	I/O	HD2	I/O	IODAT2	O	HD2	I/O	EPPD2	I/O		I	bd4rt
14		I		I	HD3	I/O	HD3	I/O	IODI0	O	HD3	I/O	EPPD3	I/O		I	bd4rt
15		I		I	HD4	I/O	HD4	I/O	IODI1	O	HD4	I/O	EPPD4	I/O		I	bd4rt
16		I		I	HD5	I/O	HD5	I/O	IODI2	O	HD5	I/O	EPPD5	I/O		I	bd4rt
17		I		I	HD6	I/O	HD6	I/O	PWRDN	O	HD6	I/O	EPPD6	I/O		I	bd4rt
18		I		I	HD7	I/O	HD7	I/O	WMSEL	O	HD7	I/O	EPPD7	I/O		I	bd4rt
19	GPIO5	I/O	GPIO5	I/O	GPIO5	I/O	GPIO5	I/O	VPI	O	DMAD0/GPIO5	I/O	GPIO5	I/O		I/O	bd4rt
20	GPIO6	I/O	GPIO6	I/O	GPIO6	I/O	GPIO6	I/O	VMI	O	DMAD1/GPIO6	I/O	GPIO6	I/O		I/O	bd4rt
21	GPIO7	I/O	GPIO7	I/O	GPIO7	I/O	GPIO7	I/O	RXD	O	DMAD2/GPIO7	I/O	GPIO7	I/O		I/O	bd4rt
22	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	
23	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	
24	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	
25	GPIO11	I/O	GPIO11	I/O	GPIO11	I/O	GPIO11	I/O	TSE0	O	DMAD6/GPIO11	I/O		I/O		I/O	bd4rt
26	GPIO12	I/O	GPIO12	I/O	GPIO12	I/O	GPIO12	I/O	RSE0	O	DMAD7/GPIO12	I/O		I/O		I/O	bd4rt
27	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	
28	IX1	I	IX1	I	IX1	I	IX1	I	IX1	I	IX1	I	IX1	I	IX1	I	Oscen2
29	IOX2	I/O	IOX2	I/O	IOX2	I/O	IOX2	I/O	IOX2	I/O	IOX2	I/O	IOX2	I/O	IOX2	I/O	Oscen2
30	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	
31	EXTRST_	I	EXTRST_	I	EXTRST_	I	EXTRST_	I	EXTRST_	I	EXTRST_	I	EXTRST_	I	EXTRST_	I	bd4rtu
32	HOME	I	HOME	I	HOME	I	HOME	I	HOME	I	HOME	I	INTI_	I		I	bd4rt
33	TSTMOD	I	TSTMOD	I	TSTMOD	I	TSTMOD	I	TSTMOD	I	TSTMOD	I	TSTMOD	I	TSTMOD	I	bd4rtd
34	MT_PH0	O	MT_PH0	O	MT_PH0	O	MT_PH0	O	MT_PH0	O	MT_PH0	O		O		O	bd4rt
35	MT_PH1	O	MT_PH1	O	MT_PH1	O	MT_PH1	O	MT_PH1	O	MT_PH1	O		O		O	bd4rt
36	MT_PH2	O	MT_PH2	O	MT_PH2	O	MT_PH2	O	MT_PH2	O	MT_PH2	O		O		O	bd4rt
37	MT_PH3	O	MT_PH3	O	MT_PH3	O	MT_PH3	O	MT_PH3	O	MT_PH3	O		O		O	bd4rt
38	MT_PH4	O	MT_PH4	O	MT_PH4	O	MT_PH4	O	MT_PH4	O	MT_PH4	O		O		O	bd4rt
39	MT_PH5	O	MT_PH5	O	MT_PH5	O	MT_PH5	O	MT_PH5	O	MT_PH5	O		O		O	bd4rt
40	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	
41	XPA_SW	O	XPA_SW	O	XPA_SW	O	XPA_SW	O	XPA_SW	O	XPA_SW	O		O		O	bd4rt
42	LAMP_SW	O	LAMP_SW	O	LAMP_SW	O	LAMP_SW	O	LAMP_SW	O	LAMP_SW	O		O		O	bd4rt
43	LED_B	O	LED_B	O	LED_B	O	LED_B	O	LED_B	O	LED_B	O		O	EB05O	O	bd4rt
44	*AVDD*	*P*	*AVDD*	*P*	*AVDD*	*P*	*AVDD*	*P*	*AVDD*	*P*	*AVDD*	*P*	*AVDD*	*P*	*AVDD*	*P*	
45	VMO	I/O	VMO	I/O	VMO	I/O	VMO	I/O	VMO	I/O	VMO	I/O	VMO	I/O	VMO	I/O	
46	VPO	I/O	VPO	I/O	VPO	I/O	VPO	I/O	VPO	I/O	VPO	I/O	VPO	I/O	VPO	I/O	
47	VPP	O	VPP	O	VPP	O	VPP	O	VPP	O	VPP	O	VPP	O	VPP	O	
48	*AGND*	*P*	*AGND*	*P*	*AGND*	*P*	*AGND*	*P*	*AGND*	*P*	*AGND*	*P*	*AGND*	*P*	*AGND*	*P*	
49	CCD_CK1X	O	CCD_CK1X	O	CCD_CK1X	O	CCD_CK1X	O	CCD_CK1X	O	CCD_CK1X	O		O		O	bd4rt
50	CCD_CK2X	O	CCD_CK2X	O	CCD_CK2X	O	CCD_CK2X	O	CCD_CK2X	O	CCD_CK2X	O		O		O	bd4rt
51	CCD_CPX	O	CCD_CPX	O	CCD_CPX	O	CCD_CPX	O	CCD_CPX	O	CCD_CPX	O		O		O	bd4rt
52	CCD_RSX	O	CCD_RSX	O	CCD_RSX	O	CCD_RSX	O	CCD_RSX	O	CCD_RSX	O		O		O	bd4rt

53	CCD_TGX	O	CCD_TGX	O	CCD_TGX	O	CCD_TGX	O	CCD_TGX	O	CCD_TGX	O		O		O	bd4rt
54	CCD_TGG	O	CCD_TGG	O	CCD_TGG	O	CCD_TGG	O	CCD_TGG	O	CCD_TGG	O		O		O	bd4rt
55	CCD_TGB	O	CCD_TGB	O	CCD_TGB	O	CCD_TGB	O	CCD_TGB	O	CCD_TGB	O		O		O	bd4rt
56	RGBSEL0	O	RGBSEL0	O	RGBSEL0	O	RGBSEL0	O	RGBSEL0	O	RGBSEL0	O		O		O	bd4rt
57	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	
58	*DVSS*	*P*	*DVSS*	*P*	*DVSS*	*P*	*DVSS*	*P*	*DVSS*	*P*	*DVSS*	*P*	*DVSS*	*P*	*DVSS*	*P*	
59	*DVDD*	*P*	*DVDD*	*P*	*DVDD*	*P*	*DVDD*	*P*	*DVDD*	*P*	*DVDD*	*P*	*DVDD*	*P*	*DVDD*	*P*	
60	*R_IN*	*I*	*R_IN*	*I*	*R_IN*	*I*	*R_IN*	*I*	*R_IN*	*I*	*R_IN*	*I*	*R_IN*	*I*	*R_IN*	*I*	*Pesd7042*
61	*G_IN*	*I*	*G_IN*	*I*	*G_IN*	*I*	*G_IN*	*I*	*G_IN*	*I*	*G_IN*	*I*	*G_IN*	*I*	*G_IN*	*I*	*Pesd7042*
62	*B_IN*	*I*	*B_IN*	*I*	*B_IN*	*I*	*B_IN*	*I*	*B_IN*	*I*	*B_IN*	*I*	*B_IN*	*I*	*B_IN*	*I*	*Pesd7042*
63	*VRLC*	*O*	*VRLC*	*O*	*VRLC*	*O*	*VRLC*	*O*	*VRLC*	*O*	*VRLC*	*O*	*VRLC*	*O*	*VRLC*	*O*	*Pesd7042*
64	*VMID*	*O*	*VMID*	*O*	*VMID*	*O*	*VMID*	*O*	*VMID*	*O*	*VMID*	*O*	*VMID*	*O*	*VMID*	*O*	*Pesd7042*
65	*VRT*	*O*	*VRT*	*O*	*VRT*	*O*	*VRT*	*O*	*VRT*	*O*	*VRT*	*O*	*VRT*	*O*	*VRT*	*O*	*Pesd7042*
66	*VRB*	*O*	*VRB*	*O*	*VRB*	*O*	*VRB*	*O*	*VRB*	*O*	*VRB*	*O*	*VRB*	*O*	*VRB*	*O*	*Pesd7042*
67	*VRU*	*I*	*VRU*	*I*	*VRU*	*I*	*VRU*	*I*	*VRU*	*I*	*VRU*	*I*	*VRU*	*I*	*VRU*	*I*	*Pesd7042*
68	*AVSS*	*P*	*AVSS*	*P*	*AVSS*	*P*	*AVSS*	*P*	*AVSS*	*P*	*AVSS*	*P*	*AVSS*	*P*	*AVSS*	*P*	
69	*AVDD*	*P*	*AVDD*	*P*	*AVDD*	*P*	*AVDD*	*P*	*AVDD*	*P*	*AVDD*	*P*	*AVDD*	*P*	*AVDD*	*P*	
70	DBUS0	I/O	DBUS0	I/O	DBUS0	I/O	DBUS0	I/O	DBUS0	I/O	DBUS0	I/O	TSTPC0	I/O		I/O	bd4rt
71	DBUS1	I/O	DBUS1	I/O	DBUS1	I/O	DBUS1	I/O	DBUS1	I/O	DBUS1	I/O	TSTPC1	I/O		I/O	bd4rt
72	DBUS2	I/O	DBUS2	I/O	DBUS2	I/O	DBUS2	I/O	DBUS2	I/O	DBUS2	I/O	TSTPC2	I/O		I/O	bd4rt
73	DBUS3	I/O	DBUS3	I/O	DBUS3	I/O	DBUS3	I/O	DBUS3	I/O	DBUS3	I/O	TSTPC3	I/O		I/O	bd4rt
74	DBUS4	I/O	DBUS4	I/O	DBUS4	I/O	DBUS4	I/O	DBUS4	I/O	DBUS4	I/O	TSTPC4	I/O		I/O	bd4rt
75	DBUS5	I/O	DBUS5	I/O	DBUS5	I/O	DBUS5	I/O	DBUS5	I/O	DBUS5	I/O	TSTPC5	I/O		I/O	bd4rt
76	DBUS6	I/O	DBUS6	I/O	DBUS6	I/O	DBUS6	I/O	DBUS6	I/O	DBUS6	I/O	TSTPC6	I/O		I/O	bd4rt
77	DBUS7	I/O	DBUS7	I/O	DBUS7	I/O	DBUS7	I/O	DBUS7	I/O	DBUS7	I/O	TSTPC7	I/O		I/O	bd4rt
78	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	DGND	P	
79	DBUS8	I/O	DBUS8	I/O	DBUS8	I/O	DBUS8	I/O	DBUS8	I/O	DBUS8	I/O		I/O		I/O	bd4rt
80	DBUS9	I/O	DBUS9	I/O	DBUS9	I/O	DBUS9	I/O	DBUS9	I/O	DBUS9	I/O		I/O		I/O	bd4rt
81	DBUS10	I/O	DBUS10	I/O	DBUS10	I/O	DBUS10	I/O	DBUS10	I/O	DBUS10	I/O		I/O		I/O	bd4rt
82	DBUS11	I/O	DBUS11	I/O	DBUS11	I/O	DBUS11	I/O	DBUS11	I/O	DBUS11	I/O		I/O		I/O	bd4rt
83	DBUS12	I/O	DBUS12	I/O	DBUS12	I/O	DBUS12	I/O	DBUS12	I/O	DBUS12	I/O		I/O		I/O	bd4rt
84	DBUS13	I/O	DBUS13	I/O	DBUS13	I/O	DBUS13	I/O	DBUS13	I/O	DBUS13	I/O		I/O		I/O	bd4rt
85	DBUS14	I/O	DBUS14	I/O	DBUS14	I/O	DBUS14	I/O	DBUS14	I/O	DBUS14	I/O		I/O		I/O	bd4rt
86	DBUS15	I/O	DBUS15	I/O	DBUS15	I/O	DBUS15	I/O	DBUS15	I/O	DBUS15	I/O		I/O		I/O	bd4rt
87	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	
88	RASX	O	RASX	O	RASX	O	RASX	O	RASX	O	RASX	O		O	OP0	O	bd4rt
89	CASX	O	CASX	O	CASX	O	CASX	O	CASX	O	CASX	O		O	OP1	O	bd4rt
90	NOEX	O	NOEX	O	NOEX	O	NOEX	O	NOEX	O	NOEX	O		O	OP2	O	bd4rt
91	NWEX	O	NWEX	O	NWEX	O	NWEX	O	NWEX	O	NWEX	O		O	OP3	O	bd4rt
92	RASY	O	RASY	O	RASY	O	RASY	O	RASY	O	RASY	O		O	OP4	O	bd4rt
93	CASY	O	CASY	O	CASY	O	CASY	O	CASY	O	CASY	O		O	OP5	O	bd4rt
94	NOEY	O	NOEY	O	NOEY	O	NOEY	O	NOEY	O	NOEY	O		O	OP6	O	bd4rt
95	NWEY	O	NWEY	O	NWEY	O	NWEY	O	NWEY	O	NWEY	O		O	OP7	O	bd4rt
96	ABUS0	O	ABUS0	O	ABUS0	O	ABUS0	O	ABUS0	O	ABUS0	O		O	OP8	O	bd4rt
97	ABUS1	O	ABUS1	O	ABUS1	O	ABUS1	O	ABUS1	O	ABUS1	O		O	OP9	O	bd4rt
98	ABUS2	O	ABUS2	O	ABUS2	O	ABUS2	O	ABUS2	O	ABUS2	O		O	OP10	O	bd4rt
99	ABUS3	O	ABUS3	O	ABUS3	O	ABUS3	O	ABUS3	O	ABUS3	O		O	OP11	O	bd4rt
100	ABUS4	O	ABUS4	O	ABUS4	O	ABUS4	O	ABUS4	O	ABUS4	O		O	OP12	O	bd4rt
101	ABUS5	O	ABUS5	O	ABUS5	O	ABUS5	O	ABUS5	O	ABUS5	O		O	OP13	O	bd4rt
102	ABUS6	O	ABUS6	O	ABUS6	O	ABUS6	O	ABUS6	O	ABUS6	O		O		O	bd4rt
103	ABUS7	O	ABUS7	O	ABUS7	O	ABUS7	O	ABUS7	O	ABUS7	O		O		O	bd4rt
104	ABUS8	O	ABUS8	O	ABUS8	O	ABUS8	O	ABUS8	O	ABUS8	O		O		O	bd4rt
105		I	OP0	I	DMAD0	I/O		I	OP0	O	OP0	I	TSTPB0	I	OEB	I	bd4rt
106		I	OP1	I	DMAD1	I/O		I	OP1	O	OP1	I	TSTPB1	I	CDSCLK2	I	bd4rt
107		I	OP2	I	DMAD2	I/O		I	OP2	O	OP2	I	TSTPB2	I	ADCCLK	I	bd4rt
108		I	OP3	I	DMAD3	I/O		I	OP3	O	OP3	I	TSTPB3	I	SMPTIMG	I	bd4rt
109		I	OP4	I	DMAD4	I/O		I	OP4	O	OP4	I	TSTPB4	I	RLC	I	bd4rt
110		I	OP5	I	DMAD5	I/O		I	OP5	O	OP5	I	TSTPB5	I	OOP0	Z	bd4rt
111		I	OP6	I	DMAD6	I/O		I	OP6	O	OP6	I	TSTPA0	I	OOP1	Z	bd4rt
112		I	OP7	I	DMAD7	I/O		I	OP7	O	OP7	I	TSTPA3	I		I	bd4rt
113	VSMP	O	VSMP	O	VSMP	O	VSMP	O	VSMP	O	VSMP	O	TSTPA4	I	VSMP	I	bd4rtu
114	BSMP	O	BSMP	O	BSMP	O	BSMP	O	BSMP	O	BSMP	O	TSTPA5	I	CDSCLK1	I	bd4rtu
115		I	SCLK	O		I		I	SCLK	O	SCLK	O		I	SCK	I	bd4rtu
116		I	SENLOAD	O	MPUCLK	O		I	SENLOAD	O	SENLOAD	O		I	SEN	I	bd4rtu
117	MCLK	O	MCLK	O	MCLK	O	MCLK	O	MCLK	O	MCLK	O		I	MCLK	I	bd4rtu
118		I	SDI	O	MPUCKOE	I		I	SDI	O	SDI	O			SDI	I	bd4rtd

119		I	SDO	I	CKSEL	I		I		I	SDO	I	TSTPA7	I		I	bd4rtd
120	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	DVDD	P	
121	MTR_SEL	I	MTR_SEL	I	MTR_SEL	I	MTR_SEL	I	MTRS_EL	I	MTR_SEL	I	MTR_SEL	I	MTR_SEL	I	bd4rtd
122	MPU_SEL	I	MPU_SEL	I	MPU_SEL	I	MPU_SEL	I	MPUS_EL	I	MPUS_EL	I	MPUS_EL	I	MPUS_EL	I	bd4rtd
123	GPIO1	I/O	GPIO1	I/O	GPIO1	I/O	GPIO1	I/O	GPIO1	I/O	GPIO1	I/O	GPIO1	I/O	GPIO1	I/O	bd4rt
124	GPIO2	I/O	GPIO2	I/O	GPIO2	I/O	GPIO2	I/O	GPIO2	I/O	GPIO2	I/O	GPIO2	I/O	GPIO2	I/O	bd4rt
125	GPIO3	I/O	GPIO3	I/O	GPIO3	I/O	GPIO3	I/O	GPIO3	I/O	WMSEL/GPIO3	I/O	GPIO3	I/O	GPIO3	I/O	bd4rt
126	GPIO4	I/O	GPIO4	I/O	GPIO4	I/O	GPIO4	I/O	GPIO4	I/O	RLCSEL/GPIO4	I/O	GPIO4	I/O	GPIO4	I/O	bd4rt
127	TSTSEL0	I	TSTSEL0	I	TSTSEL0	I	TSTSEL0	I	TSTSEL0	I	TSTSEL0	I	TSTSEL0	I	TSTSEL0	I	bd4rtd
128	TSTSEL1	I	TSTSEL1	I	TSTSEL1	I	TSTSEL1	I	TSTSEL1	I	TSTSEL1	I	TSTSEL1	I	TSTSEL1	I	bd4rtd

NOTE:

In TCD2950D CCD:

Pin No :	Pin Name	NORMAL	FAST
49	CCD_CK1X	Clock 1	Clock 3
50	CCD_CK2X	Clock 2	Clock 2
56	RGB_SEL0	Clock 2	Clock 1

In Mode 6 (SC TEST) :

Pin No :	MPU_SEL = 0	MPU_SEL = 1
19	GPIO5	DMAD0
20	GPIO6	DMAD1
21	GPIO7	DMAD2
22	GPIO8	DMAD3
23	GPIO9	DMAD4
24	GPIO10	DMAD5
25	GPIO11	DMAD6
26	GPIO12	DMAD7
125	GPIO3	(WMSEL)
126	GPIO4	(RLCSEL)

In Mod 1,2,5,9
If Input clock = 12MHZ
If CKSEL = 0 => Scanner controller run 24MHZ
If CKSEL = 1 => Scanner controller run 32MHZ

In Mode 3:
If MPUCKOE = 1, MPUCLK = (Input clock frequency)/2
If CKSEL = 1 => Scanner controller run (Input clock frequency) /2
If CKSEL = 0 => Scanner controller run (Input clock frequency)
If MPUCKOE = 0, MPUCLK = 0

In Mode 4:
Scanner controller run (Input clock frequency)

5.2 Pin Descriptions :

MPU or DMA/EPP Interface		
HSLCTIN(MPU_ALE)	I	EPP nAStrb or MPU ALE
HI_INIT(MPU_CS)	I	EPP nINIT or MPU Chip select
HAFXTIN(MPU_RD)	I	EPP nDStrb or MPU Read
HSTBIN(MPU_WR)	I	EPP nWrite or MPU Write

H_BUSY(DMA_ACK)	O	EPP nWait or DMA Acknowledge
H_ACK(IO_RD)	O	EPP Intr or DMA IO Read
H_PE(IO_WR)	O	EPP AckDataReq or DMA IO Write
H_ERR(DMA_DRQ)	B	EPP nDataAvail or DMA Data Request
HD0~HD7	B	EPP Data Bus or MPU Data Bus
DMAD0~7	B	DMA Data Bus
Support IO Ports		
GPIO1~12	B	General Purpose Input Output
MT_PH0~5	O	Bi-polar : MT_PH5=PHASE1 MT_PH4=PHASE2 MT_PH3=I11 MT_PH2=I01 MT_PH1=I12 MT_PH0=I02 Uni-polar : MT_PH3=PHASE A MT_PH2=PHASE B MT_PH1=PHASE /A MT_PH0=PHASE /B
HOME	I	Sense carriage home position
USB Interface		
VMO	B	D+
VPO	B	D-
VCP	P	3.3V
CCD/CIS Control Signals		
CCD_CK1X	O	CCD Shift register clock1 or CIS clock output
CCD_CK2X	O	CCD Shift register clock2 or CIS clock output
CCD_CPX	O	CCD Clamp gate clock or CIS clock output
CCD_RSX	O	CCD Reset gate clock or CIS clock output
CCD_TGX	O	CCD Transfer gate clock for R channel or CIS Line start pulse
CCD_TGG	O	CCD Transfer gate clock for G channel
CCD_TGB	O	CCD Transfer gate clock for B channel
RGBSEL0	O	RGB channel selection pin or CCD Shift register clock3
XPA_SW	O	Transparency lamp power control or CIS Green LED array control
LAMP_SW	O	Flatbed lamp power control or CIS Red LED array control
LED_B	O	CIS Blue LED array control
FRONT-END		
R_IN	AI	Red channel input signal
G_IN	AI	Green channel input signal
B_IN	AI	Blue channel input signal
VRLC	AO	Selectable analog output voltage for RLC
VMID	AO	ADC reference voltage. Derived from VRU. Normally is 2.5V
VRT	AO	ADC reference voltage. Derived from VRU. Normally is 3.3V
VRB	AO	ADC reference voltage. Derived from VRU. Normally is 1.7V
VRU	AI	ADC reference voltage. Normally connected to 5V analog supply
OP0~OP7	O	ADC digital data output
VSMP(CDSCLK2)	O	Wolfson type : Video sample synchronization pulse.

		This signal is applied synchronously with MCLK to specify the point of time that the input is sampled. Analog Device type : CDS image sampling clock
BSMP(CDSCLK1)	O	Analog Device type : Black level sampling clock
SCLK	O	Serial interface clock output for Front-end
SENLOAD	O	Serial interface data latch-in signal for Front-end
MCLK(ADCCLK)	O	Wolfson type : Master clock. This clock is applied at either six or three times the input pixel rate depending on the operational mode. Analog Device type: ADC Converter sampling clock
SDI	O	Serial interface data output signal for Front-end
SDO	I	Serial interface data input signal for Front-end
DRAM		
DBUS0~15	B	DRAM data bus
ABUS0~8	O	DRAM address bus
RASX	O	DRAM RAS signal of first memory chip
CASX	O	DRAM CAS signal of first memory chip
NOEX	O	DRAM OE(output enable) signal of first memory chip
NWEX	O	DRAM WE signal of first memory chip
RASY	O	DRAM RAS signal of second memory chip
CASY	O	DRAM CAS signal of second memory chip
NOEY	O	DRAM OE(output enable) signal of second memory chip
NWEY	O	DRAM WE signal of second memory chip
Miscellaneous		
TSTMOD TSTSEL0 TSTSEL1 MPU_SEL	I	Test mode selection pins : {TSTMOD,TSTSEL0,TSTSEL1,MPU_SEL}= 0000 : mode1 0100 : mode2 0011 : mode3 0010 : mode4 0110 : mode5 100x : mode6 110x : mode7 101x : mode8 1110 : mode9
MTR_SEL	I	MTR_SEL=1 select Bi_polar MTR_SEL=0 select Uni_polar
IX1	I	Clock input for crystal
IOX2	O	Clock output for crystal
CKSEL MPUCLOE	I	Scanner controller clock selection
MPUCLK	O	Clock output
EXTRST_	I	Hardware reset input
POWER		
AVDD	P	Analog power input
AVSS	P	Analog ground input
AGND	P	Analog ground input for USB1.1
DVDD	P	Digital power input
DGND	P	Digital ground input

5.3 Electrical Characteristics:

5.3.1 Absolute Maximum Ratings (Voltages referenced to GND)

SYMBOL	Description	MIN	MAX
DVDD	DC supply voltage	-0.5V	+7V
V_I	DC input voltage	-0.5V	VCC+0.5V
$V_{I/O}$	DC input voltage range for I/O	-0.5V	VCC+0.5V
$V_{AI/O}$	DC input voltage for USB D+/D- pins	-0.5V	VCC+0.5V
$V_{I/OZ}$	DC voltage applied to outputs in High Z state	-0.5V	VCC+0.5V
V_{ESD}	static discharge voltage	4000V	
T_{STQ}	Storage temperature range	-60°C	+150°C
I_{OUT}	DC output current, per pin	-25mA	+25mA
T_{amb}	Operating ambient temperature	0°C	70°C

5.3.2 DC Characteristics (Digital Pins)

SYMBOL	Description	MIN	TYP	MAX	UNIT
DVDD (or AVDD)	Power Supply Voltage	4.5	5.0	5.5	V
I_O	DC output sink current	4			mA
V_{IL}	LOW level input voltage			0.8	V
V_{IH}	HIGH level input voltage	2.4			V
V_{OL}	LOW level output voltage when I_{OL}=4mA			0.4	V
V_{OH}	HIGH level output voltage when I_{OH}=4mA	2.4			V
I_{OLK}	Leakage current for pads with internal pull up or pull down resistor	-50		50	µA
I_{OZ}	Tri-state output leakage current	-50		50	µA
R_{DN}	Pad internal pulldown resister	120K	200K	290K	Ohms
R_{UP}	Pad internal pullup resister	150K	250K	360K	Ohms

5.3.3 DC Characteristics (VCP/D+/D-)

SYMBOL	Description	MIN	TYP	MAX	UNIT
$V_{3.3}$	VCP regulator output	3.0	3.3	3.6	V
$I_{3.3}$	VCP maximum supply current	27	41	56	mA
V_{OL}	D+/D- static output LOW(R_L of 1.5K to 3.6V)			0.3	V
V_{OH}	D+/D- static output HIGH (R_L of 15K to GND)	2.8		3.6	V
V_{DI}	Differential input sensitivity	0.2			V
V_{CM}	Differential common mode range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold	0.2			V
C_{IN}	Transceiver capacitance			20	pF
I_{LO}	Hi-Z state data line leakage	-10		+10	µA
Z_{DRV}	Driver output resistance	28		43	Ohms

Note: bd4rt without pull up or pull down resister.
bd4rtu with 250k pull up resister.

6. Application Description

6.1. System Clock

Internal PLL or external clock input.

A. PLL: 12MHz input , 24 or 32 MHz output to internal system and 48MHz output to internal USB controller.

B. USB2.0 supply: External USB2.0 controller support 24,30,48 MHz to three in one ASIC.

C. Crystal supply: depend on crystal input (receptible frequency of ASIC: 12 to 48 MHz)

6.2. Pixel Clock

A. Normal Mode(three line in):

a. 24 system clock/pixel

b. Chunky color scan(three line in) or fine gray scan for CCD.

B. Fast Mode(one line in) :

a. 9,12 or 15 system clock/pixel three type.

b. Planar color scan (one line in) or Monochrome scan.

c. Fast gray or black & white scan for CCD.

d. Planar color(one line in) for CCD line by turns or line by line.

e. Planar color(one line in),gray, true gray or black & white scan for CIS.

Note : Chunky Color is R1G1B1,R2G2B2,R3G3B3,……

Planar Color is R1,R2,R3,…..;G1,G2,G3,…….;B1,B2,B3,……..

CCD : Chunky color or planar color.

CIS : Planar color

6.3. Scan Speed

A. System clock = 24 MHz :

a. Normal Mode: Chunky color or fine gray scan.

24x41.666ns/pixel = 1.0us/pixel

(1). 600dpi : 5.4ms/line

(2). 1200dpi : 10.4ms/line

b. Fast Mode: Planar color, fast gray or black&white scan.

9x41.666ns/pixel = 0.375us/pixel

12x41.666ns/pixel = 0.5us/pixel

15x41.666ns/pixel = 0.625us/pixel

(1). 600dpi : 2.025~3.375ms/line

(2). 1200dpi : 4.05~6.75ms/line

B. System clock = 32MHz :

a. Normal Mode :

24x31.25ns/pixel = 0.75us/pixel

(1). 600dpi : 4.05ms/line

(2). 1200dpi : 8.1ms/line

b. Fast Mode :

9x31.25ns/pixel = 0.281us/pixel

12x31.25ns/pixel = 0.375us/pixel

15x31.25ns/pixel = 0.469us/pixel

(1). 600dpi : 1.517~2.533ms/line

(2). 1200dpi : 3.034~5.066ms/line

6.4. Fast scan for low DPI

Multiple CCD clocking rates allows speed up scan speed. You can speed up 2 times, 3 times or 4 times scanning time for low resolution.

For example,600dpi scanner: if 75dpi speed up 4 times then 5.4ms/4=1.35ms/line. Scan speed is equal to 1.18s/page.

Chunky scan: You can speed up 2 times,3 times or 4 times scanning time.

Planar scan: 9 system clock/pixel: You can not speed up scanning time

12 system clock/pixel : You can speed up 2 times scanning time

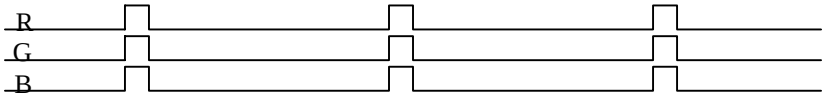
15 system clock/pixel : You can speed up 2 times scanning time

6.5. Scanning Type

Support three line in(parallel) for CCD, one line in for CCD or CIS, RGB line by turns in for CCD three types.

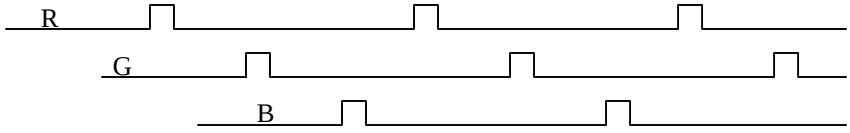
A. CCD

a. Three line in :



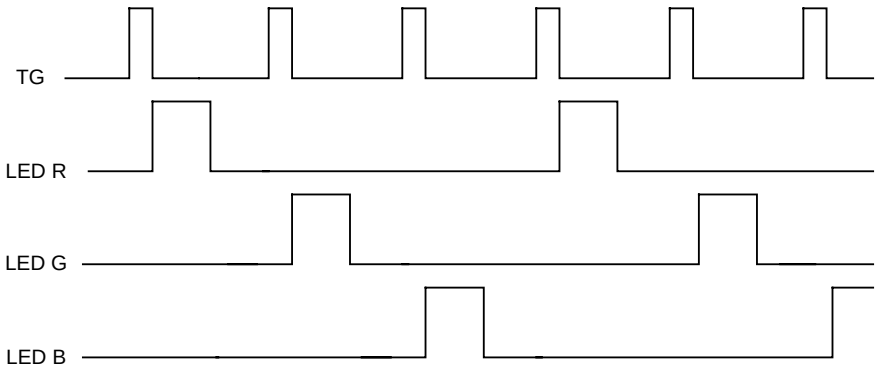
b. Line by line :

c. Line by turns :

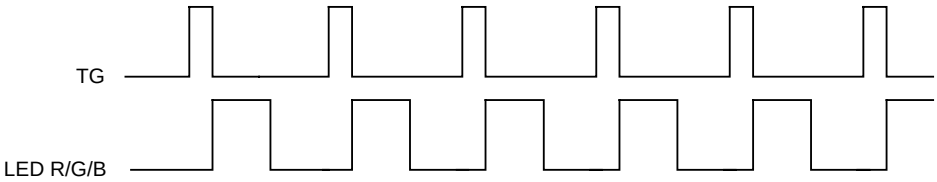


B. CIS

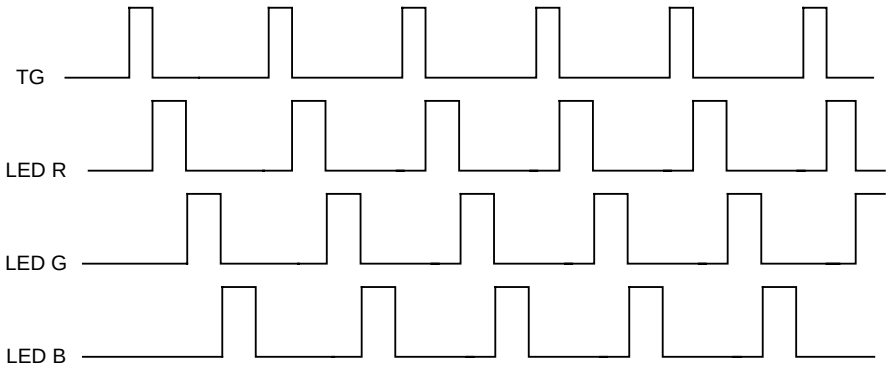
a. color scan :



b. gray scan:



c. true gray scan:



6.6. Image Sensor Timing

Can be programmed.

A. CCD : support 600,1200 or 2400 dpi CCD.

For example NEC, TOSHIBA, Sony ……etc.

B. CIS : support 600,1200 or 2400 dpi CIS.

For example Canon , Toshiba , Mitsubishi ……etc.

6.7. Dummy Line

Support programmable dummy lines to resolve (overcome) Start/Stop problem.

You can insert dummy lines to reduce scanner stop and wait events (buffer full) or always no-stop.

A. Line base of dummy lines:

The range of dummy lines is 0 line ~ 15 lines.

B. Adjustable dummy line:

The range is CCD or CIS minimum shift out time to 512k pixels time, can be adjusted by 1 pixel time increment.

6.8. Analog Front End Timing :

Internal 16 bits Front-End : Operation is similar to Wolfson or Analog Device.

6.9. Image Type

Support color, fine gray, fast gray and fast Black & White scan.

Support color filters selection for gray and B/W scan. The filters include Red, Green and Blue.

Note: The scan style of fine gray and color is same. So, fine gray scanning speed is slow.

The exposure time of fast gray scan is shorter than fine gray scan. So, fast gray Scanning speed is high.

6.10. Bits Depth

16 x3 Bits true color , 16 bits gray level and one bit Black & White.

Image data type : 16 bits , 8 bits and 1 bit data type.

6.11. Shading & Correction

a. White Shading & Dark Shading:

Internal white shading by pixel (16 bits resolution) and dark shading by pixel (16 bits resolution) can be enabled or disabled By S/W. The white shading curve is calculated by S/W.

Data arrangement: Normal mode: dark R1,white R1,dark G1,white G1,dark B1,white B1,
dark R2,white R2,dark G2,white G2,dark B2,white B2,
dark R3,white R3,dark G3,white G3,dark B3,white B3,……

Fast mode: dark R1,white data R1,dark R2,white R2,dark R3, white R3…
dark G1,white data G1,dark G2,white G2,dark G3,white G3…
dark B1,white data B1,dark B2,white B2,dark B3,white B3…

White shading formula : 2000H x Target / (Wn-Dn) = White Gain data ----- for 8 times system

White shading formula : 4000H x Target / (Wn-Dn) = White Gain data ----- for 4 times system

For example : Target = 3FFFH Wn = 2FFFH Dn = 0040H and 8 times system operation

then White Gain = 2000H x 3FFFH / (2FFFH-0040H) = 2AE4H (1.34033 times)

b. Correction :

GAMMA correction table by S/W calculation. The resolution is 12 or 14 bits gamma table.

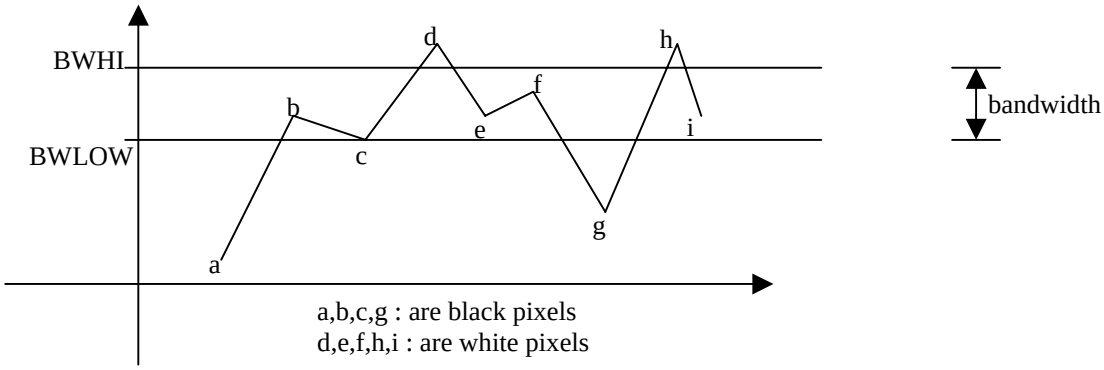
Range: 0 to 64k (16 bits) input mapping to 0 to 4k (12 bits) output ;
0 to 64k (16 bits) input mapping to 0 to 16k (14 bits)output;
0 to 64k (16 bits) input mapping to 0 to 255 (8 bits) output ;
0 to 64k (16 bits) input mapping to 0 to 255 (8 bits) output;

6.12. Threshold Level Setting

Can be programmed by S/W.

Range: 0 to 255 can be adjusted by one increment.

The threshold with bandwidth in order to reduce image noise.



6.13. Exposure Time Adjustable

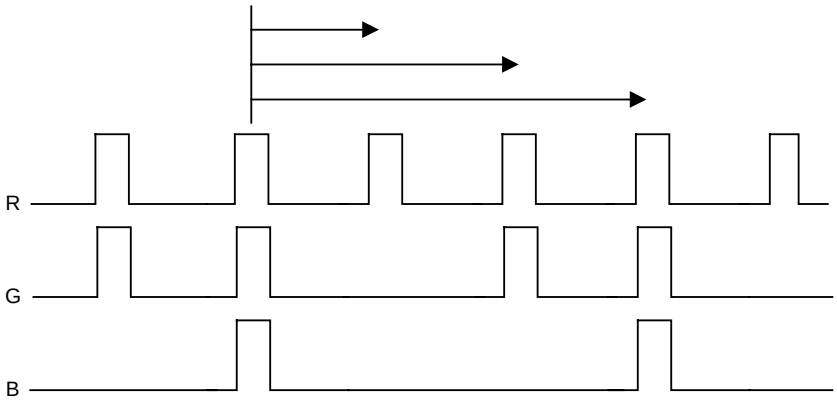
Maximum: 512k pixels time (about 524 ms/line)

Adjustment step: 1 pixel time.

For Transparency scan, the exposure time can up to 524 ms.

6.14. To Control RGB Exposure Time Separately

Scanning type: line by turns



You can control R, G or B exposure time separately.

For example, above case B exposure time is three times of R; G exposure time is two times of R.

6.15. Scan Width control

Scan width control for horizontal line

a. Support start pixel address, end pixel address and dummy pixel number setting

b. Maximum length: 64k pixels.

Minimum length: 1 pixel

6.16. Support built-in USB(1.1) , external USB(2.0) and external IEEE1394 Interface

Support 4-type operation.

Three in one: USB1.1 + AFE + scanner controller

Two in one: A. AFE + scanner controller + (external) USB2.0

B. AFE + scanner controller + (external) IEEE 1394

C. USB1.1 + scanner controller + (external) AFE

Note: Instead of our build-in AFE, you can use other external AFE.

6.17. DRAM Timing

Support 4Mx1 or x2 Bits EDO DRAM (16 x 256K) image buffer and calibration buffer timing.

You can select single or double DRAM for scanner. DRAM speed is 35ns and above for 24MHz system clock,28ns and above for 32MHz system clock.

6.18. Horizontal Resolution Adjustable for DPI Function

A. Digital deletion type :

The resolution from 1 DPI to 1200 DPI , can be adjusted by 1 DPI increment by S/W.

B. Digital average type :

Support 1/2,1/3,1/4,1/5,1/6,1/8,1/10,1/12,1/15 digital average function.

For example, 1200dpi scanner: 600dpi, 400dpi, 300dpi, 240dpi, 200dpi,150dpi, 120dpi, 100dpi, 80dpi average function.

C. CCD DPI process :

Support 1/2,1/3 and 1/4 resolution.

For example, 1200dpi scanner: output 600dpi, 400dpi and 300dpi process.

6.19. Vertical Resolution Adjustable for DPI Function

The resolution of motor speed control is 16 bits, so, we can control vertical resolution

By one dpi increment, the resolution can be from 1 DPI to 4800DPI for 1200DPI scanner

And 1 DPI to 9600 DPI for 2400dpi scanner.

Note: The resolution of quarter step can up to four times resolution.

6.20. Acceleration/Deceleration Double Table

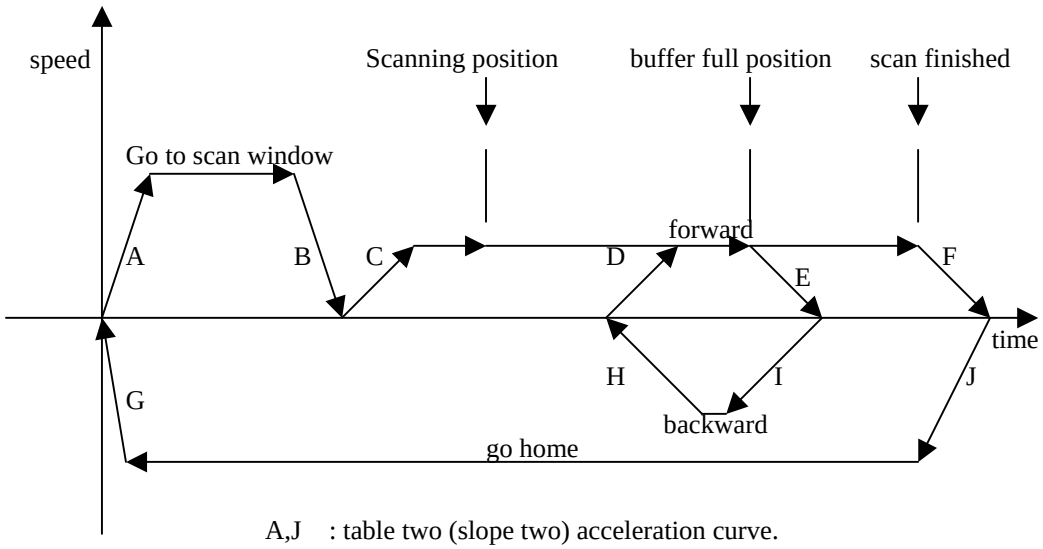
The acceleration/deceleration slope tables are store in DRAM, can be download by S/W.

The slope can be programmed by S/W for each table. Resolution is 16 bits pixel-time. The number of slope steps is 1~255 steps. One table is for scanning The other is for fast move.

The forward and backward steps can be programmed by S/W. The resolution is 16 bits pixel-time. The number of slope steps is 1~255 steps. You can adjust any non-linear curve.

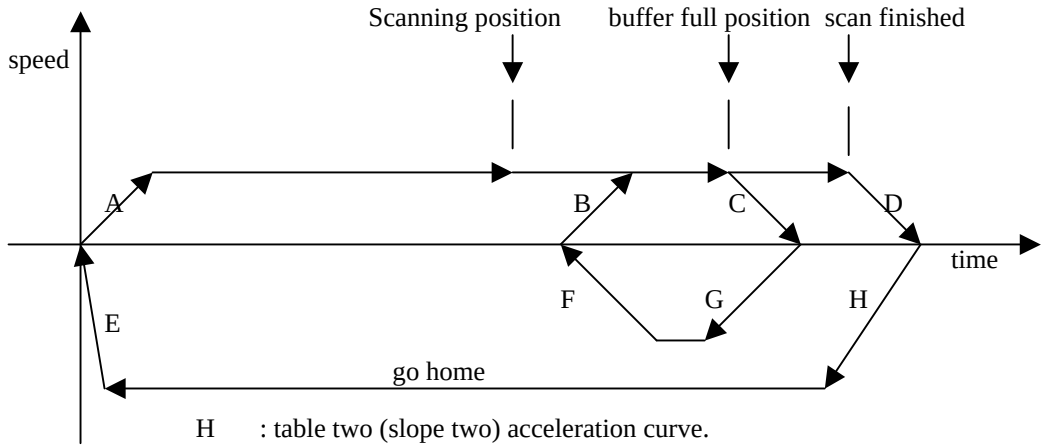
Note: what is fast move? Such as move back to go home or move to window any position to scan.

(1). Two table moving :



A,J : table two (slope two) acceleration curve.
B : table two (slope two) deceleration curve.
C,D,I : table one (slope one) acceleration curve.
E,F,H : table one (slope one) deceleration curve.
G : touch home sensor deceleration curve.

(2). One table moving :



H : table two (slope two) acceleration curve.
A,B,G : table one (slope one) acceleration curve.
C,D,F : table one (slope one) deceleration curve.
E : touch home sensor deceleration curve.

6.21. Stepping Motor Phase Control

There is 6 output control pins to control stepping motor.mtr_ph0~5 for bi-polar and mtr_ph0~3 for Uni-polar.

A. bi-polar :

a. Support 2916 motor driver timing and 2916 compatible driver IC,such as L6219.

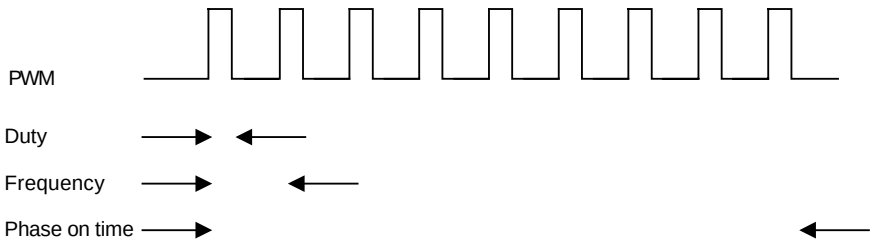
b. Include full, half and quarter step control.

B. uni-polar :

a. Support 2003 motor driver timing and 2003 compatible driver IC.

b. Include full step two phases on, full step single phase on and half step.

c. PWM control, include frequency and duty control.



6.22. Watch-Dog Protection

This function can automatically reset the system to initial state, whenever the system is held (no access signal) beyond the time limit.Be able to enable or disable this function by S/W.

This function can protect motor power, lamp power and ASIC system.

Calculation formula : (line period) x (16k) x (setting no.).

The range of setting no. is 1~15.

6.23. Lamp Timeout Control

This circuitry can automatically reset the lamp power, whenever the system is setting. Be able to enable or disable this function by S/W.

Calculation formula: (line period) x (64k) x (setting no.).

The range of setting no. is 1~7.

6.24. Lamp Power Control

These are two power control ports for lamp. One is for Flatbed and the other is for XPA (Transparency or film).

The resolution of it's PWM type is 9 bits. Duty range is 1/512~512/512.

Note : carrier frequency is (system clock)/512.

6.25. 6.25 Sensor Input

The system support home sensor input port.

6.26. 9 GPIO ports

You can set input or output for each GPIO pin separately.

Such as keypads inputs, document sensor for sheet-fed or motor power control…etc.

Note : there are two pins for special function. One is GPIO12,the other is GPIO11.

GPIO12 : 1. Pull up by resister to indicate that ASIC turn on lamp power whenever power on initial.

2. Pull down by resister to indicate that ASIC turn off lamp power whenever power on initial.

3. This pin can control bi-polar motor driver 2916 or 6219 Vref in order to control max. current.

GPIO11 : This pin can control bi-polar motor driver 2916 or 6219 Vref in order to control max. current.

6.27 Lossless Data Compression

A. Support lossless 8 bits image data compression.

B. The best ratio is 4 times.

C. Real-time decompression type.

D. This function can be enabled or disabled by S/W.

6.28. Motor Trigger signal for ADF

Motor trigger signal for ADF motor moving ,can be controlled under scanning condition.

6.29. Operation Mode

There is 9 mode to operate this chip.

A. Mode1 : SC+AFE+USB1.1---------- three in one

B. Mode2 : SC+USB1.1 ---------- external AFE

C. Mode3 : SC+AFE(for IEEE1394) ---------- external IEEE1394

D. Mode4 : SC+AFE(for USB2.0) ---------- external USB2.0

E. Mode5 : test PLL & Debug

F. Mode6 : test internal SC

G. Mode7 : test internal USB1.1

H. Mode8 : test internal AFE

I. Mode9 : test internal CPU

Note: SC is scanner controller; AFE is analog front-end.

6.30. Power on Check

The default status of the PWRBIT is reset.You can set the PWRBIT and then read back the status in order to check the power status. This operation be able to check first time power on or not.

6.31. DMA image read.

Support DMA image read for DMA operation.

6.32. DMA DRAM read/write

Support DMA read/write function for Gamma Table, Shading Data and Acceleration/Deceleration Table down-load

or read back

6.33. RAM Test

S/W can test DRAM IC by write and read back data.

7. COMMAND SET DESCRIPTION

Reg.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01	CISSET	DOGENB	DVDSET	FASTMOD	COMPENB	DRAMSEL	SHDAREA	S CAN
02	NOTHOME	ACDCDIS	AGOHOME	MTRPWR	FASTFED	MTRREV	STEPSEL[1:0]	
03	TG3	AVEENB	XPASEL	LAMPPWR	LAMPDOG	LAMPTIM[2:0]		
04	LINEART	BITSET	ADTYPE[1:0]		FILTER[1:0]		FESET[1:0]	
05	DPIHW[1:0]		GMMTYPE[1:0]		GMMENB	LEDADD	BASESEL[1:0]	
06				PWRBIT	GAIN4	OPTEST[2:0]		
07							DMASEL	DMARDWR
08	RSH[4:0]							
09	RSL[4:0]							
0A	CPH[4:0]							
0B	CPL[4:0]							
0E	SCANRESET							
0F	MOVE							
10	EXPR[15:8]							
11	EXPR[7:0]							
12	EXPG[15:0]							
13	EXPG[7:0]							
14	EXPB[15:8]							
15	EXPB[7:0]							
16	CTRLHI	SELINV	TGINV	CK1INV	CK2INV	CTRLINV	CKDIS	CTRLDIS
17	TGMODE[1:0]		TGW[5:0]					
18	CNSET	DCKSEL[1:0]		CKTOGGLE	CKDELAY[1:0]		CKSEL[1:0]	
19	EXPDMY[7:0]							
1A	CKH[4:0]							
1B	CKL[4:0]							
1C	CK3SEL	CK3INV	TGSEL[5:0]					
1D	CKMANUAL	TCDFAST	DMYPIX	TGSHLD[4:0]				
1E	WDTIME[3:0]				LINESEL[3:0]			
1F	SCANFED[7:0]							
20	BUFSEL[7:0]							
21	STEPNO[7:0]							
22	FWDSTEP[7:0]							
23	BWDSTEP[7:0]							
24	FASTNO[7:0]							
25							LINCNT[17:16]	
26	LINCNT[15:8]							
27	LINCNT[7:0]							
28								LAMPPWM[8]

Reg.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
29	LAMPPWM[7:0]							
2A		RAMA[14:0]						
2B	RAMA[7: 0]							
2C					DPISET[11:8]			
2D	DPISET[7:0]							
2E	BWHI[7:0]							
2F	BWLOW[7:0]							
30	STRPIXEL[15:8]							
31	STRPIXEL[7:0]							
32	ENDPIXEL[15:8]							
33	ENDPIXEL[7:0]							
34	DUMMY[7:0]							
35						MAXWD[18:16]		
36	MAXWD[15:8]							
37	MAXWD[7:0]							
38	LPERIOD[15:8]							
39	LPERIOD[7:0]							
3A							FEWRDATA[9:8]	
3B	FEWRDATA[7:0]							
3C	RAMWRDATA[7:0]							
3D							FEEDL[17:16]	
3E	FEEDL[15:8]							
3F	FEEDL[7:0]							
41	PWRBIT	BUFEMPTY	FEEDFSH	SCANFSH	HOMESNR	LAMPSTS	FEBUSY	MOTMFLG
42						VALIDWORD[18:16]		
43	VALIDWORD[15:8]							
44	VALIDWORD[7:0]							
45	RAMRDDATA[7:0]							
46							FERDDATA[9:8]	
47	FERDDATA[7:0]							
48							FEDCNT[17:16]	
49	FEDCNT[15:8]							
4A	FEDCNT[7:0]							
4B							SCANCNT[17:16]	
4C	SCANCNT[15:8]							
4D	SCANCNT[7:0]							
4E	LPERIODRD[15:8]							
4F	LPERIODRD[7:0]							
50			FERDA[5:0]					
51			FEWRA[5:0]					
Reg.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

52				RHI[4:0]				
53				RLOW[4:0]				
54				GHI[4:0]				
55				GLOW[4:0]				
56				BHI[4:0]				
57				BLOW[4:0]				
58	VSMP[4:0]				VSMPW[2:0]			
59	BSMP[4:0]				BSMPW[2:0]			
5A	WMSEL	RLCSEL	CDSREF[1:0]		RLC[3:0]			
5B				CKFH[4:0]				
5C				CKFL[4:0]				
5D				CKSH[4:0]				
5E				CKSL[4:0]				
60	Z1MOD[15:8]							
61	Z1MOD[7:0]							
62	Z2MOD[15:8]							
63	Z2MOD[7:0]							
64	PHFREQ[7:0]							
65			MTRPWM[5:0]					
66			GPO12	GPO11				GPO7
67			GPO6	GPO5	GPO4	GPO3	GPO2	GPO1
68	GPOM12	GPOM11	GPOE12	GPOE11				GPOE7
69			GPOE6	GPOE5	GPOE4	GPOE3	GPOE2	GPOE1
6A	FSTPSEL[1:0]		FASTPWM[5:0]					
6B	FMOVNO[7:0]							
6C	TGTIME[1:0]		Z2MOD[18:16]			Z1MOD[18:16]		
6D	DECSEL[2:0]			STOPTIM[4:0]				
70			GPI12	GPI11				GPI7
71			GPI6	GPI5	GPI4	GPI3	GPI2	GPI1

Note: Reg4x , Reg7x are read ports. The other are write ports.

7.1. Reg : 01H (Write)

Default : 00H

B7:CISSET : set: CIS scan type.
: reset: CCD scan type.

B6:DOGENB : set: enable watch dog of ASIC(set time out:Reg1E[7:4]).
: reset: disable.

B5:DVDSET : set : enable shading (include whole line shading and area shading two kinds).
: reset : disable shading.

B4:FASTMOD : set: enable fast mode scanning type (include fast gray and Black & White scan).
: reset: enable normal mode scanning type (include fine gary and color scan).

B3:COMPENB : set: enable data compression.
: reset: disable

B2:DRAMSEL : set : the DRAM size is 4Mx2 (256kx16x2) bits.
: reset : the DRAM size is 4Mx1(256kx16x1) bits.

B1:SHDAREA : set: enable shading area (depend on scan area and scan dpi).
: reset: shading area is whole line.

B0:SCAN : set: enable scan process.
: reset: disable scan process.

7.2. Reg : 02H (Write)

Default : 01H

B7:NOTHOME : set: auto-go-home doesn't go back to home position.
: reset: go back to home position automatically.

B6:ACDCDIS : set: disable forward/backward moving whenever buffer full.
: reset: enable forward/backward moving whenever buffer full.

B5:AGOHOME : set: whenever scan is finished, carriage go home automatically.
: reset: disable auto-go-home function.

B4:MTRPWR : set: turn on MOTOR power and phase.
: reset: turn off MOTOR power and phase.

B3:FASTFED : set: enable two table for motor moving of theacceleration/deceleration.
: reset: disable two table, only use single table.

B2:MTRREV : set: set motor reverse moving.
: reset: set motor forward moving.

B1~0:STEPSEL[1:0] : for table one scanning move step type selection.

(1).bi-polar :
a.00: full step.
b.01: half step.
c.10: quarter step.
d.11: reserved.

(2).uni-polar :
a.00: two-phase-on full step.
b.01: half step.
c.10: reserved.
d.11: single-phase-on full step.

7.3. Reg : 03H (Write)

Default : 0CH

B7:TG3 : set: enable alternated CCD TG function.
: reset: disable.

B6:AVEENB : set: select dpi average function
: reset: select dpi deletion function.

B5:XPASEL : set: select transparency lamp on.
: reset: select flatbed lamp on.

B4:LAMPPWR: set: turn on LAMP power.
: reset: turn off LAMP power.

B3:LAMPDOG : set: to start lamp sleeping mode(default on).
: reset: to disable lamp sleeping mode.

B2~0:LAMPTIM[2:0] : lamp on time setting (default: 4)
FASTMOD=1: LAMPTIM*2*(64k)*Line-Period.
FASTMOD=0: LAMPTIM*(64k)*Line-Period.

7.4. Reg : 04H (Write)

Default : 03H

B7:LINEART : set: Black/White scan.
: reset: Color/Gray scan.

B6:BITSET : set : 16 bits image data type (= word).
: reset : 8 bits image data type (= byte).

B5~4:ADTYPE[1:0] : front end bits type: a.00: reserved.
b.01: 16 bits.
c.10: reserved.
d.11: reserved.

B3~2:FILTER[1:0] : scan color type : a.00: color
b.01: R

c.10: G
d.11: B

B1~0:FESET[1:0] : front-end selection. a.00: reserved
b.01: reserved
c.10: Analog Device control style
d.11: Wolfson control style

7.5. Reg : 05H (Write)

Default:00H

B7~6: DPIHW[1:0] : set CCD/CIS resolution 00=600dpi
01=1200dpi
10=2400dpi
11=reserved.

B5~4: GMMTYPE[1:0] : set gamma bits depth. 00: 12 bits gamma table.
01: 14 bits gamma table.
10: reserved.
11: reserved.

B3: GMMENB : set: enable gamma correction.
: reset: bypass gamma correction.

B2:LEDADD : set: enable true gray by controlling CIS RGB LED array.
: reset: normal gray by controlling CIS single color LED array.

B1~0: BASESEL[1:0] : (1).fast mode : set clocks/pixel of ASIC.
00: 9 clocks/pixel.
01: 12 clocks/pixel.
10: 15 clocks/pixel.
11: reserved.
(2). Normal mode : set clocks/pixel of CCD.
00: 24 clocks/pixel.
01: 12 clocks/pixel.
10: 8 clocks/pixel.
11: 6 clocks/pixel.

7.6. Reg : 06H (Write)

Default:00H

B4: PWRBIT :When power on, set this bit.To indicate power has on.
Default is reset.

B3: GAIN4 : set: digital shading gain=4 times system.
: reset: digital shading gain=8 times system.
Note: If you want to get more precise image quality, you can set GAIN4 bit.

B2~0: OPTEST[2:0]: select ASIC operation type.
000: set normal mode to capture AFE image.
001: set DRAM bank, power on carriage initiated and ADF(motortgo) test for ASIC simulation.
010: pixel count pattern for ASIC image test.
011: line count pattern for ASIC image test.
100: counter and adder test for ASIC simulation test.
101:CCD TG test for TGMODE

7.7. Reg : 07H (Write)

Default:00H

B1:DMASEL : set: DMA access DRAM under command mode.
: reset: MPU access DRAM under command mode.

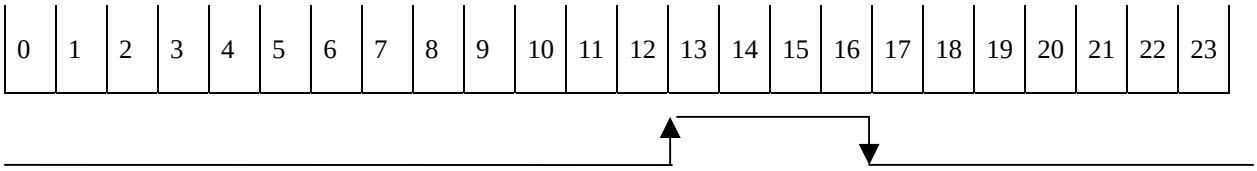
B0:DMARDWR : set: DMA read DRAM under command mode.
: reset: DMA write DRAM under command mode.
Note: DMA operation can be processed under CPU and DMA type.

7.8. Reg : 08H,09H (Write)

Default:12H,14H

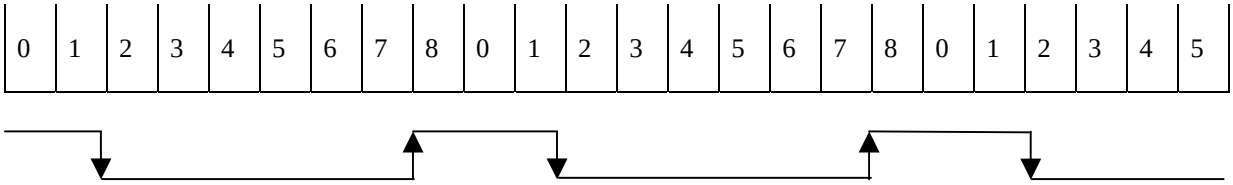
RSH[4:0]: set CCD RS rising edge position.
RSL[4:0]: set CCD RS falling edge position.

(1). Color or fine gray : 24 clocks/pixel



CCD RS : RSH=0CH RSL=10H

(2).Fast gray or B&W : 9 clocks/pixel

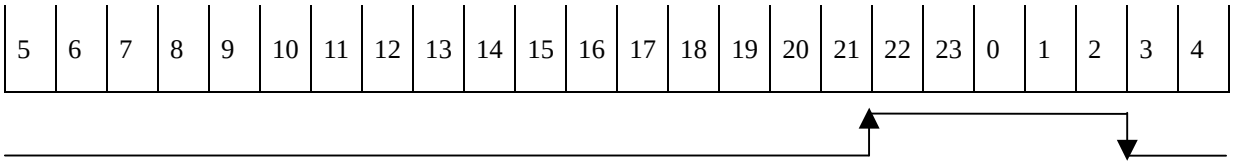


CCD RS : RSH=07H RSL=01H

7.9. Reg : 0AH,0BH (Write)

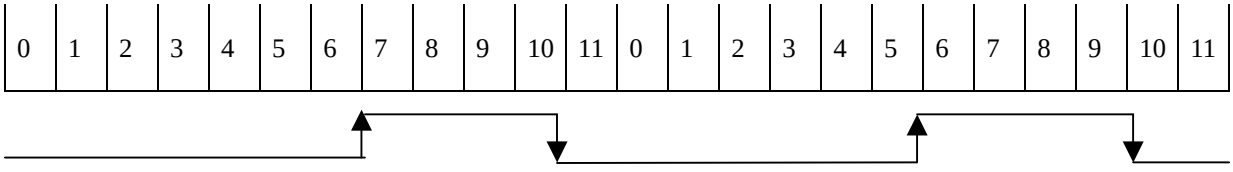
Default:15H,17H
CPH[4:0]: set CCD CP rising edge position.
CPL[4:0] : set CCD CP falling edge position.

(1). Color or fine gray : 24 clocks/pixel



CCD CP : CPH=15H CPL=02H

(2).Fast gray or B&W : 12 clocks/pixel



CCD CP : CPH=06H CPL=0AH

7.10. Reg : 0EH (Write)

Command : scanner software reset.
It can initiate AISC system, including lamp motor,
Control registers, internal circuit and status, but doesn't include tables in
DRAM, like gamma table, shading table and acceleration/deceleration table.

7.11. Reg : 0FH (Write)

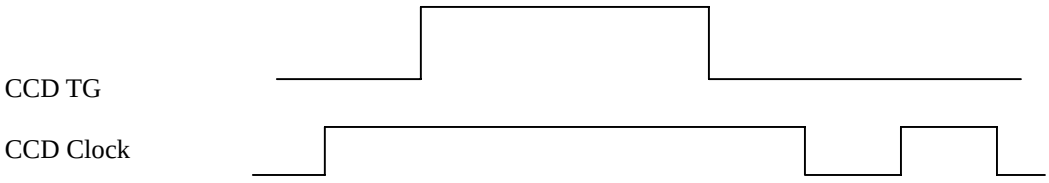
Command : motor moving.
Start motor farward/backward moving.

7.12. Reg : 10,11H (Write)
Default : 00H,00H
EXPR[15:0]: Red-LED array of CIS or Red channel TG of CCD exposure time setting.

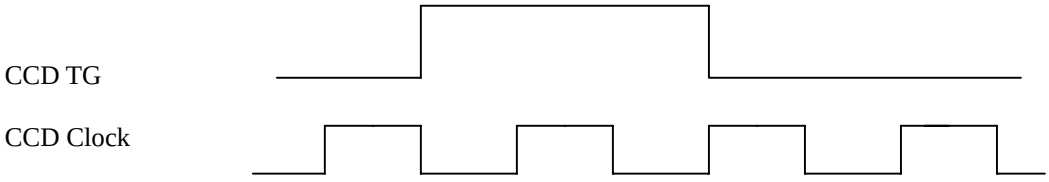
7.13. Reg : 12H,13H (Write)
Default : 00H,00H
EXPG[15:0]: Green-LED array of CIS or Green channel TG of CCD exposure time setting.

7.14. Reg : 14H,15H (Write)
Default : 00H,00H
EXPB[15:0]: Blue-LED array of CIS or Blue channel TG of CCD exposure time.

7.15. Reg : 16H (Write)
Defalut : 32H
B7:CTRLHI : set: CCD CP & RS are high under TG high position.
: reset: CCD CP & RS are low under TG high position.
B6:SELINV : set: inverse CCD RGBSEL selection pins.
: reset: don't inverse.
B5:TGINV : set: inverse CCD TG.
: reset: don't inverse.
B4:CK1INV : set: inverse CCD Clock 1.
: reset: don't inverse.
B3:CK2INV : set: inverse CCD Clock 2.
: reset: don't inverse.
B2:CTRLINV : set: inverse CCD CP & RS.
: reset: don't inverse.
B1:CKDIS : set: disable CCD TG position Clock 1/2 signals.

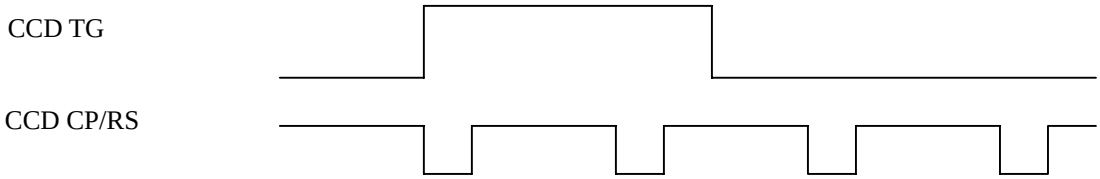


: reset: enable CCD TG position Clock 1/2 signals.



B0:CTRLDIS : set: disable CCD TG position CP & RS signals.

: reset: enable CCD TG position CP & RS signals.



7.16. Reg : 17H (Write)

Default : 14H

B7~6:TGMODE[1:0] : to set CCD TG mode.
00:without dummy line CCD TG type.
01:with dummy line CCD TG type.
10:reserved.
11:reserved.

B5~0:TGW[5:0] : to set CCD TG width.

7.17. Reg : 18H (Write)

Defalut : 00H

B7 : CNSET : set : TG and clock set to Canon CIS style.
: reset: TG and clock is non-Canon CIS style.

B6~5 :DCKSEL: 00 one time CCD Clocks speed for dummy line.
01 two time CCD Clocks speed for dummy line.
10 three time CCD Clocks speed for dummy line.
11 four time CCD Clocks speed for dummy line.

B4 :CKTOGGLE : set : half cycle per pixel for CCD Clock 1/2.
: reset : one cycle per pixel

B3~2 :CKDELAY: 00 no delay
01 delay one system clock for CCD Clock 1/2.
10 delay two system clock for CCD Clock 1/2.
11 delay three system clock for CCD Clock 1/2.

B1~0 :CKSEL : 00 one time CCD Clock speed for capture image.
01 two time CCD Clock speed for capture image.
10 three time CCD Clock speed for capture image.
11 four time CCD Clock speed for capture image.

7.18. Reg : 19H (Write)

Default : 00H

EXPDMY[7:0] : to set dummy line exposure time (unit = 256 pixels time).

7.19. Reg : 1AH,1BH (Write)

Defalut : 00H,00H

CKH[4:0]: set CCD Clock rising edge position.

CKL[4:0]: set CCD Clock falling edge position.

7.20. Reg : 1CH (Write)

Default : 00H

B7: CK3SEL : to enable CCD Clock3

B6:CK3INV : to reverse CCD Clock3

B5~B0: TGSEL[5:0] : to set CCD TG for R,G and B output control
B0~1: control R Channel TG.
B2~3: control G Channel TG.
B4~5: control B Channel TG.

7.21. Reg : 1DH (Write)

Defalut : 04H

B7 : CKMANUAL : to program CCD Clock1/2 by manual.

Programming registers are Reg5B/5C/5D/5E.
B6 : TCDFAST :reserved.
B5 : DMYPIX :reserved.
B4~0 :TGSHLD[4:0] : to set CCD TG shoulder width.

7.22. Reg : 1EH (Write)
Defalut : 20H
B7~4:WDTIME[3:0] : to set watch-dog time.
Time : fast mode : WDTIME*2*(16K)*(Line-Priod).
normal mode: WDTIME*(16K)*(Line-Priod).
B3~0:LINESEL[3:0] : to set CIS Vertical DPI or dummy lines.
CIS : LINESEL =0 full dpi.
=1 1/2 dpi
=2 1/3 dpi
=3 1/4 dpi
…..
=15 1/16 dpi
CCD : LINESEL=0 no dummy line.
=1 1 dummy line.
=2 2 dummy lines.
=3 3 dummy lines.
……
=15 15 dummy lines.
Note : CIS can be implemented dummy line by motor move method, not dummy lines.

7.23. Reg : 1FH (Write)
Default : 00H
SCANFED[7:0]: move to scanning position by table one.

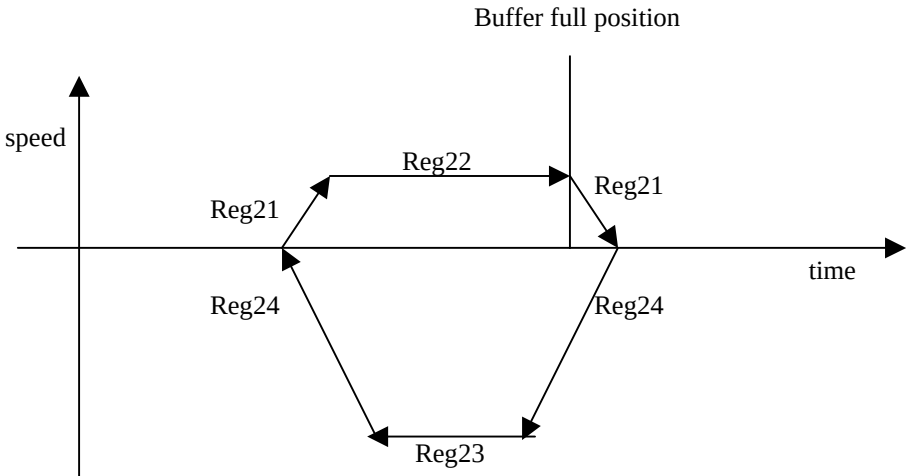
7.24. Reg : 20H (Write)
Default : 00H
BUFSEL[7:0] : to set buffer condition (unit = 2k word).
Scanner execute backward/forward moving whenever buffer full.
If MAXWD < buffer condition, then motor move forward to scan.

7.25. Reg : 21H (Write)
Defalut : 00H
STEPNO[7:0]: to set table one steps number for forward slope curve of the acceleration/deceleration.

7.26. Reg : 22H (Write)
Defalut : 00H
FWDSTEP[7:0] : to set steps number of the forward steps.

7.27. Reg : 23H (Write)
Defalut : 00H
BWDSTEP[7:0] : to set steps number of the backward steps.

7.28. Reg : 24H (Write)
Defalut : 00H
FASTNO[7:0]: to set table one steps number for backward slope curve of the acceleration/deceleration under scanning



7.29. Reg : 25H,26H,27 H (Write)

Defalut : 00H,00H,00H

LINCNT[17:0]: to set the scan lines number.

7.30. Reg : 28H,29H (Write)

Defalut : 01H,FFH

LAMPPWM[8:0] : to set PWM duty for lamp power control.

0: 1/512 duty.

1: 2/512 duty.

…..

511:512/512 duty.

7.31. Reg : 2AH,2BH (Write)

Default : 00H.00H

RAMA[14:0] : to set DRAM start address to access data.

note: IRAM_A[18:0]={RAMA[14:0],4'b0000}.

7.32. Reg : 2CH,2DH (Write)

Default : 00H,00H

DPISET[10:0] : set resolution of DPI for average type or deletion type.

A. average type : digital average function support 1/2,1/3,1/4,1/5,1/6,1/8,1/10,1/12,1/15

2400 dpi scanner : can set 1200,800,600,480,400,300,240,200,160 dpi.

1200 dpi scanner : can set 600,400,300,240,200,150,120,100 and 80 dpi.

600 dpi scanner : can set 300,200,150,120,100,75,60,50 and 40 dpi.

B. deletion type : 2400,1200 or 600dpi to 1 dpi setting decrement by one dpi.

7.33. Reg : 2EH (Write)

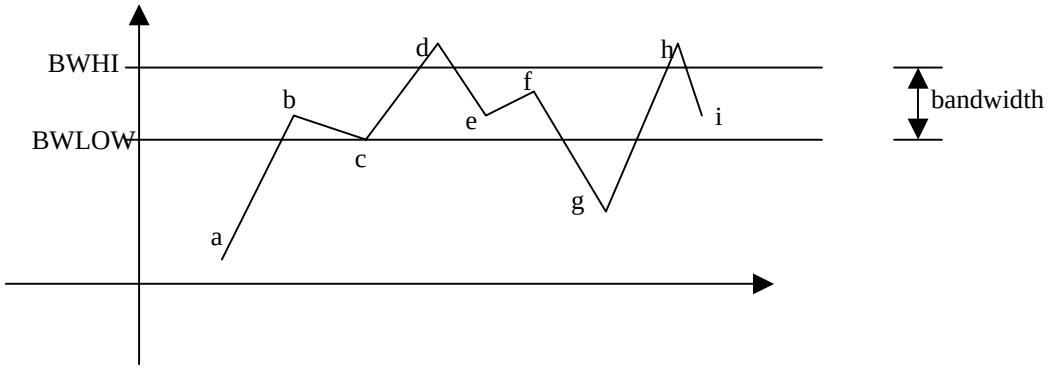
Default : 00H

BWHI[7:0] : to set Black & White threshold high level.

7.34. Reg : 2FH (Write)

Default : 00H

BWLOW[7:0] : to set Black & White threshold low level.



a,b,c,g : are black pixels
d,e,f,h,i : are white pixels

7.35. Reg : 30H,31H (Write)

Defalut : 00H,00H

STRPIXEL[15:0] : to set the begin pixel position (unit : pixel count).

STRPIXEL=(TGW+2*TGSHLD)+Begin pixels number.

7.36. Reg : 32H,33H (Write)

Defalut : 00H,00H

ENDPIXEL[15:0] : to set the end pixel position (unit : pixel count).

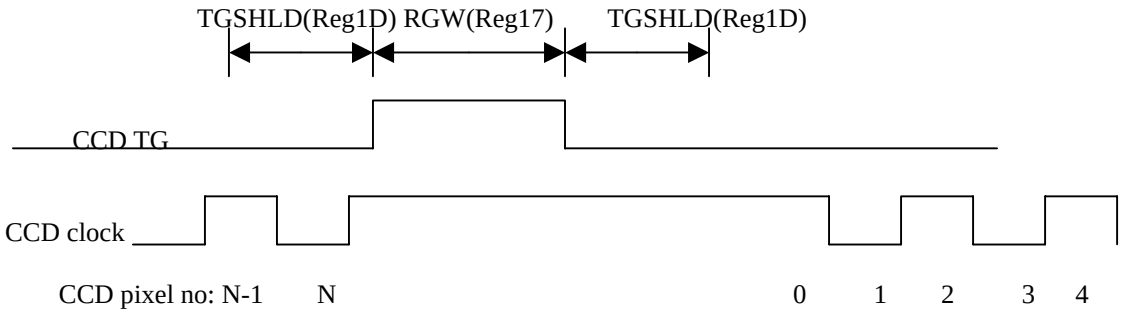
ENDPIXEL=(TGW+2*TGSHLD)+End pixels number.

7.37. Reg : 34H (Write)

Default : 00H

DUMMY[7:0] : to set the CCD dummy & optical black pixels position (unit : pixel count).

Note : Reg30,31,32,33 and 34 setting rule.



For example begin pixel is 65 ,end pixel is 100 and CCD dummy pixel is 64,

Then STRPIXEL=(TGW+2*TGSHLD)+65.

ENDPIXEL=(TGW+2*TGSHLD)+100.

DUMMY =(TGW+2*TGSHLD)+64.

7.38. Reg : 35H,36H,37H (Write)

Defalut : 00H,00H,00H

MAXWD[18:0] : to set maximum word size per line for ASIC estimation.

If usable buffer size < MAXWD, then buffer is full. The scanner execute forward and Backward moving.

7.39. Reg : 38H,39H (Write)

Defalut : 15H,18H

LPERIOD[15:0] : to set Line period(or exposure time) for CCD.

Unit : pixel count

7.40. Reg : 3AH,3BH (Write)
Defalut : 00H,00H
FEWRDATA[9:0] : This port is used to write data to control register of front-end.

7.41. Reg : 3CH (Write)
Defalut : 00H
RAMWRDATA[7:0] : This port is used to write data to DRAM.

7.42. Reg : 3DH,3EH,3FH (Write)
Defalut : 00H,00H,00H
FEEDL[17:0] : to set feeding steps number of motor move.

7.43. Reg : 41H (Read)
PWRBIT: To indicate power status.
BUFEMPTY : set: To indicate that the image buffer is empty.
: reset: To indicate that the image buffer is not empty.
FEEDFSH : set: To indicate that motor feeding is finished.
: reset: To indicate that motor feeding is not finished.
SCANFSH : : set: To indicate that scan is finished.
: reset: To indicate that scan is not finished.
HOMESNR : : set: home sensor is off (is home position).
: reset: home sensor is on (is not home position).
LAMPSTS : : set: lamp is on.
: reset: lamp is off.
FEBUSY : set: front end is busy and can not read/write again.
: reset: front end is ready and be able to read/write again.
MOTMFLG : set: motor is moving.
: reset: motor is stop.

7.44. Reg : 42H,43H,44H (Read)
VALIDWORD[18:0] : to indicate available words to read out in the image buffer of DRAM.

7.45. Reg : 45H (Read)
RAMRDDATA[7:0] : this port for read DRAM data.

7.46. Reg : 46H,47H (Read)
FERDDATA[9:0] : this port for read front end control register.

7.47. Reg : 48H,49H,4AH (Read)
FEDCNT[17:0] : to read motor feeding steps number.
For example, if you have set moving steps no. and execute moving command.
You can read out steps no. moved.

7.48. Reg : 4BH,4CH,4DH (Read)
SCANCNT[17:0] : to read scanner finished lines number.

7.49. Reg : 4EH,4FH (Read)
LPERIODRD[15:0] : to read back Reg38,Reg39 value.

7.50. Reg : 50H (Write)
Default : 00H
FERDA[5:0] : this port is read address setting for Front End control register read.

7.51. Reg : 51H (Write)
Default : 00H
FEWRA[5:0] : this port is write address setting for Front End control register write.

7.52. Reg : 52H,53H (Write)

Defalut : 00H,00H

RHI[4:0] : to latch R channel high byte data of AFE.

RLOW[4:0] : to latch R channel low byte data of AFE.

7.53. Reg : 54H,55H (Write)

Defalut : 00H,00H

GHI[4:0] : to latch G channel high byte data of AFE.

GLOW[4:0] : to latch G channel low byte data of AFE.

7.54. Reg : 56H,57H (Write)

Defalut : 00H,00H

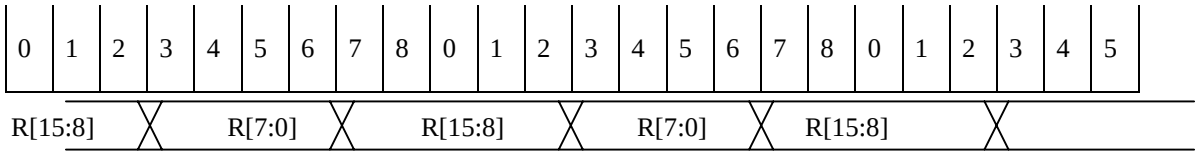
BHI[4:0] : to latch B channel high byte data of AFE.

BLOW[4:0] : to latch B channel low byte data of AFE.

(1). Color or fine gray : 24 clocks/pixel

RHI = 01H
RLOW = 05H
GHI = 09H
GLOW = 0DH
BHI = 11H
BLOW = 15H

(2).Fast gray or B&W : 9 clocks/pixel



RHI = 02H
RLOW = 06H

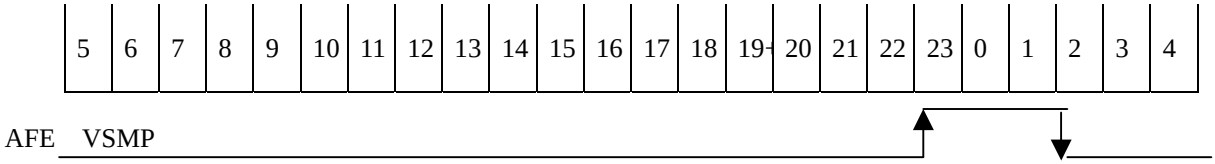
7.55. Reg : 58H (Write)

Defalut : 00H

B7~3:VSMP[4:0] : to set the rising edge position of image sampling for AFE.

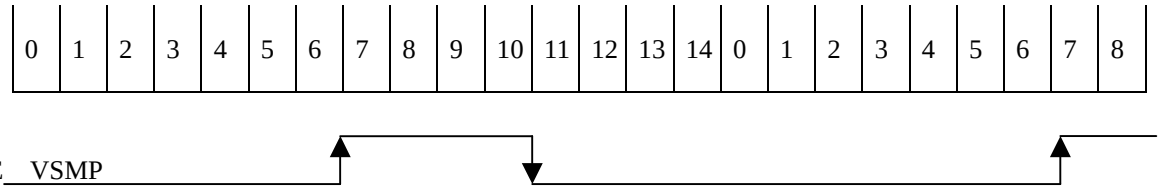
B2~0:VSMPW[2:0] : to set the pulse width of image sampling.

(1). Color or fine gray : 24 clocks/pixel



Reg58=B3H : VSMP[4:0]=16H VSMPW=3H

(2).Fast gray or B&W : 15 clocks/pixel



Reg58=34H : VSMP[4:0]=06H VSMPW=4H

7.56. Reg : 59H (Write)

Defalut : 00H

B7~3:BSMP[4:0] : to set the rising edge position of dark voltage sampling for AFE.

B2~0:BSMPW[2:0] : to set the pulse width of image sampling.

7.57. Reg : 5AH (Write)

Defalut : C0H

B7 :WMSEL : set: to select Wolfson working type.
: reset: to select Analog Device working type.

B6 : RLCSEL : set: select reset level clamp on a pixel-by-oixel basis.
: reset: don't select.

B5~4:CDSREF[1:0] : to set the frontend CDSREF for line rate scanning type.

B3~0:RLC[3:0] : to set the frontend RLC for line rate scanning type.

7.58. Reg : 5BH,5CH,5DH,5EH (Write)

Defalut : 00H,00H,00H,00H

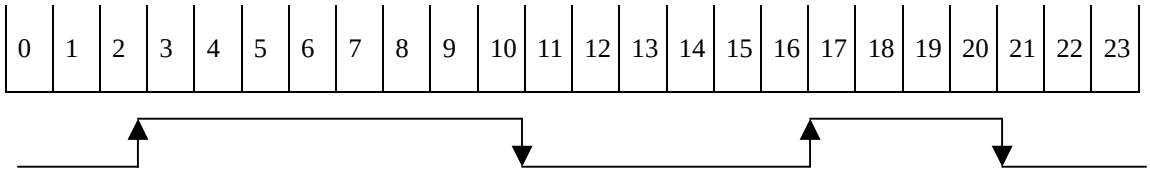
CKFH[4:0] : First point of rising edge.

CKFL[4:0] : First point of falling edge.

CKSH[4:0] : Second point of rising edge.

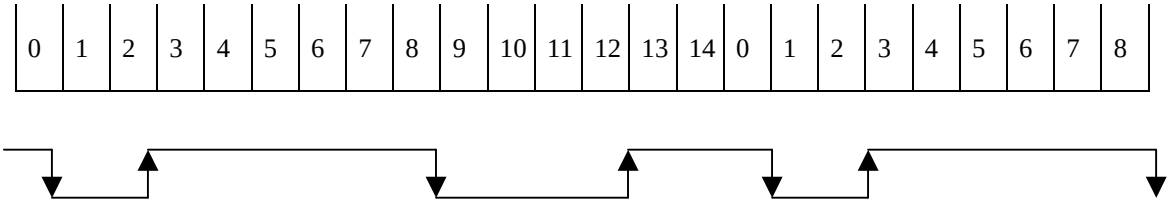
CKSL[4:0] : Second point of falling edge.

(1). Color or fine gray : 24 clocks/pixel



CKFH = 02H
CKFL = 0AH
CKSH = 10H
CKSL = 14H

(2).Fast gray or B&W : 15 clocks/pixel



CKFH = 02H
CKFL = 08H
CKSH = 0CH
CKSL = 00H

7.59. Reg : 60H,61H (Write)

Defalut : 00H,00H

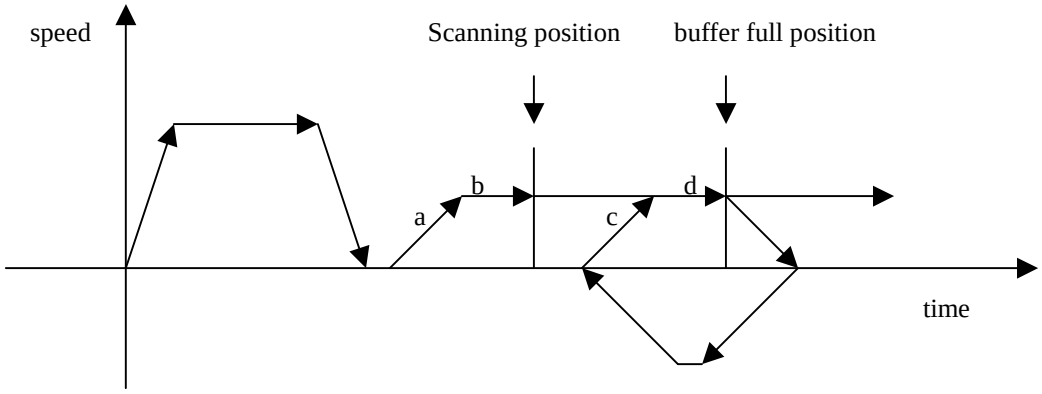
Z1MOD[15:0]: to set the slope curve of acceleration/deceleration table mode value
Under buffer full moving.

7.60. Reg : 62H,63H (Write)

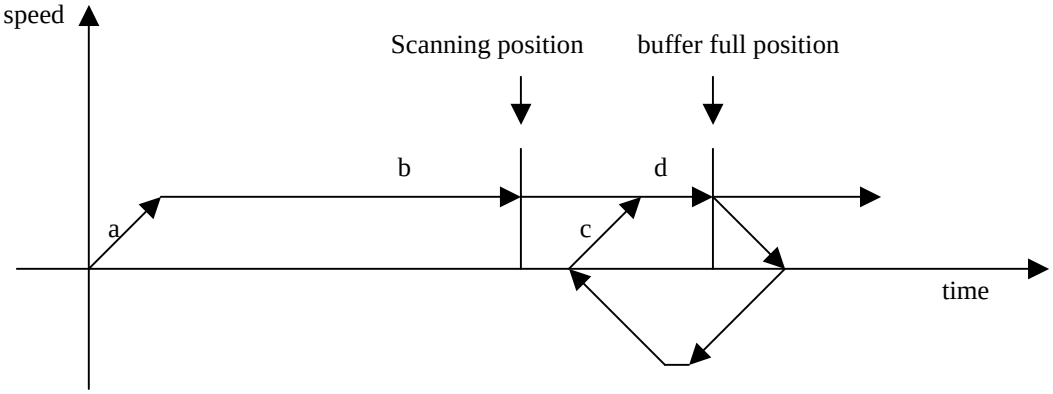
Defalut : 00H,00H

Z2MOD[15:0]: to set the slope curve of acceleration/deceleration mode value
Under first time moving to scanning .

(1). Two table moving :



(2). One table moving :



(a+b) mode LPERIOD = Z2MOD
(c+d) mode LPERIOD = Z1MOD

7.61. Reg : 64H (Write)

Defalut : 00H

PHFREQ[7:0]: to set PWM frequency for motor phase of uni-polar.
Frequency : (24MHz)/[(PHFREQ+1)*4

7.62. Reg :65H (Write)

Defalut : 3FH

MTRPWM[5:0]: to set PWM duty cycle for table one motor phase of uni-polar.

MTRPWM = 0 1/64 duty
= 1 2/64 duty
= 2 3/64 duty
……
= 63 64/64 duty

note: If PHFREQ < 0FH,then PWM setting must < (PHFREQ+1)*4

7.63. Reg :66H,67H (Write)

Defalut : 00H,00H
GPO[12:7] : GPO12~7 outputs ports
GPO[6:1] : GPO6~1 outputs ports

7.64. Reg :68H,69H (Write)

Defalut : 00H,00H
GPOE[12:7] : GPO12~7 ports output enable set.
GPOE[6:1] : GPO6~1 ports output enable set.
Set '1' : output.
Reset '0' : input.
GPOM12~11 : to select GPIO12~11 as Bi-polar motor driver V-ref input voltage in order to control drive current.

7.65. Reg :6AH (Write)

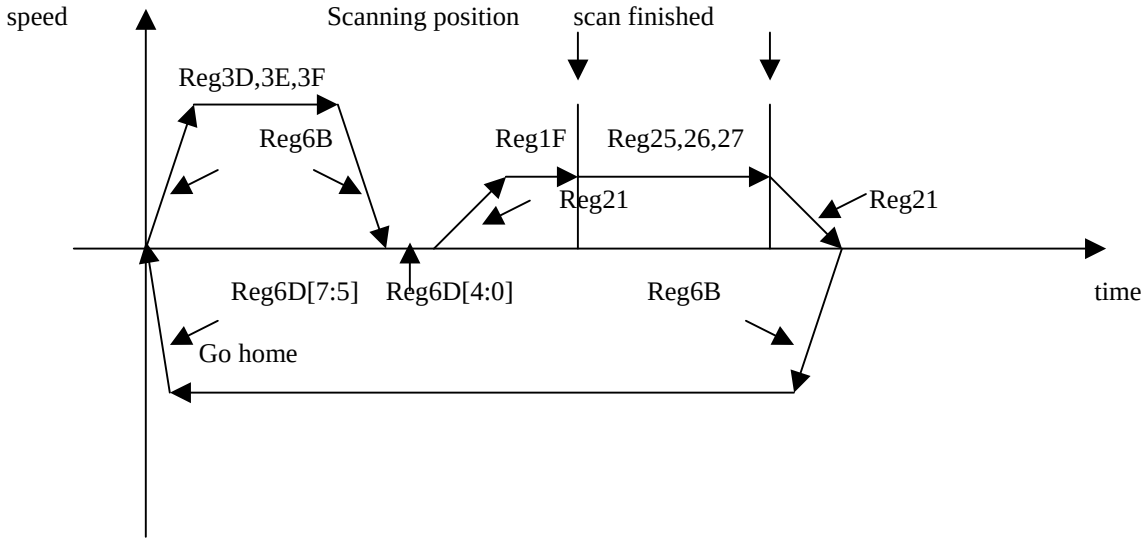
Defalut : 00H
FSTPSEL[1:0] : for table two fast moving step type selection.
(1).bi-polar :
a.00: full step.
b.01: half step.
c.10: quarter step.
d.11: reserved.
(2).uni-polar :
a.00: two-phase-on full step.
b.01: half step.
c.10: reserved.
d.11: single-phase-on full step.

FASTPWM[5:0] : to set PWM duty cycle for table two motor phase of uni-polar.
FASTPWM =0 1/64 duty
=1 2/64 duty
=2 3/64 duty
……
=63 64/64 duty
note: If PHFREQ < 0FH,then PWM setting must < (PHFREQ+1)*4

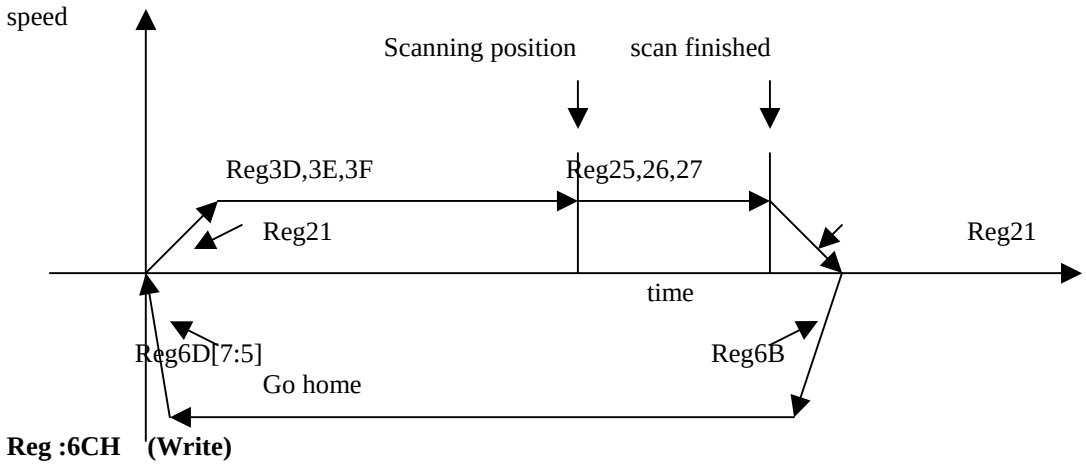
7.66. Reg :6BH (Write)

Defalut : 00H
FMOVNO[7:0]: Set fast moving slop steps(table two slope).

(1). Two table moving :



(2). One table moving :



7.67. Reg :6CH (Write)

Defalut : 00H

B7~6:TGTIME[1:0] : Set period times for LINPRDWR,EXPR,EXPG & EXPB
- 00:one time period.
- 01:two times period.
- 10:four times period.
- 11:eight times period.

B5~3:Z1MOD[18:16] : Set Z1MOD bit 16,17 & 18.

B2~0:Z2MOD[18:16] : Set Z2MOD bit 16,17 & 18.

7.68. Reg :6DH (Write)

Defalut : 60H

B7~5:DECSEL[2:0] :select deceleration steps whenever go home.
- 000:1 steps deceleration
- 001:2 steps deceleration
- 010:4 steps deceleration
- 011:8 steps deceleration
- 100:16 steps deceleration
- 101:32 steps deceleration
- 110:64 steps deceleration

111:128 steps deceleration
B4~0:STOPTIM[4:0]:select acceleration/deceleration stop time.
The unit is LPERIOD.

7.69. Reg :70H (Write)
GPI[12:7] : GPIO12~7 input ports.

7.70. Reg :71H (Write)
GPI[6:1] :GPIO6~1 input status.

7.71. Shading mapping(Chunky)

Attribute	Resolution	A[18:0]
Shading Mapping	600dpi (RGB Chunky)	00000H~07FFFH SIZE : 32k
	1200dpi (RGB Chunky)	00000H~0FFFFH SIZE : 64k
	2400dpi (RGB Chunky)	00000H~1F7FFH SIZE : 126k

7.72. Shading mapping(Planer)

Attribute	Resolution		A[18:0]
Shading Mapping	600dpi (RGB Planer)	R LINE	00000H~029FFH
		G LINE	02A00H~053FFH
		B LINE	05400H~07DFFH
	1200dpi (RGB Planer)	R LINE	00000H~054FFH
		G LINE	05500H~0A9FFH
		B LINE	0AA00H~0FEFFH
	2400dpi (RGB Planer)	R LINE	00000H~0A7FFH
		G LINE	0A800H~14FFFH
		B LINE	15000H~1F7FFH

7.73. Gamma mapping

Attribute		Color	A[18:0]
		RED	09000H~09FFFH SIZE : 4K

600DPI	12 BITS GAMMA	GREEN	0A000H~0AFFFH SIZE : 4K
		BLUE	0B000H~0BFFFH SIZE : 4K
	14 BITS GAMMA	RED	09000H~0CFFFH SIZE : 16K
		GREEN	0D000H~10FFFH SIZE : 16K
		BLUE	11000H~14FFFH SIZE : 16K
1200DPI	12 BITS GAMMA	RED	11000H~11FFFH SIZE : 4K
		GREEN	12000H~12FFFH SIZE : 4K
		BLUE	13000H~13FFFH SIZE : 4K
	14 BITS GAMMA	RED	11000H~14FFFH SIZE : 16K
		GREEN	15000H~18FFFH SIZE : 16K
		BLUE	19000H~1CFFFH SIZE : 16K
2400DPI	12 BITS GAMMA	RED	20000H~20FFFH SIZE : 4K
		GREEN	21000H~21FFFH SIZE : 4K
		BLUE	22000H~22FFFH SIZE : 4K
	14 BITS GAMMA	RED	20000H~23FFFH SIZE : 16K
		GREEN	24000H~27FFFH SIZE : 16K
		BLUE	28000H~2BFFFH SIZE : 16K

7.74. Image Buffer Mapping :

DRAM	**Resolution**	A[18:0]

4M BITS X 1	600DPI	12 BITS GAMMA	0C000H~3FFFFH
		14 BITS GAMMA	15000H~3FFFFH
	1200DPI	12 BITS GAMMA	14000H~3FFFFH
		14 BITS GAMMA	1D000H~3FFFFH
	2400DPI	12 BITS GAMMA	23000H~3FFFFH
		14 BITS GAMMA	2C000H~3FFFFH
4M BITS X 2	600DPI	12 BITS GAMMA	0C000H~7FFFFH
		14 BITS GAMMA	15000H~7FFFFH
	1200DPI	12 BITS GAMMA	14000H~7FFFFH
		14 BITS GAMMA	1D000H~7FFFFH
	2400DPI	12 BITS GAMMA	23000H~7FFFFH
		14 BITS GAMMA	2C000H~7FFFFH

7.75. Slope Curve Table Mapping :

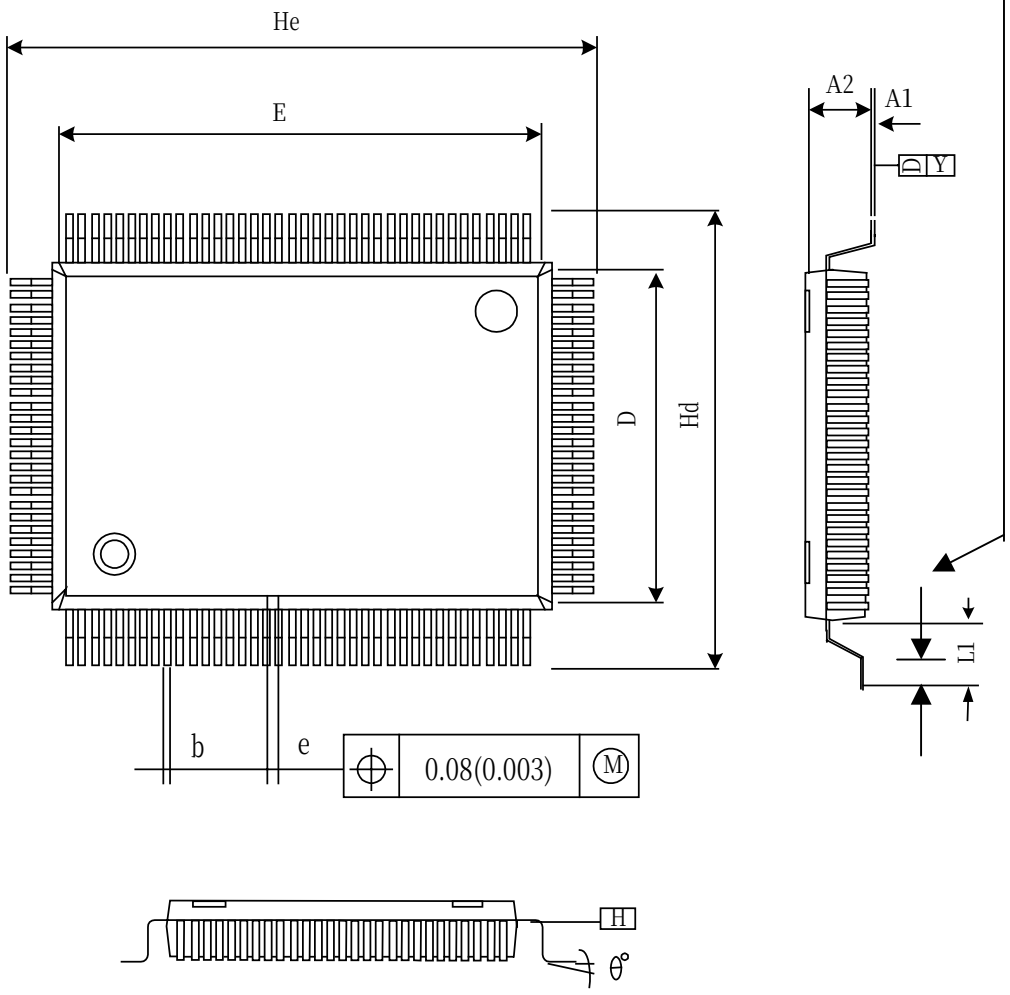
Attribute	Resolution	A[18:0]
Slope Curve Table	600DPI table I (DPIHW=00)	08000 ~ 080FF (for scan)
	600DPI table II (DPIHW=00)	08100 ~ 081FF (for fast feed)
	1200DPI table I (DPIHW=01)	10000 ~ 100FF (for scan)
	1200DPI table II (DPIDW=01)	10100 ~ 101FF (for fast feed)
	2400DPI table I (DPIHW=10)	1F800 ~ 1F8FF (for scan)

	2400DPI table II (DPIDW=10)	1F900 ~ 1F9FF (for fast feed)

7.76. Package

QFP-128L (14*20 mm, F/P: 3.2 mm):

SYMBOLS	MIN(mm)	NOM(mm)	MAX(mm)
A1	0.25	0.35	0.45
A2	2.57	2.72	2.87
b	0.10	0.20	0.30
C	0.10	0.15	0.20
D	13.90	14.00	14.10
E	19.90	20.00	20.10
e	-	0.50	-
Hd	17.00	17.20	17.40
He	23.00	23.20	23.40
L	0.65	0.80	0.95
L1	-	1.60	-
Y	-	-	0.08
Θ	0	-	12



8. Revision History

Rev	Date	Description
1.4	20020813	• Package description updated (p.42) • Revision History item added (p.43)