AN-EVAL-3AR4780VJZ

12W 5V SMPS evaluation board with ICE3AR4780VJZ

Application Note

About this document

Scope and purpose

This document is a 12W 5.0V, universal input off-line flyback converter evaluation board using Infineon CoolSET™ F3R80 family, ICE3AR4780VJZ.

Intended audience

This document is intended for users of the ICE3AR4780VJZ who wish to design low cost and high reliable system of off-line SMPS for enclosed adapter or open frame auxiliary power supply of white goods, PC, server, DVD, TV, Set-top box, etc.

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1 Abstract

This document is an engineering report of a universal input 12W 5V off-line flyback converter power supply utilizing F3R80 CoolSET™ ICE3AR4780VJZ. The application evaluation board is operated in Discontinuous Conduction Mode (DCM) and is running at 100 kHz switching frequency. It has a single output voltage with secondary side control regulation. It is especially suitable for small power supply such as DVD player, set-top box, game console, charger and auxiliary power of white goods, server, PC and high power system, etc. The ICE3AR4780VJZ is the latest version of the CoolSET™. Besides having the basic features of the F3R CoolSET™ such as Active Burst Mode, propagation delay compensation, soft gate drive, auto restart protection for major fault (Vcc over voltage, Vcc under voltage, adjustable input OVP, over temperature, over-load, open loop and short opto-coupler), it also has the BiCMOS technology design, selectable entry and exit burst mode level, adjustable AC line input over voltage protection feature, built-in soft start time, built-in and extendable blanking time and frequency jitter feature, etc. The particular features are the best-in-class low standby power and the good EMI performance.

2 Evaluation board

This document contains the list of features, the power supply specification, schematic, bill of material and the transformer construction documentation. Typical operating characteristics such as performance curve and scope waveforms are showed at the rear of the report.

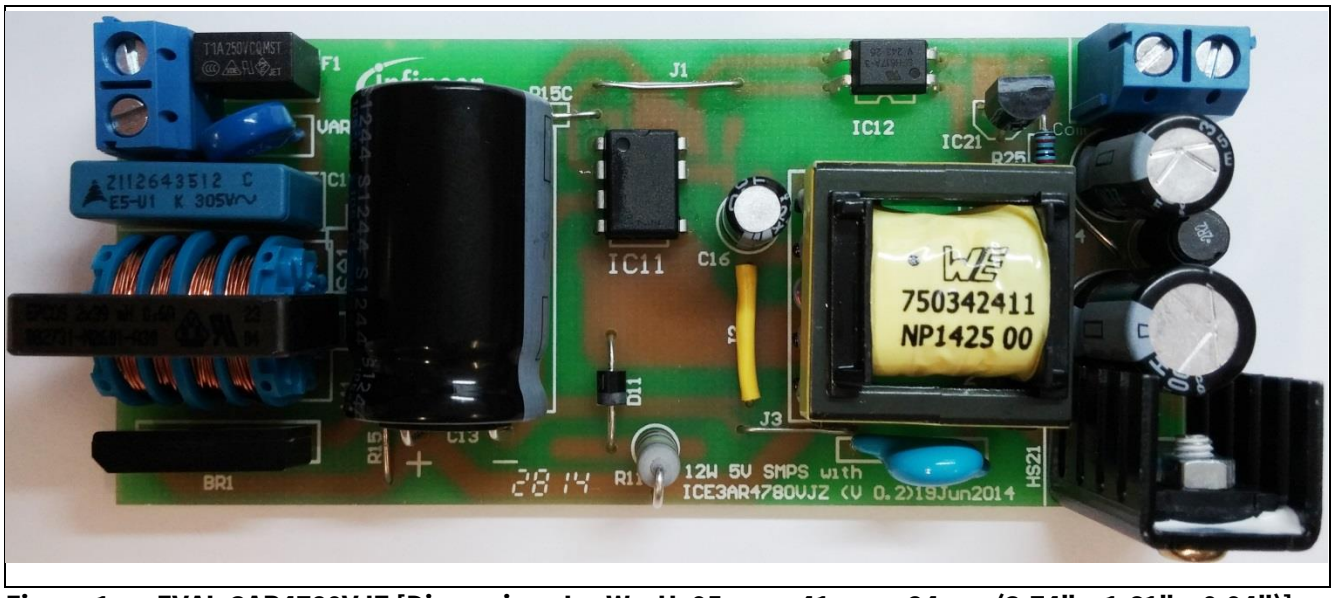


Figure 1 EVAL-3AR4780VJZ [Dimensions L x W x H: 95mm x 41mm x 24mm (3.74" x 1.61" x 0.94")]

3 Evaluation board specifications

Input voltage	85VAC~265VAC
Input frequency	50~60Hz
Output voltage	5V
Output current	2.4A
Output power	12W
Steady state output ripple voltage (±1% of norminal output voltage)	$V_{ripple_P_P}$< 50mV
Dynamic load response undershoot & overshoot (±3% of norminal output voltage)	$V_{ripple_P_P}$< 250mV
Active mode four point average efficiency (25%,50%,75% & 100%load) (EU CoC Version 5, Tier 1) Active mode at 10% load efficiency (EU CoC Version 5, Tier 1)	>80% at 115Vac and >79% at 230Vac >73%
No-load power consumption (EU CoC Version 5, Tier 2)	< 75mW
Maximum input power(Peak Power) for universal input range (<±5% of average maximum input power)	<±3% of average maximum input power
Form factor case size (L x W x H)	95mm x 41mm x 24mm (3.74" x 1.61" x 0.94")

4 List of features (ICE3AR4780VJZ)

800V avalanche rugged CoolSET™ with Startup Cell
Active Burst Mode for lowest Standby Power
Selectable entry and exit burst mode level
100kHz internally fixed switching frequency with jittering feature
Auto Restart Protection for Over load, Open Loop, VCC Under voltage & Over voltage and Over temperature
Over temperature protection with 50°C hysteresis
Built-in 10ms Soft Start
Built-in 20ms and extendable blanking time for short duration peak power
Propagation delay compensation for both maximum load and burst mode
Adjustable input OVP
Overall tolerance of Current Limiting < ±5%
BiCMOS technology for low power consumption and wide VCC voltage range
Soft gate drive with 50Ω turn on resistor

5 Circuit description

5.1 Introduction

The EVAL-3AR4780VJZ evaluation board is a low cost off-line flyback switch mode power supply (SMPS) using the ICE3AR4780VJZ integrated power IC from the CoolSET™-F3R80 family. The circuit shown in Figure 3, details a 5V, 12W power supply that operates from an AC line input voltage range of 85Vac to 265Vac and line input OVP detect/reset voltage is 300/282Vac, suitable for applications in enclosed adapter or open frame auxiliary power supply for different system such as white goods, PC, server, DVD, LED TV, Set-top box, etc.

5.2 Line input

The AC line input side comprises the input fuse F1 as over-current protection. The choke L11, X-capacitors C11, C14 and Y-capacitor C12 act as EMI suppressors. Optional spark gap device SG1, SG2 and varistor VAR can absorb high voltage stress during lightning surge test. After the bridge rectifier BR1 and the input bulk capacitor C13, a voltage of 90 to 424 V_{DC} is present which depends on input line voltage.

5.3 Line input over voltage protection

The AC line input OVP mode is detected by sensing the voltage level at BV pin through the resistors divider from the bulk capacitor. Once the voltage level at BV pin hits above 1.98V, the controller stops switching and enters into input OVP mode. When the BV voltage drops to 1.91V and the Vcc hits 17V, the input OVP mode is released.

5.4 Start up

Since there is a built-in startup cell in the ICE3AR4780VJZ, no external start up resistor is required. The startup cell is connecting the drain pin of the IC. Once the voltage is built up at the Drain pin of the ICE3AR4780VJZ, the startup cell will charge up the Vcc capacitor C16 and C17. When the Vcc voltage exceeds the UVLO at 17V, the IC starts up. Then the Vcc voltage is bootstrapped by the auxiliary winding to sustain the operation.

5.5 Operation mode

During operation, the Vcc pin is supplied via a separate transformer winding with associated rectification D12 and buffering C16, C17. In order not to exceed the maximum voltage at Vcc pin due to poor coupling of transformer winding, an external zener diode ZD11 and resistor R13 can be added.

5.6 Soft start

The Soft-Start is a built-in function and is set at 10ms.

5.7 RCD clamper circuit

While turns off the CoolMOS™, the clamper circuit R11, C15 and D11 absorbs the current caused by transformer leakage inductance once the voltage exceeds clamp capacitor voltage. Finally drain to source voltage of CoolMOS™ is lower than maximum break down voltage ($V_{(BR)DSS}$ = 800V) of CoolMOS™.

5.8 Peak current control of primary current

The CoolMOS™ drain source current is sensed via external shunt resistors R14 and R14A which determine the tolerance of the current limit control. Since ICE3AR4780VJZ is a current mode controller, it would have a cycle-by-cycle primary current and feedback voltage control which can make sure the maximum power of the converter is controlled in every switching cycle. Besides, the patented propagation delay compensation is implemented to ensure the maximum input power can be controlled in an even tighter manner. The evaluation board shows approximately ±2.2% of average maximum input power (refer to Figure 11).

5.9 Output stage

On the secondary side the power is coupled out by a schottky diode D21. The capacitor C22 & C23 provides energy buffering following with the LC filter L21 and C24 to reduce the output voltage ripple considerably. Storage capacitors C22 & C23 are selected to have a very small internal resistance (ESR) to minimize the output voltage ripple.

6 Circuit diagram

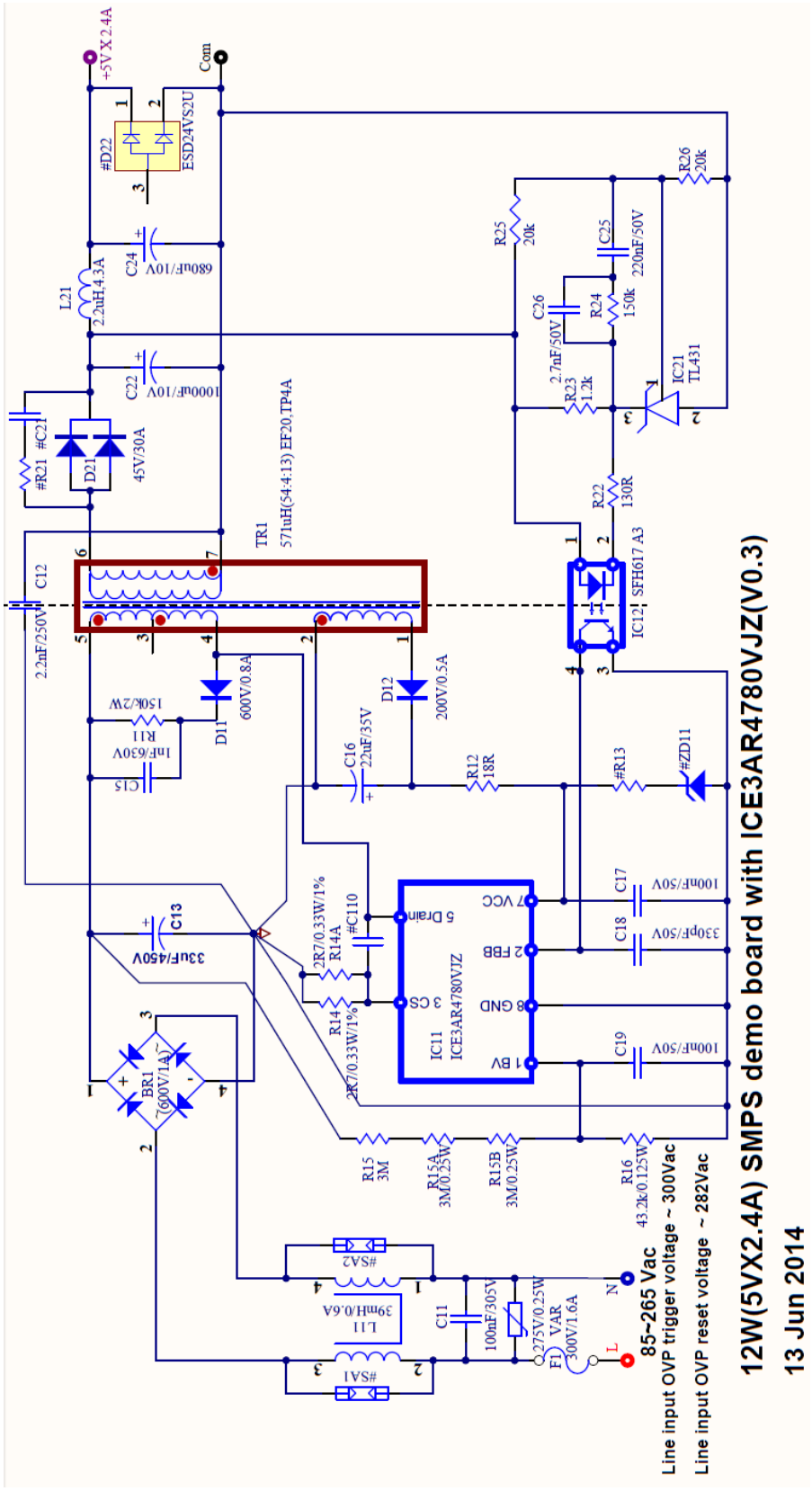


Figure 2 Schematic of EVAL-3AR4780VJZ

PCB layout

N.B. : In order to get the optimized performance of the CoolSET™, the grounding of the PCB layout must be connected very carefully. From the circuit diagram above, it indicates that the grounding for the CoolSET™ can be split into several groups; signal ground, Vcc ground, Current sense resistor ground and EMI return ground. All the split grounds should be connected to the bulk capacitor ground separately.

Signal ground includes all small signal grounds connecting to the CoolSET™ GND pin such as filter capacitor ground, C17, C18, C19 and opto-coupler ground.

Vcc ground includes the Vcc capacitor ground, C16 and the auxiliary winding ground, pin 2 of the power transformer.

Current Sense resistor ground includes current sense resistor R14 and R14A.

EMI return ground includes Y capacitor, C12.

7 PCB layout

7.1 Top side

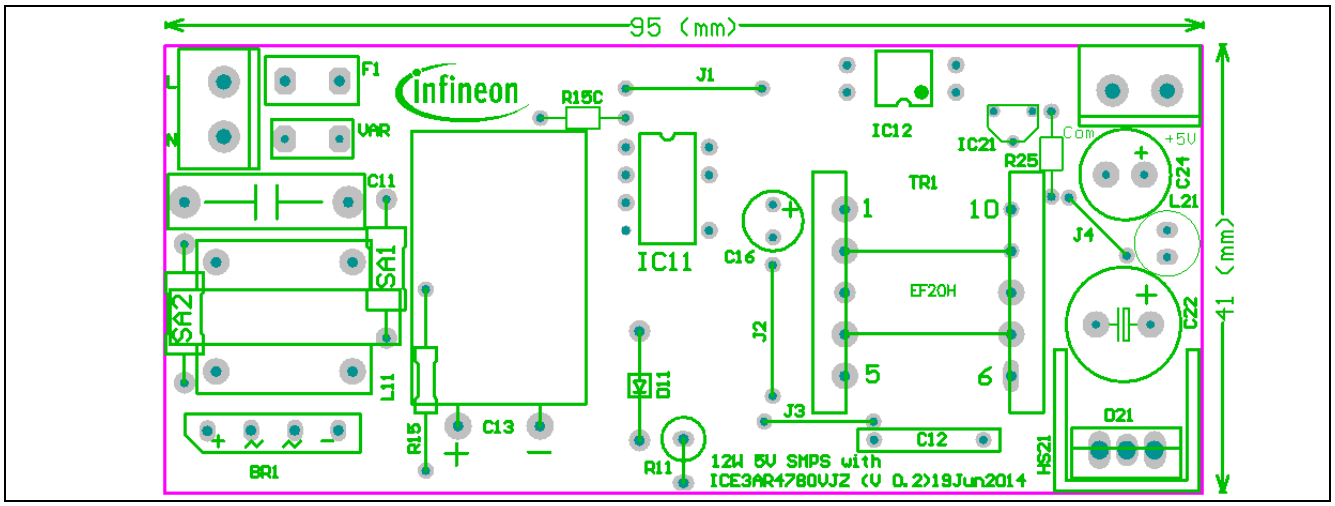


Figure 3 Top side component legend

7.2 Bottom side

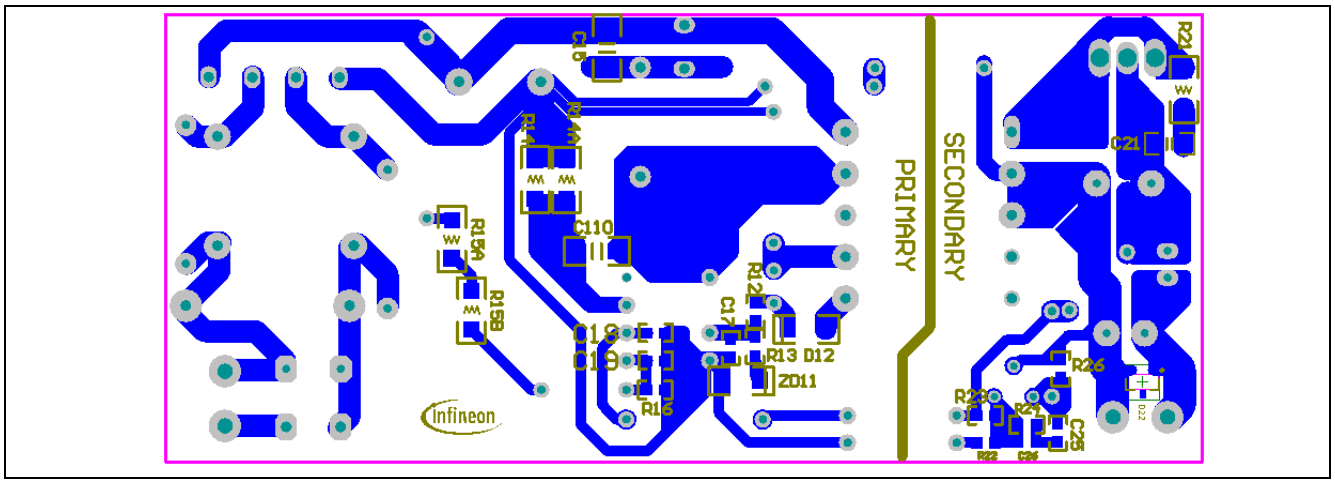


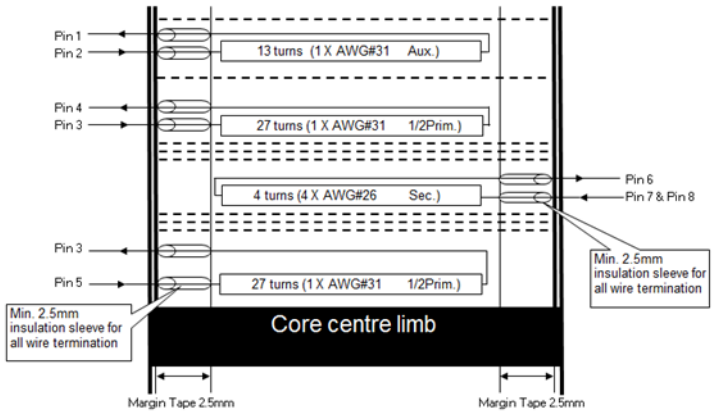
Figure 4 Bottom side copper and component legend

8 Component list

No.	Designator	Component Description	Footprint	Part Number	Manufacturer	Quantity
1	+5V Com, L N	12V Test Point	Connector	691102710002	Wurth Electronics	2
2	BR1	600V/1A	1V	S1VBA60	SHINDENGEN	1
3	C11	100nF/305V	MKT5/18/15	B329221C3104K	EPCOS	1
4	C12	2.2nF/250V	MKT2/13/10	DE1E3KX222MA4BN01F	MURATA	1
5	C13	33uF/450V	RB16X25	450BXC33MEFC16X25	RUBYCON	1
6	C15	1nF/630V	1206	GRM31A7U2J102JW31D	MURATA	1
7	C16	22uF/50V	RB5.5	50PX22MEFC5X11	RUBYCON	1
8	C17,C19	100nF/50V	0603	GRM188R71H104KA93D	MURATA	2
9	C18	330pF/50V	0603	GRM1885C1H331GA01D	MURATA	1
10	C22	1000uF/10V	RB10	10ZLH1000MEFC10X12.5	RUBYCON	1
11	C24	680uF/10V	RB8	10ZLH680MEFC8X11.5	RUBYCON	1
12	C25	220nF/50V	0603	GRM188R71H224KAC4D	MURATA	1
13	C26	2.7nF/50V	0603	GRM188R71H272KA01D	MURATA	1
14	D11	600V/0.8A	DIODE0.4	D1NK60	SHINDENGEN	1
15	D12	200V/0.5A	1206D	GL34D		1
16	D21	45V/30A	TO-220FPAB	STPS30L45CFP		1
17	F1	300V/1.6A	MKT4.3/8.4/5	36911600000		1
18	HS1	TO220 heat sink	HS TO220	577202B00000G		1
19	IC11	ICE3AR4780VJZ	DIP7	ICE3AR4780VJZ	INFINEON	1
20	IC12	SFH617 A3	DIP4			1
21	IC21	TL431	TO92-TL431-			1
22	J1,J2,J3,J4,R15C	Jumper	Axial 0.4			5
23	L11	39mH/0.6A	EMI_C_U21	B82731M2601A030	EPCOS	1
24	L21	2.2µH/4.3A	CH6 2.5	7447462022	Wurth Electronics	1
25	R11	150k/2W	AXIAL0.4_V 4mm			1
26	R12	18R	0603			1
27	R14,R14A	2R7/0.33W/1%	1206	ERJ8BQF2R7V		2
28	R15	3M/1%	AXIAL0.4_15			1
29	R15A,R15B	3M/1%	1206			2
30	R16	43.2k/1%	0603			1
31	R22	130R	0603			1
32	R23	1.2k	0603			1
33	R24	150k	0603			1
34	R25	20k	AXIAL0.3			1
35	R26	20k	0603			1
36	TR1	571µH(54:4:13)	TR_EF20_H	750342411	Wurth Electronics Midcom	1
37	VAR	275V/0.25W	MKT3.5/7.5/5	B72207S2271K101	EPCOS	1

9 Transformer construction

Core and material: EE20/10/6(EF20), TP4A (TDG)
Bobbin: 070-4989(10-Pins, TH-H, Horizontal version)
Primary Inductance, Lp=571µH (±10%), measured between pin 4 and pin 5
Manufacturer and part number: Wurth Electronics Midcom (750342411)



Start	Stop	No. of turns	Wire size	Layer
5	3	27	1XAWG#31	1/2 Primary
7,8	6	4	4XAWG#26	Secondary
3	4	27	1XAWG#31	1/2 Primary
2	1	13	1XAWG#31	Auxiliary

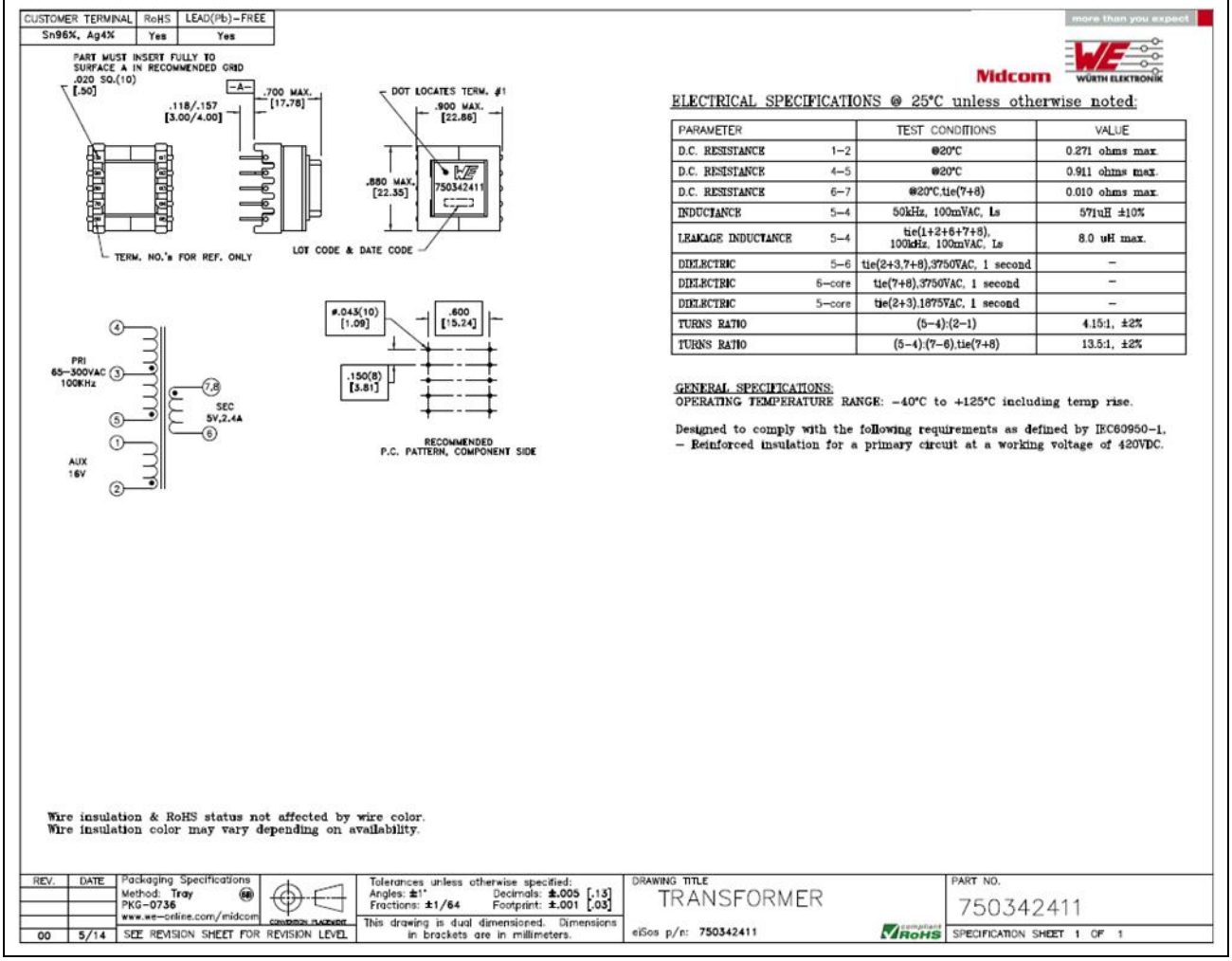


Figure 5 Transformer structure

10 Test results

Vin(Vac)	Pin(W)	Vo(Vdc)	Io(A)	$V_{Out_ripple_pk_pk}$ (mV)	Po(W)	η (%)	Average η (%)	OLP P_{in} (W)	OLP I_{out} (A)
85	0.0288	5.23	0.00	14.10			79.82	17.85	2.72
	1.6200	5.21	0.24	25.70	1.25	77.19			
	3.8500	5.19	0.600	10.70	3.11	80.88			
	7.6200	5.15	1.200	13.80	6.18	81.10			
	11.5600	5.11	1.800	15.50	9.20	79.57			
	15.6200	5.06	2.400	18.40	12.14	77.75			
115	0.0306	5.23	0.00	14.40			80.87	17.54	2.75
	1.6300	5.21	0.24	26.50	1.25	76.71			
	3.8300	5.19	0.600	10.70	3.11	81.31			
	7.5700	5.15	1.200	13.40	6.18	81.64			
	11.3700	5.11	1.800	15.60	9.20	80.90			
	15.2500	5.06	2.400	17.10	12.14	79.63			
230	0.0425	5.23	0.00	15.40			79.95	17.92	2.85
	1.6800	5.21	0.24	24.40	1.25	74.43			
	4.0000	5.19	0.600	10.60	3.11	77.85			
	7.6800	5.15	1.200	13.70	6.18	80.47			
	11.3700	5.11	1.800	16.10	9.20	80.90			
	15.0700	5.06	2.400	17.20	12.14	80.58			
265	0.0494	5.23	0.00	15.10			79.15	18.33	2.89
	1.7100	5.21	0.24	24.90	1.25	73.12			
	4.1000	5.19	0.600	10.00	3.11	75.95			
	7.7500	5.15	1.200	13.20	6.18	79.74			
	11.4300	5.11	1.800	16.00	9.20	80.47			
	15.1000	5.06	2.400	17.30	12.14	80.42			

10.1 Efficiency

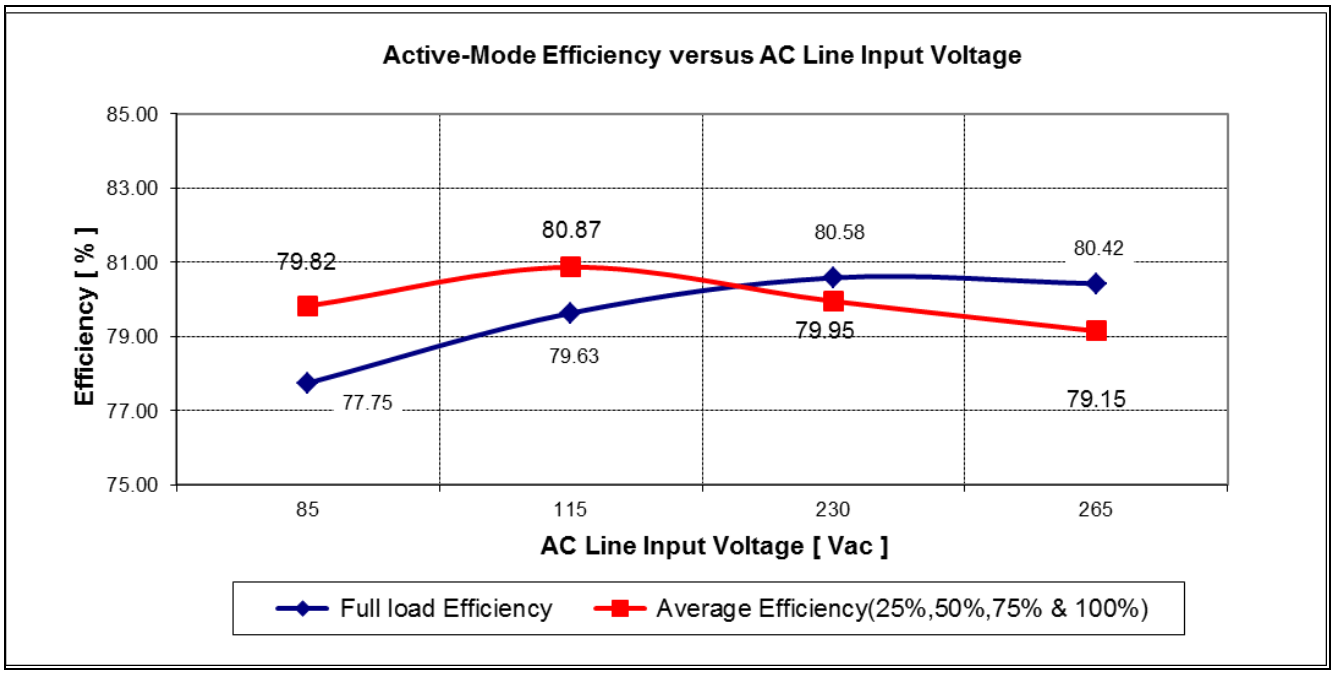


Figure 6 Efficiency vs AC line input voltage

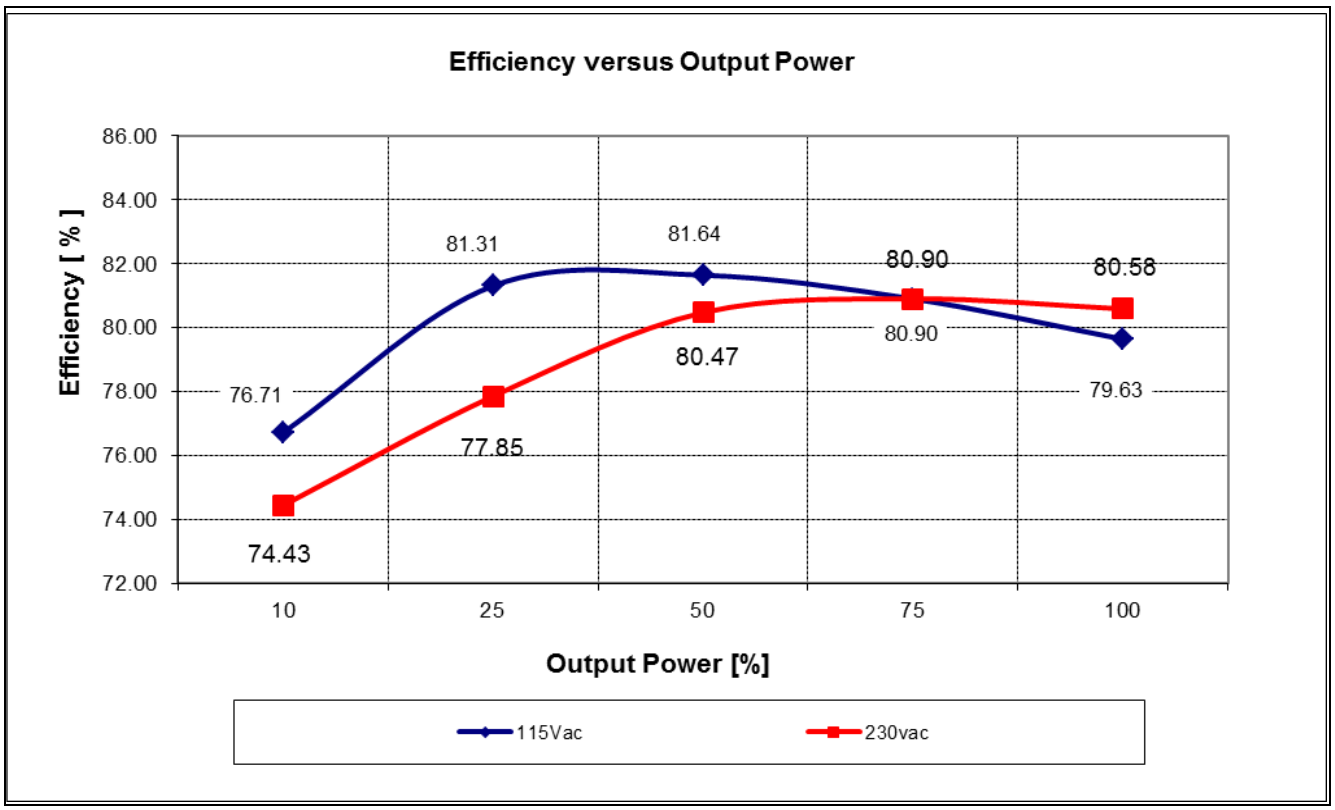


Figure 7 Efficiency vs output power @ 115Vac and 230V line

10.2 Standby power

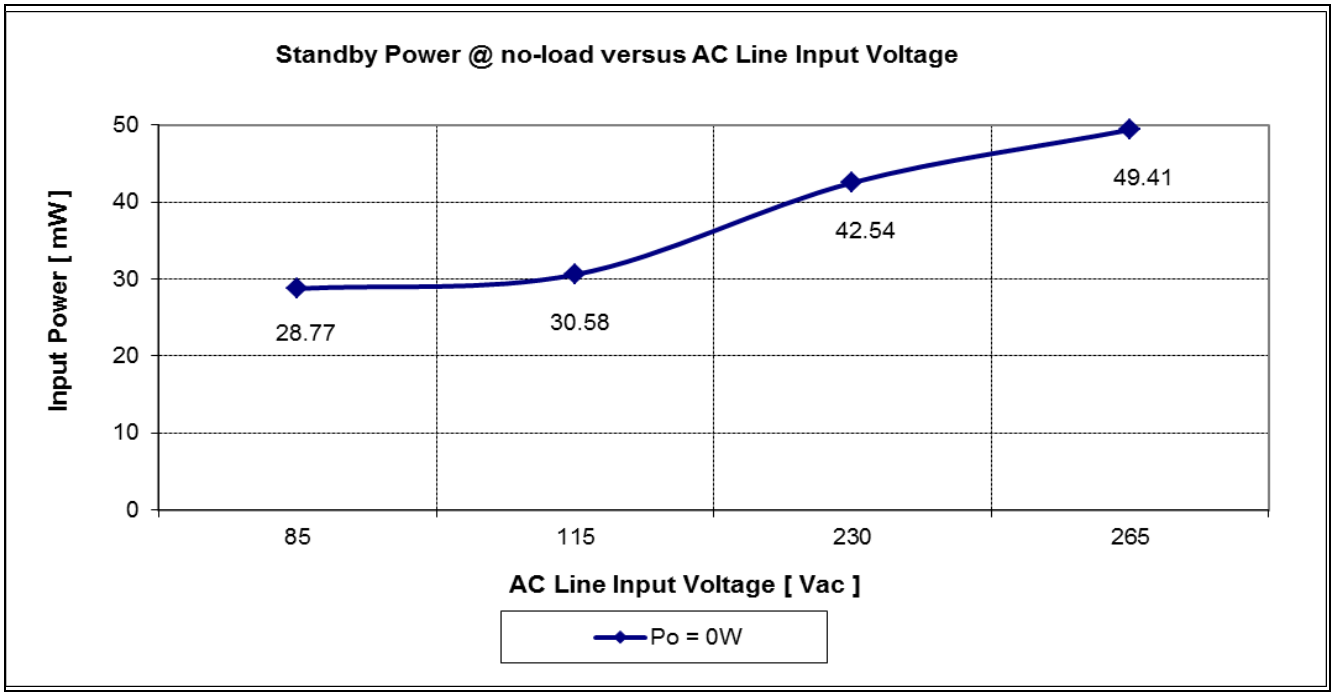


Figure 8 Standby power @ no load vs AC line input voltage (measured by Yokogawa WT210 power meter - integration mode)

10.3 Line regulation

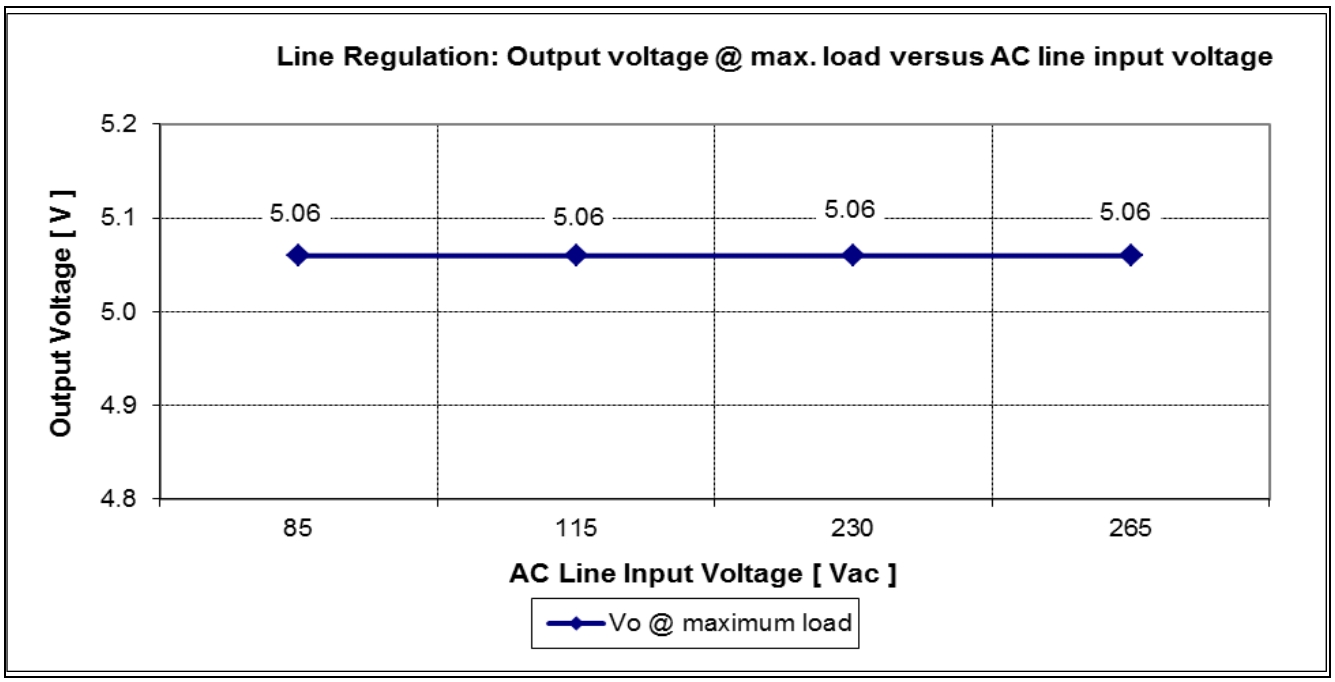


Figure 9 Line regulation Vo @ full load vs AC line input voltage

10.4 Load regulation

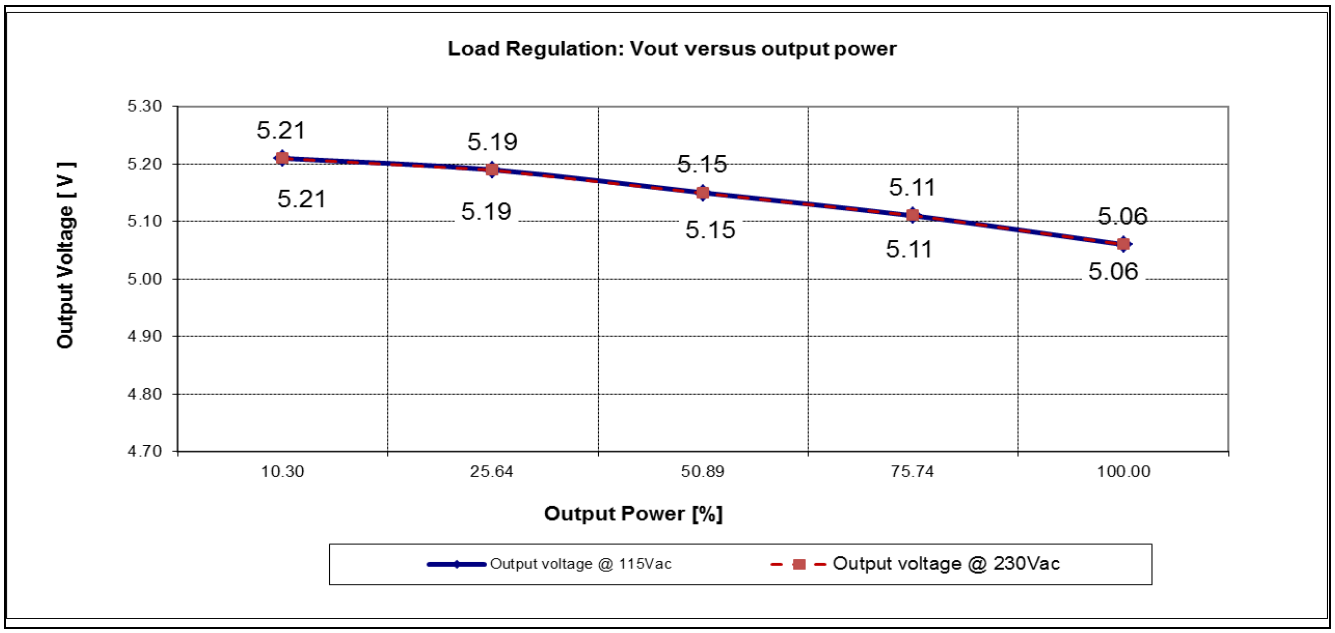


Figure 10 Load regulation Vo vs output power

10.5 Maximum power

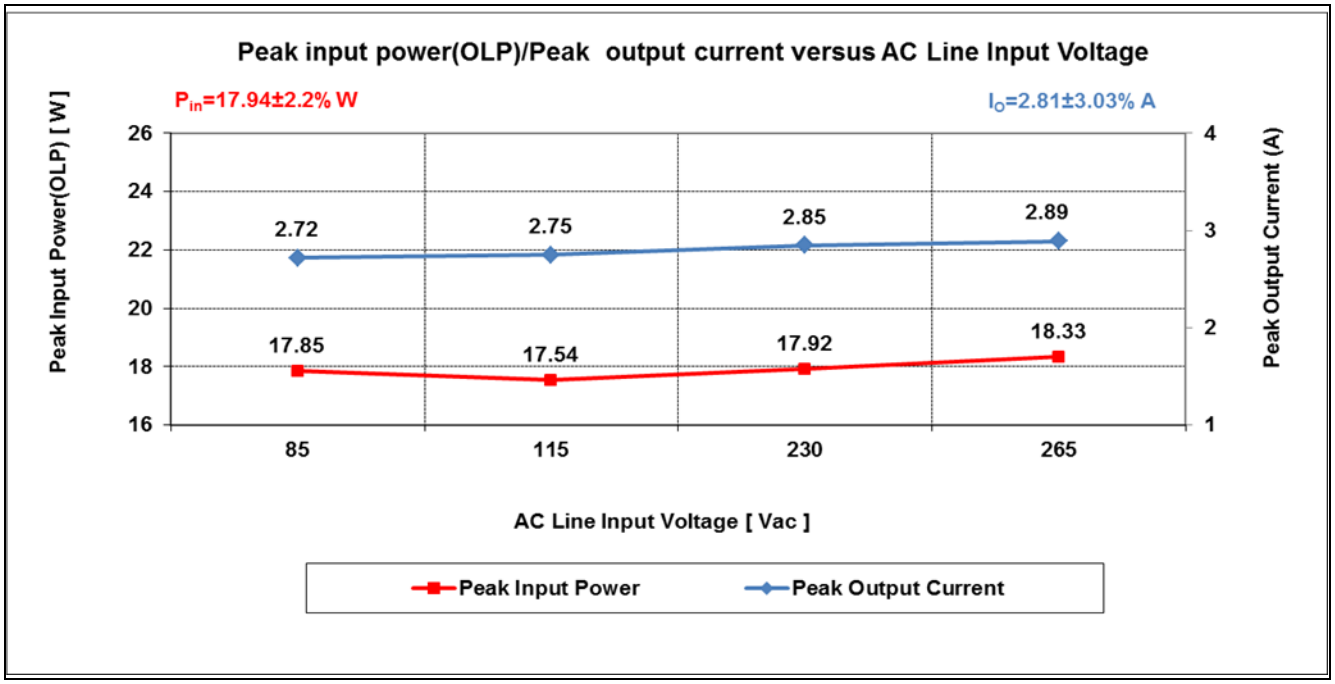


Figure 11 Maximum input power (before over-load protection) vs AC line input voltage

10.6 ESD immunity (EN61000-4-2)

Pass [special level (±18kV) for contact discharge].

10.7 Surge immunity (EN61000-4-5)

Pass [Installation class 3, 2kV (line to earth) and 1kV (line to line)].

10.8 Conducted emissions (EN55022 class B)

The conducted EMI was measured by Schaffner (SMR25503) and followed the test standard of EN55022 (CISPR 22) class B. The evaluation board was set up at maximum load (12W) with input voltage of 115Vac and 230Vac.

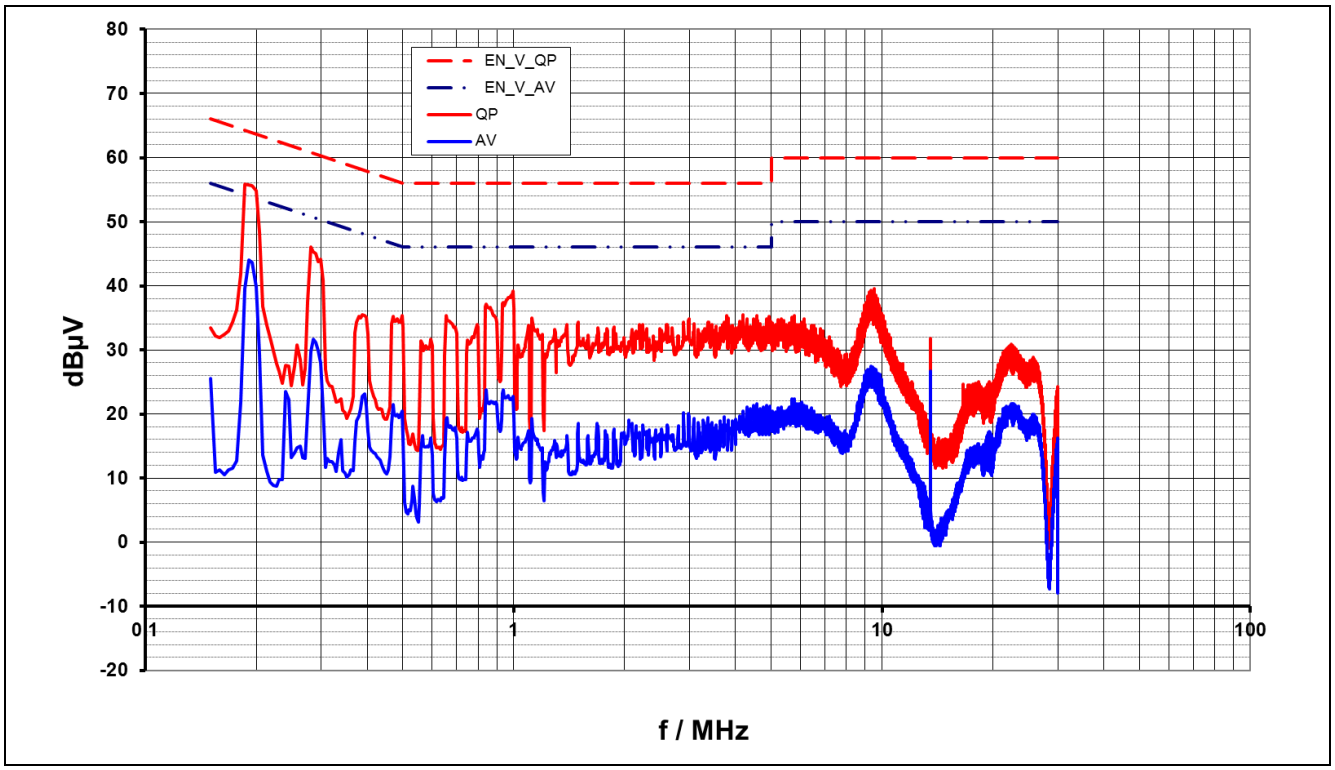


Figure 12 Conducted emissions(Line) at 115Vac and maximum Load

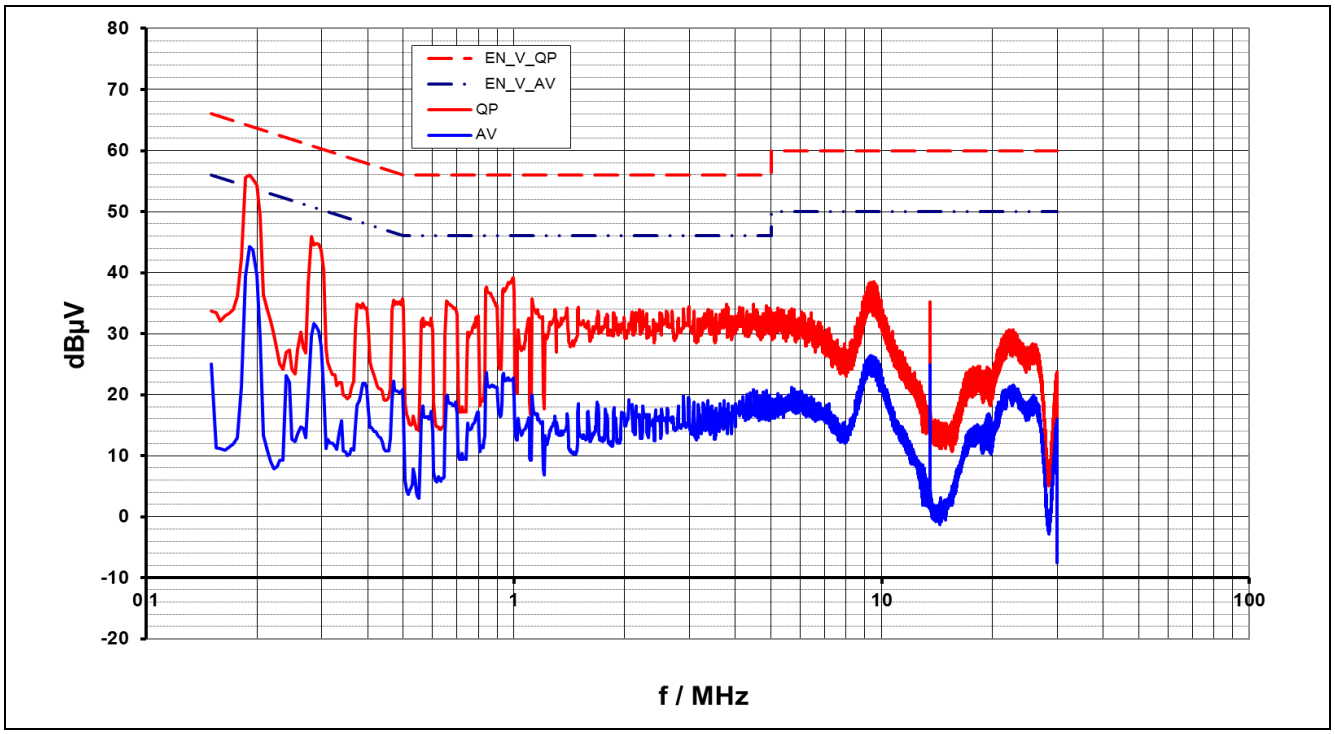


Figure 13 Conducted emissions(Neutral) at 115Vac and maximum Load

Test results

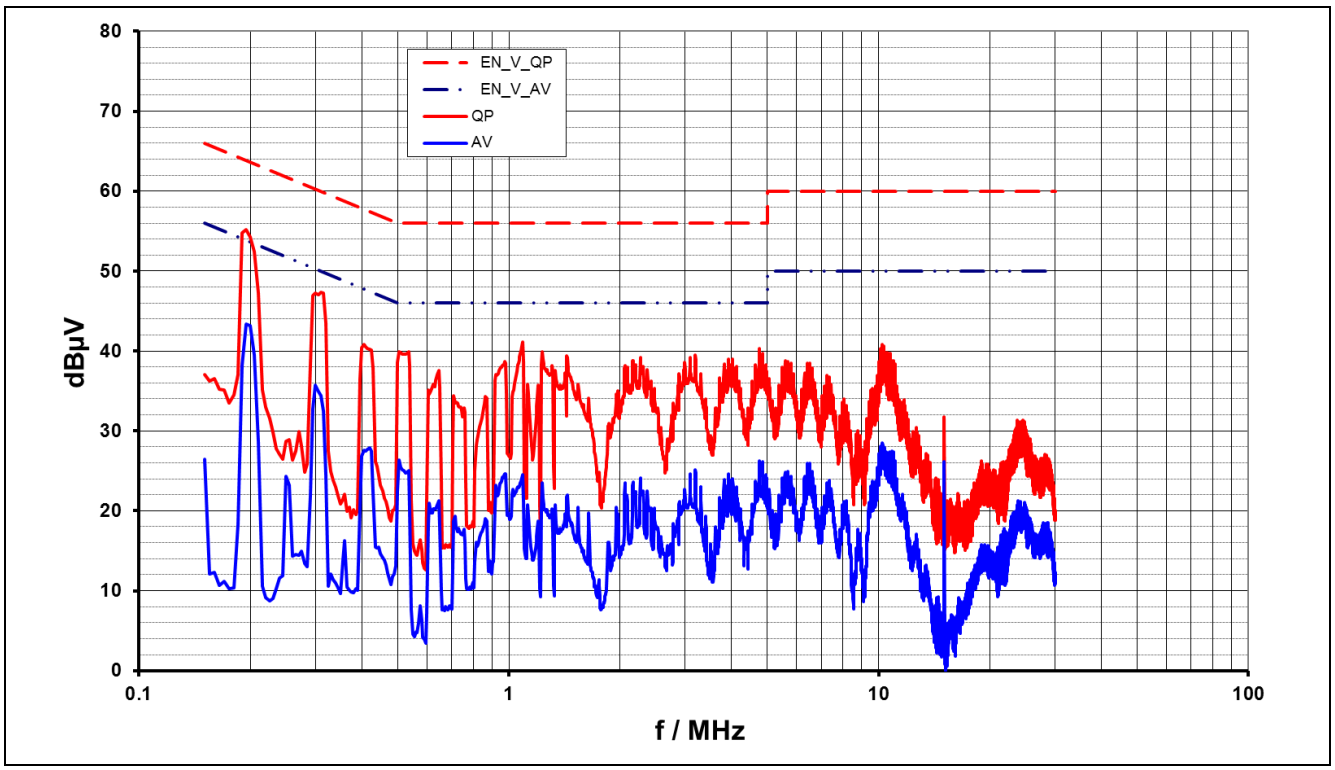


Figure 14 Conducted emissions(line) at 230Vac and maximum Load

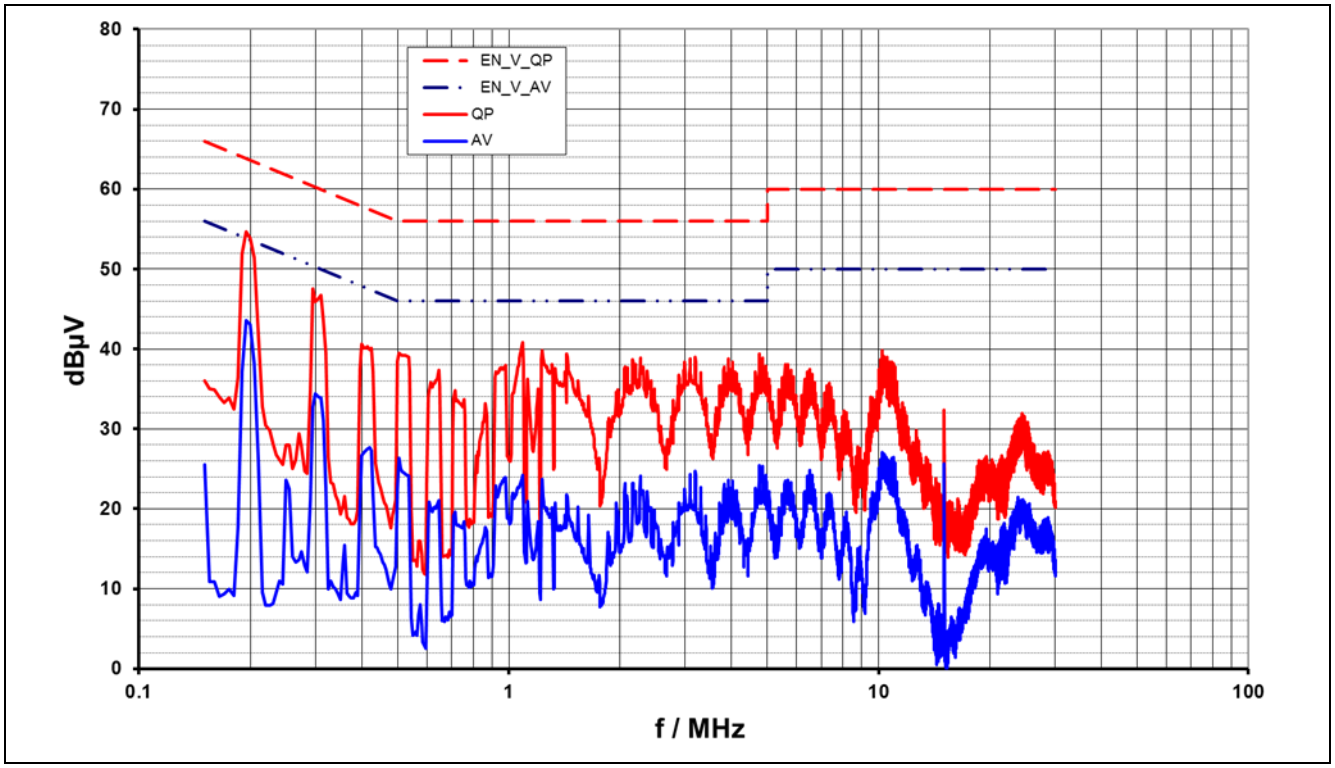


Figure 15 Conducted emissions(Neutral) at 230Vac and maximum Load

Pass conducted EMI EN55022 (CISPR 22) class B with > 7dB margin for QP.

10.9 Thermal measurement

The thermal test of open frame evaluation board was done using an infrared thermography camera (TVS-500EX) at ambient temperature 25°C. The measurements were taken after two hours running at full load (12W).

No.	Major component	85Vac (°C)	115Vac (°C)	230Vac (°C)	265Vac (°C)
1	IC11 (ICE3AR4780VJZ)	57.5	50.7	49.9	50.7
2	BR1	46.9	40.2	33.6	33.1
3	L11	44.0	39.1	32.3	31.6
4	TR1	51.5	51.4	53.3	53.9
5	D21	54.2	54	54.5	54.9

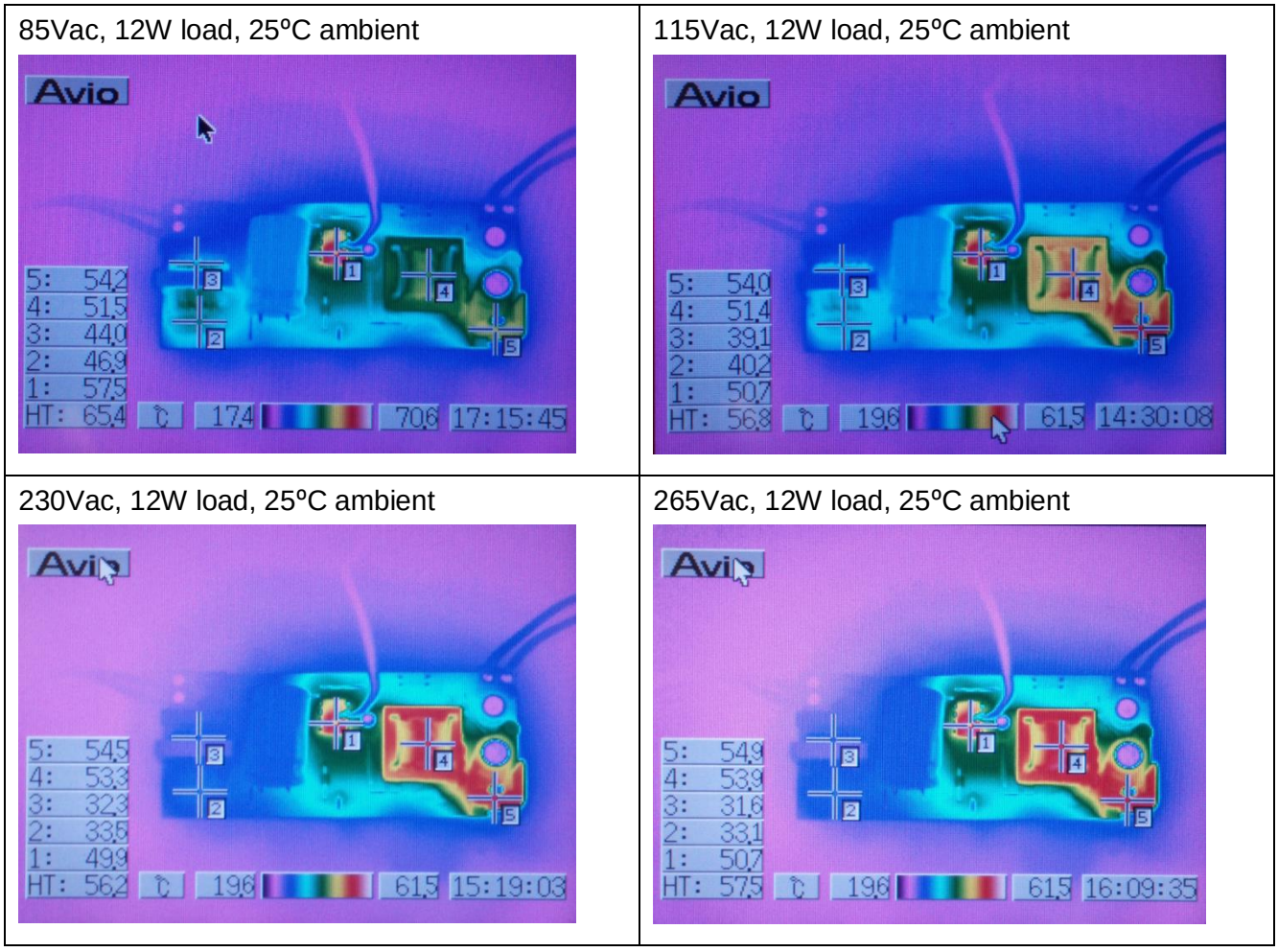
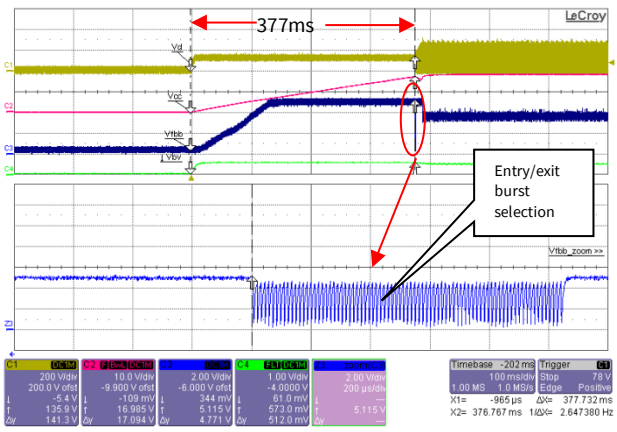


Figure 16 Infrared thermal image of EVAL-ICE3AR4780VJZ

11 Waveforms and scope plots

All waveforms and scope plots were recorded with a LeCroy 6050 oscilloscope

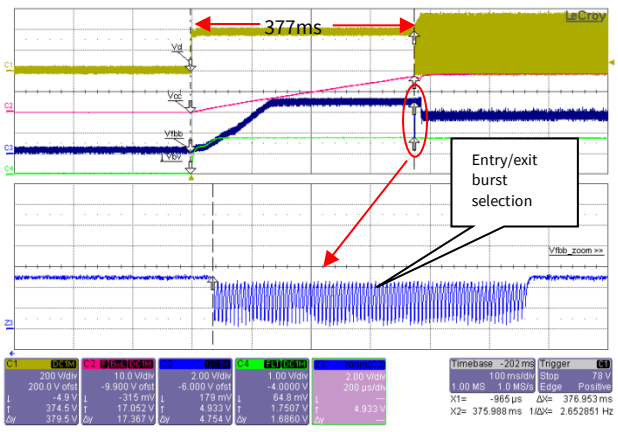
11.1 Start up at low/high AC line input voltage with maximum load



Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FBB})
Channel 4; C4 : BV voltage (V_{BV})

Startup time = 377ms

Figure 17 Startup @ 85Vac & max. load

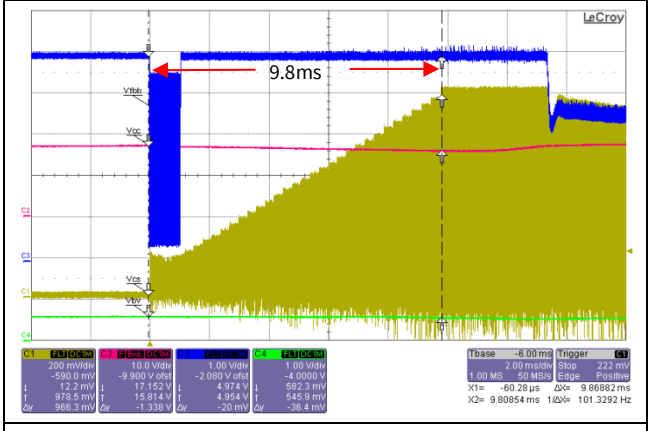


Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FBB})
Channel 4; C4 : BV voltage (V_{BV})

Startup time = 377ms

Figure 18 Startup @ 265Vac & max. load

11.2 Soft start

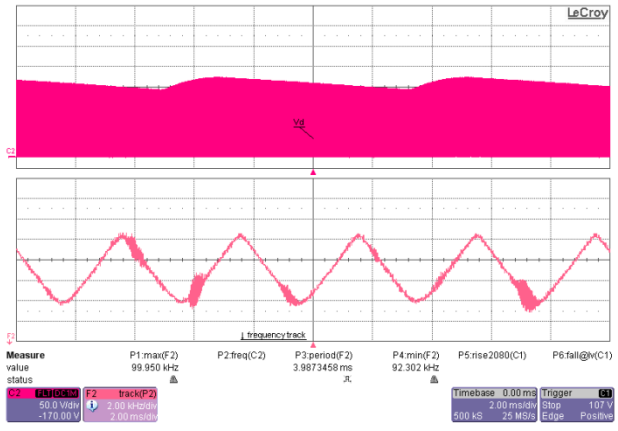


Channel 1; C1 : Current sense voltage (V_{CS})
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FBB})
Channel 4; C4 : BV voltage (V_{BV})

Soft Star time = 9.8ms

Figure 19 Soft start @ 85Vac & max. load

11.3 Frequency jittering



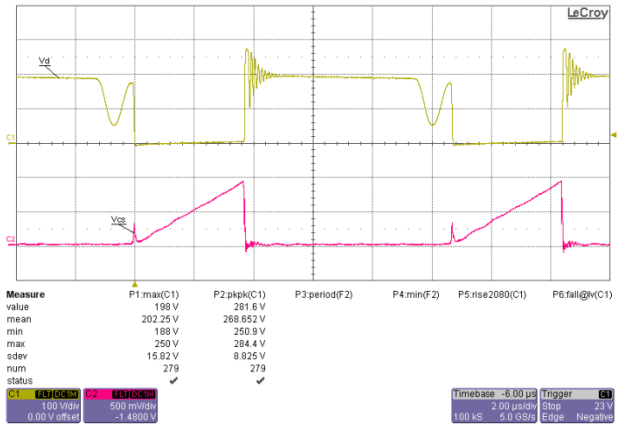
Channel 2; C2 : Drain voltage (V_{Drain})

Channel F2 : Frequency track of C2

Frequency jittering from 92 kHz ~ 100 kHz, Jitter period is set at 4ms internally

Figure 20 Frequency jittering@ 85Vac and max. load

11.4 Drain voltage and current at maximum load

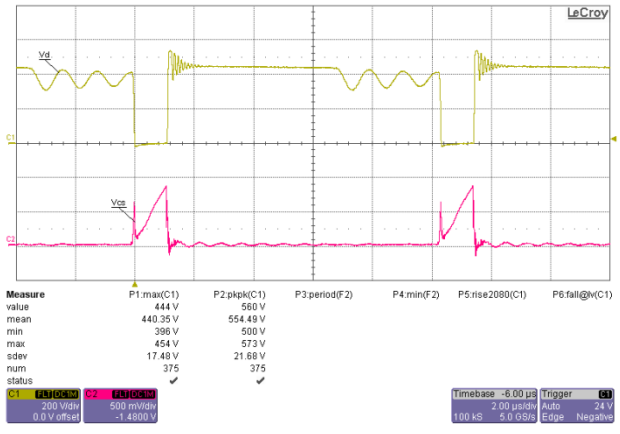


Channel 1; C1 : Drain voltage (V_{Drain})

Channel 2; C2 : Current sense voltage (V_{CS})

V_{Drain_peak} = 284V

Figure 21 Operation @ 85Vac and max. load



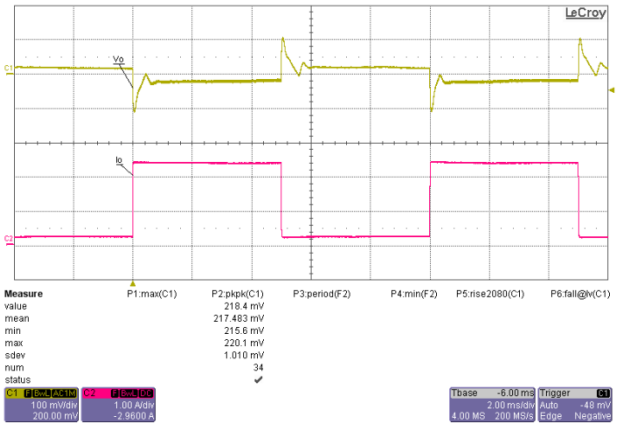
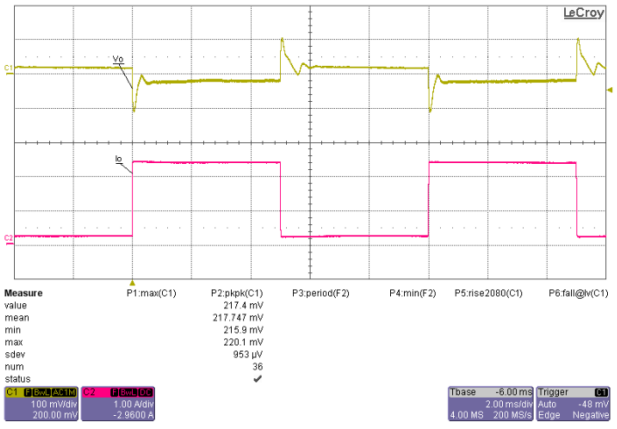
Channel 1; C1 : Drain voltage (V_{Drain})

Channel 2; C2 : Current sense voltage (V_{CS})

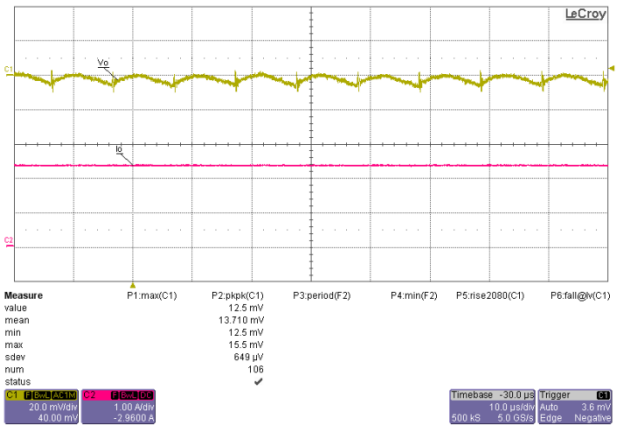
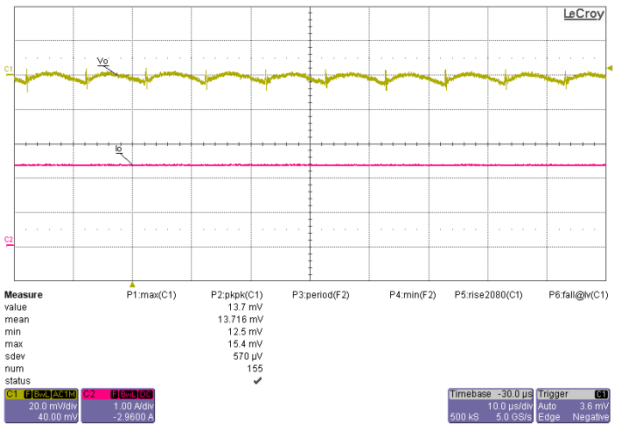
V_{Drain_peak} = 573V

Figure 22 Operation @ 265Vac and max. load

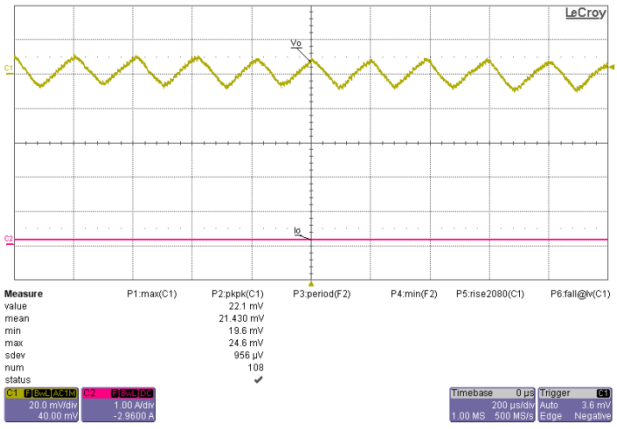
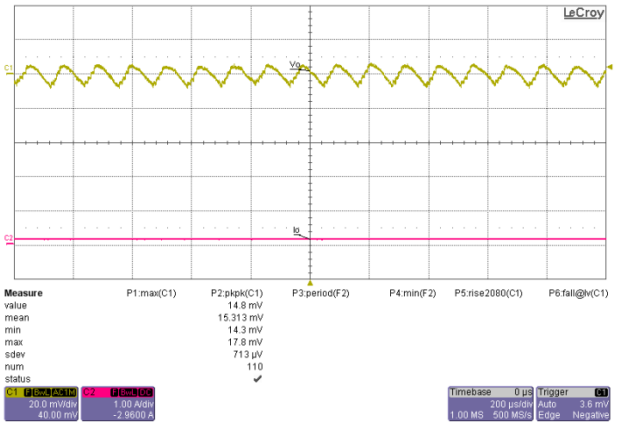
11.5 Load transient response (Dynamic load from 10% to 100%)

	
Channel 1; C1 : Output ripple voltage (Vo) Channel 2; C2 : Output current (Io)	Channel 1; C1 : Output ripple voltage (Vo) Channel 2; C2 : Output current (Io)
$V_{ripple_pk_pk}$=220mV (Load change from10% to 100%,100Hz,0.4A/µS slew rate) Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter	$V_{ripple_pk_pk}$=220mV (Load change from10% to 100%,100Hz,0.4A/µS slew rate) Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter
Figure 23 – Load transient response @ 85Vac	**Figure 24 Load transient response @ 265Vac**

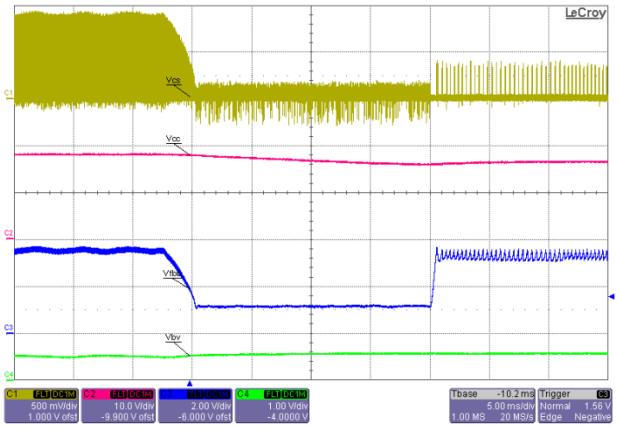
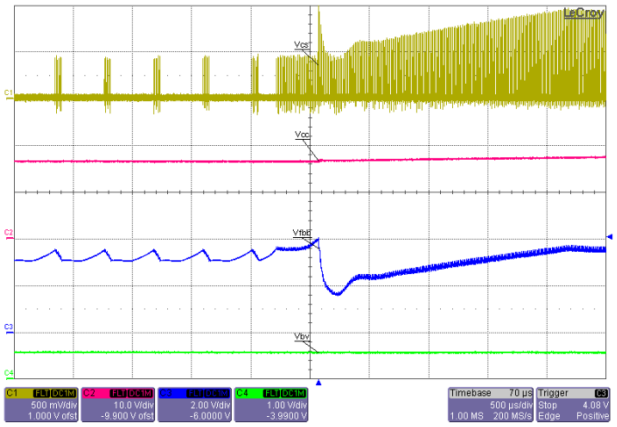
11.6 Output ripple voltage at maximum load

	
Channel 1; C1 : Output ripple voltage (Vo) Channel 2; C2 : Output current (Io)	Channel 1; C1 : Output ripple voltage (Vo) Channel 2; C2 : Output current (Io)
$V_{ripple_pk_pk}$=16mV Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter	$V_{ripple_pk_pk}$ = 16mV Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter
Figure 25 AC output ripple @ 85Vac and max. load	**Figure 26 AC output ripple @ 265Vac and max. load**

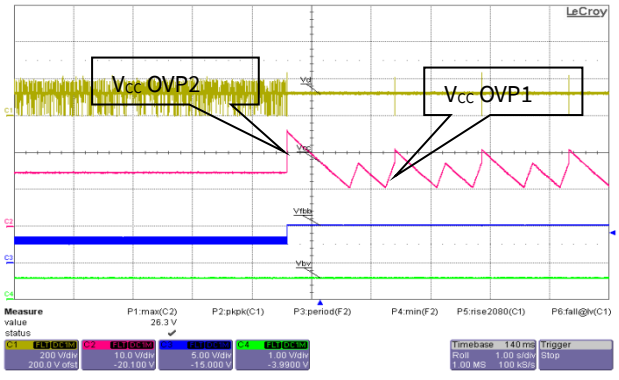
11.7 Output ripple voltage during burst mode at 1 W load

	
Channel 1; C1 : Output ripple voltage (Vo) Channel 2; C2 : Output current (Io)	Channel 1; C1 : Output ripple voltage (Vo) Channel 2; C2 : Output current (Io)
$V_{ripple_pk_pk}$=25mV Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter	$V_{ripple_pk_pk}$ = 18mV Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter
Figure 27 AC output ripple @ 85Vac and 1W load	**Figure 28 AC output ripple @ 265Vac and 1W load**

11.8 Active Burst mode operation

	
Channel 1; C1 : Current sense voltage (V_{CS}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FBB}) Channel 4; C4 : BV voltage (V_{BV})	Channel 1; C1 : Current sense voltage (V_{CS}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FBB}) Channel 4; C4 : BV voltage (V_{BV})
Condition: V_{FB}<1.27V & last for 20ms (load change form full load to 0.5W load)	Condition: V_{FB}>4.5V (load change form 0.5W load to full load)
Figure 29 Entering active burst mode @ 85Vac	**Figure 30 Leaving active burst mode @ 85Vac**

11.9 Vcc over voltage protection (Odd skip auto restart mode)



Channel 1; C1 : Current sense voltage (V_{CS})

Channel 2; C2 : Supply voltage (V_{CC})

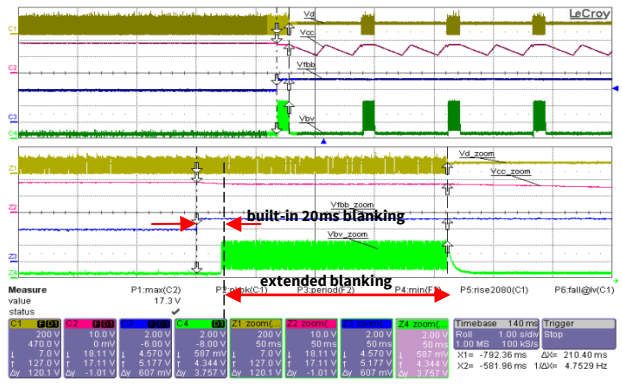
Channel 3; C3 : Feedback voltage (V_{FBB})

Channel 4; C4 : BV voltage (V_{BV})

Condition: V_{CC}>20.5 & last for 150µs
V_{CC}>20.5 & V_{FB}>4.5V & during soft start
& last for 30µs
(J4 disconnected during system operating at no load)

Figure 31 Vcc overvoltage protection @ 85Vac

11.10 Over load protection (Auto restart mode)



Channel 1; C1 : Current sense voltage (V_{CS})

Channel 2; C2 : Supply voltage (V_{CC})

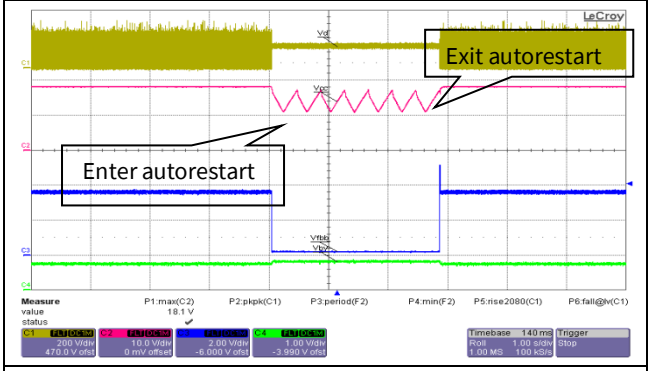
Channel 3; C3 : Feedback voltage (V_{FBB})

Channel 4; C4 : BV voltage (V_{BV})

Condition: V_{FB}>4.5V & last for 20ms & V_{BV}>4.5V &
last for 30µs
(output load change from 2.4 to 3A)

Figure 32 Over load protection with built-in+extended blanking time @85Vac

11.11 V_{CC} under voltage/Short optocoupler protection (Normal auto restart mode)



Channel 1; C1 : Current sense voltage (V_{CS})

Channel 2; C2 : Supply voltage (V_{CC})

Channel 3; C3 : Feedback voltage (V_{FBB})

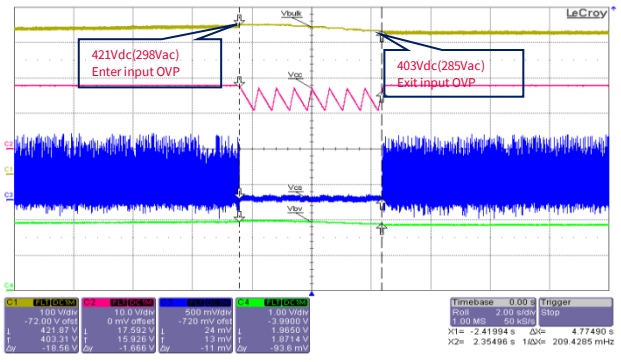
Channel 4; C4 : BV voltage (V_{BV})

Condition: V_{CC}<10.5V

(short the transistor of optocoupler during system operating @ full load and release)

Figure 33 V_{cc} under voltage/short optocoupler protection @ 85Vac

11.12 AC Line input OVP mode



Channel 1; C1 : Bulk voltage(V_{bulk})

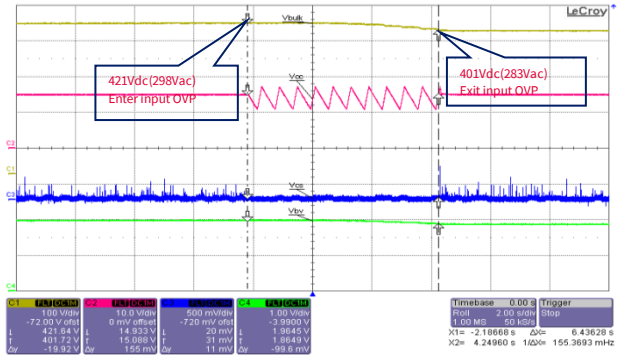
Channel 2; C2 : Supply voltage (V_{CC})

Channel 3; C3 : Current sense voltage (V_{CS})

Channel 4; C4 : BV voltage (V_{BV})

Condition: V_{BV}>1.98V & last for 400µs (OVP detect)
V_{BV}<1.91V & last for 5µs (OVP reset)
(gradually increase AC line voltage until OVP detect and decrease AC line until OVP reset)

Figure 34 Input OVP mode at max. load condition



Channel 1; C1 : Bulk voltage(V_{bulk})

Channel 2; C2 : Supply voltage (V_{CC})

Channel 3; C3 : Current sense voltage (V_{CS})

Channel 4; C4 : BV voltage (V_{BV})

Condition: V_{BV}>1.98V & last for 400µs (OVP detect)
V_{BV}<1.91V & last for 5µs (OVP reset)
(gradually increase AC line voltage until OVP detect and decrease AC line until OVP reset)

Figure 35 Input OVP mode at no load condition

12 References

[1] Infineon Technologies, Datasheet “CoolSET™-F3R80 ICE3AR4780VJZ Off-Line SMPS Current Mode Controller with integrated 800V CoolMOS™and Startup cell(input OVP & Frequency Jitter) in DIP-7”

[2] Infineon Technologies, AN-PS0044-CoolSET F3R80 DIP-7 brownout/input OVP & frequency jitter version design guide-V1.5

Revision History

Major changes since the last revision

Page or Reference	Description of change
5	Add section 5.3 under circuit description

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