GC3011A

3.3V DIGITAL RESAMPLER CHIP

DATASHEET

October 2002

This datasheet contains information which may be changed at any time without notice.

REVISION HISTORY

This datasheet is revised from the GC3011 datasheet to reflect the changes in the GC3011A replacement.

Revision	Date	Description
1.0	9 Sept 2002	First GC3011A datasheet. Major changes in specifications to reflect 3.3volt operation.

0.1 GC3011A TO GC3011 COMPARISON

The GC3011A is designed to be a functional and footprint compatible replacement for the GC3011 chip. The timing specifications for the GC3011A meet and exceed the timing specifications for the GC3011. Electrically the GC3011A is a 3.3 volt only part, making it incompatible with the GC3011's 5 volt mode. The GC3011A is fully compatible with the GC3011's 3.3 volt mode, but at a lower power consumption. See Section 4 for timing and electrical specifications. NOTE: The GC3011A inputs are NOT 5 volt tolerant; chip damage may occur if the input voltages exceed Vcc + 0.5V (3.8 volts). Designs using the GC3011 at 5 volts will need to add a 3.3 volt supply and voltage level translators to use the GC3011A.

The function of the GC3011A has been slightly enhanced, but any enhancements are "backward" compatible with the GC3011 so that a GC3011 user will not need to change any software or processing algorithms to use the GC3011A chip. Highlights of the enhancements follow.

0.1.1 Clock Loss Detect and Power Down Modes

The GC3011 chip used a slow internal clock to power down the chip or to put it into a low power mode if the clock is stopped. The slow clock has been removed in the GC3011A and replaced with a mode that will put the chip in a fully static mode if the clock has stopped. The fully static mode powers down the chip and reduces the power consumption down to a few microwatts until the clock resumes. The user can also force the power down state if desired. Two control bits (address 13 bits 6 and 7) are used to control the clock loss detect and power down modes. One control bit turns off the clock loss detect circuit, the other forces the power down mode. Both bits are cleared at power up to keep GC3011 compatibility.

See Section 2.9 for details.

0.1.2 Control Interface

The control interface has been enhanced to use either the R/$\overline{W}$ and $\overline{CS}$ strobes of the original GC3011, or to use the $\overline{RE}$, $\overline{WE}$ and $\overline{CE}$ strobes used by most memory interfaces. If the $\overline{RE}$ pin is grounded, then the interface behaves in the R/$\overline{W}$ and $\overline{CS}$ mode, where the $\overline{WE}$ pin becomes the R/$\overline{W}$ pin and the $\overline{CE}$ pin becomes the $\overline{CS}$ pin. The $\overline{RE}$ pin on the GC3011A chip is a ground pin (pin 58) on the GC3011 chip, so that a GC3011A chip soldered into a GC3011 socket will automatically operate in the GC3011 R/$\overline{W}$ and $\overline{CS}$ mode.

See Section 2.1 for details.

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GC3011A DATASHEET

1.0 KEY FEATURES

- 100 million samples per second (MSPS) input rate
- Fractional rate change down to 1/4th the input rate
- Synchronization logic to allow multi-chip complex data operation.
- Multiple chips can be synchronized with fixed delay offsets.
- Two chips allow rate changes up or down.
- 12 bit data I/O
- 32 bit rate control accumulator
- 16 sample output FIFO
- 15 tap linear phase interpolator
- 4096 interpolation steps
- 80% input passband (0 to 0.4F_{CK})
- +/- 0.1 dB passband ripple
- Less than +/- 0.02 degrees rms phase jitter
- -73 dB image rejection
- 60 dB worst case NPR
- Adaptive rate change to lock the resampling ratio to the output clock rate
- PLL/VCO to generate an output clock to match the rate change
- Microprocessor interface for control, output, and diagnostics
- Built in diagnostics
- 500 mW at 100 MHz, 3.3 volts
- 100 pin QFP package

1.1 BLOCK DIAGRAM

A block diagram illustrating the major functions of the chip is shown in Figure 1

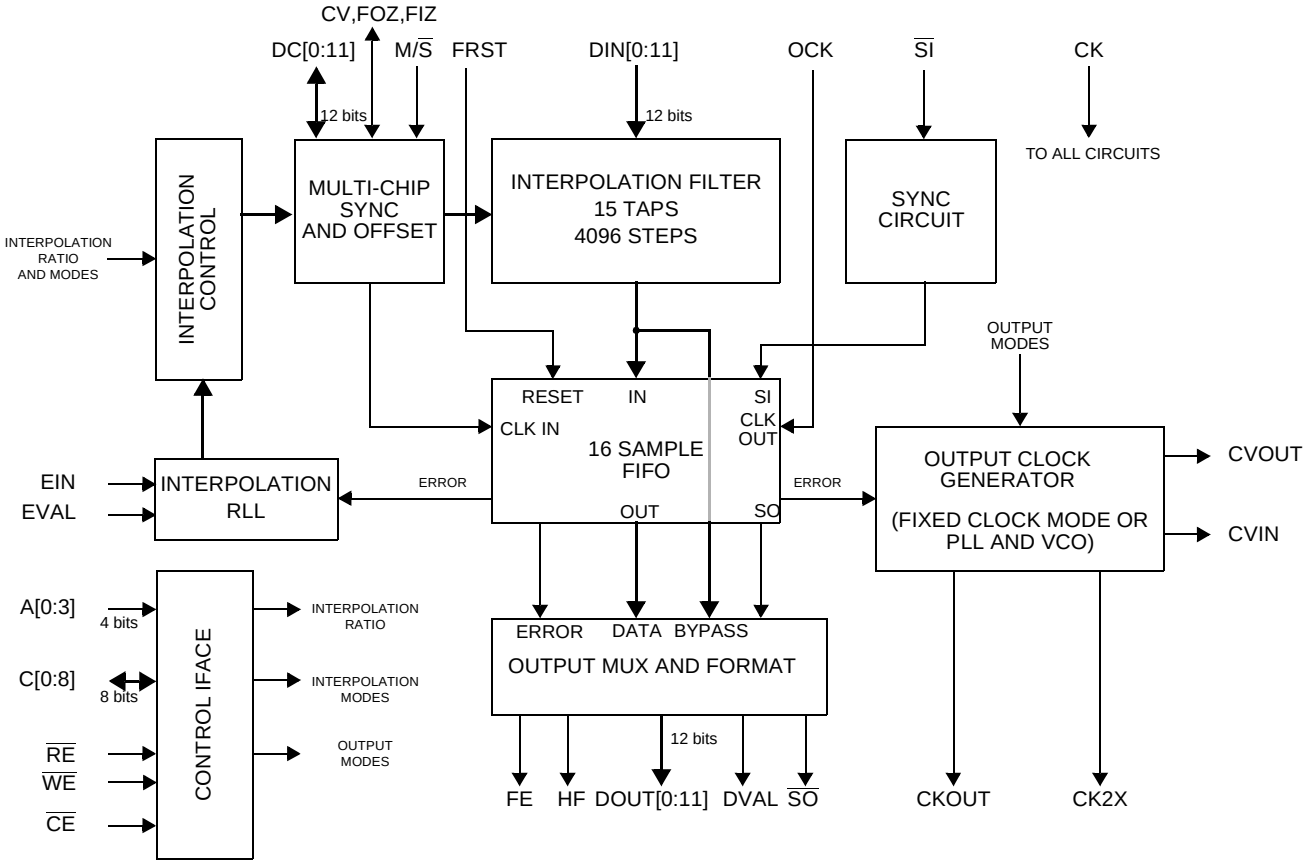


Figure 1. GC3011A Block Diagram

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2.0 FUNCTIONAL DESCRIPTION

Fabricated in 0.5 micron CMOS technology, the GC3011A chip is a general purpose digital resampler chip designed to accurately reduce the sample rate of the input data stream by a fractional amount ranging from 1.0 down to 0.25. The chip includes an interpolation control block, a multi-chip synchronization and offset circuit, a 15 tap interpolation filter, a 16 word output FIFO memory, an output clock generator and an interpolation ratio rate-lock loop (RLL) circuit. In addition, an output multiplexor circuit allows the user to by-pass the FIFO and output the resampled samples directly. A control interface allows the user to set the resampling modes, resampling rate and output clocking modes.

The multi-chip sync and offset circuit allows multiple GC3011A chips to be synchronized in a master/slave configuration. The offset portion of the circuit allows each chip's interpolation delay to be offset by a fixed amount relative to the other chips.

The GC3011A chip accepts input rates up to 100 MHz.

The chip can operate in a fixed resampling mode where the user specifies the desired output rate, or the chip can be configured to adapt the resampled rate to match an externally provided output clock. The resampled data can be output synchronous to the input clock or can be output synchronous to the output clock. When output synchronous to the input clock the samples are accompanied by a data valid flag to indicate which samples are valid and which are invalid. When output synchronous to the output clock the chip uses the internal 16 word FIFO to smooth the data. The output clock can be provided externally, or can be generated within the chip using the internal oscillator which is locked to the resampled data rate.

The chip does not provide any anti-alias filtering. The user must bandlimit the input signal before it is down-sampled by the GC3011A chip. The GC2011A digital filter chip can be used for this purpose.

Fractional upsampling can be achieved by using the GC2011A digital filter chip to up sample the signal by a factor of two before it is downsampled by the GC3011A.

On chip diagnostic circuits are provided to simplify system debug and maintenance.

The chip receives configuration and control information over a microprocessor compatible bus consisting of an 8 bit data I/O port, a 4 bit address port, a read/$\overline{\text{write}}$ bit, and a control select strobe. The chip's 16 control registers (8 bits each) are memory mapped into the 4 bit address space of the control port.

2.1 CONTROL INTERFACE

The chip is configured by writing control information into sixteen control registers within the chip. The contents of these control registers and how to use them are described in Section 4.0. The registers are written to or read from using the **C[0:7]**, **A[0:3]**, **$\overline{\text{RE}}$**, **$\overline{\text{WE}}$**, and **$\overline{\text{CE}}$** pins. Each control register has been assigned a unique address within the chip. An external processor (a microprocessor, computer, or DSP chip) can write into a register by setting **A[0:3]** to the desired register address, setting the **$\overline{\text{CE}}$** pin low, setting **C[0:7]** to the desired value and then pulsing **$\overline{\text{WE}}$** low. **$\overline{\text{RE}}$** must remain high

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To read from a control register the processor must set **A[0:3]** to the desired address, set **$\overline{\text{CE}}$** low, and then set **$\overline{\text{RE}}$** low. The chip will then drive **C[0:7]** with the contents of the selected register. After the processor has read the value from **C[0:7]** it should set **$\overline{\text{RE}}$** and **$\overline{\text{CE}}$** high. The **C[0:7]** pins are turned off (high impedance) whenever **$\overline{\text{CE}}$** is high or **$\overline{\text{WE}}$** is low. The chip will only drive these pins when both **$\overline{\text{CE}}$** and **$\overline{\text{RE}}$** are low and **$\overline{\text{WE}}$** is high.

If **$\overline{\text{RE}}$** is held low, then the interface will behave in the GC3011 mode, where **$\overline{\text{CE}}$** is **$\overline{\text{CS}}$**, and **$\overline{\text{WE}}$** is **R/$\overline{\text{W}}$**.

2.2 SYNC CIRCUIT

The sync circuit is used to synchronize the chip during diagnostics or system initialization. The sync circuit includes a 20 bit counter which can be programmed to generate terminal count (TC) sync pulses every 2^8, 2^{12}, 2^{16} or 2^{20} input clock cycles. The counter can be synchronized to the $\overline{\text{SI}}$ sync input, or left to free run. The $\overline{\text{SI}}$ and TC sync pulses can be used to synchronize or clear the counters, accumulators or state machines found within the rest of the chip. The lower 12 bits of the counter are used as input samples to the resampler during diagnostics.

The user may select which sync signal is output from the chip on the $\overline{\text{SO}}$ pin. The $\overline{\text{SO}}$ signal can be either a delayed version of the sync input, the counter's TC sync, or a one-shot pulse. The sync output signal is one clock cycle wide, synchronized to the output clock (OCK).

2.3 INTERPOLATION FILTER

The interpolation filter is used to interpolate between input data samples in order to generate output samples at fractional time delays relative to the input samples. The filter is a 15 tap FIR filter with 4096 sets of coefficients. Each set of coefficients corresponds to a different time delay between input samples. The circuit accepts a new delay control word (12 bits) every clock cycle which tells it which set of coefficients to use during that clock cycle. This allows the interpolation time delays to vary every clock sample. Interpolating to 4096 delay values gives a worst case phase error (phase jitter) of +/- 360/8192 = +/- 0.09 degrees.

The delay control word can either come from the interpolation control circuit described below, or from an external source. The external input allows multiple resamplers to be synchronized to controls coming from a common resampler chip in a master/slave arrangement.

2.4 INTERPOLATION CONTROL

The interpolation control circuit is used to generate the time delay control words used by the interpolation filter. The interpolated output rate is specified as the ratio of the input rate to the output rate. This ratio is limited to be within the range of 1 to 4 and is formatted as a 32 bit word. The most significant 2 bits are the integer portion of the ratio and the lower thirty bits are the fractional part. This ratio is equivalent to the ratio of the output sample spacing to the input sample spacing. The interpolation ratio feeds a 32 bit accumulator. The 2 bit integer portion of the accumulator's output is used to determine the number of input

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samples to skip between output samples, and the upper 12 bits of the fractional part is used as the interpolation filter's delay control word.

2.5 INTERPOLATION RLL

The interpolation ratio can be fixed by the user, or can be allowed to adapt to the ratio that keeps the output FIFO half-full. The adaption is performed by the interpolation rate lock loop (RLL) circuit. Figure 2 is a block diagram showing the interpolation RLL circuit and the interpolation control circuit.

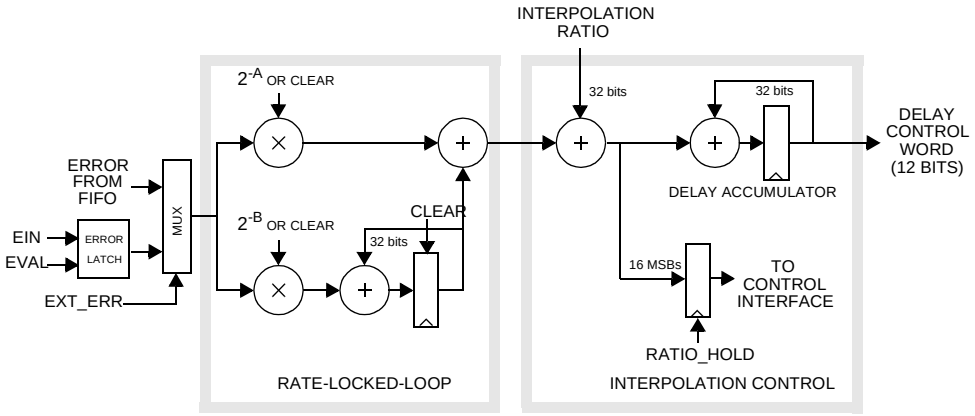


Figure 2. Interpolation RLL And Control Circuits

2.5.1 Fixed Interpolation Mode

The fixed interpolation mode is used when the user knows what the desired output rate should be relative to the input rate. For example, a user may wish to use this mode when he is using the resampler to baud synchronize a modem signal. In this case the user has an external baud rate detection circuit which tells the user how to adjust the interpolation ratio.

The user fixes the interpolation ratio by turning off (clearing) the Rate-Locked-Loop (RLL) circuit. Clearing the RLL output fixes the delay accumulator's input to be the 32 bit value supplied by the user.

2.5.2 Adaptive Interpolation Mode

In this mode the RLL circuit automatically adjusts the interpolation ratio to keep the FIFO half full. This mode is used when the output clock is fixed and the chip's interpolation ratio must exactly match the ratio between the chip's input clock and the output clock. For example, a user may wish to use the adaptive interpolation mode in order to interface two asynchronous signal processing systems, or when an external baud sync circuit has provided a baud synchronous output clock.

The adaption uses an error signal from the FIFO. The error is a bit indicating the error is plus or minus one. A minus one indicates that the FIFO is less than half full and the interpolation ratio (the ratio of the input rate to the output rate) needs to be decreased. A plus one indicates that the FIFO is more than half full and the interpolation ratio needs to be increased. The user sets up the adaptive interpolation mode

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by setting the interpolation ratio to a value close to the actual ratio[1] and setting the adaption constants 2^{-A} and 2^{-B}, where A and B are constants ranging from 0 to 31.

These constants set the adaption rate and the tracking bandwidth of the adaption loop. These constants can also be set to zero in order to clear the 2^{-A} or 2^{-B} feedback paths or to freeze the adaption process. A large value for B will slow the adaption process and will reduce the phase jitter, but will also decrease the tracking bandwidth of the loop. The adaption time when the interpolation ratio starts at zero will be approximately 2^{B} clock cycles. The tracking bandwidth of the loop is determined by how fast the loop will adapt to an output rate change and if it adapts fast enough to prevent a FIFO overflow or underflow error. Since the FIFO has a range of +/- 8 samples, the tracking range in Hz is approximately $2^{(3-B)}$ times the input clock rate[2].

The constant 2^{-A} is used to dampen the adaption loop to prevent ringing. The value of A should be approximately one-half of B. Note that small values of A will introduce residual phase jitter equal to +/- $360x2^{-A}$ degrees.

The values of A and B are application dependant. If adaption time is important, then a two-stage adaption process may be desirable. An initial setting of B equal to 16 and A equal to 12 will allow the loop to converge rapidly. Once the loop has converged, A and B can be set to minimize residual phase noise. Settings between 22 and 31 for B and between 14 and 15 for A are suggested. A setting of B=22 gives a tracking bandwidth of 128 Hz. A setting of B=31 would reduce the tracking bandwidth to about 0.25 Hz.

2.5.3 External Adaption Mode

The RLL can be adapted from an external error signal using the EIN and EVAL inputs to the chip. In this mode the user uses an external circuit to detect resampling rate errors and drives the EIN with a 0 or a 1. A ‘1’ means increase the ratio and a‘0’ means decrease it. A high level on the EVAL signal identifies when the EIN signal is valid. The EVAL and EIN signals are clocked into the chip on the rising edge of the input clock.

2.5.4 The Ratio-Hold Register

The user can monitor current resampling ratio using the Ratio-Hold Register. This register captures and holds the most significant 16 bits of the current resampling ratio when the RATIO_HOLD bit is set (See Section 4.8). This register can be used to determine if the resampler has converged in the adaptive interpolation mode (See Section 2.5.2 above).

1. This speeds up the adaption, but is not necessary for the adaption to work. The ratio can be set to zero if desired.
2. The chip will converge to the correct interpolation ratio outside of the tracking bandwidth, but while it is converging the FIFO will overflow or underflow so that the data output will be corrupted until it re-converges.

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2.6 MULTI-CHIP SYNC AND OFFSET CIRCUIT

The multi-chip sync and offset circuit allows multiple chips to be used in parallel, all locked to the same resampling ratio and phase. The circuit also allows each chip to be offset by a fixed time delay relative to the others. A block diagram of the circuit is shown in Figure 3.

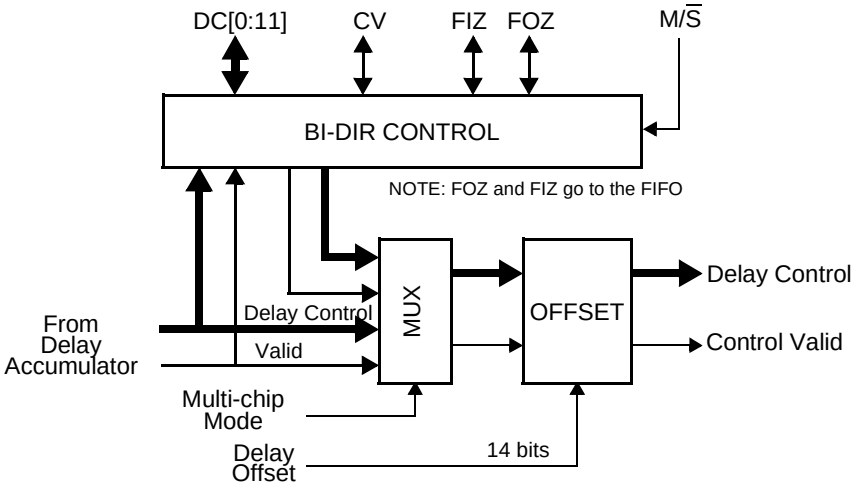


Figure 3. Multi-chip Synchronization And Offset Circuit

Multiple chips are synchronized in a master/slave configuration. The M/$\overline{S}$ control pin is high for the master chip and is low for the slave chip. The master chip drives the bi-directional DC, CV, FIZ, and FOZ pins as outputs. The slave chips use the pins as inputs. The multi-chip mode control signal selects between the internal filter controls and the external ones.

The master chip sends the 12 delay control bits (DC) and the control valid strobe (CV) to the slave chips. The slave chips accept the DC and CV signals, add a delay offset to them and output the delay control and control valid strobes to the resampler filter.

The FIZ and FOZ flags are used to lock the FIFOs in the slave chips to the master chip's FIFO. The FOZ and FIZ flags go high each time the fifo read or write address counters on the master chip go to zero. These flags clear the read or write counters on the slave chips. FOZ controls the read counters, FIZ controls the write counters.

2.7 OUTPUT FIFO

The 16 sample FIFO is used to smooth the output interface between data being generated synchronous to the input clock and data being output synchronous to the output clock. If the interpolation ratio is correct, then the FIFO would only need to be one or two samples deep. Since the ratio can not be exact, the FIFO has been expanded to 16 words to allow a +/- 8 sample buffer. The +/- 8 sample buffer prevents the FIFO from overflowing or underflowing while the RLL circuit (or an external adaption loop) adapts to variations in the output clock.

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Output samples are clocked into the FIFO by the interpolation control circuit at a rate determined by the interpolation ratio. For example, if the interpolation ratio is set at 1.5, then two samples will be clocked into the FIFO for every 3 input clocks. If the ratio is 2.25, then four samples would be stored in the FIFO for every nine input clocks. The FIFO timing for a ratio of 1.5 is shown in Figure 4.

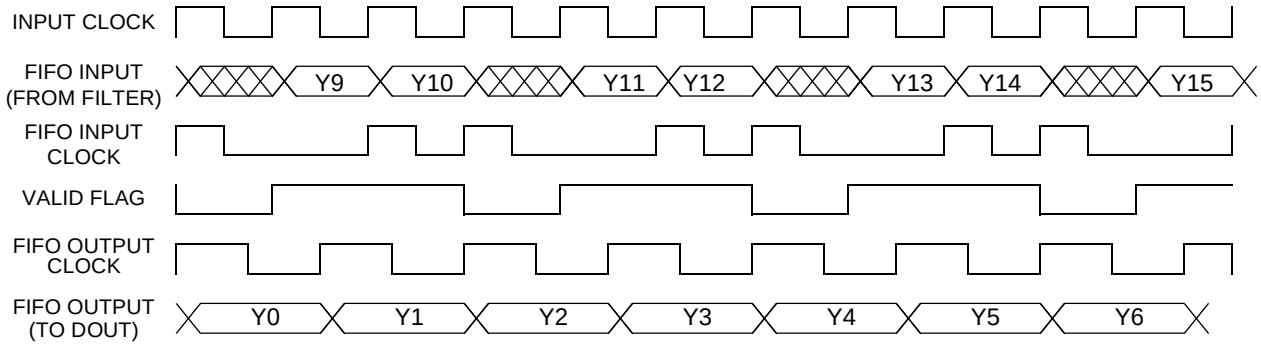


Figure 4. Fifo Timing

2.7.1 FIFO ERRORS

Notice that the output data samples in Figure 4 are delayed by 8 clock cycles relative to the input samples. This is the ideal case when the FIFO is half full. If the output clock is faster than the FIFO input clock, then the FIFO will empty and an underflow error will occur. If the output clock is slower than the FIFO input clock, then the FIFO will fill up and an overflow error will occur. The FIFO will remain in the overflow or underflow condition until the I/O rates change and the FIFO begins to empty or fill, or until the FIFO is reset. The output samples will not be valid when an underflow/overflow error occurs.

The FIFO generates half full and FIFO error flags. The half full flag is high whenever the FIFO contains more than 8 samples. The FIFO error flag is high whenever the FIFO contains less than 2 or more than 14 samples. The FIFO half full and error flags are output from the chip on the HF and FE pins. The user can also monitor the FIFO using the HALF_FULL, FIFO_FULL, FIFO_EMPTY and FIFO_DEPTH control bits in the FIFO control register (see Sections 4.8 and 4.9). The FIFO_FULL and FIFO_EMPTY control bits are set when an overflow or underflow condition occurs and will remain set until the user clears the bits. The FIFO_DEPTH is a read only 4 bit field which reflects the depth of the FIFO. The depth is encoded as a 4 bit gray scale number to minimize errors when reading the FIFO depth. The mapping between grayscale and binary is as follows:

	FIFO_EMPTY						HALF_FULL				FIFO_FULL					
GRAY SCALE:	0	1	3	2	6	7	5	4	C	D	F	E	A	B	9	8
HEX:	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

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2.7.2 FIFO RESET

The FIFO is initialized to its half full state by setting the FRST pin high or by using the FIFO_RESET control mode (See Section 4.6). The FIFO will remain in the half full state until the FRST pin is set low. The 8 outputs following a FIFO_RESET will be invalid.

2.8 OUTPUT CLOCK GENERATOR

The resampled data can be output either synchronous to the input clock, synchronous to an internally generated output clock, or synchronous to an externally provided output clock. A separate clock input pin (OCK) is provided for the output data clock. The user connects this clock pin to either the input clock, the internally generated resampled clock (CKOUT), or to an externally provided clock as described below.

2.8.1 Synchronous Output Mode

In this mode the output FIFO is bypassed and the data is output synchronous to the input clock. The samples are accompanied by a data valid strobe (DVAL) which indicates whether the user should skip or accept each output sample. The polarity of the strobe can be programmed as active high or low depending upon how the user wants to use it. A typical use of the DVAL strobe would be as an enable strobe to external registers or FIFOs. In the DVAL_EARLY mode (See Section 4.6) the DVAL signal is active one clock cycle early so that it can be used as a clock enable to the GC2011 or GC3021 chips which expect the clock enable to arrive one clock earlier than the data.

In the synchronous output mode the input clock pin (CK) must be tied to the output clock pin (OCK).

2.8.2 Internally Generated Clock

A voltage controlled oscillator (VCO) and charge-pump phase-lock-loop (PLL)[1] is built into the GC3011A to generate a smooth clock to match the resampled data rate. The VCO consists of a odd number of inverters connected in a ring (commonly known as a ring oscillator). The clock frequency is controlled by dividing the ring oscillator output by a factor of 2^n, by varying the number of stages in the ring and by adjusting a control voltage. The output of the ring oscillator can be divided by 2^n where n ranges from 0 to 15. The number of stages in the ring oscillator can be varied digitally from 1 to 16. Each stage is non-inverting, a final stage provides the feedback inversion. The control voltage adjusts the delay of each stage and hence the frequency of oscillation. The control voltage can adjust the oscillation frequency in either a narrow range adjust mode or wide range adjust mode. In the narrow mode the control voltage can adjust the frequency by ±12%. These parameters allow the output clock to be generated with a minimum frequency of 10 KHz and a maximum frequency of 80 MHz.

1. F. M. Gardner, “Charge-Pump Phase-Lock-Loops”, IEEE Transactions on Communications, vol. COM-28, pp. 1849-1858, Nov. 1980

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The chip outputs the resampled clock on the CKOUT pin. This clock will drive up to 40 pF of load. In a typical application the user will connect the CKOUT pin to an external clock buffer or driver chip. The output of the driver chip is then used to drive the output clock (OCK) pin as well as any circuitry accepting the GC3011A chip's output data. This guarantees that the output data will be clocked out of the GC3011A chip using the same clock edge that the follow-on circuitry uses to accept it.

The chip also generates a double rate clock (CK2X). This clock is twice the rate of the CKOUT clock and is locked to the CKOUT clock so that the rising and falling edges of CKOUT line up with rising edges of the CK2X.

The chip automatically adapts the clock division ratio, the number of stages in the ring oscillator and the control voltage so as to generate a clock which matches the resampled data rate and keeps the FIFO half full. The adaption time is typically very short (less than 2000 output clock cycles). The VCO/PLL will then track variations in temperature, supply voltage and resampling ratio over a ± 12% range.

The user must check that the ± 12% is adequate for the application. To do this one must estimate the maximum temperature variation, the maximum supply voltage variation and the maximum resampling rate variation for the resampler and then use the following dependencies to estimate the adequate tracking range. The temperature dependence of the VCO is -0.27%/C. The voltage dependence of the VCO is 18%/V at 5 volts and 40% per volt at 3.3 volts.

For example, if the temperature at adaption time is 100 °C and is expected to vary ± 20 °C, and if the voltage at adaption time is 5V and is expected to vary ± 0.1V, and if the resampled data rate is expected to change by 0.1%, then the total range required is:

$$\text{VCO range} = \pm (0.27 \times 20 + 18 \times 0.1 + 0.1) = \pm 7.3\%$$

which is well within the ±12% allowable range.

The CLOCK control registers (see Section 4.7) allow the user to force, if necessary, the divider and ring oscillator length settings. The VCO status register allows the user to monitor the divider and length settings.

2.8.3 Extended VCO Range Mode

The pull range of the VCO can be extended by setting the EXTENDED_RANGE bit in the CLOCK control registers (See Section 4.7). This mode doubles the pull range to ±24%to allow a wider variance due to temperature or voltage fluctuations. This mode increases the phase jitter of the VCO.

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2.8.4 Selecting External Components for the PLL

The recommended analog supply filter and loop filter is shown in Figure 5.

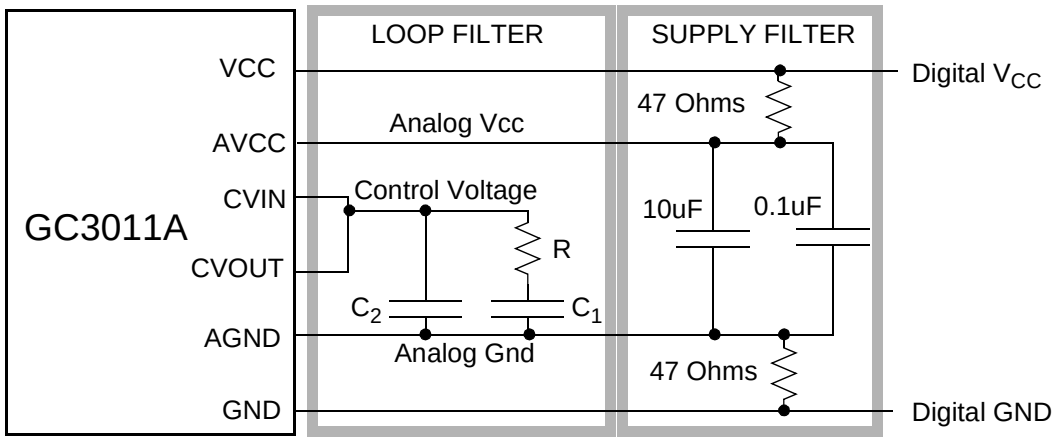


Figure 5. Supply and Loop Filters

All components shown in figure 5 should be placed as close as possible to the package. CVIN and CVOUT should be shorted together. Separate CVIN and CVOUT pins are provided for specialized applications that need an active loop filter.

The supply filter is used to isolate the analog power pins from the noise on the digital supply. This filter will cause a slight drop in the analog VCC voltage. At 3.3 volts the drop is about 0.1 volts.

The PLL bandwidth and damping are set by the resistor R and the capacitors C_1 and C_2. The resistor R sets the loop gain K

The PLL uses a third order loop to reduce jitter due to voltage across R while the pump current is active. The third order loop is accomplished using a second capacitor C_2, which should be significantly smaller than C_1. Generally, $C_2 = C_1 / 100$

Suggested values for R, C_1 and C_2 are R=220 Ohms, C1=0.22 uF, and C2 = 0.0022uF

2.8.5 External Output Clock Mode

The FIFO output can be clocked using an externally provided clock. Samples will be output from the chip synchronous to the rising edge of this clock. This mode is used when the user has an external output clock, or when multiple chips are being synchronized to an output clock generated by one of a bank of resampler chips. In this mode the OCK clock pin is driven by the external clock.

2.9 POWER DOWN MODES

The chip has a power down and clock loss detect circuit. This circuit detects if the clock is absent long enough to cause dynamic storage nodes to lose state. If clock loss is detected, an internal reset state

is entered to force the dynamic nodes to become static. The control registers are not reset and will retain their values, but any data values within the chip will be lost. When the clock returns to normal the chip will automatically return to normal. In the reset state the chip consumes only a small amount of standby power. The user can select whether this circuit is in the automatic clock-loss detect mode, is always on (power down mode), or is disabled (the clock reset never kicks in) using the DISABLE_CK_LOSS control bit in address 13 bit 7 and the GLOBAL_RESET control bit in address 13 bit 6.

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2.10 DIAGNOSTICS

An input ramp generator, a sync period generator, and a checksum generator are provided on the chip in order to run diagnostic tests. Diagnostics are performed by turning on the ramp generator, enabling the diagnostic syncs, letting the chip operate for at least 4 sync periods, reading the checksum and comparing it to its predicted value. A new checksum is generated every sync period. The input ramp sequence is the same for every sync period and the chip is re-initialized at the beginning of each sync period so that each checksum should be the same once the chip's data path has been flushed. The chip requires at least 3 sync periods to flush, so the fourth and following checksums should be valid. The test is then repeated for several different resampling ratios and mode settings.

The sync period is 2^{20} clocks, or approximately 1 million clock cycles, so four sync periods will be about 4 million clocks. This represents a delay of less than 70 milliseconds for a clock rate of 60 MHz.

The following table lists the expected checksums for four test configurations. These tests do not check the RLL circuit, only the resampling operation. These tests are only valid when CK is tied to OCK, or if CKOUT is tied (possibly through a buffer) to OCK. These tests do not work for boards that have independent CK and OCK clocks (i.e., the boards that use the RLL circuit to resample between two clock rates). If CKOUT drives OCK, then the maximum clock rate for these tests is 40MHz at 5 volts, and 20 MHz at 3.3 volts.

All values are HEX

	TEST NUMBER							
Register	1	2	3	4	5	6	7	8
0	00	AA	55	11	44	88	88	AA
1	00	AA	55	22	55	99	99	AA
2	00	AA	55	33	66	BB	BB	AA
3	40	4A	55	66	99	F8	E8	4A
4	00	00	AA	55	88	55	55	55
5	C0	C0	EA	D5	F0	D5	D5	D5
6	00	<- Same ->						
7	C0	<- Same ->						
8	AB	<- Same ->						
9	47	<- Same ->						
A	47	<- Same ->				47	42	42
B	00	<- Same ->						
C	6E	<- Same ->						
D	83	<- Same ->						

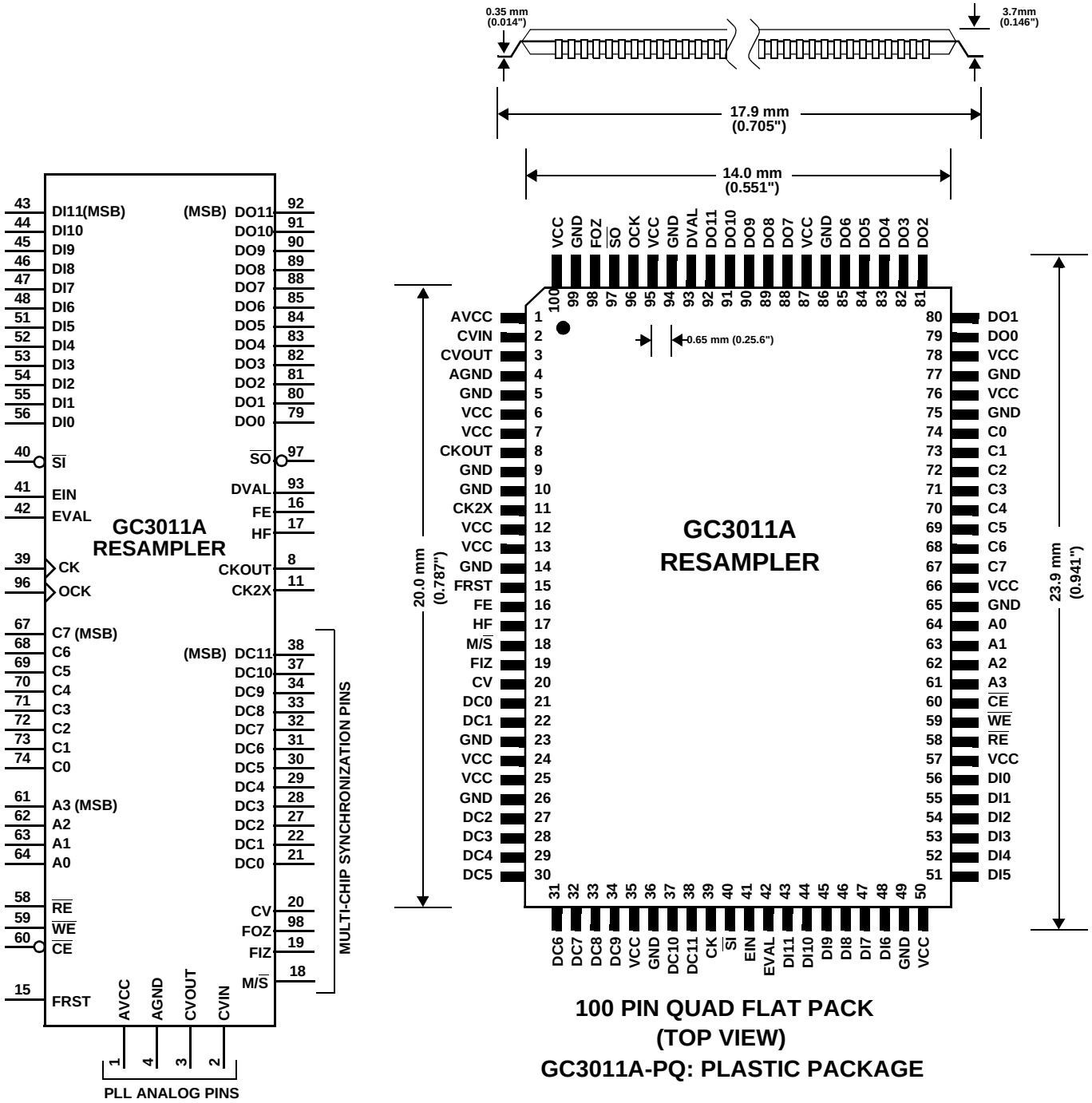
Load the chip with these values, wait for checksum to stabilize, about 2^20 clocks, then read the checksum and compare it with:

Checksum	48	94	53	CD	51	72	34	1B

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3.0 PACKAGING

The GC3011A chip comes in a 100 pin plastic quad flatpack package



100 PIN QUAD FLAT PACK
(TOP VIEW)
GC3011A-PQ: PLASTIC PACKAGE

VCC PINS:6,7,12,13,24,25,35,50,57,66,76,78,87,95,100

GND PINS:5,9,10,14,23,26,36,49,65,75,77,86,94,99

NOTE: 0.01 to 0.1 μf DECOUPLING CAPACITORS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO EACH SIDE OF THE CHIP

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3.1 PIN DESCRIPTIONS

SIGNAL	DESCRIPTION
DI[0:11]	**INPUT DATA.** *Active high* The 12 bit two's complement input samples. New samples are clocked into the chip on the rising edge of the clock. The input data rate is assumed to be equal to the clock rate.
CK	**INPUT CLOCK.** *Active high* The clock input to the chip. The input signals are clocked into the chip on the rising edge of this clock.
OCK	**OUTPUT CLOCK.** *Active high* The output signals are clocked out of the chip on the rising edge of this clock.
$\overline{\text{SI}}$	**SYNC IN**. *Active low* The sync input to the chip. All timers, accumulators, and control counters are, or can be, synchronized to **$\overline{\text{SI}}$**. This sync is clocked into the chip on the rising edge of the input clock (**CK**).
EIN	**ERROR IN**. *Active high* The external error input to the rate-lock-loop circuit. This signal is sampled on the rising edge of the input clock (**CK**).
EVAL	**ERROR VALID**. *Active high* **EVAL** identifies when the error input **EIN** signal is valid. The rate-lock-loop circuit updates using the EIN error input when **EVAL** is high and the EXT_ERR_MODE control bit is set (See Section 4.8). This signal is sampled on the rising edge of the input clock (**CK**).
DO[0:11]	**OUTPUT DATA**. *Active high* The resampled data are output as a 12 bit words on these pins. The bits are clocked out on the rising edge of the output clock (**OCK**).
DVAL	**DATA VALID**. *Programmable active high or low level* The data valid strobe. This strobe is used to identify the valid output samples when the chip is operated in the synchronous I/O mode (common I/O clock mode). This strobe is clocked out of the chip on the rising edge of the clock (**CK**). This strobe is active for the clock cycle just before **DO** changes. The high/low polarity of the strobe is programmable. See Section 2.5 for details.
$\overline{\text{SO}}$	**SYNC OUT**. *Active low* This signal is either a delayed version of the input sync **$\overline{\text{SI}}$**, the sync counter's terminal count (TC), or a one-shot strobe. The **$\overline{\text{SO}}$** signal is clocked out of the chip on the rising edge of the output clock (**OCK**).
M/$\overline{\text{S}}$	**MASTER/$\overline{\text{SLAVE}}$ CONTROL**. *High for master, low for slave* This pin determines if the chip is the master or slave in a multi-chip synchronization mode. This pin should be pulled high for the master chip and grounded for the slave chips.

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DC[0:11] — **DELAY CONTROL**. *Active high*
The 12 bit delay control word is used in the master/slave mode to lock the resampling ratio of multiple slave chips to a single master chip. The master chip broadcasts its delay control word on these pins. The slave chips accept the delay control word on these pins. The direction of the pins is determined by the **M/$\overline{S}$** pin. The **DC** word is clocked out of and into the chips on the rising edge of the input clock (**CK**).

CV — **CONTROL VALID**. *Active high*
The control valid strobe is broadcast by the master chip in the master/slave synchronization mode. The slave chips accept this signal to identify when the delay controls are valid. The direction of this pin is determined by the **M/$\overline{S}$** pin.The **CV** strobe is clocked out of and into the chips on the rising edge of the input clock (**CK**).

FOZ,FIZ — **FIFO READ ZERO, FIFO WRITE ZERO**. *Active high*
These controls are broadcast by the master chip in the master/slave synchronization mode. The slave chips use these signals to clear the FIFO input (**FIZ**) and FIFO output (**FOZ**) counters. The **FIZ** signal is clocked in and out of the chips on the rising edge of the input clock (**CK**). The **FOZ** signal is clocked in and out of the chips on the rising edge of the output clock (**OCK**). The direction of these pins are determined by the **M/$\overline{S}$** pin.

FRST — **FIFO RESET**. *Active high*
This signal resets the FIFO to the half full state. This signal is clocked into the chip on the rising edge of the input clock (**CK**) and must be active for at least one input clock cycle.

HF — **HALF FULL.** *Active high*
The FIFO half full flag. This signal is high when the FIFO is at least half full, and zero otherwise. This signal is clocked out on the rising edge of the input clock (**CK**)

FE — **FIFO ERROR.** *Active high*
The FIFO full or empty flag. This signal is high when the FIFO is either full or empty. If the FIFO is full, it will remain full until the output clock speeds up. If the FIFO is empty, it will remain empty until the output clock slows down. The output data will be unknown while this flag is high. The FRST pin can be used to force the FIFO to the half full state when a FIFO error occurs by connecting FE to FRST. This signal is clocked out on the rising edge of the input clock (**CK**).

CKOUT — **CLOCK OUTPUT.** *Active high*
The resampled clock output. The chip generates a 50% (nominal) duty cycle clock at the resampled data rate and outputs it on this pin.

CK2X — **DOUBLE RATE CLOCK OUTPUT.** *Active high*
This clock is output at twice the **CKOUT** clock rate, but not exceeding the highest clock frequency rating of the chip. This clock is useful when two chips are used in parallel to increase the data output rate.

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C[0:7]	**CONTROL DATA I/O BUS**. *Active high* This is the 8 bit control data I/O bus. Control register data is loaded into the chip or read from the chip through these pins. The chip will only drive these pins when **$\overline{\text{CE}}$** is low **$\overline{\text{RE}}$** is low and **$\overline{\text{WE}}$** is high.
A[0:3]	**CONTROL ADDRESS BUS**. *Active high* These pins are used to address the 16 control registers within the chip. Each of the 16 control registers within the chip are assigned a unique address. A control register can be written to or read from by setting **A[0:3]** to the register's address.
$\overline{\text{WE}}$,$\overline{\text{RE}}$	**READ AND WRITE STROBE**. *Active low* These pin determines if the control bus cycle is a read or write operation.
$\overline{\text{CE}}$	**CONTROL STROBE**. *Active low* This control strobe selects the chip for the read or write operation.
AVCC, AGND	**ANALOG POWER AND GROUND,** *power pins* The analog power and ground pins used by the output clock generator. See Section 2.8.3.
CVIN, CVOUT	**PLL CONTROL VOLTAGE PINS,** *analog control voltage* The control voltage for the phase lock loop. Discrete components connected to these pins as shown in Section 2.8.3 form the loop filter for the PLL.

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4.0 CONTROL REGISTERS

The chip is configured and controlled through the use of 16 eight bit control registers. These registers are accessed for reading or writing using the control bus pins (**$\overline{\text{CE}}$**, **RE, WE**, **A[0:3]**, and **C[0:7]**) described in the previous section. The register names and their addresses are:

ADDRESS	NAME	ADDRESS	NAME
0	RATIO byte 0	8	Sync Mode
1	RATIO byte 1	9	Counter Mode
2	RATIO byte 2	10	Output Mode
3	RATIO byte 3	11	Clock Mode 0
4	OFFSET byte 0	12	Clock Mode 1
5	OFFSET byte 1	13	Status Control
6	A Reg	14	Status 0
7	B Reg	15	Status 1

The following sections describe each of these registers. The type of each register bit is either R or R/W indicating whether the bit is read only or read/write. All bits are active high.

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4.1 RATIO WORD REGISTERS

Registers 0, 1, 2, and 3 contain the 32 bit resampling ratio word. Bit 0 is the LSB, bit 31 is the MSB.

ADDRESS 0: RATIO BYTE 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**RATIO**[0:7]	Byte 0 (least significant) of the ratio

ADDRESS 1: RATIO BYTE 1

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**RATIO**[8:15]	Byte 1 of the ratio

ADDRESS 2: RATIO BYTE 2

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**RATIO**[16:23]	Byte 2 of the ratio

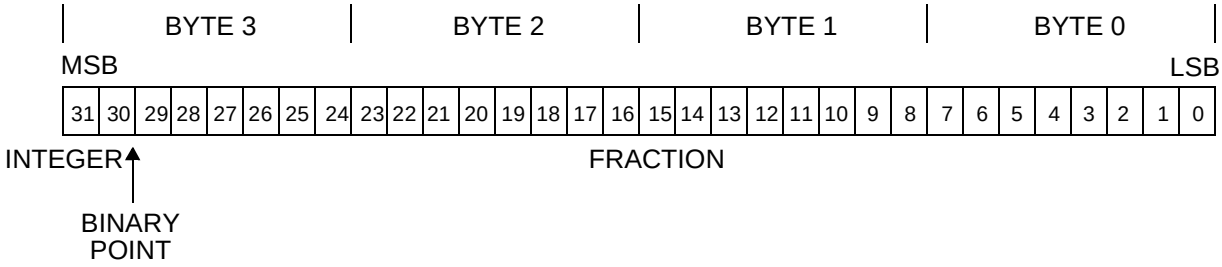
ADDRESS 3: RATIO BYTE 3

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**RATIO**[24:31]	Most significant byte of the ratio

If the desired output sampling rate is $\mathbf{F}_{OUT}$, and the input sampling rate is $\mathbf{F}_{IN}$, then the resampling ratio should be set to:

$$\mathbf{RATIO} = \mathbf{F}_{IN}/\mathbf{F}_{OUT}$$

Where **RATIO** is a unsigned fractional value ranging from 1 to 4 and formatted as follows:



Bits 30 and 31 are the integer part of **RATIO** and must equal 1, 2, or 3. An integer portion of 0 will not work. The fractional part can take on any value.

After loading the resampling ratio value the user can choose, using the LOAD_RATIO control bits in the Sync Mode register (See Section 4.4), to have it take effect immediately, or when a sync event occurs.

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4.2 OFFSET WORD REGISTERS

Registers 4, and 5 contain the 14 bit delay offset word. Bit 0 is the LSB, bit 13 is the MSB.

ADDRESS 4: OFFSET BYTE 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**OFFSET**[0:7]	Byte 0 (least significant) of the offset

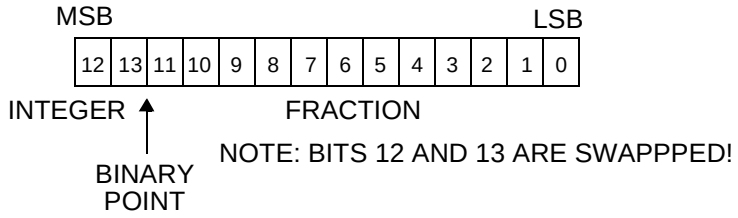
ADDRESS 5: OFFSET BYTE 1

BIT	TYPE	NAME	DESCRIPTION
0-5	R/W	**OFFSET**[8:13]	Most significant 6 bits of the offset. Note bits 12 and 13 are swapped!
6,7	R/W	LOAD_OFFSET	The sync mode for loading the offset into the offset circuit. See Table 1 in Section 4.4 for details.

If the desired delay offset is **D**, and the input sampling rate is $\mathbf{F}_{IN}$, then the offset should be set to:

$$\mathbf{OFFSET} = D*\mathbf{F}_{IN}$$

Where **OFFSET** is a unsigned fractional value ranging from 0 to 4 and formatted as follows:



Bits 12 and 13 are the integer part of **OFFSET** and can equal 0, 1, 2, or 3. The fractional part can take on any value.

After loading the offset delay value the user can choose, using the LOAD_OFFSET control bits, to have it take effect immediately, or when a sync event occurs.

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4.3 A AND B RATE-LOCK-LOOP (RLL) COEFFICIENT REGISTERS

Registers 6, and 7 contain the 5 bit A and B coefficients used in the RLL circuit.

ADDRESS 6: A REGISTER

BIT	TYPE	NAME	DESCRIPTION
0-4	R/W	**A**[0:4]	The **A** coefficient
5-7	R/W	unused	

ADDRESS 7: B REGISTER

BIT	TYPE	NAME	DESCRIPTION
0-4	R/W	**B**[0:5]	The **B** coefficient
5	R/W	ERR_POL	Invert the polarity of the EIN signal. Normally a high level on EIN will increase the resampling ratio (which decreases the output rate). With ERR_POL high a high level on EIN will decrease the resampling ratio (which increases the output rate).
6,7	R/W	LOAD_AB	The sync mode for loading A and B into the RLL circuit. See Table 1 in Section 4.4 for details.

The A and B coefficients range from 0 to 31. The FIFO error in the RLL is multiplied by 2^{-A} and 2^{-B} when A and B are non-zero. If A or B are zero, then the error for that path (See Figure 2) is cleared.

After loading the A and B coefficients, the user can choose, using the LOAD_AB control bits, to have them take effect immediately, or when a sync event occurs.

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4.4 SYNC MODE REGISTER

The Sync mode control register determines how the circuits within the chip are synchronized. Each circuit which requires synchronization can be configured to be synchronized to the sync input **(SI**), or to the terminal count of the sync counter (**TC**). The sync to each circuit can also be set to be always on or always off. Each circuit is given a two bit sync mode control which is defined as:

Table 1: SYNC MODES

MODE	SYNC DESCRIPTION
0	“0” (never asserted)
1	SI
2	TC
3	“1” (always)

NOTE: the internal syncs are active high. The **$\overline{\text{SI}}$** input has been inverted to be the active high sync **SI**.

ADDRESS 8: SYNC MODE

BIT	TYPE	NAME	DESCRIPTION
0,1 (LSBs)	R/W	LOAD_RATIO	The resampling ratio load selection
2,3	R/W	RATE_ACC	The rate accumulator sync selection. The rate accumulator in the RLL is initialized when this sync occurs.
4,5	R/W	DELAY_ACC	The delay accumulator sync selection. The delay accumulator is initialized when this sync occurs.
6,7	R/W	OUTPUT_SYNC	The selected sync is inverted and output on the **$\overline{\text{SO}}$** pin. Mode 0 in Table 1 is replaced by the one-shot sync for the output sync selection.

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4.5 COUNTER MODE REGISTER

This register controls the sync counter and the diagnostic input mode.

ADDRESS 9: Counter Mode Register

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	**COUNT[0:3]**	The counter length mode. The counter period is set using **COUNT** according to the following table:
4,5	R/W	COUNT_SYNC	The counter is synchronized as follows:
6	R/W	DIAG	Use the 12 LSBs of the counter as input data.
7 (MSB)	R/W	Unused.	

COUNT	PERIOD
0	2^4
1	2^8
3	2^{12}
7	2^{16}
15	2^{20}

COUNT_SYNC	MODE
0	never
1	SI
2	OS (one-shot)
3	always

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4.6 OUTPUT MODE REGISTER

These register sets various output mode controls.

ADDRESS 10: Output Mode Register

BIT	TYPE	NAME	DESCRIPTION
0-1	R/W	FIFO_RESET	The FIFO is reset to half full according to Table 1 in Section 4.4.
2	R/W	BYPASS	Turns off the FIFO so that the data and the data valid flag bypass the FIFO and are output directly from the chip. The OCK pin must be tied to the CK pin in this mode.
3	R/W	Unused	
4	R/W	DVAL_EARLY	Normally the DVAL is active for the clock cycle just before the DO output changes. When this bit is set the DVAL strobe comes out one clock earlier so that it can be used as a clock enable to GRAYCHIP devices which need the clock enable to be active one clock earlier.
5	R/W	DVAL_POL	The DVAL strobe is normally active high. DVAL is active low when DVAL_POL is high.
6,7	R/W	Unused	

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4.7 CLOCK MODE REGISTERS

The clock mode registers control the phase-lock-loop (PLL) and voltage controlled oscillator (VCO) in the output clock generator. NOTE: This register presets to 60 (HEX) upon power up.

ADDRESS 11: Clock Mode register 0

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	RING_LENGTH	This four bit value, if the FORCE_LENGTH bit is set, sets the length of the inverter chain used in the VCO. The longer the chain, the slower the VCO frequency.
4-7	R/W	RING_DIVIDE	This four bit value, if the FORCE_DIVIDE bit is set, sets the power-of-two divide of the VCO output. The larger the divide, the slower the clock output.

ADDRESS 12: Clock Mode register 1

BIT	TYPE	NAME	DESCRIPTION
0	R/W	EXTENDED_RANGE	This bit puts the VCO in the extended PLL range mode. This doubles the pull range of the VCO at the expense of some additional clock jitter.
1	R/W	FORCE_LENGTH	This bit forces the length of the VCO inverter chain to RING_LENGTH.
2	R/W	FORCE_DIVIDE	This bit forces the divide of the VCO output to RING_DIVIDE.
3	R/W	VCO_TEST	This bit puts the ring oscillator in a test mode by breaking the ring of inverters and using the OCK clock input as the first stage of the oscillator.
4	R/W	DIVIDE_TEST	This bit shortens the divider from 16 stages to 8 stages for test purposes.
5	R/W	PLL_RESET	This bit forces the PLL to be in the reset state ready for a new acquisition cycle. In the reset state the VCO control voltage is forced to its middle setting, the ring divider (FORCE_DIVIDE must be off) is forced to maximum, and the ring length (FORCE_LENGTH must be off) is set to 8. The PLL will adapt to the resampler's output data rate when PLL_RESET is cleared and VCO_ENABLE is set.
6	R/W	VCO_ENABLE	This bit turns on the VCO. The output clock is cleared when this bit is low.
7	R/W	CK2X_ENABLE	Turns on the 2X clock output.

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4.8 STATUS CONTROL REGISTER

This register contains miscellaneous control and status information.

ADDRESS 13: Status Control Register

BIT	TYPE	NAME	DESCRIPTION
0,1	R/W	STATUS_SELECT	Sets the mode of the STATUS registers as follows: STATUS_SELECT — MODE 0 — Read ratio 1 — Read FIFO status 2 — Read PLL status 3 — Read checksum
2	R/W	RATIO_HOLD	The ratio register tracks the value of the resampler ratio when this bit is low and holds the last value when this bit is high.
3	R/W	MULTI_MODE	This control bit turns on the multi-chip synchronization logic.
4	R/W	EXT_ERR_MODE	Use the external error signals EIN and EVAL instead of the FIFO error to update the rate-lock-loop.
5	R/W	ONE_SHOT	A one-shot strobe is generated each time this bit is set high. The bit must be cleared before another one-shot strobe can be generated.
6,7	R/W	POWER_DOWN	This two bit field controls the power down and keep alive circuit as follows: POWER_DOWN — MODE 0 — Clock loss detect mode 1,3 — Power down mode (reset) 2 — Disabled The power_down bits default to 0 (clock loss detect mode) upon power up.

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4.9 STATUS REGISTERS

These registers allow the user to read the status information selected by STATUS_SELECT.

4.9.1 READ RATIO

If STATUS_SELECT is 0 the current resampling ratio is read (see the RATIO_HOLD bit in Section 4.8 and the diagram in Figure 2.)

ADDRESS 14: Status Register 0, STATUS_SELECT=0

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**RATIO**[0:7]	Lower byte of the ratio

ADDRESS 15: Status Register 1, STATUS_SELECT=0

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**RATIO**[8:15]	Upper byte of the ratio

4.9.2 READ FIFO STATUS

If STATUS_SELECT is 1 the FIFO status is read from address 14. Address 15 is unused.

ADDRESS 14: Status Register 0, STATUS_SELECT=1

BIT	TYPE	NAME	DESCRIPTION
0-3	R	**DEPTH**[0:3]	The FIFO depth. See Section 2.7.1 for the gray scale encoding of these bits.
4	R	EMPTY	The FIFO is empty when this bit is high
5	R	HALF_FULL	The FIFO is more than half full when this bit is high
6	R	FULL	The FIFO is full when this bit is high
7	R	unused	grounded

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4.9.3 READ PLL STATUS

If STATUS_SELECT is 2 the PLL status is read from addresses 14 and 15.

ADDRESS 14: Status Register 0, STATUS_SELECT=2

BIT	TYPE	NAME	DESCRIPTION
0-3	R	**LENGTH**[0:3]	The current VCO length setting.
4-7	R	**DIVIDE**[0:3]	The current VCO divide setting.

ADDRESS 15: Status Register 1, STATUS_SELECT=2

BIT	TYPE	NAME	DESCRIPTION
0-3	R	**STATE**[0:3]	The current PLL acquisition state. Zero is reset and 15 is acquired.
4	R	BUSY	This bit is high when acquisition is in progress or has not started. This bit is forced low if the FORCE_LENGTH and FORCE_DIVIDE bits are both high.
5	R	LOCK	Indicates that the PLL is in a lock state.
6,7	R	LOCK_STATE[0:1]	Indicates the lock state. During acquisition the state is zero. After acquisition 0 means the PLL is in lock. One means that the FIFO is too empty and the VCO control voltage needs to be decreased (slows the VCO). A two means that the FIFO is too full and the VCO control voltage needs to be increased.

4.9.4 READ CHECKSUM

If STATUS_SELECT is 3 the checksum is read from addresses 14 and the keepalive clock status is read from 15. Address 15 is only used for test purposes.

ADDRESS 14: Status Register 0, STATUS_SELECT=3

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**CHECKSUM**[0:7]	The checksum (See Section 2.10).

ADDRESS 15: Status Register 1, STATUS_SELECT=3

BIT	TYPE	NAME	DESCRIPTION
0	R	NO_IN_CK	Input clock loss detected.
1	R	PD_IN	Input power down mode.
2	R	NO_OUT_CK	Input clock loss detected
3	R	PD_OUT	Output power down mode.
4-7	R	unused	

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5.0 SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 2: Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	-0.3	4.0	V	
Input voltage (undershoot and overshoot)	V_{IN}	-0.7	V_{CC}+0.7	V	
Storage Temperature	T_{STG}	-65	150	^{o}C	
Lead Soldering Temperature (10 seconds)			300	^{o}C	
Clock Rate	F_{CK}	1		KHz	1

Notes:

1. Below 1 KHz the clock loss detect circuit may power down the chip. If the clock loss detect circuit is disabled (13, bits 6 and 7) and the clock is stopped, the chip may draw up to one Amp of power supply current for approximately 10 seconds. After 10 seconds the current will go down to below 50 mAmps.

5.2 RECOMMENDED OPERATING CONDITIONS

Table 3: Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	3.0	3.6	V	
Temperature Ambient, no air flow	T_A	-40	+85	^{o}C	1
Junction Temperature	T_J		125	^{o}C	1

Notes:

1. Thermal management is required to keep T_J below MAX for full rate operation. See Table 3 below.

5.3 THERMAL CHARACTERISTICS

Table 4: Thermal Data

THERMAL CONDUCTIVITY	SYMBOL	GC3011A-PQ	UNITS
		0.5 Watts	
Theta Junction to Ambient	θja	30	^{o}C/W
Theta Junction to Case	θjc	10	^{o}C/W

Note: Air flow will reduce θ**ja** and is highly recommended.

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5.4 DC CHARACTERISTICS

All parameters are industrial temperature range of 0 to 85 ^{o}C ambient unless noted.:

Table 5: DC Operating Conditions

PARAMETER	SYMBOL	Vcc = 3.3V		UNITS	NOTES
		MIN	MAX		
Voltage input low	V_{IL}		0.8	V	1
Voltage input high	V_{IH}	2.0		V	2
Input current (V_{IN} = 0V)	I_{IN}	Typical +/- 50		uA	2
Voltage output low (I_{OL} = 2mA)	V_{OL}		0.5	V	2
Voltage output high (I_{OH} = -2mA)	V_{OH}	2.4	3.3	V	2
Data input capacitance (All inputs except **CK** and **C[0:7]**)	C_{IN}	Typical 4		pF	1
Clock input capacitance (**CK** input)	C_{CK}	Typical 10		pF	1
Control data capacitance (**C[0:7]** I/O pins)	C_{CON}	Typical 6		pF	1

Notes:

1. Controlled by design and process and not directly tested. Verified on initial parts evaluation.
2. Each part is tested at 85^{o}C for the given specification.

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5.5 AC CHARACTERISTICS

Table 6: AC Characteristics (0 TO +85^{o}C Ambient, unless noted)

PARAMETER	SYMBOL	3.3V +/- 5%		UNITS	NOTES
		MIN	MAX		
Clock Frequency	F_{CK}	0.01	100	MHz	2, 3, 4
Clock low period (Below V_{IL})	t_{CKL}	4		ns	1
Clock high period (Above V_{IH})	t_{CKH}	4		ns	1
Data setup before **CK** goes high	t_{SU}	2		ns	1
Data hold time after **CK** goes high	t_{HD}	2		ns	1
Data output delay from rising edge of **CK**.	t_{DLY}	1	5	ns	1, 5
Control Setup before $\overline{\textbf{CE}}$ goes low (**A**, **RE, WE** during read, and **A**, **RE, WE** , **C** during write)	t_{CSU}	5		ns	1
Control hold after $\overline{\textbf{CE}}$ goes high (**A**, **RE, WE** during read, and **A**, **RE, WE**, **C** during write)	t_{CHD}	5		ns	1
Control strobe ($\overline{\textbf{CE}}$) pulse width (Write operation)	t_{CSPW}	20		ns	1,6
Control output delay $\overline{\textbf{CE}}$ low to **C** (Read Operation)	t_{CDLY}		20	ns	1,6
Control tristate delay after $\overline{\textbf{CS}}$ goes high	t_{CZ}		5	ns	1
Quiescent supply current (V_{IN}=0 or V_{CC}, F_{CK} = 1KHz)	I_{CCQ}		200	uA	1
Supply current (F_{CK} =100MHz)	I_{CC}		140	mA	1, 7

Notes:

1. Controlled by design and process and not directly tested. Verified on initial part evaluation.
2. Each part is tested at 85 deg C for the given specification.
3. Temperature range is verified by lot sampling.
4. The chip may not operate properly at clock frequencies below MIN and above MAX.
5. Current load is 2ma. Delays are measured from the rising edge of the clock to the output level rising above V_{IH} or Falling below V_{IL}.
6. Capacitive output load is 80pf.
7. Current changes linearly with voltage and clock speed. Icc (MAX) $= \left(\frac{VCC}{3.3V}\right)\left(\frac{F_{CK}}{100M}\right)140mA$

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6.0 APPLICATION NOTES

6.1 POWER AND GROUND CONNECTIONS

The GC3011A chip is a very high performance chip which requires solid power and ground connections to avoid noise on the V_{CC} and GND pins. If possible the GC3011A chip should be mounted on a circuit board with dedicated power and ground planes and with at least two decoupling capacitors (0.01 and 0.1 μf) adjacent to each GC3011A chip. If dedicated power and ground planes are not possible, then the user should place decoupling capacitors adjacent to each V_{CC} and GND pair.

IMPORTANT

The GC3011A chip may not operate properly if these power and ground guidelines are violated.

6.2 STATIC SENSITIVE DEVICE

The GC3011A chip is fabricated in a high performance CMOS process which is sensitive to the high voltage transients caused by static electricity. These parts can be permanently damaged by static electricity and should only be handled in static free environments.

6.3 70 MHZ OPERATION

Care must be taken in generating the clock when operating the GC3011A chip at its full 100 MHz clock rate. The user must insure that the clock is above 2 volts for at least 4 nanoseconds and is below 1 volt for at least 4 nanoseconds.

6.4 REDUCED VOLTAGE OPERATION

The power consumed by the GC3011A chip can be greatly reduced by operating the chip at the lowest V_{CC} voltage which will meet the application's timing requirements.

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6.5 SYNCHRONIZING MULTIPLE GC3011A CHIPS

A system containing two or more GC3011A chips will need to be synchronized so that their resampling delays and output FIFOs are locked. This is done using the multi-chip synchronization signals DC[0:11], CV, FOZ, FIZ and M/$\overline{S}$ as described in Section 2.6. A block diagram showing how to configure the chips is shown in Figure 6.

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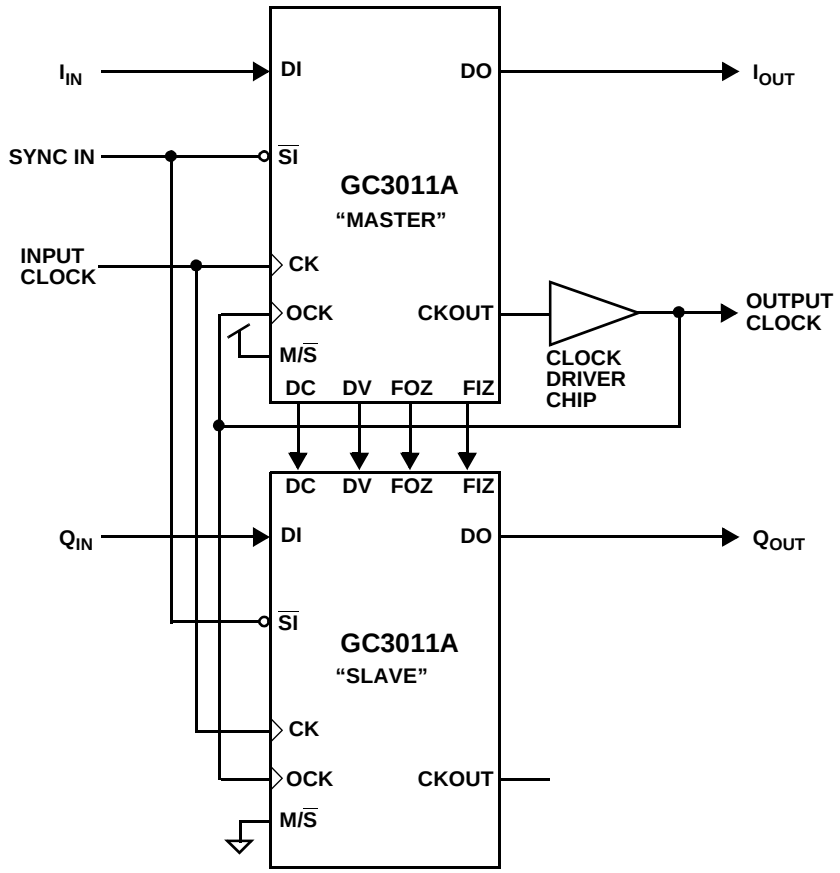


Figure 6. SYNCHRONIZING MULTIPLE GC3011A CHIPS

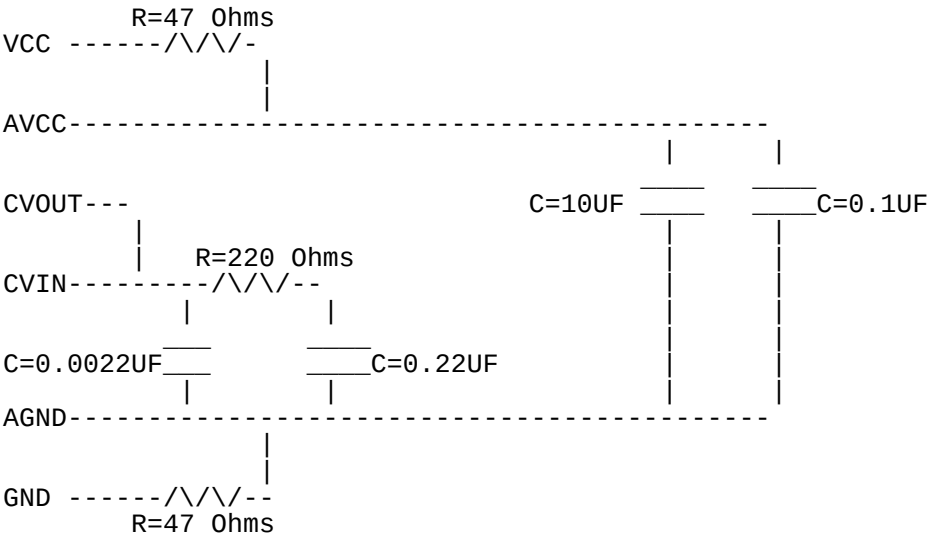
Figure 6 shows how one would configure the chips to resample complex data. The sync input is not necessary unless there are system wide diagnostics which require it.

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6.6 PLL Initialization

This note describes the suggested initialization sequence for locking the PLL/VCO to the desired resampling ratio.

The loop filter must be configured using the R, C1 and C2 components as suggested in the datasheet. A general purpose loop filter can be:



Initially the RLL should be turned off. If it is needed, such as to adapt to baud peak sampling, then it should be enabled after the PLL has adapted to the initial resampling ratio.

RATE_ACC=3 (always load) DELAY_ACC=0 (never sync) OUTPUT_SYNC=0 (one shot, if needed) LOAD_AB=3 (always load) A=B=0 (clear the RLL) COUNT_SYNC=3 (always)

The register settings are: (the slave is a second GC3011 chip which is to be locked to the first)

address	master	slave
0-3	RATIO	0x40000000 (not used in slave)
4-5	0xc000	0xc000 (no offset)
6-7	0xc000	0xc000 (RLL off)
8	0x0f	0x3f (delay acc is not used in slave)
9	0x30	0x30 (counter is not used)
10	0x00	0x00
11	0x00	0x00
12	0x20	0x20 (VCO is disabled at first to clear it)
13	0x02	0x08 (multi-mode in slave)

To start the PLL (only at initialization, or loss of lock, or change of ratio greater than 10% from last PLL initialization):

```
0)      Set register 12 to 0x20 (resets PLL, clears VCO)
1)      Set register 13 to 0x82 (turn off keepalive during acquisition)
2)      Set register 12 to 0x60 (resets PLL, enables VCO)
3)      Wait until register 15 (PLL status) reads 0x10 (almost immediately)
4)      Set register 12 to 0x40 to start acquisition
5)      Wait for register 15, bit 0x10 to go low: 0==(reg15&0x10)
```


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6)      If register 15 equals 0x2f and the lower nibble of register 14 is
        non-zero, then acquisition is complete, go to step 8
7)      If register 15 is not 0x2f, or if the lower 4 bits of register 14
        are 0, then acquisition has failed, go back to step 0.
8)      Set register 13 to 0x02 (enable keepalive).
```

Step 7, acquisition failing, occurs 1% to 10% of the time, and is almost always cleared by repeating steps 0-6.

Once PLL lock is achieved, the RLL can be turned on by writing the desired values into addresses 6 and 7 (with LOAD_AB=3) and then writing 0x03 to address 8. This only applies to the master chip. The RLL circuit is not used in the slave chips.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
GC3011A-PQ	ACTIVE	QFP	PJU	100	66	None	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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