GC2011A

3.3V DIGITAL FILTER CHIP

DATASHEET

March 21, 2000

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REVISION HISTORY

Revision	Date	Description
0.0	3 Feb 1999	Original
1.0	22 Sept, 1999	Preliminary markings removed Section 7: Electrical and timing tables changed to reflect production test Pg 19, Sec 3.7, Table 8, changed Hilbert Transform output register to 2000 Pg 25: added ball grid array package Pg 33: changed the gain equation to reference the MSBs of the input and output.
1.1	21 Mar 2000	Page 25, Rotated marking text on PBGA package Page 35, Snap rate of 2 is invalid Page 39, Changed test load to +/- 2mA from 4mA Page 40, Changed Output delay threshold (Note 4) to 1.3v. Page 40, Changed Data to output MIN delay to 1ns to match test.

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GC2011A DATASHEET

1.0 KEY FEATURES

- Improved 3.3 volt, higher speed, GC2011 replacement
- 106 million samples per second (MSPS) input rate
- Dual inputs for complex, dual path or double rate input processing
- 2's Complement to offset binary conversion
- 12 bit or 24 bit data, 14 bit coefficients
- 8, 10, 12, 14, 16, 20 or 24 bit outputs
- 32 bit internal precision
- 32 multiply-add filter cells
- Snapshot memory for adaptive filtering
- 64 taps with even or odd symmetry
- 128 tap decimate by 2
- 256 tap decimate by 4
- 128 tap interpolate by 2 or 4
- 128 taps for 1/2 rate I/O
- 256 taps for 1/4 rate I/O
- 200 MSPS real to 100 MSPS complex conversion mode
- Real to complex or complex to real conversion modes
- Snapshot memory for adaptive filter update calculations
- Gain adjust in 0.5 dB steps
- Microprocessor interface for control, output, and diagnostics
- Built in diagnostics
- 1.6 Watt at 80 MHz, 3.3 volts
- 160 pin quad flat pack package
- 160 pin ball grid array package

1.1 BLOCK DIAGRAM

A block diagram illustrating the major functions of the chip is shown in Figure 1

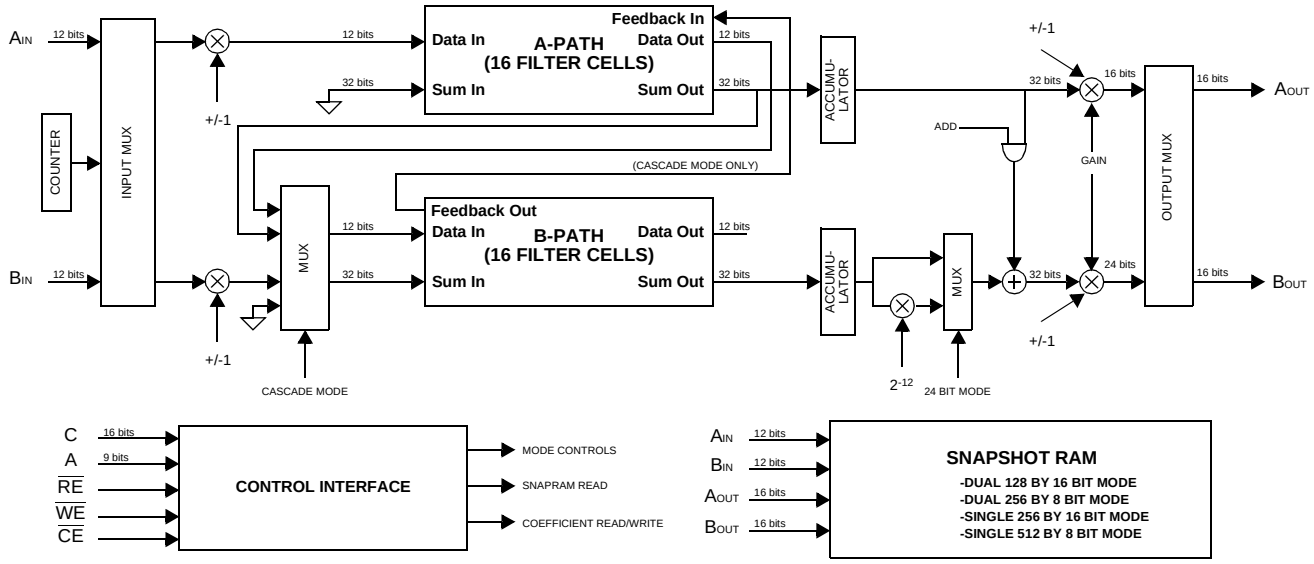


Figure 1. GC2011A Block Diagram

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1.2 GC2011A TO GC2011 COMPARISON

The GC2011A is designed to be a functional and footprint compatible replacement for the GC2011 chip. The timing specifications for the GC2011A meet and exceed the timing specifications for the GC2011. Electrically the GC2011A is a 3.3 volt only part, making it incompatible with the GC2011's 5 volt mode. The GC2011A is fully compatible with the GC2011's 3.3 volt mode, but at a lower power consumption. See Section 7 for timing and electrical specifications. NOTE: The GC2011A inputs are NOT 5 volt tolerant; chip damage may occur if the input voltages exceed Vcc + 0.5V (3.8 volts). Designs using the GC2011 at 5 volts will need to add a 3.3 volt supply and voltage level translators to use the GC2011A.

The function of the GC2011A has been slightly enhanced, but any enhancements are "backward" compatible with the GC2011 so that a GC2011 user will not need to change any software or processing algorithms to use the GC2011A chip. Highlights of the enhancements follow.

1.2.1 Offset Binary Conversion

Digital filter chips are commonly used with analog to digital converters (ADCs) or digital to analog converters (DACs) which often require an offset binary data format rather than the two's complement data format of the GC2011. Offset binary data is easily converted to two's compliment by inverting the most significant bit (MSB) of the data word. The GC2011A has been enhanced to allow conversion between offset binary and two's complement format by optionally inverting the MSB of the input or output data. Four control bits (register address 12) have been added which, when set high, invert the MSBs of the Ain, Bin Aout, and Bout data words. These control bits are cleared at power up so that the GC2011A will power up in the GC2011's two's complement mode.

See Section 6.10 for details.

1.2.2 Clock Loss Detect and Power Down Modes

The GC2011 chip draws excessive current if operated without a clock signal. This is caused by internal dynamic storage nodes being left in an unknown state when the clock is stopped. A clock loss detect circuit has been added to the GC2011A that will put the chip in a fully static mode if the clock has stopped. The fully static mode powers down the chip and reduces the power consumption down to a few microwatts until the clock resumes. The user can also force the power down state if desired. Two control bits (register address 12) are used to control the clock loss detect and power down modes. One control bit turns off the clock loss detect circuit, the other forces the power down mode. Both bits are cleared at power up to keep GC2011 compatibility.

See Section 6.10 for details.

1.2.3 Control Interface

The control interface has been enhanced to use either the R/$\overline{W}$ and $\overline{CS}$ strobes of the original GC2011, or to use the $\overline{RE}$, $\overline{WE}$ and $\overline{CE}$ strobes used by most memory interfaces. If the $\overline{RE}$ pin is grounded, then the interface behaves in the R/$\overline{W}$ and $\overline{CS}$ mode, where the $\overline{WE}$ pin becomes the R/$\overline{W}$ pin and the $\overline{CE}$ pin becomes the $\overline{CS}$ pin. The $\overline{RE}$ pin on the GC2011A chip is a ground pin on the GC2011 chip, so that a GC2011A chip soldered into a GC2011 socket will automatically operate in the GC2011 R/$\overline{W}$ and $\overline{CS}$ mode.

See Section 2.2 for details.

1.2.4 NEW_MODES Control Register

A control register at address 12 has been added to the GC2011A to control the new GC2011A modes. Address 12 was unused in the GC2011 chip so that existing GC2011 control software will not activate the new modes. This control register powers up in the GC2011 compatible mode. See Section 6.10 for details.

1.3 DATASHEET OVERVIEW

This document is organized in 8 Sections:

- Section 2 provides a functional description of the chip.
- Section 3 describes how to configure the chip to implement several commonly used filters.
- Section 4 describes the packaging specifications
- Section 5 describes the I/O signals
- Section 6 describes the control register contents.
- Section 7 describes the specifications.
- Section 8 contains application notes.

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2.0 FUNCTIONAL DESCRIPTION

Fabricated in 0.5 micron CMOS technology, the GC2011A chip is a general purpose digital filter chip with 32 multiply-add filter cells. The chip operates at rates up to 106 MHz. The input data size is 12 bits and the coefficient data size is 14 bits. The output data size is 8, 10, 12, 14, 16, 20 or 24 bits. The 32 multiply-add cells can be arranged as a 32 tap arbitrary phase filter or a 64 tap linear phase filter with even or odd symmetry.

Decimation and interpolation modes double or quadruple the number of taps in the filter.

Two input ports allow the 32 filter cells to be shared between two data paths in order to process two signals or to process complex data. Each path becomes a 16 tap arbitrary phase filter, a 32 tap symmetric filter, a 64 tap decimate by 2 filter or a 128 tap decimate by 4 filter.

Coefficient double buffering and clock synchronization logic permits the user to switch between coefficient sets without causing any undesirable transients in the filter's operation.

Complex coefficients can be handled using an add/subtract cell which combines the two data paths. A complex data by complex coefficient filter requires two chips, one for the I output and one for the Q output. The number of complex taps varies from 16 to 128 depending upon the symmetry and desired I/O rate.

The input data rate can be equal to the clock rate, half the clock rate or a quarter of the clock rate. The effective number of taps doubles for half rate data and quadruples for quarter rate data. The input data rate can be extended to 212 MHz if two chips are used. With two chips the filter size is 32 taps arbitrary phase or 64 taps linear phase. If decimation by two is desired, then only one chip is required and the filter size is 64 taps.

A single chip can be used to convert data between real and complex formats. When converting from real to complex the chip mixes the signal down by $F_S/4$ and lowpass filters the results. To convert from complex to real the chip interpolates the signal by two, mixes it up by $F_S/4$ and outputs the real part of the result.

The two 12 bit data paths can be used to process 24 bit input data by filtering the upper 12 bits in one path and the lower 12 bits in the other. A 12 bit shift and add circuit merges the results into a 24 bit output.

The chip includes a snapshot memory which can capture blocks of input or output data. The size of the snapshot can be programmed to be two 128 sample by 16 bit snapshots, two 256 sample by 8 bit snapshots, one 256 sample by 16 bit snapshot, or one 512 sample by 8 bit snapshot. These samples can be read by an external processor and used for adaptive updates of the filter coefficients.

The internal data precision is 32 bits, sufficient to preserve the full multiplier products and to prevent overflow in the filter's adder tree. The 32 bit results are passed through a gain circuit before they are rounded to 8, 10, 12, 14, or 16 bits. The gain circuit can adjust the signal's amplitude over a 96 dB range in 0.5 dB steps.

On chip diagnostic circuits are provided to simplify system debug and maintenance.

The chip receives configuration and control information over a microprocessor compatible bus consisting of a 16 bit data I/O port, a 9 bit address port, a read/$\overline{\text{write}}$ bit, and a control select strobe. The control registers, coefficient registers, and snapshot memory are memory mapped into the 512 word address space of the control port.

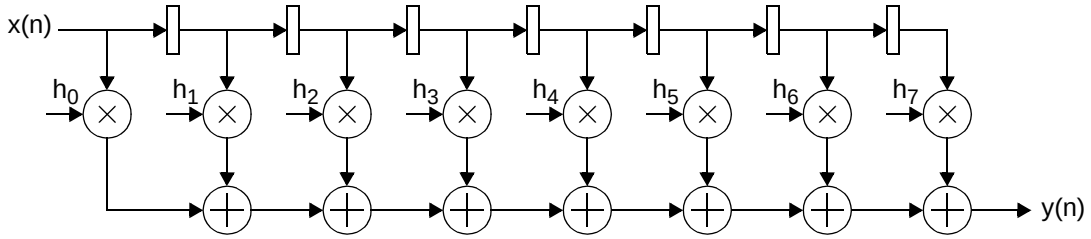
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2.1 TRANSVERSAL FILTERS

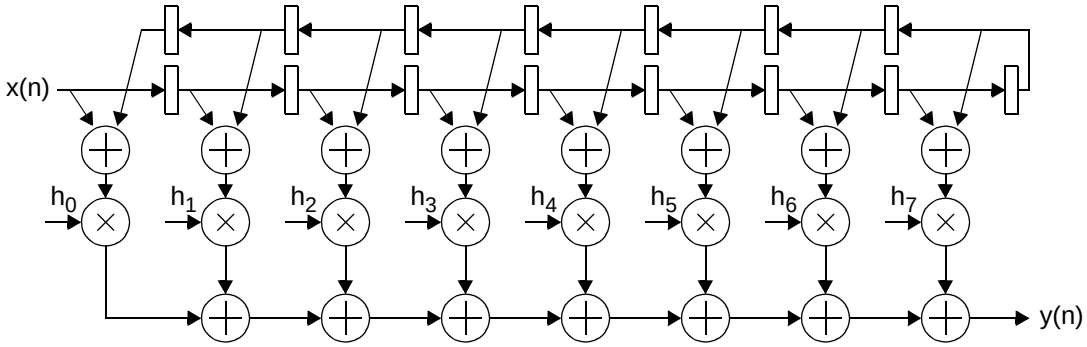
The chip implements finite impulse response (FIR) transversal filters defined by Equation (1):

$$y(n) = \sum_{k=0}^{N-1} h(k)x(n-k) \qquad \text{Eq. (1)}$$

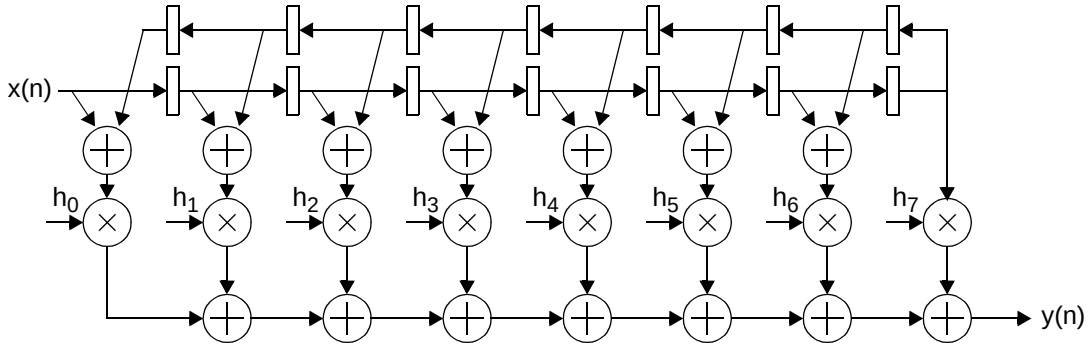
where x(n) is the input sample at time n, y(n) is the output sample at time n, N is the number of taps in the filter and h(k) are the filter coefficients. Many common filters are symmetric, meaning the tap coefficients are symmetric about the center tap. For example, the 16 coefficients (1, 2, 3, 4, 5, 6, 7, 8, 8, 7, 6, 5, 4, 3, 2, 1) have even-length symmetry. The 15 coefficients (1, 2, 3, 4, 5, 6, 7, 8, 7, 6, 5, 4, 3, 2, 1) have odd-length symmetry. Figure 2 shows the basic transversal filter structure for an 8 tap non-symmetric filter, a 16 tap even symmetry filter and a 15 tap odd symmetry filter (actual GC2011A filter sizes are up to 256 taps).



(a) 8 TAP NON-SYMMETRIC FILTER



(b) 16 TAP EVEN SYMMETRY FILTER



(c) 15 TAP ODD SYMMETRY FILTER

Figure 2. Basic Transversal Filters

The GC2011A chip implements the transversal filter structures shown in Figure 2 with the addition of pipeline delays to increase the maximum clock rate of the chip. The pipeline delays add latency to the chip but do not effect its operation.

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2.2 CONTROL INTERFACE

The control interface performs five major functions: It allows an external processor to configure the chip, it allows an external processor to load the filter coefficients, it allows an external processor to capture and read samples from the chip, it allows an external processor to perform diagnostics, and it generates a one-shot synchronization strobe.

The chip is configured by writing control information into 16 bit control registers within the chip. The contents of these control registers and how to use them are described in Section 6. The registers are written to or read from using the **C[0:15]**, **A[0:8]**, $\overline{\textbf{CE}}$, $\overline{\textbf{RE}}$ and $\overline{\textbf{WE}}$ pins. Each control register has been assigned a unique address within the chip. This interface is designed to allow the GC2011A to appear to an external processor as a memory mapped peripheral (the pin $\overline{\textbf{RE}}$ is equivalent to a memory chip's $\overline{\textbf{OE}}$ pin).

The chip's control address space is divided into thirteen control registers, 128 coefficient registers, and 256 snapshot memory words. The thirteen control registers are APATH_REG0, APATH_REG1, BPATH_REG0, BPATH_REG1, CASCADE_REG, COUNTER_REG, OUTPUT_REG, SNAP_REGA, SNAP_REGB, SNAP_START_REG,ONE_SHOT, and NEW_MODES. The control registers are mapped to addresses 0 to 12. See Section 6.0 for details about the contents of these registers.

The 128 filter coefficients are stored in 128 read/write registers which are accessed using addresses 128 through 255. There are 4 filter coefficients stored per filter cell. Addresses 128+4K, 128+4K+1, 128+4K+2 and 128+4K+3 are the four coefficient registers for filter cell K, where K ranges from 0 to 31. Filter cells 0 to 15 are in path-A and filter cells 16 to 31 are in path-B.

The contents of the snapshot memory are accessed using addresses 256 through 511.

Address 11 is used to generate a one-shot pulse. This pulse, $\overline{\textbf{OS}}$, which is one clock cycle wide, can be output from the chip on the $\overline{\textbf{SO}}$ pin.

An external processor (a microprocessor, computer, or DSP chip) can write into a register by setting **A[0:8]** to the desired register address, selecting the chip using the $\overline{\textbf{CE}}$ pin, setting **C[0:15]** to the desired value and then pulsing $\overline{\textbf{WE}}$ low. The data will be written into the selected register when both $\overline{\textbf{WE}}$ and $\overline{\textbf{CE}}$ are low and will be held when either signal goes high.

To read from a control register the processor must set **A[0:8]** to the desired address, select the chip with the $\overline{\textbf{CE}}$ pin, and then set $\overline{\textbf{RE}}$ low. The chip will then drive **C[0:15]** with the contents of the selected register. After the processor has read the value from **C[0:15]** it should set $\overline{\textbf{RE}}$ and $\overline{\textbf{CE}}$ high. The **C[0:15]** pins are turned off (high impedance) whenever $\overline{\textbf{CE}}$ or $\overline{\textbf{RE}}$ are high or when $\overline{\textbf{WE}}$ is low. The chip will only drive these pins when both $\overline{\textbf{CE}}$ and $\overline{\textbf{RE}}$ are low and $\overline{\textbf{WE}}$ is high.

One can also ground the $\overline{\textbf{RE}}$ pin and use the $\overline{\textbf{WE}}$ pin as a read/write direction control and use the $\overline{\textbf{CE}}$ pin as a control I/O strobe. This mode is equivalent to the GC2011 control interface.

Figure 3 shows timing diagrams illustrating both I/O modes.

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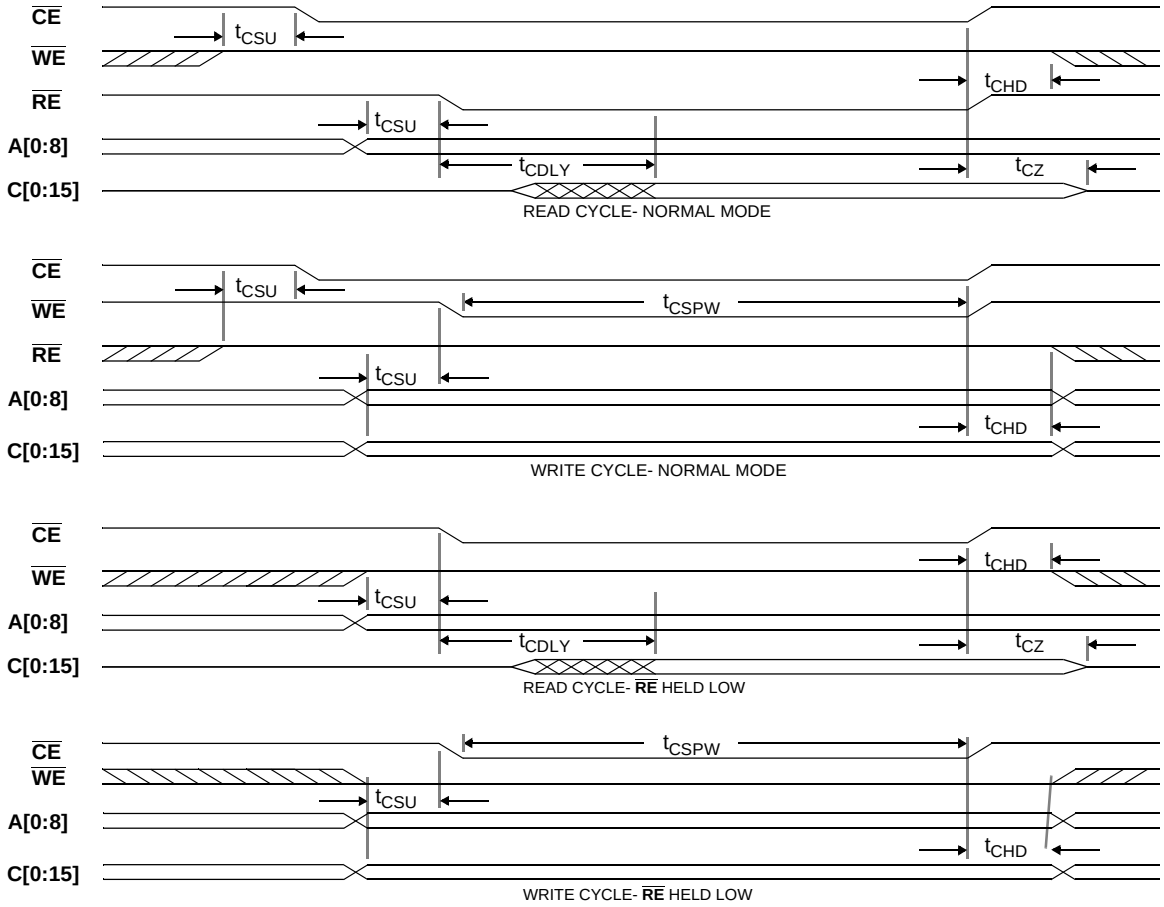


Figure 3. Control I/O Timing

The setup, hold and pulse width requirements for control read or write operations are given in Section 7.

IMPORTANT: Care should be taken to insure that the control data is stable during the write cycle and meets the T_{CSU} and T_{CHD} setup and hold requirements. If the data changes during the write cycle, then control modes may momentarily change, adversely effecting the chip's operation.

2.3 COUNTER AND SYNCHRONIZATION CIRCUIT

The chip contains a 20 bit control counter which is used to synchronize the filter chip's internal controls. The counter is synchronized to the **$\overline{SI}$** sync input pulse, or can be left to free run (see the SS_OFF control bit description in Section 6.8). The period of the counter can be set to 16*(CNT+1) clocks, where CNT ranges from 0 to 65535. The value of CNT is set using the control register COUNTER_REG. The counter counts down from (16*CNT+15) to zero and starts over again. Each time the counter reaches zero it generates a terminal count strobe (**$\overline{TC}$**). The **$\overline{TC}$** pulse can be output on the **$\overline{SO}$** pin or it can be used to trigger the snapshot memory. If the **$\overline{TC}$** pulse is output on the **$\overline{SO}$** pin, then it can be used to synchronize multiple GC2011A chips. Application notes showing the use of this pin are included in Section 8.5.

The least significant 3 bits of the counter are used to synchronize the internal operation of the chip. The least significant 12 bits of the counter can be used as diagnostic inputs to the filter paths.

The **$\overline{SO}$** sync output pin can be used to output either **$\overline{SI}$** delayed by 4 clock cycles, the one-shot pulse **$\overline{OS}$**, or the terminal count **$\overline{TC}$**.

2.4 INPUT MUX

The input multiplexor circuit performs three functions: It allows the user to select which data source to use as the input to the two filter paths, it sets the input data rate, and it optionally delays the data. The controls for the input selection, the input rate, and the data delay are independent for the A and B filter paths.

The input circuit allows the user to select either the A-input, the B-input or the 12 LSBs of the counter for the filter path's input. Typically the A-input will feed the A-path and the B-input will feed the B-path. The counter input is selected for diagnostics.

If the input rate is less than the clock rate, as is the case for the interpolation modes, the half rate I/O modes and the quarter rate I/O modes, then the input circuit can be programmed to hold every-other or every-fourth input sample.

The input delay can be set to 0, 1 or 3 clock cycles. These delays are typically set to zero, but are necessary in the real to complex and complex to real conversion modes.

The control and timing information for the input circuit are described in Section 6.1.

2.5 INPUT NEGATION

The data from the input circuit can be optionally negated by the input negate circuit. The input negation circuit allows the user to negate all samples, the even time samples (i.e., every other input), or the odd time samples. This circuit is used to mix the input data down by $F_S/4$ in the real to complex conversion mode.

The input negation controls are described in Section 6.1.

2.6 A/B FILTER PATHS

A block diagram of the 16 cell filter path is shown in Figure 4.

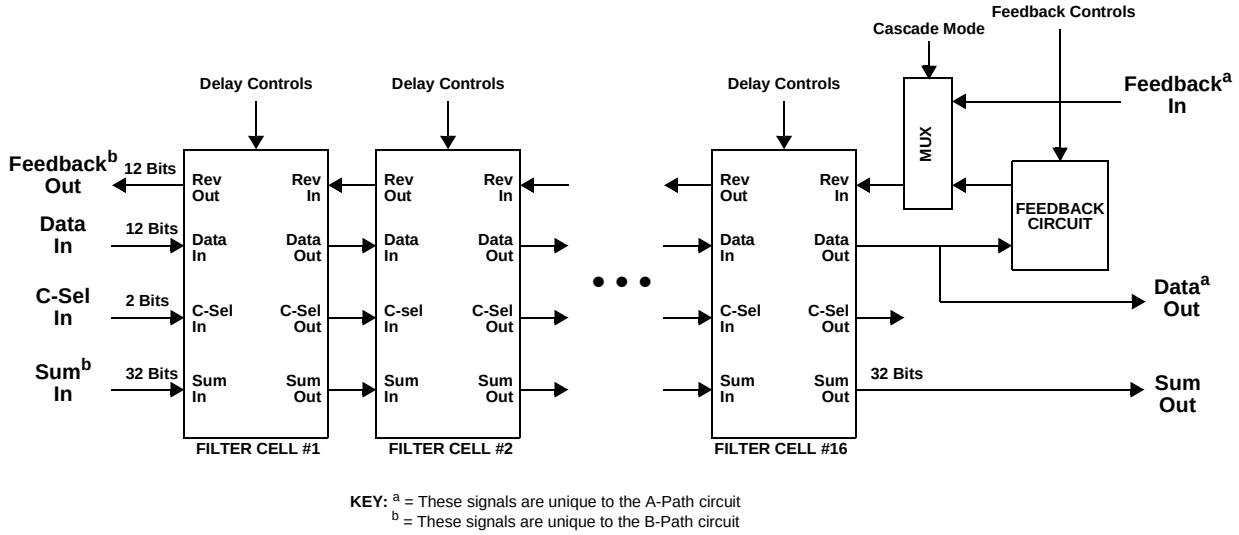


Figure 4. 16 Cell Filter Path Block Diagram

Only the data paths through the filter cells are shown. The coefficient interfaces are not shown. Each filter path contains 16 filter cells and a data feedback circuit. The filter cell contains a multiplier-adder structure described in the next section. The feedback circuit delays and feeds back the data output to provide the reverse data used in the

symmetric filter modes. The feedback circuit will also negate the reverse data, if desired, to implement anti-symmetric filters. In non-symmetric modes the feedback samples are cleared.

There are four filter coefficients stored within each filter cell. The C-Sel signal is a two bit control which selects which coefficient to use at what time. The C-Sel signal can be forced to any value, it can toggle between two coefficients, or can rotate through all four coefficients. The C-Sel signal is synchronized to the LSBs of the control counter when toggling between coefficients.

In the cascade mode the A and B paths are used in series as a single path with 32 filter cells. In this mode the data-out and sum-out outputs of path A are fed into the data-in and sum-in inputs of path B, and the feedback-out of path B is fed into the feedback-in of path A.

The two paths are independent and can be programmed differently, for example path A can be interpolating while path B is decimating.

2.7 FILTER CELL

A block diagram of the filter cell is shown in Figure 5.

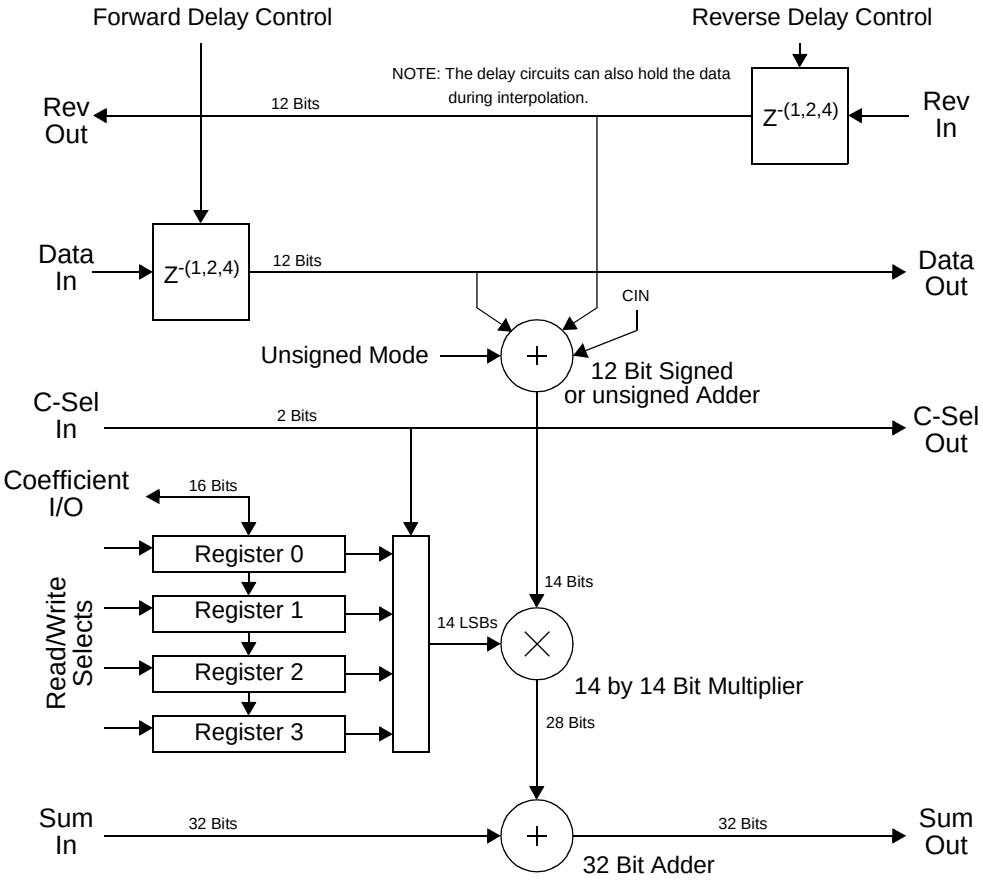


Figure 5. The Filter Cell

The 12 bit forward and reverse data samples are delayed and then passed to the 12 bit adder. The amount of delay depends upon the selected filtering modes. In the normal mode the samples are delayed by one clock. In the decimate by 2 mode the samples are delayed two cycles and in the decimate by four mode the forward samples are

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delayed by four cycles. In the interpolate modes the samples are held for multiple clock cycles rather than delayed. Details of the delay control modes are described in Section 6.1

The 12 bit adder can operate in the signed or unsigned mode. In the signed mode it outputs a 13 bit result which is sign extended to 14 bits. In the unsigned mode it outputs a 14 bit signed result, where the 14th bit (the sign bit) is forced to zero. The 14 bit adder output is multiplied by a 14 bit coefficient selected by the C-Sel control from one of four 16 bit coefficient registers. The 14 bit coefficient is taken from the 14 LSBs of the 16 bit registers.

A 32 bit adder adds the 28 bit multiplier output to the 32 bit sum in data and outputs the result to the next filter cell.

2.8 ACCUMULATOR

The sum output from the filter path is passed to a 32 bit accumulator as shown in Figure 1. The accumulator can be programmed to accumulate blocks of 1, 2 or 4 samples. The accumulator is used to expand the effective length of the filter when the output rate is less than the clock rate. Modes that use the accumulator are the decimation, half rate, and quarter rate modes.

IMPORTANT

The 32 bit accumulator does not guard against overflow. It is the user's responsibility to insure that the filter's gain will not cause overflow. Overflow will not occur if the user restricts the filter coefficients so that the sum of their absolute values is less than 2^{20}. Since the maximum absolute value of any 14 bit coefficient is 2^{13}, this restriction does not affect filters with less than 128 taps. For those filters with lengths greater than 128 taps, which are found in the decimate by 4 and quarter rate modes, this restriction only applies to the hypothetical case where every coefficient is close to full scale.

2.9 24 BIT MUX CIRCUIT

The 24 bit mux circuit is used when filtering 24 bit input data. To use this mode the user splits the 24 bit input data into the upper 12 bits and the lower 12 bits. The upper 12 bits are used as the A-path input and the lower 12 bits are used as the B-path input. The two paths are programmed the same except that the A-path is configured for signed inputs and the B-path is configured for unsigned inputs. The same filter coefficients are loaded into the two paths. The sum outputs from the two paths are then added together by shifting the B-path sum down by 12 bits, rounding the result (using the round-to-even algorithm), and adding it to the A-path output. The 32 bit result is passed through the gain circuit, rounded to 24 bits and output on the A and B output pins. The upper 16 bits of the result are output on the A-out pins and the lower 8 bits are output on the upper 8 bits of the B-out pins.

2.10 SUMMER

The summer circuit is used to add the results from the two paths together. This feature is used in the 24 bit input mode, the double rate modes, and when implementing complex filters. The adder can be converted to a subtracter by using the input negation controls.

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2.11 OUTPUT NEGATION

The output negation control allows every other output sample to be negated. This is used to mix complex data up in frequency by a quarter or half of the output sample rate. This is used primarily when converting complex data to real.

2.12 GAIN

The gain of the filter can be adjusted in 0.5 dB steps using the gain circuit. The 32 bit sum output is multiplied by the gain value $2^S(1+F/16)$ where S and F range from 0 to 15. The result is saturated to plus or minus full scale whenever the product overflows the 32 bit word. The AOF and BOF output bits pulse high for one clock cycle each time an overflow is detected. The output is then rounded to the upper 8, 10, 12, 16, 20 or 24 bits of the result. The lower bits are cleared.

The gain adjustment allows the user to scale the filter coefficients in order to optimize the filter's dynamic range, and then to readjust the overall filter gain using the gain circuit.

2.13 OUTPUT MUX

The output multiplexor circuit formats the gain outputs for output from the chip. In the dual path mode the upper 16 bit of each gain output word are passed to the A-out and B-out pins. If the output data rate is half or quarter rate, then the user can have the A-path and B-path outputs multiplexed onto the A-out pins.

In the cascade or 24 bit modes the B path result can be output as a 24 bit value using a combination of the A-out and B-out pins. In the 24 bit output mode the upper 16 bits are output on the A-out pins and the lower 8 bits are output on the upper 8 B-out pins.

2.14 SNAPSHOT MEMORY

The snapshot memory is used to capture blocks of input or output samples. The memory can be configured as two independent snapshots, or one longer snapshot. In the dual mode the memory can be configured to capture two 128 word by 16 bit snapshots, or two 256 byte by 8 bit snapshots. In the single mode the memory can be configured to capture a 256 word by 16 bit snapshot, or a 512 byte by 8 bit snapshot.

The snapshot data can come from the A-in, B-in, A-out, or B-out samples. In the dual mode the input selection for the two memories can be made independently. In the 8 bit mode the upper 8 bits of each data source is stored in the snapshot. In the 16 bit mode the 12 bit A-in or B-in samples are stored in the upper 12 bits of the 16 bit snapshot.

The snapshot can be programmed to store every sample, every-other sample, every third sample, or every forth sample. This is useful when the chip's input or output data rate is less than the clock rate.

The snapshot is started by writing configuration information to control registers SNAP_REGA, SNAP_REGB and SNAP_REGC, and then setting the START bit in SNAP_REGC (See Section 6.8). The snapshot then waits for a trigger condition plus an optional delay before starting. The trigger conditions are: start immediately after START is set, trigger on the snapshot sync (**$\overline{\text{SN}}$**) strobe, trigger on the sync input (**$\overline{\text{SI}}$**) strobe, or trigger on the counter's (see Section 2.3) terminal count (**$\overline{\text{TC}}$**) strobe. The delay from trigger can be set to multiples of 128 sample times, where the sample time depends upon the selected data rate. The delay is 128DR, where D is the delay count ranging from 0 to 15 and R is the rate ranging from 1 to 4. The delay setting is useful when there are multiple GC2011A chips running in parallel and the user wishes to capture a longer snapshot. For example, a two chip configuration could capture 1024 samples by setting up one chip to capture samples 0 to 511 and setting up the second chip with a delay setting of 512 to capture 512 samples.

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By triggering on the **$\overline{\text{TC}}$** strobe the user can guarantee that the snapshots are spaced by a known number of samples. For example, the user can program the chip to capture blocks of 512 samples every 2^{20} clocks. The blocks can then be coherently combined to calculate accurate spectral information.

Once the snapshot has been triggered, the chip clears the START control bit. When the snapshot is finished the chip will set the A_DONE or B_DONE bits in SNAP_REGC. NOTE that the delay from START being cleared to the DONE bits being set can be up to 8192 clocks when the rate is every fourth clock and the trigger delay is set to 15.

The user accesses the snapshot as 256 16 bit words using addresses 256 to 511 in the chip's control address space. If the samples were stored as bytes, the results can either be read as two byte words, or be read as sign extended bytes. If the user is reading bytes, then a control bit is used to select the upper or lower byte. The snapshot memory is read-only by the user.

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3.0 FILTERING MODES

This Section describes common filtering modes and how to configure the chip to implement them. Unless otherwise indicated, only the A-path, B-path and cascade mode control register values are given. The counter, gain, output, and snapram control registers can be given the default values listed in Table 1 below.

Table 1: Default Control Register Settings

REGISTER	DEFAULT	COMMENT
COUNTER	0	Don't care
GAIN	1030	See Section 6.5
OUTPUT	0	See Section 6.6
SNAP_REGA	0	See Sections 6.7 and 6.8 to configure the snapshot memory
SNAP_REGB	0	
SNAP_REGC	0	

The default settings configure the chip to:

- Use the A-in pins for the cascaded mode data input and the B-out pins for the cascaded mode data output. The cascaded mode results can be output on the A-out pins by setting the OUTPUT register to 0008_{HEX}.
- Round the outputs to 16 bits.
- Give an input to output gain of $2^{-13}\sum h(k)$

The input to output latency is given for each of the modes. The latency is due to pipeline delays and is defined as the delay from x_0 (see Figure 6-a) to the first filter output affected by x_0. One can measure this delay by clearing all of the filter taps except for the first tap and using an impulse as the data input. The latency is then defined as the delay in clock cycles (not data samples) from the impulse in to the impulse out

The modes described in this Section have been configured so that the input and output timing is as shown in Figure 6. In the half rate and quarter rate modes the inputs must be synchronized with **$\overline{\text{SI}}$** as shown. The output timing shows how the output samples are generated relative to **$\overline{\text{SI}}$**.

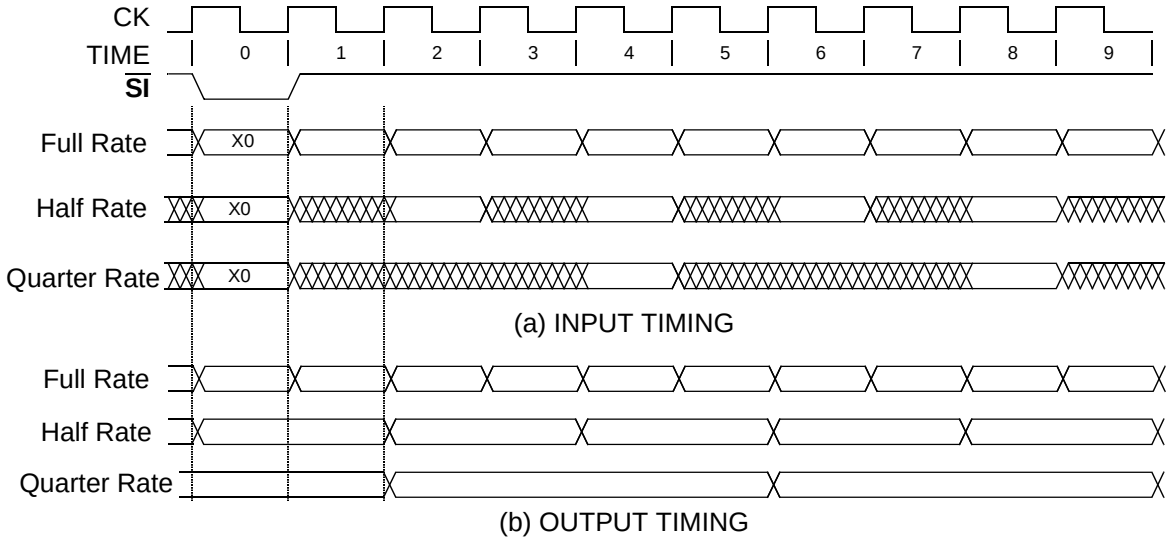


Figure 6. I/O Timing

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3.1 FULL RATE

The full rate filter implements Equation (1) using the structures shown in Figure 2. The control register settings which configure the chip in the full rate modes are tabulated below:

Table 2: Full Rate Mode Control Register Settings

Symmetry	Dual Path or Cascaded	# of Taps (N)	A-PATH		B-PATH		Cascade	Latency
			REG0	REG1	REG0	REG1	REG	
None	Dual	16	20D8	6000	00D8	6000	2000	44
	Cascaded	32	20D8	6028	00D8	6000	9E00	60
Even	Dual	32	20D8	6108	00D8	6108	2000	44
	Cascaded	64	20D8	6128	00D8	6108	9E00	60
Odd	Dual	31	20D8	6181	00D8	6181	2000	44
	Cascaded	63	20D8	61A8	00D8	6181	9E00	60

The coefficients can be stored in coefficient register 1 or 3 of each filter cell. Coefficient registers 0 and 2 are not used in the full rate mode. To store coefficients h(k) in register 1 of each filter cell use the memory addresses BASE+4*k+1, where BASE is 128 for A-path or cascaded filters and is 192 for B-path filters, and

k ranges from 0 to N-1 for filters without symmetry,
k ranges from 0 to N/2-1 for filters with even symmetry, or
k ranges from 0 to (N-1)/2 for filters with odd symmetry.

To store the coefficients in register 3 of each filter cell use the addresses BASE+4*k+3.

The control register settings in Table 2 assume the coefficients are stored in coefficient register 1 of each filter cell. To use register 3 in each cell add 0020_{HEX} to the REG0 values shown in Table 1. The coefficient access logic within each filter cell is synchronized to the clock (**CK**) so that the user can switch between taps stored in register 1 and register 3 without causing any undesirable transients in the filter's operation. This is useful for adaptive filter applications.

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3.2 HALF RATE

The number of taps in the filter can be doubled if the data rate into and out of the chip is one half the clock rate. In this mode each filter cell stores two filter coefficients and performs two tap multiplications per output sample. The cells' delay lines are adjusted so that two feed-forward and two feedback data samples are delayed within each filter cell. The accumulator at the end of the filter path sums the products to give the half rate output. The chip is configured in the half rate mode using the control settings shown in Table 3.

Table 3: Half Rate Mode Control Register Settings

Symmetry	Dual Path or Cascaded	# of Taps (N)	A-PATH		B-PATH		Cascade	Latency
			REG0	REG1	REG0	REG1	REG	
None	Dual	32	638B	AE00	438B	AE00	2000	46
	Cascaded	64	638B	AE28	438B	AE00	5E00	62
Even	Dual	64	638B	A218	438B	A218	2000	46
	Cascaded	128	638B	A228	438B	A218	5E00	62
Odd	Dual	63	638B	A294	438B	A294	2000	46
	Cascaded	127	638B	A2A8	438B	A294	5E00	62

The coefficients can be stored in coefficient registers 0 and 1 in each filter cell or registers 2 and 3. To store coefficients h(k) in registers 0 and 1 of each filter cell use memory addresses:

BASE+2*k for k even and
BASE+2*k-1 for k odd.

To use registers 2 and 3 store the coefficients in addresses

BASE+2*k+2 for k even and
BASE+2*k+1 for k odd.

Where BASE is 128 for A-path or cascaded filters, and is 192 for B-path filters.

To switch from using registers 0 and 1 to registers 2 and 3 add 0020_{HEX} to the REG0 values shown in Table 3. Register switching is synchronized by the chip to the clock in order to prevent unwanted transients.

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3.3 QUARTER RATE

The number of taps in the filter can be quadrupled if the data rate into and out of the chip is one quarter the clock rate. In this mode each filter cell stores four filter coefficients and performs two tap multiplications per output sample. The cells' delay lines are adjusted so that four feed-forward and four feedback data samples are delayed within each filter cell. The accumulator at the end of the filter path sums the products to give the quarter rate output. The chip is configured in the quarter rate mode using the control settings shown in Table 4.

Table 4: Quarter Rate Mode Control Register Settings

Symmetry	Dual Path or Cascaded	# of Taps (N)	A-PATH		B-PATH		Cascade	Latency
			REG0	REG1	REG0	REG1	REG	
None	Dual	64	A202	8E00	8202	8E00	2000	50
	Cascaded	128	A202	8E28	8202	8E00	5E00	66
Even	Dual	128	A202	9018	8202	9018	2000	50
	Cascaded	256	A202	9028	8202	9018	5E00	66
Odd	Dual	127	A202	9094	8202	9094	2000	50
	Cascaded	255	A202	90A8	8202	9094	5E00	66

The coefficients are stored in the filter cells using the formula:

Store h(k) in memory address BASE+k.

where BASE is 128 for A-path or cascaded filters and is 192 for B-path filters.

All four coefficients are active within each filter cell so the user can not switch between banks of filter coefficients. To change or update the coefficients in the quarter rate mode, the user should set the SYNC_COEF control bit. When set, this bit synchronizes the control write operation to the data clock in order to prevent any filter transients or "glitches" due to asynchronous coefficient changes. This allows single coefficients to be updated synchronously

3.4 DOUBLE RATE I/O

The chip will filter data samples which are received at twice the clock rate. The user must split the data into two data streams, each at the clock rate, one containing even time samples and one containing odd time samples. The even data stream is then used as the A-in input and the odd data stream is used as the B-in input. Two chips are required to perform the filtering, one for the even time outputs and one for the odd time outputs. The filtered samples are output on the A-out pins of each chip. If the filter is intended to be a decimate by two filter, then only one chip is needed since only the even time output samples need be generated. The double rate mode control register settings are shown in Table 5.

Table 5: Double Rate Mode Control Register Settings

Output	Symmetry	# of Taps (N)	A-PATH		B-PATH		Cascade	Output	Latency
			REG0	REG1	REG0	REG1	REG	REG	
Even Output chip	None	32	60d8	6000	00D8	6000	2000	0048	44
	Odd	63	60d8	6108	00D8	6181	2000	0048	44
Odd Output chip	None	32	00d8	6000	20D8	6000	2000	0048	44
	Odd	63	00d8	6108	20D8	6181	2000	0048	44

The filter coefficients h(k) are stored in addresses:

128+2*k+1 for k even, and

192+2*k-1 for k odd,

where k ranges from 0 to 31. h(31) is the center tap for the odd symmetry filters.

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3.5 DECIMATION

A common filtering operation is to low pass filter the input signal and then to reduce (decimate) its sample rate by a factor of two or four. The sample rate reduction is performed by only calculating every other or every fourth output sample. This allows the number of taps in the filter to be doubled or quadrupled. Table 5 shows the control register settings for the decimation modes.

Table 6: Decimation Mode Control Register Settings

I/O Rates		Symmetry	Dual Path or Cascaded	# of Taps (N)	A-PATH		B-PATH		Cascade	Latency	Tap Storage[a]
In	Out				REG0	REG1	REG0	REG1	REG		
Full	Half	None	Dual	32	208B	2E00	008B	2E00	2000	46	HR
			Cascaded	64	208B	2E28	008B	2E00	5E00	62	
		Even	Dual	64	208B	2E12	008B	2E12	2000	46	
			Cascaded	128	208B	2E28	008B	2E12	5E00	62	
		Odd	Dual	63	208B	2E91	008B	2E91	2000	46	
			Cascaded	127	208B	2EA8	008B	2E91	5E00	62	
	Quarter	None	Dual	64	2002	0200	0002	0200	2000	50	QR
			Cascaded	128	2002	0228	0002	0200	5E00	66	
		Even	Dual	128	2002	0214	0002	0214	2000	50	
			Cascaded	256	2002	0228	0002	0214	5E00	66	
		Odd	Dual	127	2002	0292	0002	0292	2000	50	
			Cascaded	255	2002	02A8	0002	0292	5E00	66	

a. HR = Use half rate coefficient storage as described in Section 3.2.
QR = Use quarter rate storage as described in Section 3.3.

The decimate by two filter coefficients should be designed with a passband between 0 and $F_S/4$ and a stopband from $F_S/4$ to $F_S/2$, where F_S is the input data rate. The decimate by 4 filter (full rate in to quarter rate out) filter should be designed with a passband between 0 and $F_S/8$ and a stopband above $F_S/8$.

The filter coefficients for the decimation modes are stored using the registers described for half rate or quarter rate operation. The decimation modes which result in half rate output samples use the half rate mode coefficient registers as described in Section 3.2. The quarter rate outputs use the quarter rate coefficient storage as described in Section 3.3.

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3.6 INTERPOLATION

Another common filtering application is to increase the signal's sample rate through interpolation. Interpolation is performed by inserting zeros between input samples so as to double or quadruple the sample rate, and then to low pass filter the result. In the interpolation modes the GC2011A chip automatically zero pads the input as it low pass filters the result. The interpolation modes double or quadruple the number of taps implemented by each filter cell. The input sample rate is one half or one fourth the clock rate as shown in Figure 6. The output rate is at the clock rate.

Table 7: Interpolation Mode Control Register Settings

I/O Rates		Symmetry	Dual Path or Cascaded	# of Taps (N)	A-PATH		B-PATH		Cascade	Latency	Tap Storage[a]
In	Out				REG0	REG1	REG0	REG1	REG		
Full	Double	Odd	Dual	63	20D8	6108	20D8	6181	2000	44	DF
Half	Full	None	Dual	32	6388	2E00	4388	2E00	2000	46	HR
			Cascaded	64	6388	2E28	4388	2E00	5E00	62	
		Odd	Dual	63	6388	2E91	4388	2E91	2000	46	
			Cascaded	127	6388	2EA8	4388	2E91	5E00	62	
Quarter	Full	None	Dual	64	A200	0000	8200	0000	2000	46	See Text
			Cascaded	128	A200	0028	9200	0000	5E00	62	

a. HR = Use half rate coefficient storage as described in Section 3.2. DF = Use double to full rate storage in Section 3.8.

In the interpolate by 4 (quarter rate in, full rate out) mode the coefficient storage is reversed within each filter cell. The interpolate by 4 coefficients, h(k), are stored in:

memory address BASE+k+0 if k modulo-4 is 0
memory address BASE+k+2 if k modulo-4 is 1
memory address BASE+k+0 if k modulo-4 is 2
memory address BASE+k-2 if k modulo-4 is 3

where BASE is 128 for A-path or cascaded filters and is 192 for B-path filters. For example,

Coefficient	Memory address
h(0)	128+0
h(1)	128+3
h(2)	128+2
h(3)	128+1
h(4)	128+4
h(5)	128+7
h(6)	128+6
h(7)	128+5
h(8)	128+8
h(9)	128+11
etc.	

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3.7 DHILBERT TRANSFORM FILTERS

A Hilbert transform filter converts real signals to complex signals by passing the signal's positive spectral frequencies and rejecting its negative frequencies. For example, a sinewave of frequency "w" has both the positive frequency component e^{jwt} and the negative frequency component e^{-jwt}. The Hilbert transform of the sinewave will be just the positive component e^{jwt}.

The coefficients for a Hilbert transform can be generated by designing a linear phase low pass filter with a passband from 0 to $F_S/4$ and a stopband from $F_S/4$ to $F_S/2$, where F_S is the signal's sample rate. The low pass filter's impulse response is then mixed up to be centered on $F_S/4$ by multiplying the coefficients by the sequence: (j, -1, -j, 1, j, -1, -j, …).

For example, the coefficients:

$(h_0, h_1, h_2, h_3, h_4, h_5, h_6, h_7, h_6, h_5, h_4, h_3, h_2, h_1, h_0)$

would become:

$(jh_0, -h_1, -jh_2, h_3, jh_4, -h_5, -jh_6, h_7, jh_6, -h_5, -jh_4, h_3, jh_2, -h_1, -jh_0).$

These coefficients then split into the real coefficients:

$(0, -h_1, 0, h_3, 0, -h_5, 0, h_7, 0, -h_5, 0, h_3, 0, -h_1, 0)$

and the imaginary coefficients:

$(h_0, 0, -h_2, 0, h_4, 0, -h_6, 0, h_6, 0, -h_4, 0, h_2, 0, -h_0).$

As seen in this example, the real coefficients of a Hilbert transform filter have odd symmetry with the center tap non-zero and every other tap equal to zero. The imaginary coefficients have negative odd symmetry.

A special, but important, version of the Hilbert transform exists when the filter has half-band symmetry. Half-band symmetry forces all of the real coefficients except the center tap to be zero. The real half filter, for the half-band Hilbert Transform, is, therefore, just a delay line.

The following table shows how to configure the GC2011A chip for the Hilbert Transform. The A-path is used for the real part and the B-path for the imaginary part.

Table 8: Hilbert Transform Mode Control Register Settings

Dual Path or Cascaded	# of Taps (N)	A-PATH		B-PATH		Cascade	Latency
		REG0	REG1	REG0	REG1	REG	
Dual	63	60C8	2E84	20C8	2E78	2000	45

Since the coefficients are symmetric, only 32 of the 63 low pass filter coefficients are stored in the chip. If the low-pass filter coefficients are h(k), for k=0 to 31, where h(31) is the center tap, then coefficient register 0 of each filter cell is loaded as:

```
Store -h(4k)   in memory address 192+8*k for k=0 to 7
Store -h(4k+1) in memory address 128+8*k for k=0 to 7
Store +h(4k+2) in memory address 196+8*k for k=0 to 7
Store +h(4k+3) in memory address 132+8*k for k=0 to 7
```

Note that the odd coefficients are stored in the A-path, and that the even coefficients are stored in the B-path. Also note that every other odd and every other even coefficient are negated. In the half-band Hilbert transform only h(31) will be non-zero in the A-path.

3.8 REAL TO COMPLEX QUADRATURE DOWN CONVERT

The chip can convert from real data to complex data by mixing the data down by $F_S/4$, low pass filtering the result and then decimating by a factor of two. The control register settings for this mode are shown in Table 9. The

Table 9: Real To Complex Conversion Mode Control Register Settings

I/O Rates		Symmetry	# of Taps (N)	A-PATH		B-PATH		Cascade	Latency
In	Out			REG0	REG1	REG0	REG1	REG	
Double	Full	Odd	63	24D8	6108	04D8	6181	2000	44
	Half		127	248B	2E12	048B	2E91	2000	46
	Quarter		255	2402	0214	0402	0292	2000	50
Full	Half		127	6B8B	A218	2B8B	A294	2000	46
Half	Quarter		255	AE02	9018	6E02	9094	2000	50

double rate input mode assumes the even time samples are in the A-path inputs and the odd time samples are the B-path inputs. The real output is the A-out and the imaginary output is the B-out.

The low pass filter coefficients h(k) are stored so that the even coefficients are stored in the A-path filter cells and the odd coefficients are stored in the B-path filter cells. The lowpass filter should be designed to cut off frequencies above $F_S/4$ for the double to full, full to half, or half to quarter modes, where F_S is the input sample rate. The cut off frequencies are $F_S/8$ and $F_S/16$ for the double to half and double to quarter modes, respectfully.

In the double rate in to full rate out mode the coefficients are stored in register 1 of each filter cell. In this mode store h(k) in addresses:

128+2*k+1 for k even, and
192+2*k-1 for k odd,

where k ranges from 0 to 31. h(31) is the center tap.

In the double or full rate in to half rate out modes the coefficients are stored in registers 0 and 1 of each filter cell. In this mode store h(k) in addresses:

128+k for k modulo 4 = 0
192+k-1 for k modulo 4 = 1
128+k-1 for k modulo 4 = 2
192+k-2 for k modulo 4 = 3

where k ranges from 0 to 63. h(63) is the center tap.

In the double or half rate in to quarter rate out modes the coefficients are stored in registers 0, 1, 2 and 3 of each filter cell. In this mode store h(k) in addresses:

128+k/2 for k even
192+(k-1)/2 for k odd

where k ranges from 0 to 127. h(127) is the center tap.

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3.9 COMPLEX TO REAL QUADRATURE UPCONVERT

Complex data can be converted to real data by doubling the sample rate, mixing the data up by $F_S/4$ and saving the real part. The control settings for this mode are shown in Table 9.

Table 10: Complex To Real Conversion Mode Control Register Settings

I/O Rates		Symmetry	# of Taps (N)	A-PATH		B-PATH		Cascade	Output	Latency
In	Out			REG0	REG1	REG0	REG1	REG	REG	
Full	Double	Odd	63	20D8	6108	00D8	6181	2000	0001	44
Half	Full		127	638B	A218	438B	A294	2000	0012	46
Quar-ter	Half		255	A202	9018	8202	9094	2000	0033	50

The filter is an interpolate by two low pass filter with a pass band from 0 to $F_S/4$ and a stop band from $F_S/4$ to $F_S/2$, where F_S is the output sample rate. The even coefficients of the filter are stored in the A-path filter cells and the odd-coefficients are stored in the B-path filter cells. The real half of the complex samples are input as A-in, and the imaginary half are input as B-in. The real results are output as A-out in all modes except for the double rate output mode. In the double rate output mode the even time samples are output as A-out and the odd time samples are output as B-out.

In the full rate in to double rate out mode the coefficients h(k) are stored in register 1 of each filter cell. In this mode store h(k) in addresses:

128+2*k+1 for k even, and
192+2*k-1 for k odd,

where k ranges from 0 to 31. h(31) is the center tap.

In the half rate in to full rate out mode the coefficients are stored in registers 0 and 1 of each filter cell. In this mode store h(k) in addresses:

128+k for k modulo 4 = 0
192+k-1 for k modulo 4 = 1
128+k-1 for k modulo 4 = 2
192+k-2 for k modulo 4 = 3

where k ranges from 0 to 63. h(63) is the center tap.

In the quarter rate in to half rate out mode the coefficients are stored in registers 0, 1, 2 and 3 of each filter cell. In this mode store h(k) in addresses:

128+k/2 for k even
192+(k-1)/2 for k odd

where k ranges from 0 to 127. h(127) is the center tap.

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3.10 DIAGNOSTICS

The user can use the ramp input and the snapshot memory to perform diagnostics on the chip. The suggested diagnostic procedure is to configure the chip as it will be used in normal operation, but to select the ramp as the data input source (see Section 6.1), to set the counter control to $0FFF_{HEX}$ (see Section 6.4), and to set the snapshot controls to capture 128 output samples (see Section 6.7). The snapshot should be triggered on $\overline{\mathbf{TC}}$ with a delay of 4 blocks from trigger. The delay guarantees that the filter has flushed and settled out before the snapshot is taken. The user can then read the snapshot from memory and compare it against a known snapshot or save it for future comparison.

Two suggested diagnostic configurations are given below along with the expected snapshot output. These configurations use all of the coefficient registers and all of the forward and reverse delay storage registers. The diagnostic procedure is, for each test configuration in table 11:

(1) Load the 11 control registers with the values shown in Table 11.

(2) Load the coefficients h(k) in addresses 128+k for k=0 to 127.

(3) Set the start bit in the snapshot register by writing 0413_{HEX} to address 10.

(4) Wait, while reading address 10, until the register value is 0463_{HEX}.

(5) Read addresses 256 through 271 and 384 through 399 and compare them to the expected values in Table 12.

Table 11: Diagnostic Test Configuration

Parameter	Address	Test A	Test B
h(k)	k modulo 4 = 0	EAAA	1555
	k modulo 4 = 1	FFFF	E000
	k modulo 4 = 2	0F0F	F0F0
	k modulo 4 = 3	0001	1FFF
A_PATH_REG0	0	C402	E402
A_PATH_REG1	1	0292	0108
B_PATH_REG0	2	D402	E402
B_PATH_REG1	3	0214	02F2
CASCADE	4	1000	2F00
COUNTER	5	0FFF	0FFF
GAIN	6	1035	103A
OUTPUT	7	0041	0041
SNAP_REGA	8	004E	004F
SNAP_REGB	9	004F	005F
SNAP_REGC	10	0403	0403
NEW_MODES	12	0000	0000

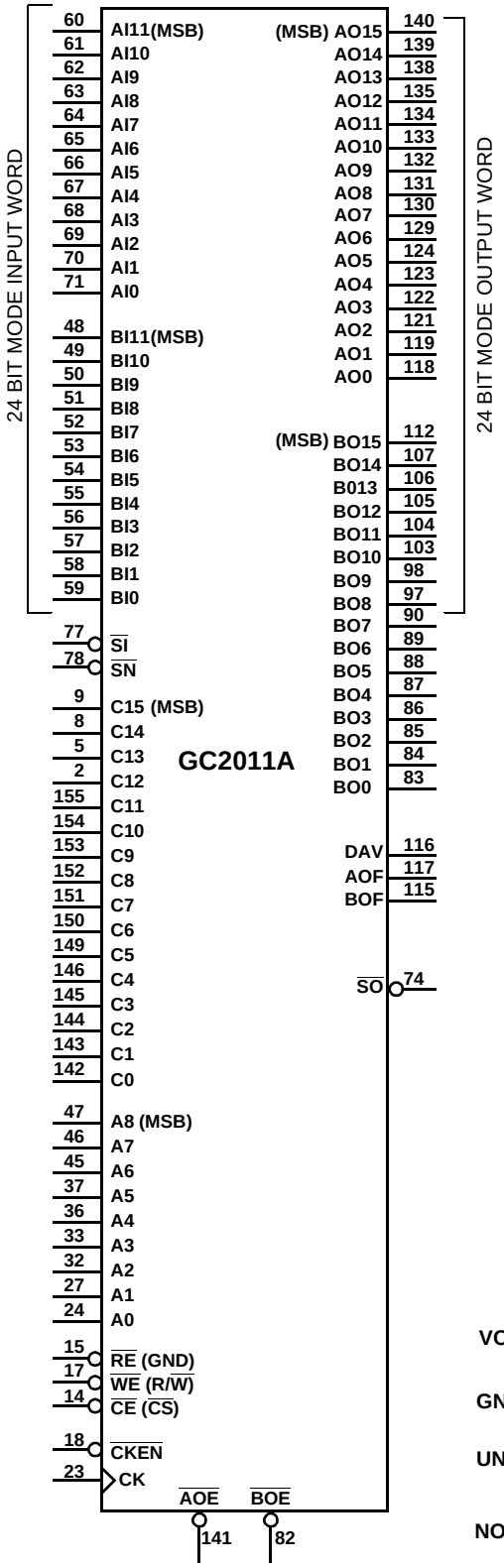
Table 12: Expected Test Results

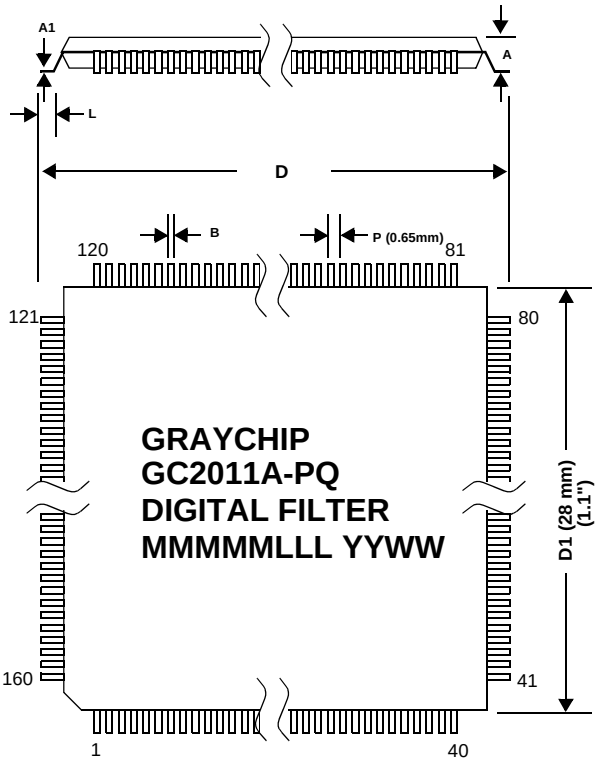
Address	Test A	Test B	Address	Test A	Test B	Address	Test A	Test B	Address	Test A	Test B
256	C302	A635	264	C621	C3D3	384	3BC2	4BAD	392	3CC2	4A33
257	C2E2	A606	265	CA1F	C8BD	385	3BE2	4B7E	393	3CE2	4A04
258	C2C2	A5D7	266	CE1E	CDA6	386	3C02	4B4F	394	3D02	49D4
259	C2A2	A5A8	267	D21D	D290	387	3C22	4B1F	395	3D22	49A5
260	C282	A578	268	D61B	F692	388	3C42	4AF0	396	3D41	4976
261	C262	A549	269	DA1A	0094	389	3C62	4AC1	397	3D61	4947
262	C243	A51A	270	DE19	0A97	390	3C82	4A91	398	3D81	4917
263	C223	A4EA	271	E217	1499	391	3CA2	4A62	399	3DA1	48E8

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4.0 PACKAGING

4.1 160 PIN QUAD FLAT PACK (QFP) PACKAGE





160 PIN QUAD FLAT PACK PACKAGE

GC2011A-PQ = Enhanced Thermal Plastic Package
GC2011A-CQ = Ceramic Package (special order only)

Package Markings: **MMMMM = Mask Code**
LLL = Lot Number
YYWW = Date Code

DIMENSION		PLASTIC	CERAMIC
D	(width pin to pin)	31.2 mm (1.228")	32.0 mm (1.260")
D1	(width body)	28.0 mm (1.102")	28.0 mm (1.102")
P	(pin pitch)	0.65 mm (0.026")	0.65 mm (0.026")
B	(pin width)	0.30 mm (0.012")	0.30 mm (0.012")
L	(leg length)	0.88 mm (0.035")	0.70 mm (0.028")
A	(height)	4.07 mm (0.160")	3.25 mm (0.128")
A1	(pin thickness)	0.17 mm (0.007")	0.2 mm (0.008")

VCC PINS: 3,4,7,12,13,16,21,22,26,30,31,35,38,39,44,75,76,80,91,92,93, 99,100,108,109,113,125,126,136,147,156

GND PINS: 6,10,11,19,20,25,28,29,34,42,43,72,73,79,94,95,96,101,102, 110,111,114,127,128,137,148,157,158,159

UNUSED PINS: 1, 40, 41, 81, 120, 160

NOTE: 0.01 to 0.1 μf DECOUPLING CAPACITORS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE MIDDLE OF EACH SIDE OF THE CHIP

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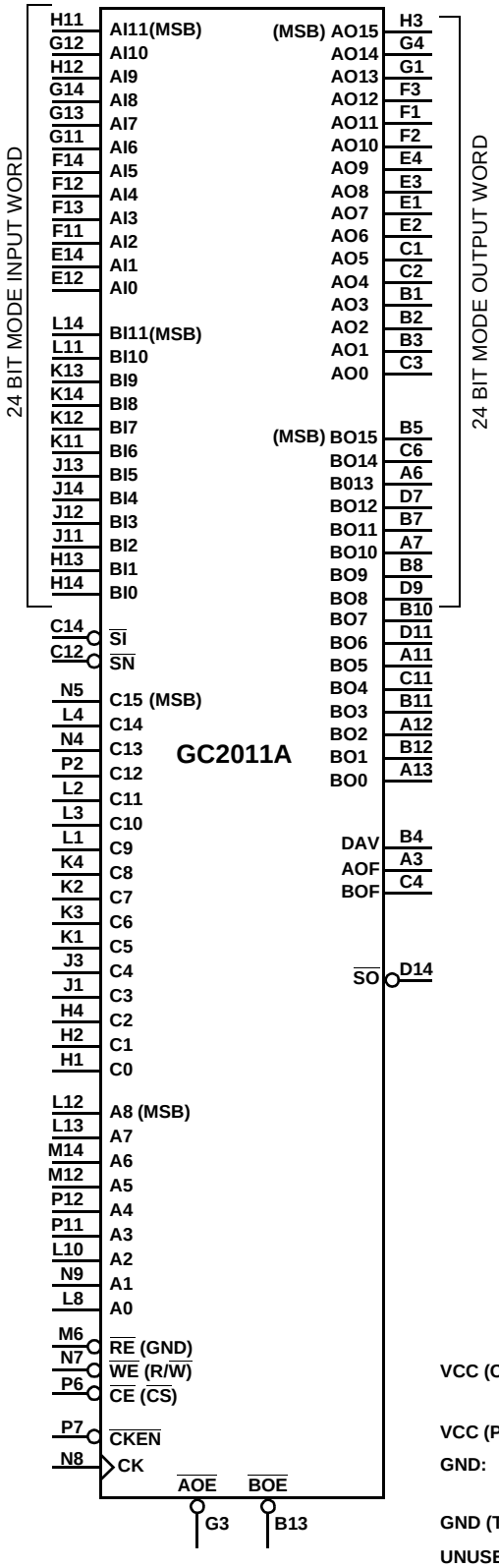
Table 13: Pin Listing For 160 Pin QFP Package

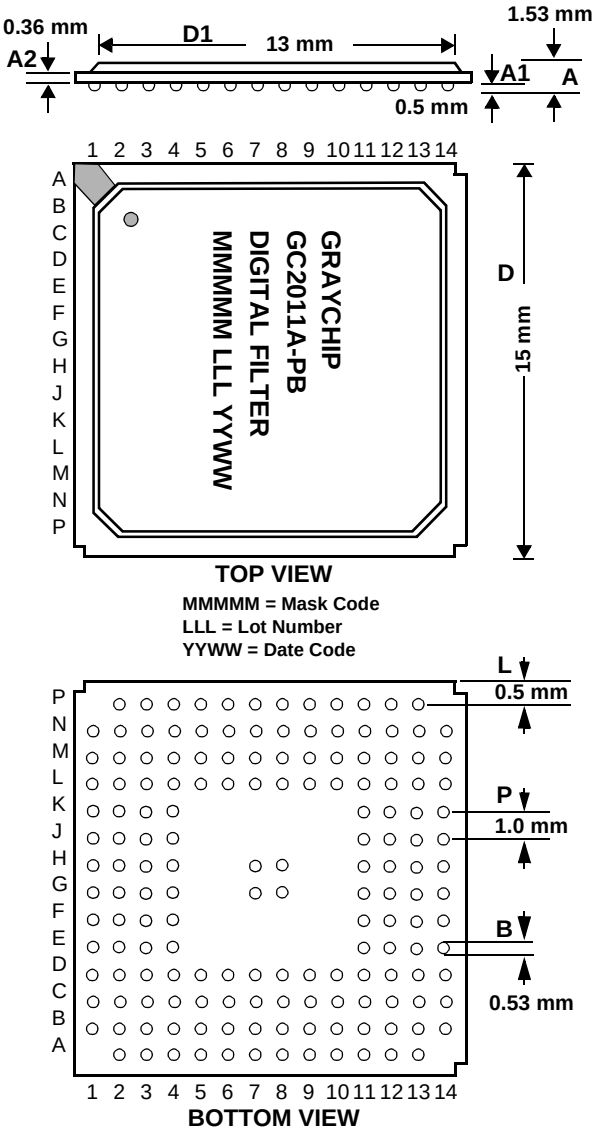
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	-	41	-	81	-	121	AO2
2	C12	42	GND	82	$\overline{BOE}$	122	AO3
3	VCC	43	GND	83	BO0	123	AO4
4	VCC	44	VCC	84	BO1	124	AO5
5	C13	45	A6	85	BO2	125	VCC
6	GND	46	A7	86	BO3	126	VCC
7	VCC	47	A8	87	BO4	127	GND
8	C14	48	BI11	88	BO5	128	GND
9	C15	49	BI10	89	BO6	129	AO6
10	GND	50	BI9	90	BO7	130	AO7
11	GND	51	BI8	91	VCC	131	AO8
12	VCC	52	BI7	92	VCC	132	AO9
13	VCC	53	BI6	93	VCC	133	AO10
14	$\overline{CE}$ ($\overline{CS}$)	54	BI5	94	GND	134	AO11
15	$\overline{RE}$ (GND)	55	BI4	95	GND	135	AO12
16	VCC	56	BI3	96	GND	136	VCC
17	$\overline{WE}$ (R/$\overline{W}$)	57	BI2	97	BO8	137	GND
18	$\overline{CKEN}$	58	BI1	98	BO9	138	AO13
19	GND	59	BI0	99	VCC	139	AO14
20	GND	60	AI11	100	VCC	140	AO15
21	VCC	61	AI10	101	GND	141	$\overline{AOE}$
22	VCC	62	AI9	102	GND	142	C0
23	CK	63	AI8	103	BO10	143	C1
24	A0	64	AI7	104	BO11	144	C2
25	GND	65	AI6	105	BO12	145	C3
26	VCC	66	AI5	106	BO13	146	C4
27	A1	67	AI4	107	BO14	147	VCC
28	GND	68	AI3	108	VCC	148	GND
29	GND	69	AI2	109	VCC	149	C5
30	VCC	70	AI1	110	GND	150	C6
31	VCC	71	AI0	111	GND	151	C7
32	A2	72	GND	112	BO15	152	C8
33	A3	73	GND	113	VCC	153	C9
34	GND	74	$\overline{SO}$	114	GND	154	C10
35	VCC	75	VCC	115	BOF	155	C11
36	A4	76	VCC	116	DAV	156	VCC
37	A5	77	$\overline{SI}$	117	AOF	157	GND
38	VCC	78	$\overline{SN}$	118	AO0	158	GND
39	VCC	79	GND	119	AO1	159	GND
40	-	80	VCC	120	-	160	-

NOTE: The pin names in parenthesis (*) indicate the GC2011 pin names.

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4.2 160 PIN BALL GRID ARRAY (PBGA) PACKAGE





DIMENSION		TYP	TOLERANCE
D	(width body)	15 mm	mm
D1	(width cover)	13 mm	mm
P	(ball pitch)	1.0 mm	mm
B	(ball width)	0.53 mm	mm
L	(overhang)	0.5 mm	mm
A	(overall height)	1.53 mm	mm
A1	(ball height)	0.5 mm	mm
A2	(substrate thickness)	0.36 mm	mm

VCC (CORE): A8, B6, C10, D2, D6, D8, D10, D12, D13, L5, L6, M7, M9, M10, N3, N6, N10, N11, N12, P3, P4, P8, P13

VCC (PAD RING): A10, B14, D3, D5, F4, J2, M1, M13

GND: A5, A9, B9, C5, C7, C8, D4, E11, E13, L7, L9, M2, M4, M5, M8, M11, N1, N13, P5, P9, P10, A4, C9, C13, D1, G2, J4, M3, N14

GND (THERMAL): G7, G8, H7, H8

UNUSED: A2, N2

NOTE: 0.01 to 0.1 μf DECOUPLING CAPACITORS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE MIDDLE OF EACH SIDE OF THE CHIP

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Table 14: Pin Listing For 160 Pin BGA Package (Top View)

	1:	2:	3:	4:	5:	6:	7:	8:	9:	10:	11:	12:	13:	14:
A:		*	AOF	GND	GND	BO13	BO10	CVCC	GND	PVCC	BO5	BO2	BO0	
B:	AO3	AO2	AO1	DAV	BO15	CVCC	BO11	BO9	GND	BO7	BO3	BO1	$\overline{\text{BOE}}$	PVCC
C:	AO5	AO4	AO0	BOF	GND	BO14	GND	GND	GND	CVCC	BO4	$\overline{\text{SN}}$	GND	$\overline{\text{SI}}$
D:	GND	CVCC	PVCC	GND	PVCC	CVCC	BO12	CVCC	BO8	CVCC	BO6	CVCC	CVCC	$\overline{\text{SO}}$
E:	AO7	AO6	AO8	AO9							GND	AI0	GND	AI1
F:	AO11	AO10	AO12	PVCC							AI2	AI4	AI3	AI5
G:	AO13	GND	$\overline{\text{AOE}}$	AO14			TGND	TGND			AI6	AI10	AI7	AI8
H:	C0	C1	AO15	C2			TGND	TGND			AI11	AI9	BI1	BI0
J:	C3	PVCC	C4	GND							BI2	BI3	BI5	BI4
K:	C5	C7	C6	C8							BI6	BI7	BI9	BI8
L:	C9	C11	C10	C14	CVCC	CVCC	GND	A0	GND	A2	BI10	A8	A7	BI11
M:	PVCC	GND	GND	GND	GND	$\overline{\text{RE}}$	CVCC	GND	CVCC	CVCC	GND	A5	PVCC	A6
N:	GND	*	CVCC	C13	C15	CVCC	$\overline{\text{WE}}$	CK	A1	CVCC	CVCC	CVCC	GND	GND
P:		C12	CVCC	CVCC	GND	$\overline{\text{CE}}$	$\overline{\text{CKEN}}$	CVCC	GND	GND	A3	A4	CVCC	

* = unused ball
CVVC = Core VCC
PVCC = Pad VCC
TGND = Thermal Ground

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5.0 PIN DESCRIPTIONS

SIGNAL	DESCRIPTION
AI[0:11]	**A-PATH INPUT DATA.** *Active high* The 12 bit two's complement input samples for path A. New samples are clocked into the chip on the rising edge of the clock.
BI[0:11]	**B-PATH INPUT DATA.** *Active high* The 12 bit two's complement input samples for path B. New samples are clocked into the chip on the rising edge of the clock.
CK	**CLOCK INPUT.** *Active high* The clock input to the chip. The **AI**, **BI**, **$\overline{\text{SI}}$**, **$\overline{\text{SN}}$** and **$\overline{\text{CKEN}}$** signals are clocked into the chip on the rising edge of this clock. The **AO**, **BO**, **DAV**, **AOF**, **BOF** and **$\overline{\text{SO}}$** signals are clocked out on the rising edge of this clock.
$\overline{\text{CKEN}}$	**CLOCK ENABLE INPUT.** *Active low* The clock enable input to the chip. This signal is gated with **CK** to generate the chip's internal clock. **$\overline{\text{CKEN}}$** is clocked into the chip on the rising edge of **CK** and will enable or disable the following clock edge. A low level on **$\overline{\text{CKEN}}$** enables the clock edge.
$\overline{\text{SI}}$	**SYNC INPUT**. *Active low* The sync input to the chip. All timers, accumulators, and control counters are, or can be, synchronized to **$\overline{\text{SI}}$**. This sync is clocked into the chip on the rising edge of the clock.
$\overline{\text{SN}}$	**SNAPSHOT SYNC**. *Active low* The snapshot sync is provided to synchronously start the data snapshot. This signal is clocked into the chip on the rising edge of the clock.
AO[0:15]	**A-PATH OUTPUT DATA**. *Active high* The A-path output samples are output as 16 bit words on these pins. The bits are clocked out on the rising edge of the clock.
BO[0:15]	**B-PATH OUTPUT DATA**. *Active high* The B-path output samples are output as 16 bit words on these pins. The bits are clocked out on the rising edge of the clock.
$\overline{\text{AOE}}$	**A-PATH OUTPUT ENABLE**. *Active low* The **A[0:15]** and AOF output pins are put into a high impedance state when this pin is high.
$\overline{\text{BOE}}$	**B-PATH OUTPUT ENABLE**. *Active low* The **B[0:15]** BOF output pins are put into a high impedance state when this pin is high.
DAV	**DATA VALID STROBE**. *Programmable active high or low level* This strobe is output synchronous with the **A** and **B** data words. The strobe is used in the decimate, half rate, or quarter rate output modes to indicate when the output words are valid. The high/low polarity of the strobe is programmable.
AOF	**A-PATH OVERFLOW** *Active high* This signal goes high for one clock cycle each time there is an overflow in the A-path gain output.
BOF	**B-PATH OVERFLOW** *Active high* This signal goes high for one clock cycle each time there is an overflow in the B-path gain output.
$\overline{\text{SO}}$	**SYNC OUT**. *Active low* This signal is either the input sync **$\overline{\text{SI}}$** delayed by 4 clock cycles, the one shot sync **$\overline{\text{OS}}$**, or the internal counter's terminal count strobe **$\overline{\text{TC}}$**.
C[0:15]	**CONTROL DATA I/O BUS**. *Active high* This is the 16 bit control data I/O bus. Control register contents are loaded into the chip or read from the chip through these pins. The chip will only drive these pins when **$\overline{\text{CE}}$** and **$\overline{\text{RE}}$** are low and **$\overline{\text{WE}}$** is high.
A[0:8]	**CONTROL ADDRESS BUS**. *Active high* These pins are used to address the control registers, coefficient registers, and the snapram memory within the chip.
$\overline{\text{RE}}$, $\overline{\text{WE}}$, $\overline{\text{CE}}$	**READ, WRITE, and CHIP ENABLE STROBES**. *active low* These pins control the reading and writing of control data. If $\overline{\text{RE}}$ is held low the chip will operate in the GC2011 read/write mode, where $\overline{\text{WE}}$ is the GC2011's R/$\overline{\text{W}}$ control and $\overline{\text{CE}}$ is the GC2011's $\overline{\text{CS}}$ control strobe. (See Section 2.2)

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6.0 CONTROL REGISTERS

The chip is configured and controlled through the use of 11 sixteen bit control registers. These registers are accessed for reading or writing using the control bus pins (**$\overline{\text{CE}}$**, **$\overline{\text{RE}}$,** **$\overline{\text{WE}}$**, **A[0:8]**, and **C[0:15]**) described in the previous section. The register names and their addresses are:

ADDRESS	NAME	ADDRESS	NAME
0	APATH_REG0	8	SNAP_REGA
1	APATH_REG1	9	SNAP_REGB
2	BPATH_REG0	10	SNAP_REGC
3	BPATH_REG1	11	ONE_SHOT
4	CASCADE_REG	12	NEW_MODES
5	COUNTER_REG	13 to 127	unused
6	GAIN_REG	128 to 255	Coefficient Registers
7	OUTPUT_REG	256 to 511	Snapram

The following sections describe each of these registers. The type of each register bit is either R or R/W indicating whether the bit is read only or read/write. All bits are active high.

The APATH_REG0, APATH_REG1, BPATH_REG0, BPATH_REG1, CASCADE_REG and OUTPUT_REG control register settings given in Section 3.0 will configure the chip into the most common modes of operation. This Section describes the meanings of the individual register bits used to set up those modes.

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6.1 A-PATH AND B-PATH CONTROL REGISTER 0

Control registers APATH_REG0 and BPATH_REG0 are identical and are described here.

ADDRESS 0: **APATH_REG0**

ADDRESS 2: **BPATH_REG0**

BIT	TYPE	NAME	DESCRIPTION
0,1 (LSBs)	R/W	ACCUM	This two bit field controls the accumulator according to the following table: ACCUM — DESCRIPTION 0,1 — don't accumulate (full rate output) 2 — accumulate 4 sums (quarter rate) 3 — accumulate 2 sums (half rate) The ACCUM control also sets the output data rate as shown in Figure 8.
2	R/W	UNSIGNED	The filter cell adder (See Figure 5) is in the unsigned mode when this bit is set.
3-7	R/W	COEF_SEL	This five bit field controls how the four coefficients are used within the filter cells. The controls are: COEF_SEL (HEX) — DESCRIPTION 1B — use coefficient reg 1 1F — use coefficient reg 3 11 — toggle between registers 0 and 1 15 — toggle between registers 2 and 3 00 — cycle through all four registers
8,9	R/W	RATE	This two bit field sets the input rate as follows: (See Figure 7) RATE — DESCRIPTION 0,1 — full rate input 2 — quarter rate input 3 — half rate input
10-12	R/W	NEG_IN	These three bits control the input sample negation as follows: NEG_IN — DESCRIPTION 0 — don't negate 1 — negate even time full rate samples 2 — negate odd time half rate samples 3 — negate even time quarter rate samples 4 — always negate 5 — negate odd time full rate samples 6 — negate even time half rate samples 7 — negate odd time quarter rate samples where the definition of even and odd time samples is shown in Figure 7.
13	R/W	AB_SEL	Select input A-in when high, B-in when low.
14,15(MSB)	R/W	DELAY_SEL	Selects the input delay or counter input as follows: DELAY_SEL — DESCRIPTION 0 — no delay 1 — one clock delay 2 — 3 clock delay 3 — use counter as input

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The operation of these control bits are illustrated in the following figures.

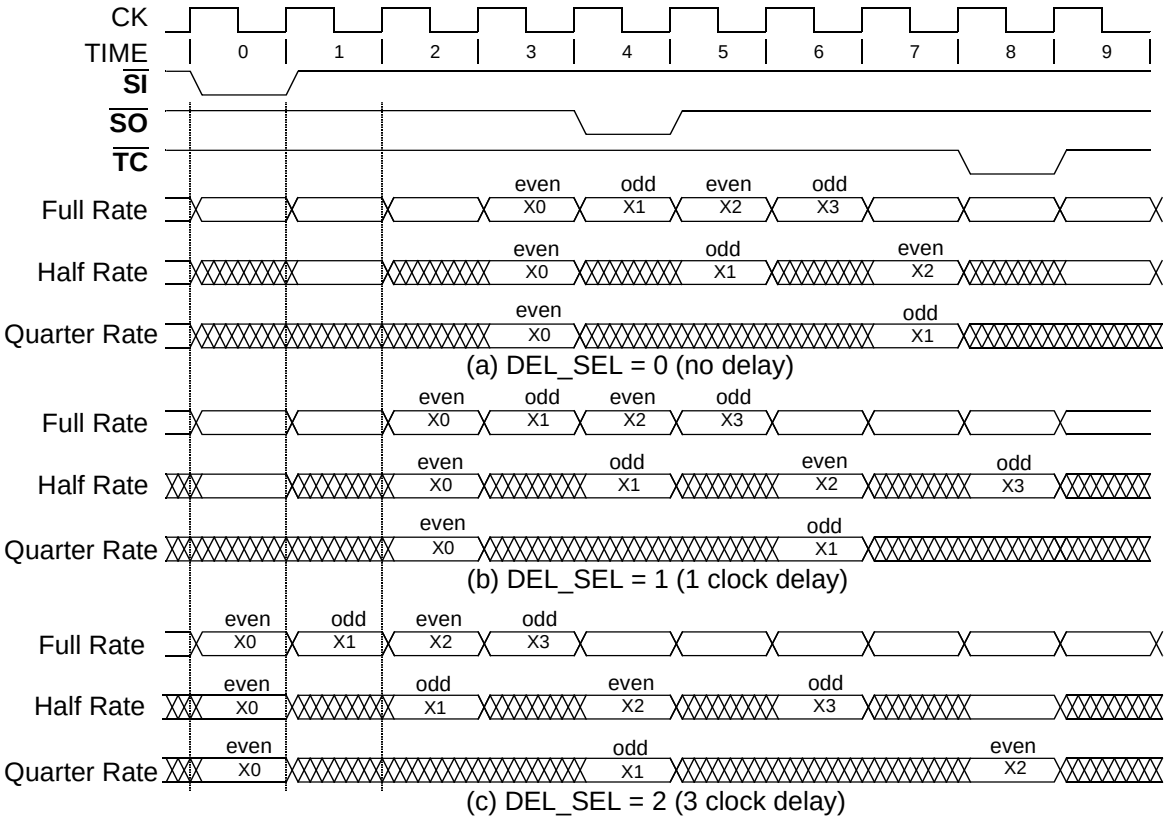


Figure 7. Input Timing

NOTES:

(1) The **TC** strobe appears 8 clocks after **SI** and every 16*(CNT+1) clocks thereafter.

(2) The input delays selected by the DEL_SEL control are clock cycle delays, not sample delays. These delays occur before the input rate circuit captures the samples as shown above.

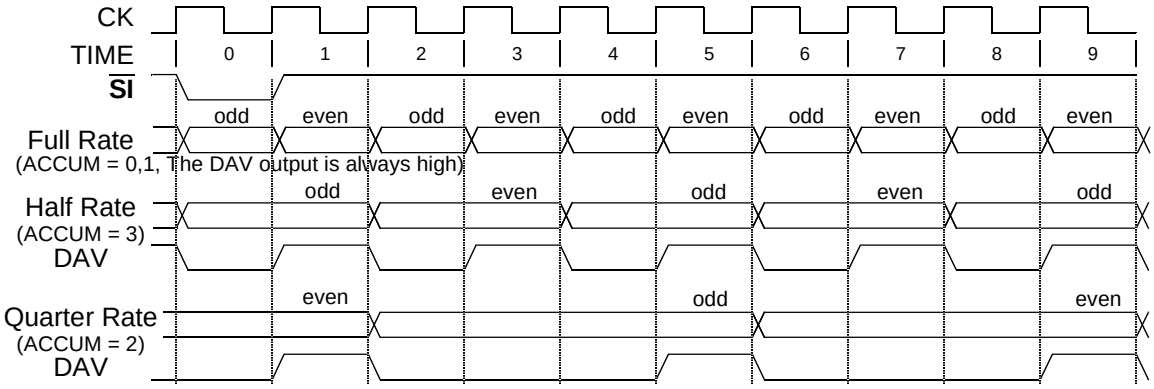


Figure 8. Output Timing

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6.2 A-PATH AND B-PATH CONTROL REGISTER 1

Control registers APATH_REG1 and BPATH_REG1 are identical and are described here.

ADDRESS 1: **APATH_REG1**

ADDRESS 3: **BPATH_REG1**

BIT	TYPE	NAME	DESCRIPTION
0-4 (LSBs)	R/W	FEED_BACK	This 5 bit field controls the symmetric filter feedback mode according to the following table: FEED_BACK (HEX) — DESCRIPTION 00 — no symmetry 01 — full rate odd symmetry 08 — full rate even symmetry and A-path cascade mode 11 — decimate and interpolate by 2 odd symmetry 12 — decimate by 2 even symmetry and decimate by 4 odd symmetry 14 — decimate by 4 even symmetry and half and quarter rate odd symmetry 18 — half and quarter rate even symmetry NOTE: the A-path FEED_BACK control must be 08 in the cascade mode.
5	R/W	ANTI_SYM	Anti-symmetric filters can be implemented by setting this bit and the CIN bit described below. This bit complements (bitwise inverts) the feedback data. EXCEPTION: In the cascade mode the A-PATH ANTI_SYM bit must be set for all filters.
6	R/W	CIN	This is the carry input to the filter cell's 12 bit adder (See Figure 5). This bit is set to create anti-symmetric filters. In the cascade mode this bit is cleared in both paths to create a symmetric filter and it is set in both paths to create an anti-symmetric filter.
7	R/W	ODD_SYM	This bit must be set for odd-symmetry filters and cleared for even or non symmetric filters.
8-12	R/W	REV_DELAY	These five bits control the filter cells' reverse delays. These bits are not used if FEED_BACK=00 (no symmetry) REV_DELAY (HEX) — DESCRIPTION 00 — no symmetry 01 — full rate filters 02 — decimate by 4 and half rate filters 0E — decimate and integrate by 2 filters 10 — quarter rate filters
13-15(MSB)	R/W	FOR_DELAY	These 3 bits control the filter cells' forward delays. FOR_DELAY — DESCRIPTION 0 — decimate and interpolate by 4 filters 1 — decimate and interpolate by 2 filters 3 — full rate filters 4 — quarter rate filters 5 — half rate filters

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6.3 CASCADE MODE CONTROL REGISTER

This register controls the cascade mode and the synchronous coefficient storage mode.

ADDRESS 4: CASCADE_REG

BIT	TYPE	NAME	DESCRIPTION
0 (LSB)	R/W	SYNC_COEF	This bit forces the filter coefficient data to be synchronized to the system clock before they are stored in the filter cell coefficient registers. NOTE: The write cycle control strobe, when storing a coefficient in this mode, must be active for at least 5 data clock cycles.
1-8	R/W	-	Unused.
9-15(MSB)	R/W	CASCADE	This 7 bit field controls the cascade mode according to the following table:

CASCADE (HEX)	DESCRIPTION
10	Dual path mode.
2F	Cascade mode for non-full rate filters
4F	Cascade mode for full rate filters.

To enable the cascade mode the user must also set ANTI_SYM to 1 and FEED_BACK to 08 in APATH_REG1.

In the cascade mode the following control bits are not used:

APATH_REG0: ACCUM
APATH_REG1: ODD_SYM
BPATH_REG0: RATE,NEG_IN, AB_SEL, DELAY_SEL, COEF_SEL
BPATH_REG1: REV_DELAY, FOR_DELAY

These bits can be treated as “don’t cares”.

The SYNC_COEF mode is only needed when the user is dynamically changing filter coefficients in the decimate by 4, interpolate by 4 or quarter rate modes. These modes use all four coefficient registers in each filter cell. Otherwise the user can dynamically change filter coefficients by switching between banks of filter coefficients using the COEF_SEL control described in Section 6.1.

6.4 COUNTER REGISTER

This register sets the cycle time of the 20 bit internal counter.

ADDRESS 5: COUNTER_REG

BIT	TYPE	NAME	DESCRIPTION
0-15	R/W	CNT	CNT is the 16 bit counter control word. The counter is preset to (16*CNT+15) by **$\overline{\text{SI}}$**, counts down to zero, and then starts over again.

A **$\overline{\text{TC}}$** terminal count strobe is generated by the counter when it is preset by **$\overline{\text{SI}}$** and every time it reaches zero. The delay from **$\overline{\text{SI}}$** to the first **$\overline{\text{TC}}$** strobe is set at 8 clocks. The **$\overline{\text{TC}}$** strobe will then repeat every 16*(CNT+1) clocks.

6.5 GAIN REGISTER

The gain register controls the filter’s output gain and rounding. Note that the gain setting is synchronized to the data clock so that gain changes will not cause “glitches” on the output when it is changed. The gain and rounding control is common to both paths of the chip.

ADDRESS 6: GAIN_REG

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	F	The 4 bit gain fraction.
4-7	R/W	S	The 4 bit gain exponent.
8-14	R/W	ROUND	Controls the output rounding according to the following table:
15 (MSB)	R/W	-	Unused

ROUND (HEX)	DESCRIPTION
00	Truncate
01	Round to the 8 MSBs
02	Round to the 10 MSBs
04	Round to the 12 MSBs
08	Round to the 14 MSBs
10	Round to the 16 MSBs
20	Round to the 20 MSBs
40	Round to the 24 MSBs

The chip's output gain is set using **F** and **S** according to the following formula:

$$GAIN = 2^{(S-20)}(1+F/16)(DC_GAIN)$$

Where DC_GAIN is the sum of the filter coefficients. Unity gain, according to this formula, will map the MSB of the12 bit input data (AI11 or BI11) into the MSB of the selected output word (AO15 or BO15).

The 32 bit filter path output is rounded to the number of most significant bits selected by the round control. The gain circuit output is saturated to plus or minus full scale if the GAIN setting causes an overflow. The **AOF** or **BOF** output pins will go high whenever an overflow is detected in the A-Path or B-path gain circuit.

For example: If the DC gain of the filter coefficients is 2^{15} (i.e., the sum of the coefficients is 2^{15}), then the overall gain of the filter can be set to unity by setting S to 5 and F to 0.

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6.6 OUTPUT MODE REGISTER

The output mode register controls the output formatting.

ADDRESS 7: OUTPUT_REG

BIT	TYPE	NAME	DESCRIPTION
0,1 (LSBs)	R/W	NEG_OUT	This two bit field controls the output sample negation as follows: NEG_OUT DESCRIPTION 0 don't negate 1 negate full rate output samples 2 negate half rate output samples 3 negate quarter rate output samples When negation is enabled the circuit will negate the even time A-Path outputs and the odd time B-path outputs where the definition of even and odd time samples is shown in Figure 8. If the user desires to negate the odd time A-path outputs, or negate the even time B-path outputs, then the NEG_IN control should be used to negate the path's input.
2	R/W	24BIT_MODE	Enables the 24 bit mode. PATH_ADD and 24BIT_OUT must also be set in this register. A-path and B-path must be configured the same except for: B-path must be in the unsigned mode, A-path CIN must be zero, A-path AB_SEL is 1, and B-path AB_SEL is 0.
3	R/W	24BIT_OUT	Enables the 24 bit output mode. The 24 bit B-path output samples are output on the A-out and B-out pins as follows: The upper 16 bits are output on the A-out pins, the lower 8 bits are output on the upper 8 bits of the B-out pins.
4,5	R/W	MUX_MODE	In the MUX_MODE the A-path and B-path outputs are multiplexed together on the A-out pins. The B-out pins are cleared. The MUX_MODE settings are: MUX_MODE DESCRIPTION 0 mux mode is off, 1 mux half rate outputs, 3 mux quarter rate outputs The multiplexed half rate outputs will generate a full rate output stream, the multiplexed quarter rate outputs will generate a half rate stream. The A-path sample is output first, followed by the B-path sample.
6	R/W	PATH_ADD	Adds the A-path and B-path results. The result is output on the B-out pins unless the 24BIT_OUT control is enabled.
7	R/W	DAV_POLARITY	Invert the polarity of the data valid (DAV) strobe. Figure 8 shows DAV with DAV_POLARITY = 0.
8-15	R/W	-	unused

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6.7 SNAPSHOT MODE CONTROL REGISTERS

The snapshot memory is divided into two halves, 128 words by 16 bits each. SNAP_REGA controls the A-half of the snapshot memory, SNAP_REGB controls the B-half.

ADDRESS 8: **SNAP_REGA**

ADDRESS 9: **SNAP_REGB**

BIT	TYPE	NAME	DESCRIPTION
0,1 (LSBs)	R/W	SEL_IN	Selects the snapshot source as: SEL_IN — DESCRIPTION 0 — **IB[0:11]** 1 — **IA[0:11]** 2 — **OA[0:15]** 3 — **OB[0:15]**
2,3	R/W	SNAP_RATE	Determines the rate at which samples are stored according to: SNAP_RATE — DESCRIPTION 0 — every clock, full rate samples 1 — every other clock, half rate samples 2 — invalid 3 — every 4th clock, quarter rate samples.
4-7	R/W	SNAP_DELAY	Delay from snapshot trigger in blocks of 128 samples until start of snapshot. The delay is: 128*SNAP_DELAY*(SNAP_RATE+1) clock cycles where SNAP_DELAY ranges from 0 to 15. This control allows the user to start the A or B-half snapshot a fixed number of samples after the other half's snapshot.
8	R/W	SNAP_HOLD	Do not start a new snapshot. This control lets the user start one half of the snapshot memory and not the other.
9	R/W	BYTE_MODE	This control reorganizes the memory half into 256 bytes instead of 128 words. The upper 8 bits of the input source are stored.
10-15(MSB)	R/W	-	unused

In the BYTE_MODE the memory is reorganized so that the first 128 bytes of the 256 byte snapshot are stored in the least significant bytes of the 128 word memory and the second 128 bytes are stored in the most significant bytes of the 128 word memory.

This document contains information which may be changed at any time without notice

6.8 SNAPSHOT START CONTROL REGISTER

This register controls the snapshot trigger settings, the snapshot read modes and the chip's sync modes.

ADDRESS 10: SNAP_REGC

BIT	TYPE	NAME	DESCRIPTION
0,1 (LSBs)	R/W	TRIGGER	This control sets the trigger condition which will start a snapshot once the ARMED bit is set. The trigger conditions are to start: TRIGGER — DESCRIPTION 0 — immediately, 1 — when the **$\overline{SN}$** strobe is received, 2 — when the **$\overline{SI}$** strobe is received, 3 — when the **$\overline{TC}$** strobe is received.
2,3	R/W	READ_MODE	Selects whether words or bytes are read from the snapshot memory according to: READ_MODE — DESCRIPTION 0,2 — read words, 1 — read the least significant bytes 3 — read the most significant bytes When reading bytes, the bytes are placed in the LSBs of the 16 bit control word and sign extended.
4	R/W	ARMED	The user sets this bit to arm the snapshot memory so that it will start on the next trigger condition. The chip clears this bit when the trigger occurs.
5	R/W	A_DONE	This bit goes high when the A-half snapshot is complete. This bit must be cleared by writing a zero to it.
6	R/W	B_DONE	This bit goes high when the B-half snapshot is complete. This bit must be cleared by writing a zero to it.
7	R/W	-	unused
8,9	R/W	SYNC_OUT	This two bit field selects the sync output (**$\overline{SO}$**) source as: SYNC_OUT — DESCRIPTION 0 — **$\overline{SI}$** delayed by 4 clocks (SYNC_OFF=0), 1 — **$\overline{TC}$**, 2 — **$\overline{OS}$**, 3 — never
10	R/W	SYNC_OFF	This bit disables the sync input to the chip. The counter will free run when this bit is high
11-15	R/W	-	unused

6.9 ONE SHOT ADDRESS

The one shot pulse is generated on the **$\overline{OS}$** pin by writing to address 11. This is a write-only address. The data written to it is irrelevant.

ADDRESS 11: ONE_SHOT

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6.10 NEW MODES REGISTER

This register controls the new modes added to the GC2011A chip. This address was not used in the GC2011 chip. Bits 8,9,12,13,14,and 15 power up low.

ADDRESS 12: NEW_MODES

BIT	TYPE	NAME	DESCRIPTION
0-7 (LSBs)	R only	REVISION	These bits read back the current mask revision number.
8	R/W	POWER_DOWN	Forces the chip to be in the static power down mode when set.
9	R/W	DISABLE_CLOCK_LOSS_DETECT	Turns off the clock loss detect circuit when set. This bit should be kept low.
10,11	R only	POWER_DOWN_STATUS	These bits go low when the chip is in the power down state, either because bit 8 (POWER_DOWN) above is set, or because clock loss has been detected. These bits are normally high.
12	R/W	INV_MSB_AOUT	Inverts the MSB of the A-output when set.
13	R/W	INV_MSB_BOUT	Inverts the MSB of the B-output when set.
14	R/W	INV_MSB_AIN	Inverts the MSB of the A-input when set.
15 (MSB)	R/W	INV_MSB_BIN	Inverts the MSB of the B-input when set.

The REVISION field can be used to determine the mask revision number for the GC2011A. The mask revision numbers and the mask change descriptions are shown in Table 15 below (the mask codes are printed on the GC2011A package).

Table 15: Mask Revisions

Mask Revision Number (bits 0-7)	Release Date	Mask Code on Package	Description
01	February 1999	55585B	Original

The INV_MSB control bits will invert the MSB of the A and B inputs or the A and B outputs in order to convert to and from offset binary and two's complement formats. If the input data is offset binary, then the INV_MSB_AIN and/or INV_MSB_BIN control bits should be set. If the output data needs to be converted to offset binary, then the INV_MSB_AOUT and/or INV_MSB_BOUT control bits should be set.

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7.0 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

Table 16: Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	-0.3	5	V	
Input voltage (undershoot and overshoot)	V_{IN}	-0.5	V_{CC}+0.5	V	
Storage Temperature	T_{STG}	-65	150	^{o}C	
Lead Soldering Temperature (10 seconds)			300	^{o}C	

7.2 RECOMMENDED OPERATING CONDITIONS

Table 17: Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	3.1	3.5	V	
Temperature Ambient, no air flow	T_A	-40	+85	^{o}C	1
Junction Temperature	T_J		125	^{o}C	1

Notes:
1. Thermal management is required to keep T_J below MAX for full rate operation. See Table 17 below.

7.3 THERMAL CHARACTERISTICS

Table 18: Thermal Data

THERMAL CONDUCTIVITY	SYMBOL	GC2011A-PB	GC2011A-PQ	UNITS
		2 Watts	2 Watts	
Theta Junction to Ambient	θja	TBD	18	^{o}C/W
Theta Junction to Case	θjc	TBD	4	^{o}C/W

Note: Air flow will reduce θ**ja** and is highly recommended.

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7.4 DC CHARACTERISTICS

All parameters are industrial temperature range of -40 to 85 ^{O}C ambient unless noted.:

Table 19: DC Operating Conditions

PARAMETER	SYMBOL	Vcc = 3.3V		UNITS	NOTES
		MIN	MAX		
Voltage input low	V_{IL}		0.8	V	2
Voltage input high	V_{IH}	2.0		V	2
Input current (V_{IN} = 0V)	I_{IN}	Typical +/- 10		uA	2
Voltage output low (I_{OL} = 2mA)	V_{OL}		0.5	V	2
Voltage output high (I_{OH} = -2mA)	V_{OH}	2.4	3.3	V	2
Data input capacitance (All inputs except **CK** and **C[0:15]**)	C_{IN}	Typical 4		pF	1
Clock input capacitance (**CK** input)	C_{CK}	Typical 10		pF	1
Control data capacitance (**C[0:15]** I/O pins)	C_{CON}	Typical 6		pF	1

Notes:

1. Controlled by design and process and not directly tested. Verified on initial parts evaluation.
2. Each part is tested at 85^{O}C for the given specification.

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7.5 AC CHARACTERISTICS

Table 20: AC Characteristics (-40 TO +85^{O}C Ambient, unless noted)

PARAMETER	SYMBOL	3.1V to 3.5V		UNITS	NOTES
		MIN	MAX		
Clock Frequency	F_{CK}	0.01	106	MHz	2, 3
Clock low period (Below V_{IL})	t_{CKL}	3.8		ns	2
Clock high period (Above V_{IH})	t_{CKH}	3.6		ns	2
Data setup before **CK** goes high (**AI**, **BI**, $\overline{\textbf{SI}}$, $\overline{\textbf{SN}}$ or $\overline{\textbf{CKEN}}$)	t_{SU}	3.0		ns	2
Data hold time after **CK** goes high	t_{HD}	1.0		ns	2
Data output delay from rising edge of **CK**. (**AO**, **BO**, **DAV**, or $\overline{\textbf{SO}}$)	t_{DLY}	1.0	8.0	ns	2,4
Data to tristate delay (**AO**, **BO**, **AOF** or **BOF** to hiZ from $\overline{\textbf{AOE}}$ or $\overline{\textbf{BOE}}$)	t_{DZ}	2.0	5.0		1
Tristate to data output delay (**AO**, **BO**, **AOF**, or **BOF** valid from $\overline{\textbf{AOE}}$ or $\overline{\textbf{BOE}}$)	t_{ZD}	3.0 Note 1	8.0 Note 2	ns	4
Control Setup before $\overline{\textbf{CE}}$ and $\overline{\textbf{RE}}$, or $\overline{\textbf{WE}}$ go low (**A**, $\overline{\textbf{WE}}$ during read, and **A**, $\overline{\textbf{RE}}$, **C** during write) See Figure 3.	t_{CSU}	5.0		ns	2
Control hold after $\overline{\textbf{CE}}$,$\overline{\textbf{RE}}$, or $\overline{\textbf{WE}}$ go high (**A**, $\overline{\textbf{WE}}$ during read, and **A**, $\overline{\textbf{RE}}$, **C** during write) See Figure 3.	t_{CHD}	5.0		ns	2
Control enable $\overline{\textbf{CE}}$ or $\overline{\textbf{WE}}$ pulse width (Write operation) See Figure 3.	t_{CSPW}	30.0		ns	2,5
Control output delay $\overline{\textbf{CE}}$ and $\overline{\textbf{RE}}$ low to **C** (Read Operation) See Figure 3.	t_{CDLY}		35.0	ns	2,6
Control tristate delay after $\overline{\textbf{CE}}$ or $\overline{\textbf{RE}}$ go high. See Figure 3.	t_{CZ}		10.0	ns	1
Quiescent supply current (V_{IN}=0 or V_{CC}, F_{CK} = 0, or POWER_DOWN=1)	I_{CCQ}		2.0	mA	1
Supply current (F_{CK} = 80 MHz)	I_{CC}		500.0	mA	2, 7

Notes:

1. Controlled by design and process and not directly tested. Verified on initial part evaluation.
2. Each part is tested at 85 deg C for the given specification.
3. The chip may not operate properly at clock frequencies below MIN and MAX.
4. Capacitive output load is 20pf. Delays are measured from the rising edge of the clock to the output level rising above or falling below 1.3v.
5. t_{CSPW} must be at least five clock cycles wide if the SYNC_COEF control bit is set (See Section 6.3).
6. Capacitive output load is 80pf.
7. Current changes linearly with voltage and clock speed. Icc (MAX) $= \left(\frac{VCC}{3.3}\right)\left(\frac{F_{CK}}{80M}\right)500\text{mA}$

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8.0 APPLICATION NOTES

8.1 POWER AND GROUND CONNECTIONS

The GC2011A chip is a very high performance chip which requires solid power and ground connections to avoid noise on the V_{CC} and GND pins. If possible the GC2011A chip should be mounted on a circuit board with dedicated power and ground planes and with at least two decoupling capacitors (0.01 and 0.1 μf) adjacent to each GC2011A chip. If dedicated power and ground planes are not possible, then the user should place decoupling capacitors adjacent to each V_{CC} and GND pair.

IMPORTANT

The GC2011A chip may not operate properly if these power and ground guidelines are violated.

8.2 STATIC SENSITIVE DEVICE

The GC2011A chip is fabricated in a high performance CMOS process which is sensitive to the high voltage transients caused by static electricity. These parts can be permanently damaged by static electricity and should only be handled in static free environments.

8.3 106 MHZ OPERATION

Care must be taken in generating the clock when operating the GC2011A chip at its full 106 MHz clock rate. The user must insure that the clock is above 2 volts for at least 3.6 nanoseconds and is below 0.8 volt for at least 3.8 nanoseconds.

8.4 REDUCED VOLTAGE OPERATION

The power consumed by the GC2011A chip can be greatly reduced by operating the chip at the lowest V_{CC} voltage which will meet the application's timing requirements.

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8.5 SYNCHRONIZING MULTIPLE GC2011A CHIPS

A system containing a bank of GC2011A chips will need to be synchronized so that the output data from each chip are aligned. This is especially important for the half rate and quarter rate I/O modes. The synchronization can be achieved by connecting the **$\overline{\text{SI}}$** inputs of all the chips to a system sync input. If a system sync is not available, then the counter within the GC2011A chip can be used to generate one. The **$\overline{\text{TC}}$** strobe of the counter can be output from a "master" GC2011A and used as the **$\overline{\text{SI}}$** input for all other GC2011A chips. The **$\overline{\text{SO}}$** should also be used as the **$\overline{\text{SN}}$** (snap strobe) input to all of the chip, including the master chip, so that the snapshot memories within all of the chips can be synchronized.

For example, two chips can be operated in parallel as a complex filter processing complex data. The suggested configuration for these chips is shown in Figure 9.

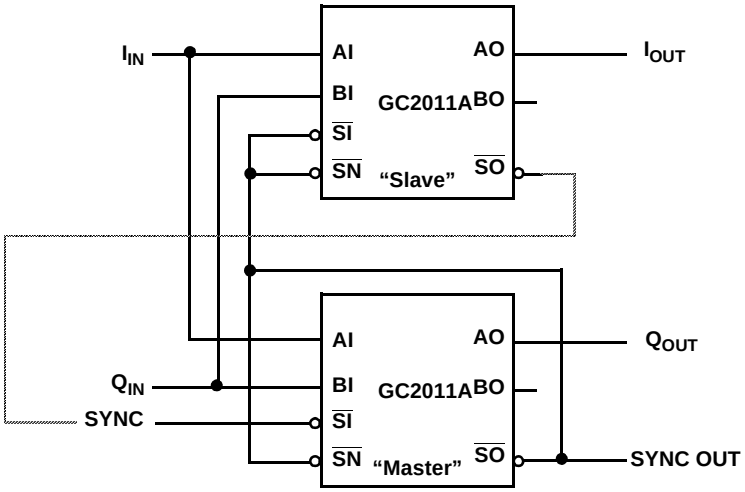


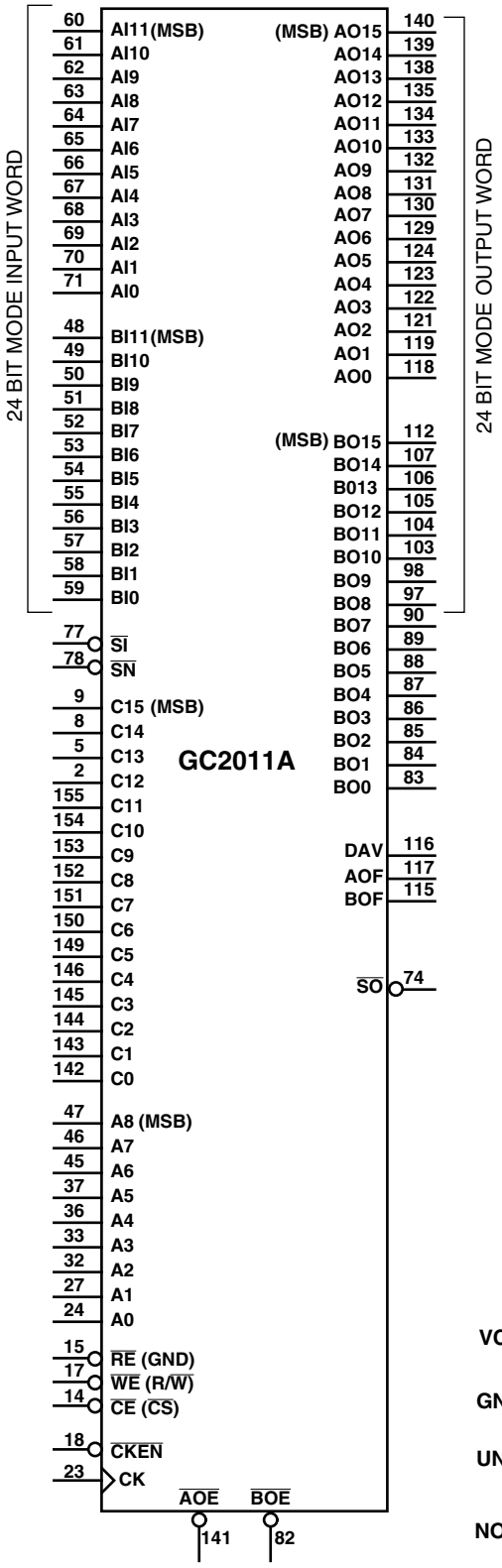
Figure 9. Processing Complex Input Data

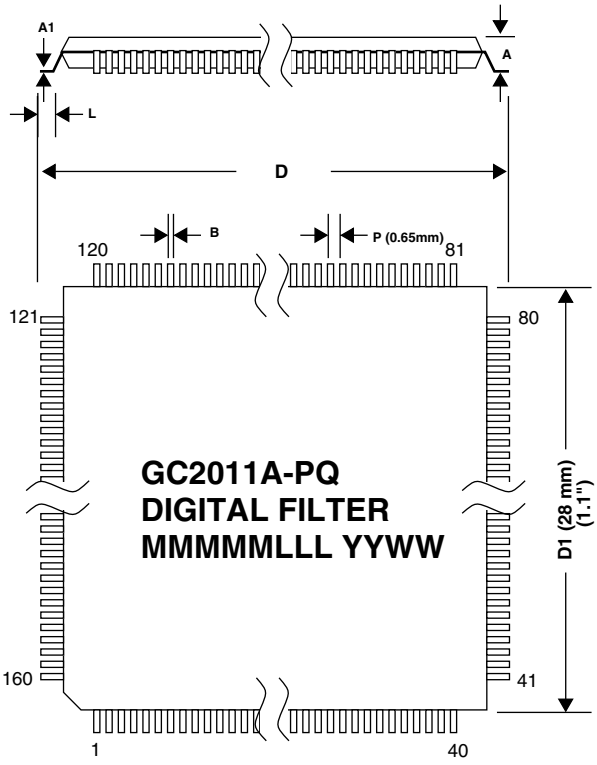
In this configuration the slave chip generates the I-outputs and the master chip generates the Q-outputs. The two chips are synchronized by connecting the **$\overline{\text{SO}}$** signal from the master chip to the **$\overline{\text{SN}}$** inputs of both chips and to the **$\overline{\text{SI}}$** input of the slave chip. A system sync, if available, can be used to synchronize the master chip to the rest of the system. If a system sync is not available, then a one shot strobe generated by the slave chip and output on the **$\overline{\text{SO}}$** pin, can be routed into the **$\overline{\text{SI}}$** input of the master chip. This is shown as the dashed line in Figure 9. The **$\overline{\text{SO}}$** from the master chip can then be used as a system sync for the rest of the system.

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PACKAGING

160 PIN QUAD FLAT PACK (QFP) PACKAGE





160 PIN QUAD FLAT PACK PACKAGE

GC2011A-PQ = Enhanced Thermal Plastic Package
GC2011A-CQ = Ceramic Package (special order only)

Package Markings: MMMMM = Mask Code
LLL = Lot Number
YYWW = Date Code

DIMENSION		PLASTIC	CERAMIC
D	(width pin to pin)	31.2 mm (1.228")	32.0 mm (1.260")
D1	(width body)	28.0 mm (1.102")	28.0 mm (1.102")
P	(pin pitch)	0.65 mm (0.026")	0.65 mm (0.026")
B	(pin width)	0.30 mm (0.012")	0.30 mm (0.012")
L	(leg length)	0.88 mm (0.035")	0.70 mm (0.028")
A	(height)	4.07 mm (0.160")	3.25 mm (0.128")
A1	(pin thickness)	0.17 mm (0.007")	0.2 mm (0.008")

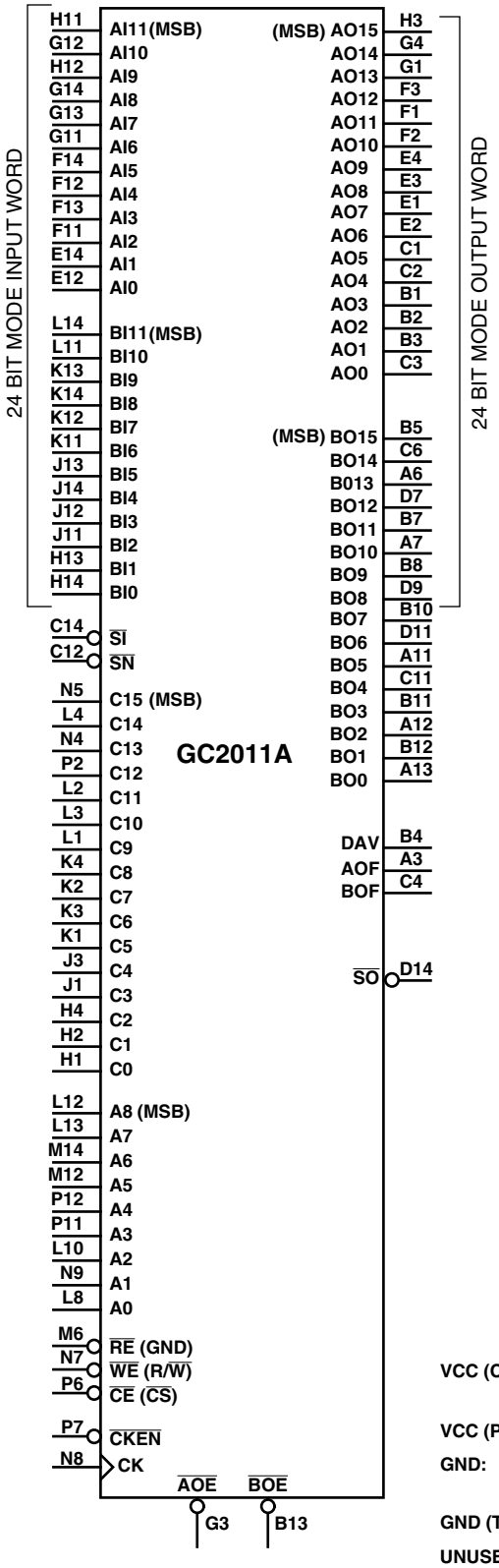
VCC PINS: 3,4,7,12,13,16,21,22,26,30,31,35,38,39,44,75,76,80,91,92,93, 99,100,108,109,113,125,126,136,147,156

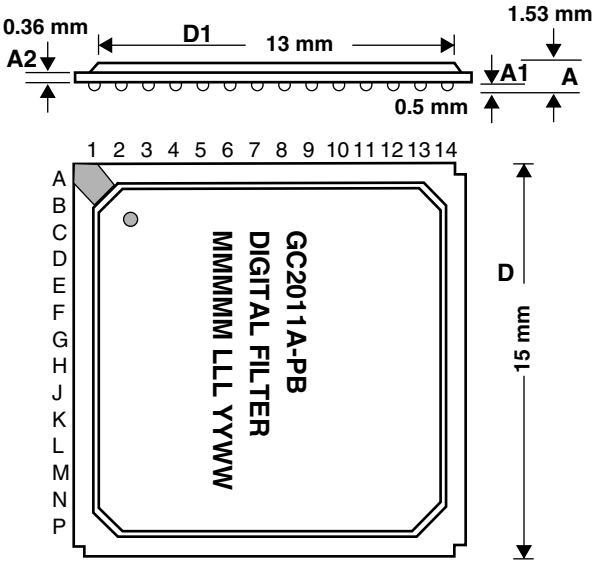
GND PINS: 6,10,11,19,20,25,28,29,34,42,43,72,73,79,94,95,96,101,102, 110,111,114,127,128,137,148,157,158,159

UNUSED PINS: 1, 40, 41, 81, 120, 160

NOTE: 0.01 to 0.1 f DECOUPLING CAPACITORS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE MIDDLE OF EACH SIDE OF THE CHIP

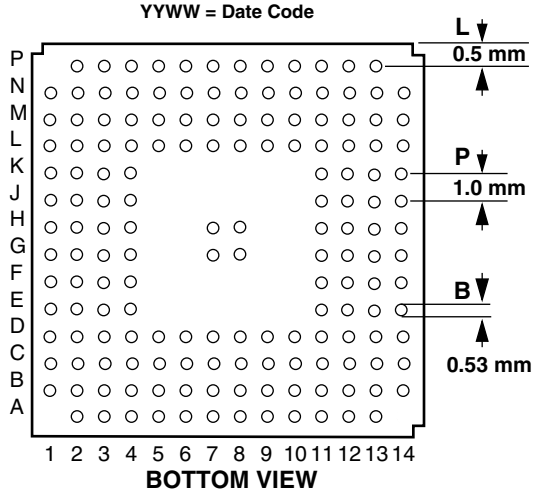
160 PIN BALL GRID ARRAY (PBGA) PACKAGE





TOP VIEW

MMMMM = Mask Code
LLL = Lot Number
YYWW = Date Code



BOTTOM VIEW

DIMENSION		TYP	TOLERANCE
D	(width body)	15 mm	mm
D1	(width cover)	13 mm	mm
P	(ball pitch)	1.0 mm	mm
B	(ball width)	0.53 mm	mm
L	(overhang)	0.5 mm	mm
A	(overall height)	1.53 mm	mm
A1	(ball height)	0.5 mm	mm
A2	(substrate thickness)	0.36 mm	mm

VCC (CORE): A8, B6, C10, D2, D6, D8, D10, D12, D13, L5, L6, M7, M9, M10, N3, N6, N10, N11, N12, P3, P4, P8, P13

VCC (PAD RING): A10, B14, D3, D5, F4, J2, M1, M13

GND: A5, A9, B9, C5, C7, C8, D4, E11, E13, L7, L9, M2, M4, M5, M8, M11, N1, N13, P5, P9, P10, A4, C9, C13, D1, G2, J4, M3, N14

GND (THERMAL): G7, G8, H7, H8

UNUSED: A2, N2

NOTE: 0.01 to 0.1 f DECOUPLING CAPACITORS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE MIDDLE OF EACH SIDE OF THE CHIP

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
GC2011A-PB	ACTIVE	BGA	GJZ	160	126	TBD	Call TI	Level-3-220C-168 HR
GC2011A-PQ	ACTIVE	QFP	PCM	160	24	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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