ft2920

8W Boosted Class-G Audio Power Amplifier with Automatic Level Control & Battery Tracking AGC

GENERAL DESCRIPTION

The ft2920 is a highly efficient 8W boosted Class-G audio power amplifier with automatic level control (ALC) and battery tracking AGC. It integrates a filterless Class-D audio amplifier with an adaptive multi-level Class-G boost regulator and operates with a range of supply voltages from 3V to 5.5V. When a supply voltage at 3.6V, the ft2920 can deliver an output power of 8W with 10% THD+N, or an ALC output power of 6W with 0.4% THD+N, into a 4Ω speaker load.

In ft2920, the power supply rail of the audio amplifier's output stage is internally boosted and regulated by an asynchronous PWM switching regulator with an integrated power switch. The boost regulator employs current-mode PWM control with proprietary multi-level operation to regulate the boosted supply voltage in response to the voltage level of the audio output. To facilitate various output power applications, three boosted supply voltage settings are available. The adaptive nature of the multi-level Class-G boost regulator improves overall efficiency.

The ft2920 features ALC function to constantly monitor and safeguards the audio output against the boosted supply voltage of the audio amplifier's output stage, preventing output clipping distortion, excessive power dissipation, and speaker over-load. Once an over-level condition is detected, the ALC lowers the voltage gain of the audio amplifier proportionally to limit the peak audio output.

In conjunction with ALC, as the battery supply voltage drops, the battery tracking AGC lowers the voltage gain of the audio amplifier to limit the peak audio output, preventing the collapse of battery voltage.

FEATURES

- Wide range of supply voltages from 3V to 5.5V
- Filterless Class-D audio amplifier integrated with an adaptive multi-level Class-G boost regulator
- Automatic level control to eliminate output clipping
- Battery tracking AGC to prevent battery collapse
- Soft drive mode for EMI reduction
- Three boosted voltage settings: 8.0V/7.4V/6.8V
- Maximum output power in Non-ALC mode
  (VBAT=3.6V, 4Ω load, ALC=High, THD+N=10%)

PVDD (V)	Po (W)
8.0	8.0
7.4	6.8
6.8	5.7

- ALC output power in ALC mode
  (VBAT=3.6V, 4Ω load, ALC=Low, THD+N=0.4%)

PVDD (V)	Po (W)
8.0	6.0
7.4	5.1
6.8	4.2

- Wide ALC dynamic range: 11dB
- Three gain settings: 26dB/30dB/34dB
- High efficiency up to 82%
- Auto-recovering over-current & short-circuit protection
- Available in TSSOP-24L package

APPLICATIONS

- Blue Tooth Speakers
- Portable Audio Docks
- Consumer Audio Electronics

APPLICATION CIRCUIT

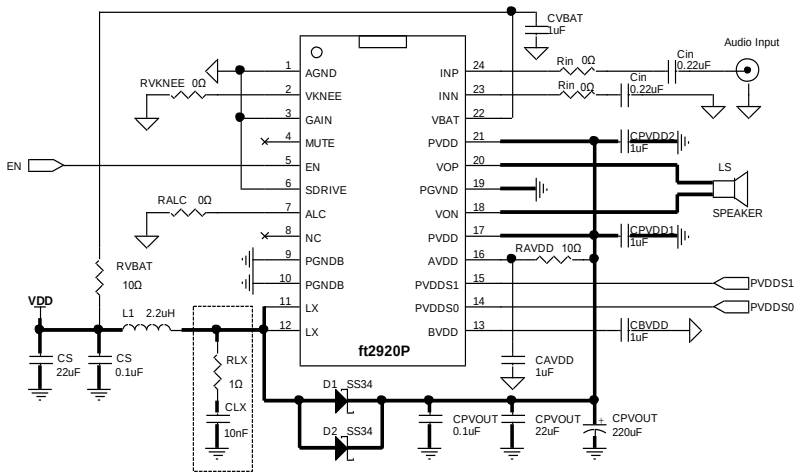
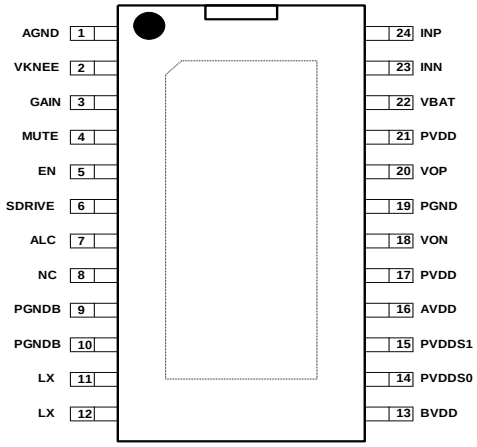


Figure 1: Typical Application Circuit of ft2920

PIN CONFIGURATION AND DESCRIPTION



ft2920P (Top View)

NAME	Pin #	TYPE	DESCRIPTION
AGND	1	G	Analog ground.
VKNEE	2	DI	**Battery Tracking AGC Control** with an internal 300kΩ pullup resistor to VBAT and an internal 300kΩ pulldown resistor to ground.
GAIN	3	DI	**Gain Select** with an internal 300kΩ pullup resistor to VBAT and an internal 300kΩ pulldown resistor to ground.
MUTE	4	DI	**Mute Enable** (Active High) with an internal 300kΩ pulldown resistor to ground.
EN	5	DI	**Chip Enable** (Active High) with an internal 300kΩ pulldown resistor to ground.
SDRIVE	6	DI	**Soft Drive Control** with an internal 300kΩ pullup resistor to VBAT and an internal 300kΩ pulldown resistor to ground. When unconnected, the boost regulator is disabled.
ALC	7	DI	**ALC Control** with an internal 300kΩ pullup resistor to VBAT and an internal 300kΩ pulldown resistor to ground. When asserted high, the ALC function is disabled.
PGNDB	9, 10	G	Power ground for the output stage of the boost regulator. It must be directly shorted to the system ground plane GND.
LX	11, 12	AO	Switching output of the boost regulator.
BVDD	13	AO	Internally generated voltage reference. Connect it to a 1μF capacitor for decoupling.
PVDDS0	14	DI	**LSB of Boosted Voltage Select** with an internal 300kΩ pulldown resistor to ground.
PVDDS1	15	DI	**MSB for Boosted Voltage Select** with an internal 300kΩ pulldown resistor to ground.
AVDD	16	AI	Boosted Input Voltage. Connect it to a 1μF capacitor for decoupling. It must be externally connected to PVDD through a small decoupling resistor of 10Ω.
PVDD	17, 21	P	Power supply for the audio amplifier's output stage. Connect the pins individually to a 1μF capacitor for decoupling.
VON	18	AO	Negative audio output terminal.
PGND	19	G	Power ground for the output stage of the audio power amplifier. It must be directly shorted to the system ground plane GND.
VOP	20	AO	Positive audio output terminal.
VBAT	22	P	Supply input voltage. Connect it to a 1μF capacitor for decoupling. It must be externally connected to the system supply through a small decoupling resistor of 10Ω.
INN	23	AI	Inverting audio input terminal.
INP	24	AI	Non-inverting audio input terminal.
N/C	8		No internal connection.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ft2920P	-40°C to +85°C	TSSOP-24L

REVISION HISTORY

Initial Release 1.0 (Jan. 2016)

Changed from Initial 1.0 (Jan. 2016) to Revision 1.1 (Aug. 2016)

1. Added decoupling capacitors for VBAT, AVDD, BVDD, and PVDD pins in Recommended Operating Conditions table on Page 4.
2. Added voltage gain settings for various pin configurations at GAIN (Low, High, and Unconnected) in Table 5.
3. Changed the recommended inductor values from 2.2µH ~ 4.7µH to 1.5µH ~ 3.3µH.
4. Changed the inductor value from3.3µH to 2.2µH in Electrical and Performance Characteristics sections.
5. Simplified the description of Selection of Supply Decoupling Capacitors on Page 16.
6. Simplified the description of Voltage Gain Setting on Page 18.
7. Added the description of Supply Decoupling Capacitors (C_{VBAT}, C_{AVDD}, C_{BVDD}, and C_{PVDD}) on Page 22.
8. Changed suggested capacitor value of the boost regulator snubber circuit in Figure 21.

Changed from Revision 1.1 (Aug. 2016) to Revision 1.2 (Feb. 2017)

1. Changed boost regulator's input capacitor C_S from 10µF//470µF to 22µF//220µF.
2. Changed supply decoupling capacitors C_{VBAT} and C_{PVDD} from 10µF to 1µF.
3. Changed input resistors R_{IN} from 15kΩ to 0Ω in Electrical and Performance Characteristics sections.
4. Update Recommended Operating Conditions table on Page 4.

ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	VALUE
Supply voltage, VBAT	-0.3V to 6V
LX, AVDD, PVDD, VOP, VON	-0.3V to 9V
PGND, PGNDB	-0.3V to 0.3V
All other Pins	-0.3V to VBAT+0.3V
Storage Temperature	-65°C to +150°C
ESD Ratings-Human Body Model (HBM)	2000V
Junction Temperature	150°C
Maximum Soldering Temperature (@10 second duration)	260°C

Note 1: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may also affect device reliability.

POWER DISSIPATION RATINGS (Note 2, 3)

PACKAGE	TA ≤ +25°C	TA = +70°C	TA = +85°C	Θ_{JA}
TSSOP-24L	4.2W	2.7W	2.2W	30°C/W

Note 2: The thermal pad of the package must be directly soldered onto a grounded metal island (as a thermal sink) on the system board.
Note 3: The power dissipation ratings are for a two-side, two-plane printed circuit board (PCB).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}		3.0		5.5	V
Minimum Load Impedance	R_L	Across VOP & VON	2.5	4		Ω
Audio Input Resistor	R_{IN}	@ INP, INN	0		47	kΩ
Audio Input Capacitor	C_{IN}	@ INP, INN	0.1	0.22	1.0	μF
Boost Regulator Inductor	L		1.0	2.2	3.3	μH
Boost Regulator Input Capacitor	C_S	Ceramic	10	22		μF
Boost Regulator Output Capacitor	C_{PVOUT}	Ceramic	22	44		μF
		Electrolytic or Tantalum (Note 4)	100	220		μF
Supply Decoupling Capacitors		@ VBAT, PVDD, AVDD, BVDD		1		μF
Ambient Temperature	T_A		-40		85	°C
Operating Mode Control	SDRIVE	High η Drive, Boost regulator Enabled	Short to GND			
		Soft Drive, Boost regulator Disabled	Unconnected			
		Soft Drive, Boost regulator Enabled	Short to VBAT			
Boosted Voltage Select	PVDDS0/1	PVDD=8.0V	PVDDS1=Low			
		PVDD=7.4V	PVDDS1=High, PVDDS0=High			
		PVDD=6.8V	PVDDS1=High, PVDDS0=Low			
Voltage Gain Select	GAIN	750 / (R_{IN} + 37.5)	Short to GND			
		750 / (R_{IN} + 15)	Unconnected			
		750 / (R_{IN} + 25)	Short to VBAT			
ALC Mode Control	ALC	ALC-1	Short to GND			
		ALC-2	Unconnected			
		Non-ALC	Short to VBAT			
Battery Tracking AGC Control	VKNEE	Battery Tracking AGC De-biased	Short to GND			
		VKNEE=3.1V	Unconnected			
		VKNEE=3.4V	Short to VBAT			

Note 4: Although larger output capacitances can facilitate higher voltage margin for higher output power at low frequencies, do not use any output capacitances more than 100μF as it might adversely slow the boost regulator's response to load transients to a large extent affecting audio dynamics when playing music.

IMPORTANT APPLICATION NOTES

1. It is crucial to place the ft2920 in close proximity to the inductor, Schottky diodes, and input/output capacitors of the boost regulator on the system board, minimizing parasitic resistances and inductances of high-current traces. Also, these passive components must be placed on the same layer with ft2920 and connected with wide and short metal lines without vias. Failure to do a proper layout on the system board can result in significant degradation of maximum output power, efficiency, THD, and EMI performance. It might even induce excessive ringing at the switch node LX and damage the device permanently.
2. Use wide open areas on the top and bottom layers of the system board as the ground plane (GND) for ft2920. Place lots of solid vias connecting the top and bottom layers of GND. Furthermore, for proper thermal dissipation, reserve wide and uninterrupted GND areas along the thermal flow on the top layer, i.e., no wires cutting through the GND layer and obstructing the thermal flow.
3. The ft2920 is packaged with an exposed thermal pad on the underside of the device. Solder the thermal pad directly onto a large grounded metal island, as a thermal sink, underneath the package for proper thermal dissipation. On the grounded metal island, place several rows of solid, equally-spaced vias connecting to the bottom layer of GND. Failure to do so can severely limit its thermal dissipation capability. It might even cause the device going into over-temperature shutdown occasionally.
4. All the ground pins (AGND, PGND and PGNDB) are directly connected to the ground plane (GND). The power supply inputs (PVDD) for the audio amplifier's output stage are directly connected to the output capacitors of the boost regulator with wide and short metal traces.
5. As a high-performance Class-G audio amplifier, the ft2910 requires adequate power supply decoupling to ensure its high-efficiency, low distortion, and low EMI. Place each decoupling capacitor as individually close to VBAT, AVDD, BVDD, and PVDD pins as possible.
6. For best noise performance, use differential inputs from the audio source for ft2920. In single-ended input applications, the unused input of ft2920 should be AC-grounded at the audio source.
7. For applications where speaker load resistances are 4Ω or less, use a pair of Schottky diodes in parallel instead of a single one to improve overall power efficiency and operational reliability of the boost regulator. Both diodes are rated for a current no less than 3A and a reverse breakdown voltage no less than 15V.
8. Additional EMI suppression can be achieved using a ferrite bead filter constructed from a ferrite bead and a capacitor, as shown in Figure 25. Choose a ferrite bead with a rated current no less than 2A for an 8Ω load and 3A for a 4Ω load. Also, place the ferrite beard filter tightly together and individually close to VOP and VON pins respectively.
9. Add a simple RC snubber circuit from the switch node LX to PGNDB, as shown in Figure 21, to lower the peak voltage at LX during PWM switching, reduce EMI emissions, and improve operational reliability of the boost regulator.
10. Add a simple RC snubber circuit across two audio outputs (VOP and VON), as shown in Figure 26, to prevent the device from accelerated deterioration or abrupt destruction due to excessive inductive flybacks that are induced on fast output switching or by an over-current or short-circuit condition.
11. The operation of the battery tracking AGC can be highly influenced by the electrical characteristics of the battery. Place a small decoupling resistor of 10Ω between the battery supply voltage and the VBAT pin, coupled with a decoupling capacitor of 1μF, mitigating the detrimental effect of high battery current ripples on the detection of battery voltage.
12. Place a small decoupling resistor of 10Ω between AVDD and PVDD pins, coupled with a decoupling capacitor of 1μF, preventing high frequency transients from interfering with the on-chip linear amplifiers.
13. Do not short either audio output (VOP or VON) directly to GND, AVDD, or PVDD as this may damage the device permanently.
14. Do not alter the PVDD setting while the device is in operation. To change the PVDD setting, the device must be first placed in either shutdown or mute mode for a minimum of 100 milliseconds.

FUNCTIONAL BLOCK DIAGRAM

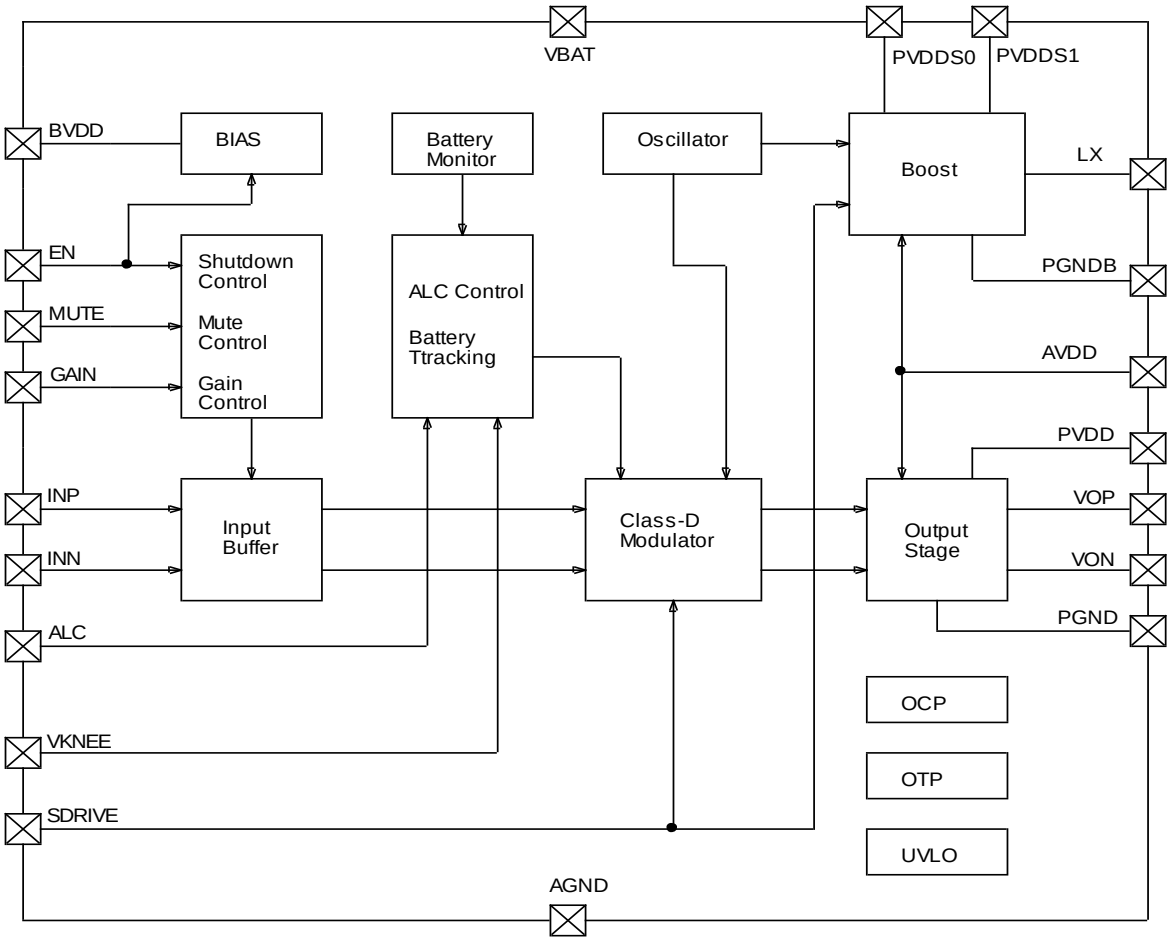


Figure 2: Simplified Functional Block Diagram of ft2920

ELECTRICAL CHARACTERISTICS

VBAT=3.6V, f=1kHz, Load=4Ω+33μH, L=2.2μH, C_{IN}=0.22μF, R_{IN}=0Ω (A_V=26dB), PVDDS1=Low, MUTE=Low, GAIN=Low, SDRIVE=Low, ALC=Low, VKNEE=Low, C_S=22μF, C_{PVOUT}=22μF//220μF, R_{VBAT}=10Ω, C_{VBAT}=1μF, R_{AVDD}=10Ω, C_{AVDD}=1μF, C_{BVDD}=1μF, C_{PVDD}=1μF, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VBAT	Supply Input Voltage		3.0		5.5	V
V_{UVLOUP}	Power-on Threshold Voltage	VBAT from Low to High		2.2		V
V_{UVLODN}	Power-off Threshold Voltage	VBAT from High to Low		2.0		V
I_{VBAT}	Supply Quiescent Current	Inputs AC-Grounded, No Load Mute=Low	3.5	5.0	7.0	mA
I_{MUTE}	Mute Supply Current	Inputs AC-Grounded, No Load Mute=High	3.0	4.2	6.0	mA
I_{SD}	Shutdown Supply Current	EN=Low			10	μA
BVDD	Voltage Reference	V_{IN}=0.14V_{RMS}, No Load	4.7	5.0	5.3	V
V_{IH}	Digital High Input Voltage	EN, MUTE, PVDDS0/1	1.2			V
		GAIN, ALC, VKNEE, SDRIVE	VBAT-0.5		VBAT	V
V_{IL}	Digital Low Input Voltage	EN, MUTE, PVDDS0/1 GAIN, ALC, VKNEE, SDRIVE			0.4	V
R_{DOWN}	Pulldown Resistor to Ground	EN, MUTE, PVDDS0/1 GAIN, ALC, VKNEE, SDRIVE		300		kΩ
R_{UP}	Pullup Resistor to VBAT	GAIN, ALC, VKNEE, SDRIVE		300		kΩ
T_{OTSD}	Over-Temperature Threshold			160		°C
T_{HYS}	Over-Temperature Hysteresis			20		°C
BOOST REGULATOR						
PVDD	Boosted Voltage (No Load)	PVDDS1=Low	7.7	8.0	8.2	V
		PVDDS1=High, PVDDS0=High	7.1	7.4	7.6	V
		PVDDS1=High, PVDDS0=Low	6.5	6.8	7.0	V
f_{BOOST}	Boost Regulator Frequency			750		kHz
CLASS-D AMPLIFIER (SDRIVE=Low, High Efficiency Drive)						
$P_{O, MAX}$	Maximum Output Power R_L=4Ω+33μH, THD+N=10%	PVDD=8.0V		8.0		W
		PVDD=7.4V		6.8		W
		PVDD=6.8V		5.7		W
	Maximum Output Power R_L=4Ω+33μH, THD+N=1%	PVDD=8.0V		6.4		W
		PVDD=7.4V		5.4		W
		PVDD=6.8V		4.5		W
	Maximum Output Power R_L=8Ω+33μH, THD+N=10%	PVDD=8.0V		4.4		W
		PVDD=7.4V		3.8		W
		PVDD=6.8V		3.1		W
	Maximum Output Power R_L=8Ω+33μH, THD+N=1%	PVDD=8.0V		3.5		W
		PVDD=7.4V		3.0		W
		PVDD=6.8V		2.5		W
$P_{O, ALC}$	ALC Output Power R_L=4Ω+33μH	PVDD=8.0V, V_{IN}=0.25V_{RMS}		6.0		W
		PVDD=7.4V, V_{IN}=0.22V_{RMS}		5.1		W
		PVDD=6.8V, V_{IN}=0.20V_{RMS}		4.2		W
	ALC Output Power R_L=8Ω+33μH	PVDD=8.0V, V_{IN}=0.25V_{RMS}		3.3		W
		PVDD=7.4V, V_{IN}=0.22V_{RMS}		2.8		W
		PVDD=6.8V, V_{IN}=0.20V_{RMS}		2.3		W

ELECTRICAL CHARACTERISTICS (Cont'd)

VBAT=3.6V, f=1kHz, Load=4Ω+33μH, L=2.2μH, C_{IN}=0.22μF, R_{IN}=0Ω (A_V=26dB), PVDDS1=Low, MUTE=Low, GAIN=Low, SDRIVE=Low, ALC=Low, VKNEE=Low, C_S=22μF, C_{PVOUT}=22μF//220μF, R_{VBAT}=10Ω, C_{VBAT}=1μF, R_{AVDD}=10Ω, C_{AVDD}=1μF, C_{BVDD}=1μF, C_{PVDD}=1μF, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
CLASS-D AMPLIFIER (Cont'd)						
THD+N	Total Harmonic Distortion+Noise (Non-ALC Mode)	R_L=4Ω, V_{IN}=0.14V_{RMS} (Po=3W)		0.07		%
		R_L=8Ω, V_{IN}=0.14V_{RMS} (Po=1.5W)		0.07		%
	Total Harmonic Distortion+Noise (ALC Mode)	R_L=4Ω, V_{IN}=0.25V_{RMS} (Po=6W)		0.4		%
		R_L=8Ω, V_{IN}=0.25V_{RMS} (Po=3.3W)		0.4		%
η	Power Efficiency (Excluding the power dissipated by the external Schottky diode)	Passthrough Mode, R_L=4Ω, Po=0.3W		80		%
		Boost-1 Mode, R_L=4Ω, Po=1.5W		82		%
		Boost-2 Mode, R_L=4Ω, Po=4W		76		%
A_V	Overall Voltage Gain	R_{IN}=15kΩ, GAIN=Unconnected		28		dB
		R_{IN}=15kΩ, GAIN=High		26		dB
		R_{IN}=15kΩ, GAIN=Low		23		dB
R_{IN}	Input Resistance @ INP & INN	GAIN=Unconnected		15		kΩ
		GAIN=High		25		kΩ
		GAIN=Low		37.5		kΩ
$V_{IN, MAX}$	Maximum Input Level THD+N =0.3% (ALC Mode)	R_{IN}=15kΩ, GAIN=Unconnected		0.70		V_{RMS}
		R_{IN}=15kΩ, GAIN=High		0.88		V_{RMS}
		R_{IN}=15kΩ, GAIN=Low		1.20		V_{RMS}
V_{COMM}	Input Common-Mode Bias @ INP, INN	VKNEE=Low		1.4		V
		VKNEE=Unconnected		1.4		V
		VKNEE=High		1.6		V
R_{OUT-SD}	Output Resistance in Shutdown @ VOP, VON	EN=Low		2.5		kΩ
V_{OS}	Output Offset Voltage	No Load		±10		mV
V_N	Idle-Channel Noise	AV=28dB, Inputs AC-Grounded A-weighted		200		$μV_{RMS}$
PSRR	Power Supply Rejection Ratio	f=1kHz, Inputs AC-Grounded		65		dB
CMRR	Common Mode Rejection Ratio	f=1kHz		70		dB
SNR	Signal-to-Noise Ratio	Maximum Output (5V_{RMS}), R_L=4Ω AV=28dB, A-weighted		90		dB
T_{STUP}	Startup Time			80		ms
T_{SD}	Shutdown Settling Time			40		ms
f_{SW}	PWM Output Carrier Frequency			375		kHz
I_{LIMIT}	Over-Current Limit	PVDDS1=Low		3.7		A
		PVDDS1=High, PVDDS0=High		3.4		A
		PVDDS1=High, PVDDS0=Low		3.1		A

ELECTRICAL CHARACTERISTICS (Cont'd)

VBAT=3.6V, f=1kHz, Load=4Ω+33μH, L=2.2μH, C_{IN}=0.22μF, R_{IN}=0Ω (A_V=26dB), PVDDS1=Low, MUTE=Low, GAIN=Low, SDRIVE=Low, ALC=Low, VKNEE=Low, C_S=22μF, C_{PVOUT}=22μF//220μF, R_{VBAT}=10Ω, C_{VBAT}=1μF, R_{AVDD}=10Ω, C_{AVDD}=1μF, C_{BVDD}=1μF, C_{PVDD}=1μF, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
AUTOMATIC LEVEL CONTROL (Note 5)						
A_{MAX}	Maximum ALC Attenuation	PVDDS1=Low		11		dB
T_{ATTACK}	ALC Attack Time (V_{IN}=0.18V_{RMS} → 0.57V_{RMS})	ALC-1 Mode (ALC=Low)		8		ms
		ALC-2 Mode (ALC=Unconnected)		16		ms
$T_{RELEASE}$	ALC Release Time (V_{IN}=0.57V_{RMS} → 0.18V_{RMS})	ALC-1 Mode (ALC=Low)		1000		ms
		ALC-2 Mode (ALC=Unconnected)		500		ms
Note 5: The device operates in Non-ALC mode when ALC pin is asserted High.						
VOLUME FADE-IN & FADE-OUT						
T_{FADEIN}	Fade-In Time			20		ms
$T_{FADEOUT}$	Fade-Out Time			20		ms
BATTERY TRACKING AGC (Note 6)						
V_{KNEE}	Knee Voltage	VKNEE=High		3.4		V
		VKNEE=Unconnected		3.1		V
S_{ATT}	Output Attenuation Slope	@ VOP, VON		3		V/V
Note 6: The battery tracking AGC is disabled when either VKNEE pin is pulled Low or ALC pin asserted High.						
CLASS-D AMPLIFIER (SDRIVE=High, Soft Drive)						
THD+N	Total Harmonic Distortion+Noise (Non-ALC Mode)	R_L=4Ω, V_{IN}=0.14V_{RMS} (Po=3W)		0.07		%
		R_L=8Ω, V_{IN}=0.14V_{RMS} (Po=1.5W)		0.07		%
	Total Harmonic Distortion+Noise (ALC Mode)	R_L=4Ω, V_{IN}=0.25V_{RMS} (Po=6W)		0.4		%
		R_L=8Ω, V_{IN}=0.25V_{RMS} (Po=3.3W)		0.4		%
η	Power Efficiency (Excluding the power dissipated by the external Schottky diode)	Passthrough Mode, R_L=4Ω, Po=0.3W		75		%
		Boost-1 Mode, R_L=4Ω, Po=1.5W		76		%
		Boost-2 Mode, R_L=4Ω, Po=4W		67		%

Note 7: All parameters are measured according to the conditions specified in Electrical and Typical Performance Characteristics sections with the following notes, unless otherwise specified:

7.1 The two differential inputs are shorted for common-mode input voltage measurement. All other parameters are taken with input resistors R_{IN}=0Ω and input capacitors C_{IN}=0.22μF, unless otherwise specified.
7.2 The boost regulator's supply decoupling capacitor C_S=22μF is placed close to the boost regulator's inductor.
7.3 The boost regulator's inductor L=2.2μH and Schottky diodes are placed close to the LX pins.
7.4 The boost regulator's output capacitors C_{PVOUT}=22μF//220μF are placed close to the Schottky diodes.
7.5 The boosted supply decoupling capacitors C_{PVDD}=1μF are placed close to individual PVDD pins.
7.6 An output inductor of 33μH is placed in series with the load resistor to emulate a speaker load for all AC and dynamic parameters.
7.7 A 33kHz lowpass filter is added even if the analyzer has an internal lowpass filter. An RC lowpass filter (100Ω, 47nF) is used on each output for the data sheet graphs.

TYPICAL PERFORMANCE CHARACTERISTICS

VBAT=3.6V, f=1kHz, Load=4Ω+33μH, L=2.2μH, C_{IN}=0.22μF, R_{IN}=0Ω (A_V=26dB), PVDDS1=Low, MUTE=Low, GAIN=Low, SDRIVE=Low, ALC=Low, VKNEE=Low, C_S=22μF, C_{PVOUT}=22μF//220μF, R_{VBAT}=10Ω, C_{VBAT}=1μF, R_{AVDD}=10Ω, C_{AVDD}=1μF, C_{BVDD}=1μF, C_{PVDD}=1μF, T_A=25°C, unless otherwise specified.

List of Performance Characteristics

DESCRIPTION	CONDITIONS	FIGURE #
Output Power vs. Supply Voltage	Vin=0.3V_{RMS}, PVDD=8.0V, R_L=4Ω+33μH VKNEE=High/Unconnected/Low	3
Output Peak Voltage vs. Supply Voltage	Vin=0.3V_{RMS}, PVDD=8.0V, R_L=4Ω+33μH VKNEE=High/Unconnected/Low	4
Output Power vs. Input Voltage	R_L=4Ω+33μH, ALC Mode, Av=28dB/26dB/23dB	5
	R_L=4Ω+33μH, ALC and Non-ALC Modes	6
Efficiency vs. Output Power (Excluding Schottky diodes' power dissipation)	R_L=4Ω+33μH, Non-ALC Mode SDRIVE=Low/High	7
THD+N vs. Output Power	R_L=4Ω+33μH, Non-ALC Mode	8
THD+N vs. Input Voltage	R_L=4Ω+33μH, ALC Mode	9
THD+N vs. Input Frequency	Po=3W, R_L=4Ω+33μH, ALC Mode	10
PSRR vs. Input Frequency	R_L=4Ω+33μH, Inputs AC-Grounded	11
Quiescent Current vs. Supply Voltage	Inputs AC-Grounded, No Load, Normal and Mute Modes	12
ALC Attack & Release Time	Vin=0.18V_{RMS} ~ 0.57V_{RMS}, R_L=4Ω+33μH ALC-1 Mode (ALC=Low)	13
	Vin=0.18V_{RMS} ~ 0.57V_{RMS}, R_L=4Ω+33μH ALC-2 Mode (ALC=Unconnected)	14
(VOP-VON) Startup Waveforms	R_L=4Ω+33μH, Vin=0.1V_{RMS}	15
(VOP-VON) Shutdown Waveforms	R_L=4Ω+33μH, Vin=0.1V_{RMS}	16
Wideband Output Spectrum	SDRIVE=High, R_L=4Ω+33μH, Vin=0.1V_{RMS}	17
	SDRIVE= Low, R_L=4Ω+33μH, Vin=0.1V_{RMS}	18
Voltage Gain vs. Input Frequency	Vin=0.1V_{RMS}, Cin=1μF, PVDD=8.0V, R_L=4Ω+33μH, 33kHz Lowpass Filter	19
Mode Transitions of Boost Regulator	R_L=4Ω+33μH	20

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

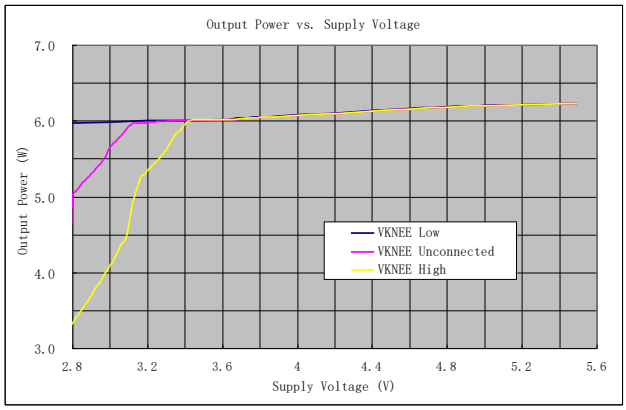


Figure 3: Output Power vs. Supply Voltage

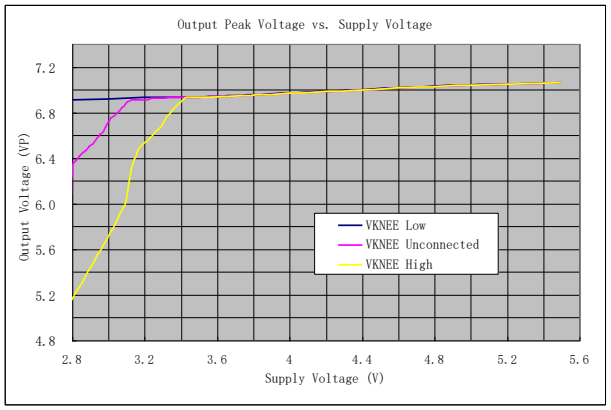


Figure 4: Output Peak Voltage vs. Supply Voltage

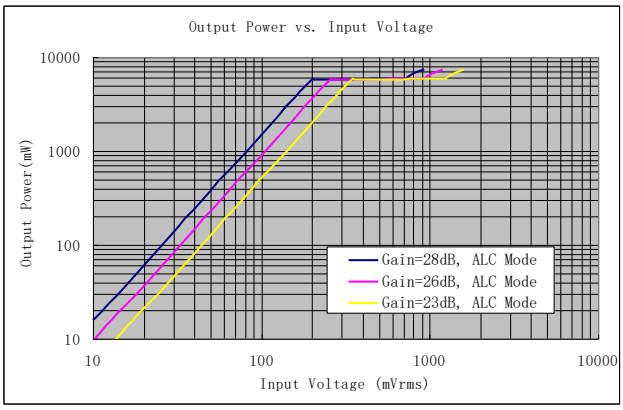


Figure 5: Output Power vs. Input Voltage

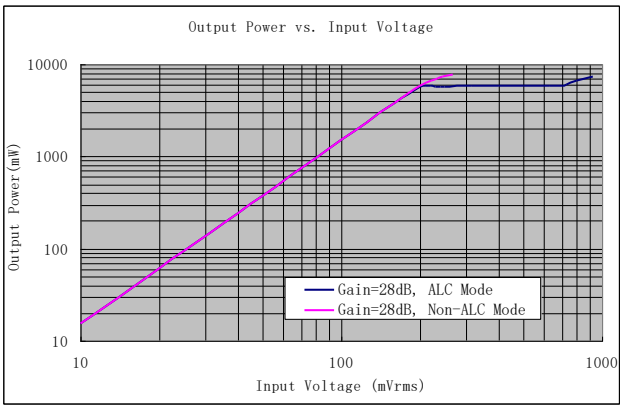


Figure 6: Output Power vs. Input Voltage

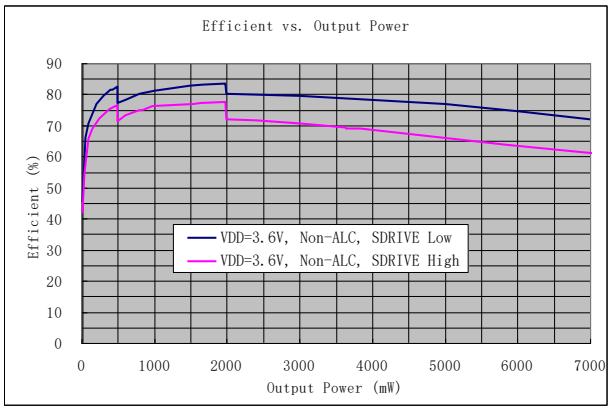


Figure 7: Efficiency vs. Output Power
(Excluding Schottky diodes' power dissipation)

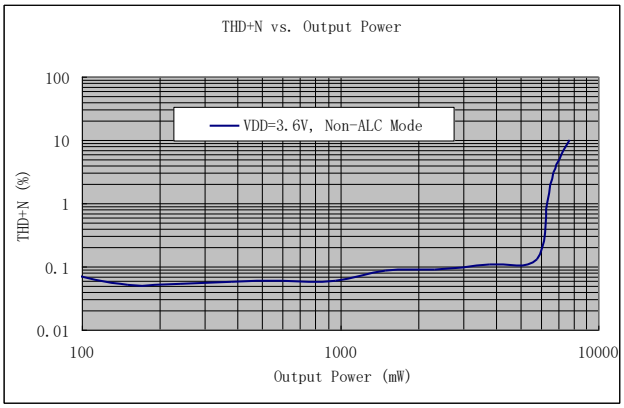


Figure 8: THD+N vs. Output Power

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

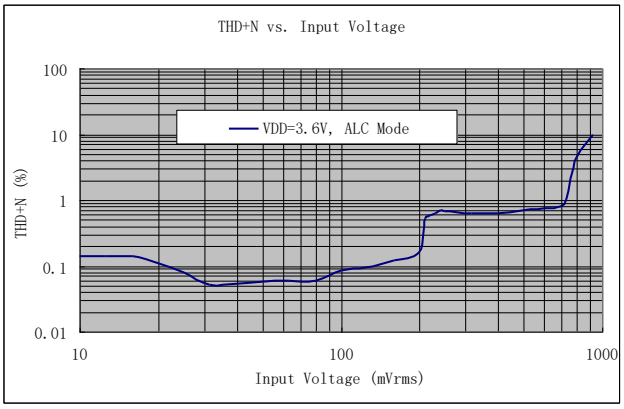


Figure 9: THD+N vs. Input Voltage

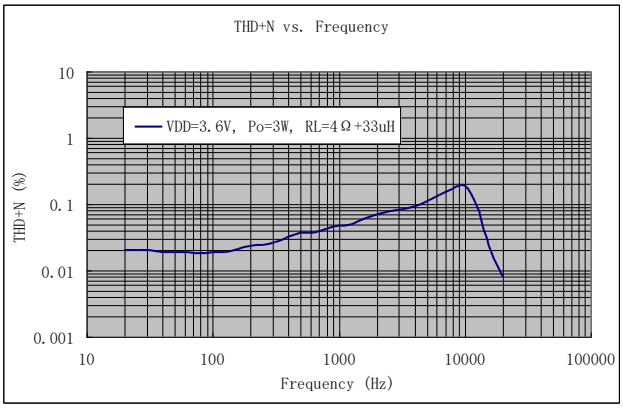


Figure 10: THD+N vs. Frequency

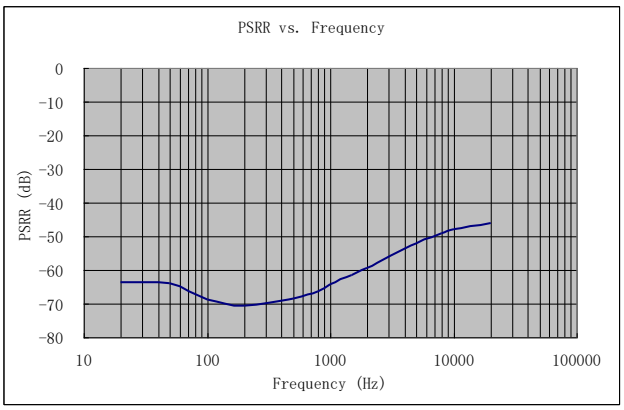


Figure 11: PSRR vs. Input Frequency

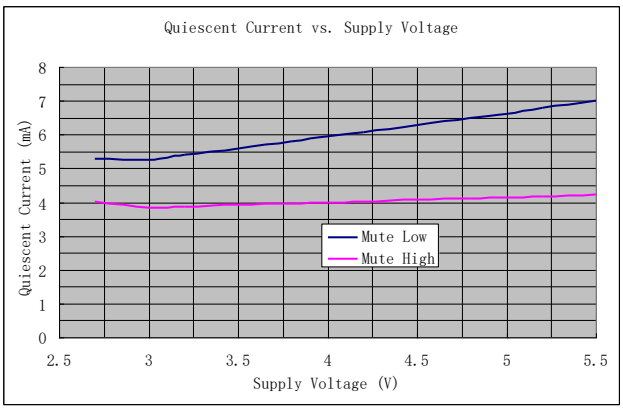


Figure 12: Quiescent Current vs. Supply Voltage

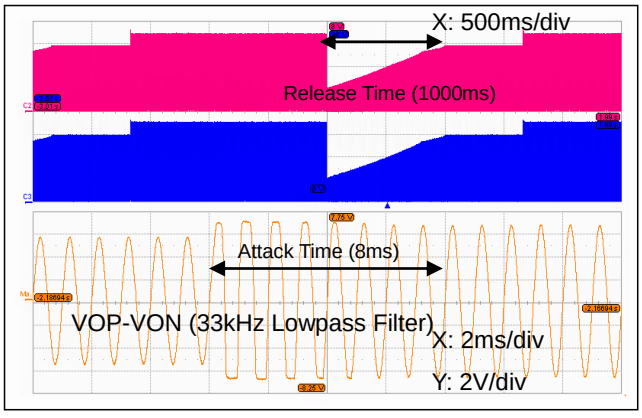


Figure 13: ALC-1 Attack & Release Time

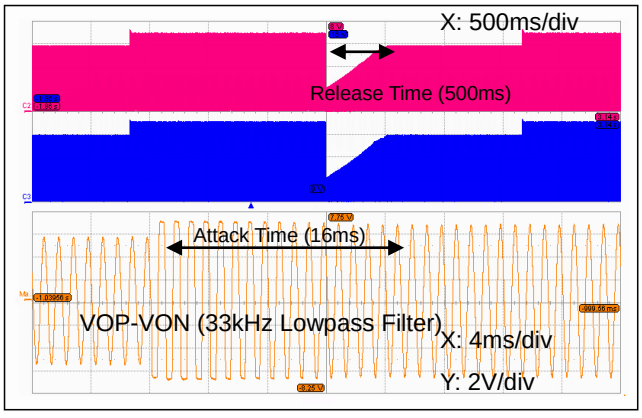


Figure 14: ALC-2 Attack & Release Time

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

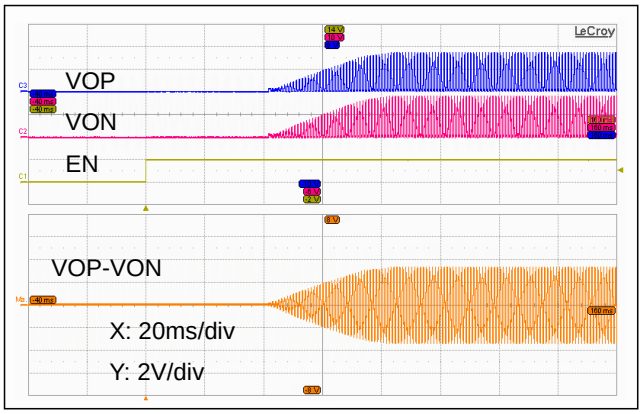


Figure15: Startup Waveforms

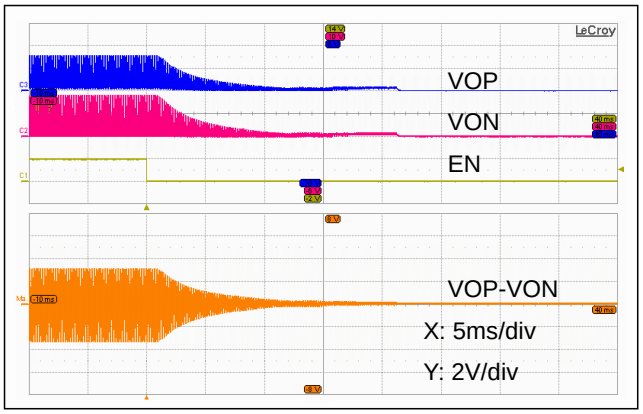


Figure 16: Shutdown Waveforms

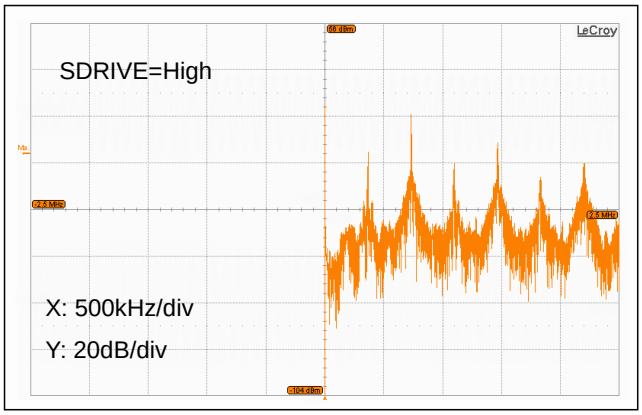


Figure 17: Wideband Output Spectrum

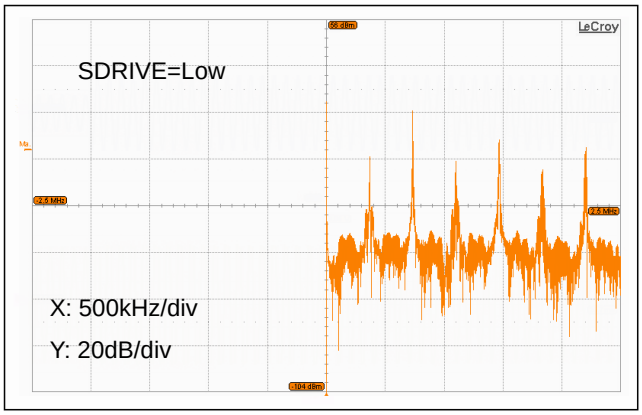


Figure 18: Wideband Output Spectrum

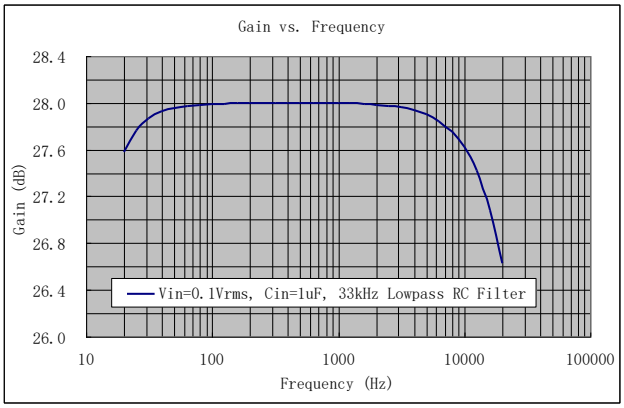


Figure 19: Voltage Gain vs. Input Frequency

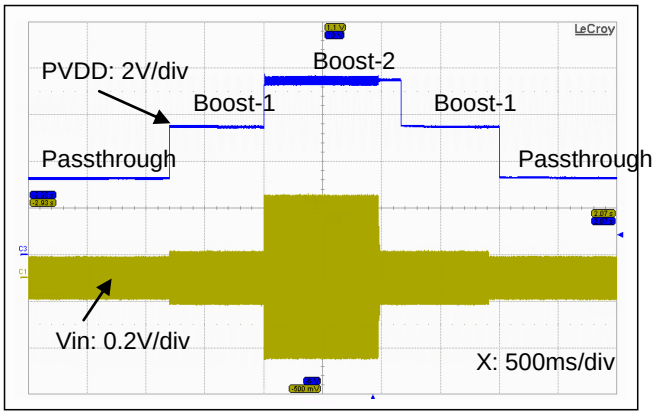


Figure 20: Mode Transition of Boost Regulator

APPLICATION INFORMATION

The ft2920 is a highly efficient 8W boosted Class-G audio power amplifier with automatic level control (ALC) and battery tracking AGC. It integrates a filterless Class-D audio amplifier with an adaptive Class-G boost regulator and operates with a range of supply voltages from 3V to 5.5V. With a supply voltage at 3.6V, it can deliver an output power of 8W with 10% THD+N, or 6.4W with 1% THD+N, into a 4Ω speaker load.

In ft2920, the power supply rail of the audio amplifier's output stage is boosted and regulated by an asynchronous PWM switching regulator with an integrated power switch. The boost regulator employs current-mode PWM control with proprietary multi-level operation to regulate the boosted output voltage. The adaptive nature of the Class-G boost regulator, whose output voltage varies dynamically in response to the voltage level of the audio output, improves overall power efficiency and extends battery life when playing music. The higher output power and greater power efficiency resulted from the Class-G boost regulator make ft2920 an ideal audio solution for battery-powered electronic devices.

The ft2920 features two modes of operation, i.e., ALC and Non-ALC, which can be selected via the ALC pin. When the ALC pin is shorted to VBAT, the ft2920 operates in Non-ALC mode, where the audio amplifier is configured as a conventional Class-D amplifier without ALC. Conversely, when the ALC pin is unconnected or shorted to GND, the ft2920 operates in ALC mode, where it constantly monitors and safeguards the audio output against the boosted supply voltage, preventing output clipping distortion, excessive power dissipation, and speaker over-load. Once an over-level condition is detected, the ALC lowers the voltage gain of the audio amplifier proportionally to eliminate output clipping while maintaining at a maximally-allowed dynamic range of the audio output. The ft2920 features two ALC dynamic characteristics for two distinctive sound effects, which are also selected via the ALC pin. In ALC mode, with a supply voltage at 3.6V, the ft2920 can deliver an ALC output power of 6W with 0.4% THD+N, into a 4Ω speaker load.

In conjunction with ALC, as the battery supply voltage drops below a prescribed value, the battery tracking AGC lowers the voltage gain of the audio amplifier to limit the peak audio output, thus preventing the collapse of battery voltage.

Furthermore, the Class-D audio amplifier of ft2920 features a filterless PWM modulator that substantially lowers or completely eliminates the requirement for an external LC filter, thus reducing the number of external components, the system board space, and the system cost.

As specifically designed for portable applications, the ft2920 incorporates shutdown mode to minimize the power consumption. It also includes comprehensive protection features against various operating faults such as over-current, short-circuit, over-temperature, or under-voltage for a safe and reliable operation.

ADAPTIVE BOOST REGULATOR

To allow for higher audio loudness, an adaptive boost regulator is integrated in ft2920 to boost PVDD, the power rail of the audio amplifier's output stage, from VBAT to a higher value. The boosted supply voltage PVDD can be set via PVDDS1 and PVDDS0 pins, as described in Table 1. For proper operation, PVOUT, the output voltage of the boost regulator, must be directly shorted to PVDD with sufficiently wide metal trace on the system board.

PVDDS1	PVDDS0	PVDD (V)	Speaker Load (Ω)	ALC Output Power (W) (0.2% THD+N)	Output Power (W) (1% THD+N)	Output Power (W) (10% THD+N)
High	Low	6.8	4	4.2	4.5	5.7
			8	2.3	2.5	3.1
High	High	7.4	4	5.1	5.4	6.8
			8	2.8	3.0	3.8
Low	X	8.0	4	6.0	6.4	8.0
			8	3.3	3.5	4.4

Table 1: Boosted Voltage Select

Do not alter the logic state of either PVDDS0 or PVDDS1 pin while the device is in operation. To modify the PVDD setting, the device must be first placed in shutdown or mute mode for a minimum of 100 milliseconds before the logic state of either PVDDS0 or PVDDS1 pin can be changed. Failure to do it properly may damage the device permanently.

The integrated boost regulator employs fixed-frequency, peak-current PWM scheme with current-mode control. The PWM switching frequency is internally set at 750kHz, requiring small external inductor and output capacitor. The adaptive boost regulator features proprietary multi-stage operation. As the audio output is higher than the first prescribed value for an extended period of time, the ft2920 enters into Boost-1 mode, where the boost regulator is activated to boost and regulate PVDD at an intermediate value. As the audio output grows higher than the second prescribed value for an extended period of time, the ft2920 enters into Boost-2 mode, where PVDD is further boosted and regulated at its final value set by the PVDDS1 and PVDDS0 pins.

On the other hand, when the audio output is reduced lower than the second prescribed value for an extended period of time, the boost regulator returns back to Boost-1 mode. If the audio output is further reduced lower than the first prescribed value for an extended period of time, the boost regulator will be de-biased. In this case, the ft2920 is forced into Passthrough mode where the audio amplifier's output stage is powered directly from the system power supply VDD, through the external inductor and Schottky diode. Note that in the Passthrough mode, PVDD is equal to the supply input voltage minus the forward voltage drop of the Schottky diode. The adaptive nature of the boost regulator can improve overall efficiency when playing audio and thus extend battery life.

BOOST REGULATOR DESIGN REQUIREMENTS

Selection of Boost Regulator Inductor

The selection of the inductor is the most important parameter in the design of power switching regulators since it affects boost regulator's steady-state operation as well as its dynamic response and loop stability. Three important inductor specifications are to be considered: Inductor value, DC resistance (DCR), and Saturation current. Note that inductor values may have tolerance up to ±20% with zero-current bias. Also, when the inductor current approaches its saturation limit, the effective inductance can fall to a fraction of its zero-current value. Table 2 shows the recommended inductor peak (saturation) current ratings for typical applications of ft2920.

PVDD (V)	R_{LOAD} (Ω)	L (μH)	I_{PEAK} (A)
8.0	4	2.2 ~ 3.3	6
7.4	4	2.2 ~ 3.3	5
6.6	4	2.2 ~ 3.3	4
8.0	8	1.5 ~ 2.2	3
7.4	8	1.5 ~ 2.2	3
6.6	8	1.5 ~ 2.2	2

Table 2: Recommended Inductor Peak (Saturation) Current Ratings

In general, a larger inductance value produces less inductor current ripple, which results in lower inductor peak current, higher output current, lower EMI, and higher efficiency. On the other hand, a smaller inductance value, with a physically small size, results in an improved load transient response with higher inductor peak current, potentially worse EMI, and lower efficiency. An inductor in the range from 1.0μH to 3.3μH suffices for most applications of ft2920. Do not use any inductance higher than 4.7μH as it requires a larger output capacitance for stability of the PWM control loop, which in turn slows the boost regulator's response to load transients to a large extent with little improvement on the output current capability or efficiency. Select an inductor with DCR less than 30mΩ for higher overall power efficiency (from the system power supply to the speaker load).

Selection of Output Capacitor

The output capacitor of the boost regulator is required to keep the output voltage ripple small and ensure the stability of the PWM control loop. The output capacitor must have low equivalent-series-resistance (ESR) at

the PWM switching frequency, so ceramic capacitors are the best choice. Make sure that the output capacitor maintains its capacitance over the specified range of DC bias and operating temperature. A 22μF low-ESR ceramic capacitor suffices for most applications with speaker load impedances of 8Ω. For applications where the speaker load impedances are 4Ω or less, use 22//220μF low-ESR ceramic capacitors.

Also, add a small, good quality, low-ESR ceramic capacitor of 0.1μF in close proximity to the Schottky diodes for high-frequency filtering.

Although larger output capacitances can facilitate higher voltage margin for higher audio power at low frequencies, do not use any output capacitance higher than 220μF as it might adversely slow the boost regulator's response to load transients to a large extent affecting audio dynamics when playing music.

The boost regulator's output, PVOUT, must be externally connected to the power supply rail of the audio amplifier's output stage, PVDD, on the system board with wide and short metal traces.

Selection of Schottky Diode

The high PWM switching frequency of ft2920 demands fast rectification for optimum efficiency. It is essential that the diode's average and peak current ratings exceed the average output current and peak inductor current. Furthermore, the diode must be rated for a reverse breakdown voltage higher than the regulated output voltage and also for the power dissipation greater than the value calculated by Equation 1. In the equation, V_D is the forward voltage drop of the Schottky diode and I_O the average output current.

$$P_D = V_D \times I_O \quad (1)$$

For higher power applications, use a pair of Schottky diodes in parallel instead of a single Schottky diode to enhance the overall power efficiency and reliability of the boost regulator. In this case, both diodes are rated for a current higher than 3A and a reverse breakdown voltage higher than 15V.

Selection of Supply Input Capacitor

In practice, supply input capacitors are required for boost regulators. The supply input capacitor acts as a charge reservoir for the inductor current, providing energy faster than the system power supply, mitigating current surges or voltage droops of the supply voltage.

At least 10μF of input capacitance is required for supply decoupling for ft2920. The rated voltage of the input capacitor must be higher than the supply input voltage with sufficient tolerance to limit the effects of dc bias. For most applications where the power supply is reasonably designed, a low-ESR ceramic capacitor of 22μF, 16V with 10mΩ ESR is sufficient for ft2920. Also, add a small, good quality, low-ESR ceramic capacitor of 0.1μF in close proximity to the inductor for high-frequency supply decoupling.

For applications where additional input capacitance is required to meet the requirement of the input current ripple or transient response, place an electrolytic or tantalum bulk capacitor between 47μF and 100μF in close proximity to ft2920. The bulk capacitor acts as a charge reservoir for the inductor current, providing energy faster than the system power supply, mitigating current surges and/or voltage droops of the supply voltage.

Boost Regulator Snubber Circuit

It is not uncommon for a boost regulator to observe voltage oscillations in a frequency range of 100 ~ 200MHz at the switch node LX due to parasitic inductances and capacitances on its high-current traces. If the amplitude of the voltage ringing is above the absolute maximum rating of the LX pin, the on-chip power switch can be damaged permanently.

For applications where excessive voltage spikes or oscillations are observed due to severe restrictions on the board layout, it may become necessary to add a snubber circuit from the switch node LX to the power ground PGNDB to lower voltage spikes and eliminate voltage oscillations at the switch node. A snubber circuit, a small resistor in series with a small capacitor, is an energy-absorbing circuit to provide an alternative path to ground for the current flowing through the parasitic inductances. In practice, the snubber circuit is added to lower EMI emissions as well as enhance the operational reliability of the boost regulator.

Figure 21 shows an RC snubber circuit with suggested values of R_{LX}=1Ω and C_{LX}=2.2 ~ 10nF. Note that the design of the RC snubber circuit is specific to each individual application and board layout, thus the parasitic inductances and capacitances must be taken into consideration to reach proper values of R_{LX} and C_{LX}. Evaluate and ensure that the voltage spikes at LX are within the absolute maximum rating of LX on the actual system board. Pay close attention to the layout of the snubber circuit to be tight and in close proximity to LX and PGNDB pins.

Note that the RC snubber circuit will adversely affect the overall efficiency of the boost regulator by a few percent, which is a function of the C_{LX} value.

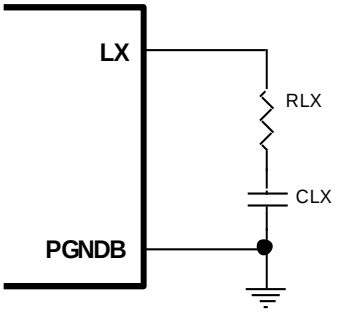


Figure 21: Boost Regulator RC Snubber Circuit

AUTOMATIC LEVEL CONTROL (ALC)

The automatic level control is to maintain the audio output signals for a maximum voltage swing without distortion when an excessive input that may cause output clipping is applied. With the ALC function, the ft2920 lowers the gain of the amplifier to an appropriate value such that the clipping at the outputs is substantially eliminated. It also eliminates the clipping of the output signal due to lower power-supply voltages.

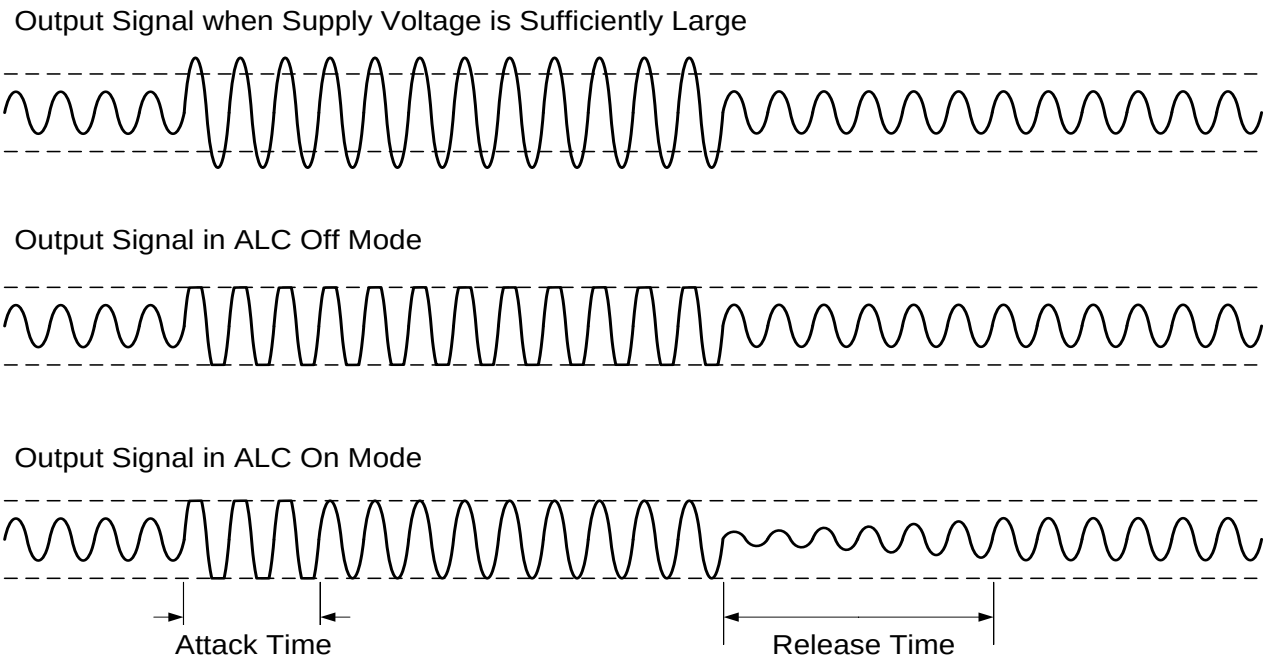


Figure 22: Automatic Level Control Diagram

The attack time and release time of ALC are shown in Table 3. The attack time is defined as the time interval required for the gain to fall to its steady-state gain less 3dB approximately, assumed that a sufficiently large input signal is applied. The release time is the time interval required for the amplifier to exit out of the present mode of operation.

ALC MODE CONTROL

The ft2920 can be configured in either ALC or Non-ALC mode via the ALC pin, as described in Table 3. If the ALC pin is set high, the ft2920 operates in Non-ALC mode. The Non-ALC operation is typically chosen for the applications where maximum audio loudness is much desired and possible output clipping distortion can be largely eliminated at the audio sources. In other two settings (low and unconnected) of the ALC pin, the ft2920 operates in ALC mode with two sets of dynamic response characteristics. For most applications, the ALC mode of operation is much preferred for its merits to eliminate output clipping distortion, excessive power dissipation, and speaker over-load.

As shown in Table 3, two different response times of the ALC control loop can be selected for different audio characteristics. The ALC-1 mode tends to play music in a mellower manner with minimum output clipping distortion. On the other hand, the ALC-2 mode tends to play music in a more dynamic manner with slightly higher average output power (loudness).

ALC	Mode of Operation	Attack Time (ms)	Release Time (ms)
Low	ALC-1	8	1000
Unconnected	ALC-2	16	500
High	Non-ALC	N/A	

Table 3: ALC Mode Control

VOLTAGE GAIN SETTING

In ft2920, the voltage gain of the audio amplifier is determined by the GAIN pin, as described in Table 4. In addition, the voltage gain can be externally adjusted by inserting additional input resistors, R_{IN}, in series with the input capacitors. In the equations in Table 4, A_V is the voltage gain of the amplifier and R_{IN} is the external input resistance in kΩ.

GAIN	Av	RIN=0kΩ		RIN=15kΩ	
		Av (V/V)	Av (dB)	Av (V/V)	Av (dB)
Low	750 / (RIN + 37.5)	20	26	14.3	23
High	750 / (RIN + 25)	30	30	18.8	26
Unconnected	750 / (RIN + 15)	50	34	25.0	28

Table 4: Voltage Gain Setting

The choice of the voltage gain will strongly influence the loudness and quality of audio sounds. In general, the higher the voltage gain is, the louder the sound is perceived. However, an excessive voltage gain may cause the audio output to be severely compressed (in ALC mode) or prematurely clipped (in Non-ALC mode) for high-level (loud) audio sounds. On the other hand, an unusually low gain may cause relatively low-level (quite) sounds soft or inaudible. Thus it is crucial to choose a proper voltage gain for well balanced audio quality.

The voltage gain is chosen based upon various system-level considerations including the supply voltage, the dynamic range of audio sources and speaker loads, and the desired sound effects. As a general rule, the voltage gain can be simply expressed in Equation 2. In the equation, $V_{IN,MAX}$ (in V_{RMS}) is the maximum input level from the audio source, PVDD (in volts) is the boosted supply voltage, and α is the design parameter, which ranges from 0.66 to 2.2. The higher α is, the higher the average output power (louder) is, with some degree of compression for high-level audio sounds.

$$A_V = \frac{\alpha \times PVDD}{V_{IN,MAX}} \qquad (2)$$

As a general guideline, Table 5 shows the voltage gains for various input levels and GAIN pin configurations with PVDD at 8.0V and α at about 1.25. In the table, R_{IN} is the external input resistor in series with the input capacitor. For other PVDD settings, Equation 2 can be used to calculate the input resistor in a similar manner.

$V_{IN, MAX}$ (V_{RMS})	GAIN Pin Configuration	R_{IN} (kΩ)	A_V (V/V)	A_V (dB)
0.50	Low	0	20	26
0.70		16	14	23
1.0		39	10	20
0.30	High	5.1	25	28
0.50		12	20	26
0.70		27	14	23
1.0		51	10	20
0.30	Unconnected	15	25	28
0.50		22	20	26
0.70		39	14	23

Table 5: Typical Voltage Gain Settings for Various Input Levels

BATTERY TRACKING AGC

The ft2920 features battery tracking AGC to limit the peak audio output as the battery voltage droops. Although it will affect audio output loudness, the battery tracking AGC limits high battery current at the end-of-charge battery voltage and consequently prevents the battery voltage from collapsing, which might cause a reset of the system. The battery tracking AGC keeps the peak audio output below a value that is a function of the battery supply voltage. The output peak voltage is maintained at PVDD for battery voltages down to the knee voltage and reduced proportionally at a rate of 3V/V for lower battery voltages. The knee voltage of the battery tracking AGC can be selected via the VKNEE pin, as described in Table 6. Note that the battery tracking AGC can be enabled only when the ALC function is enabled where the ALC pin is pulled low or left unconnected.

VKNEE	Knee Voltage (V)
Low	Battery Tracking AGC Disabled
Unconnected	3.1
High	3.4

Table 6: Battery Tracking AGC Control

The operation of the battery tracking AGC can be highly influenced by the electrical characteristics of the battery used with ft2920. Place a small decoupling resistor of 10Ω between the battery supply voltage and the VBAT pin, coupled with a small decoupling capacitor 1μF, minimizing the detrimental effect of high battery current ripples on the detection of battery voltage.

SOFT DRIVE MODE

To facilitate low-EMI operation to minimize FM interference, the ft2920 features proprietary edge-rate-control gate drivers for both Class-D audio amplifier and the Class-G boost regulator. In the soft drive mode, the EMI emissions will be largely reduced at the expense of lower power efficiency, however, much higher than the traditional Class-AB audio amplifiers. Furthermore, to further reduce EMI emissions, the boost regulator can be disabled at the expense of much lower maximum output power due to the limited power supply (the battery voltage) available to the audio amplifiers. Three operating modes are available in ft2920 and can be selected via the SDRIVE pin, as described in Table 7.

SDRIVE	Mode	Description
Low	Normal	High Efficiency, High Power Operation
Unconnected	Boost Disabled	Lowest EMI, Low Power Operation
High	Soft Drive	Low EMI, Medium Power Operation

Table 7: Soft Drive Mode Control

SHUTDOWN AND STARTUP

The ft2920 employs the EN pin to minimize power consumption while it is not in use. When the EN pin is pulled to ground, the ft2920 is forced into shutdown mode, where all the analog circuitry is de-biased and the supply current is thus reduced to less than 10μA, and the differential outputs are shorted to ground through an internal resistor (2.5kΩ) individually. Once in shutdown mode, the EN pin must remains low for at least 40ms (T_{SD}), the shutdown settling time, before it can be brought high again. When the EN pin is asserted high, the device exits out of the shutdown mode and enters into the normal mode of operation after the startup time (T_{STUP}) of 80ms.

Note that an internal pulldown resistor of 300kΩ is implemented onto the EN pin. Furthermore, the shutdown mode is the state when the power supply is first applied to the device. Whenever possible, it is recommended to assert EN high to exit the device out of the shutdown mode only after the device is properly started up. Also, place the amplifier in the shutdown mode prior to removing the power supply voltage.

MUTE CONTROL

In ft2920, the MUTE pin is used to control the operation of the output stages of both audio amplifiers. A logic-low on the MUTE pin enables the output stages of audio amplifiers. A logic-high on the MUTE pin disables the output stages of audio amplifiers. In the latter case, the differential audio outputs VOP and VON are pulled to ground through on-chip resistors individually.

VOLUME FADE-IN & FADE-OUT

The volume fade-in and fade-out operate automatically whenever EN or MUTE pin is toggled. The fade-in/out function reduces intermittent sound considerably and eliminates uncomfortable hearing experiences during the transitions that the device is enabled or shutdown.

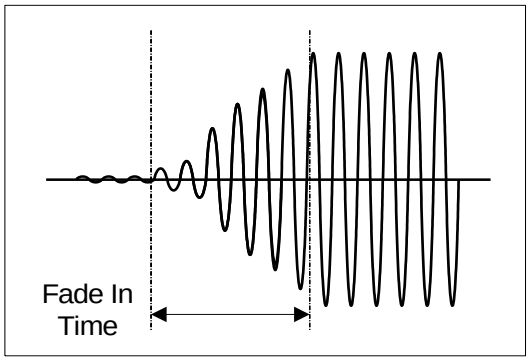


Figure 23: Fade-In Waveform

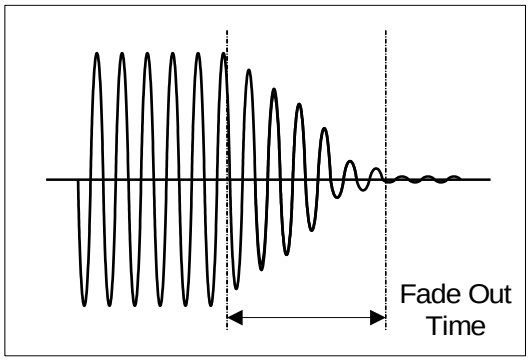


Figure 24: Fade-Out Waveform

CLICK-AND-POP SUPPRESSION

The ft2920 features comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces any audible transients internal to the device. When entering into shutdown, the differential audio outputs ramp down to ground quickly and simultaneously.

PSRR ENHANCEMENT

Without a dedicated pin for the common-mode voltage bias, the ft2920 achieves a PSRR, 65dB at 1kHz.

PROTECTION MODES

Against possible operating faults for safe operation, the ft2920 features various protection functions including Under-Voltage Lockout (UVLO), Over-Current Protection (OCP), and Over-Temperature Shutdown (OTSD).

Under-Voltage Lockout (UVLO)

The ft2920 incorporates a circuitry to detect a low supply voltage for a safe and reliable operation. When the supply voltage is first applied, the ft2920 will remain inactive until the supply voltage exceeds 2.2V (V_{UVLU}). When the supply voltage is removed and drops below 2.0V (V_{UVLD}), the ft2920 enters into shutdown mode immediately.

Over-Temperature Shutdown (OTSD)

When the die temperature exceeds a preset threshold (160°C), the device enters into the over-temperature shutdown mode, where two differential outputs are pulled to ground through an internal resistor (2.5kΩ) individually. The device will resume its normal operation once the die temperature returns to a lower temperature, which is 20°C lower than the threshold.

Over-Current Protection (OCP)

During operation, the output of Class-D amplifier constantly monitors for any over-current and/or short-circuit conditions. When a short-circuit condition between two differential outputs, differential output to PVDD or PGND is detected, the output stage of the amplifier is immediately forced into high impedance state. Once the fault condition persists over a prescribed period, the ft2920 then enters into the shutdown mode and remains in this mode for about 40ms (T_{OCP}), the over-current recovery time. When the shutdown mode times out, the ft2920 will initiate another start-up sequence and then check if the short-circuit condition has been removed. If the fault condition is still present, the ft2920 will repeat itself for the process of a start-up followed by detection, qualification, and shutdown. It is so-called the hiccup mode of operation. Once the fault condition is removed, the ft2920 automatically restores to its normal mode of operation.

Although the output stage of the Class-D audio amplifiers can withstand a short between VOP and VON, do not connect either output directly to AGND, PGND, PGNDB, AVDD, or PVDD as this might damage the device permanently.

CLASS-D AUDIO AMPLIFIER

The Class-D audio amplifier in the ft2920 operates in much the same way as traditional Class-D amplifiers and similarly offers much higher power efficiency than Class-AB amplifiers. The high efficiency of Class-D operation is achieved by the switching operation of the output stage of the amplifier. The power loss associated with the output stage is limited to the conduction and switching loss of the power switches, which are much less than the power loss associated with a linear output stage in Class-AB amplifiers.

Fully Differential Amplifier

The ft2920 includes a fully differential amplifier with differential inputs and outputs. The fully differential amplifier ensures that the differential output voltage is equal to the differential input voltage times the amplifier gain. Although the ft2920 supports for a single-ended input, differential inputs are much preferred for applications where the environment can be noisy in order to ensure maximum SNR.

Low-EMI Filterless Output Stage

Traditional Class-D audio amplifiers require for the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. The ft2920 applies an edge-rate control circuitry to reduce EMI emissions, while maintaining high power efficiency.

Filterless Design

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filter adds cost, increases the solution size of the amplifier, and can adversely affect efficiency and THD+N performance. The traditional PWM scheme uses large differential output swings (twice of the supply voltage) and causes large ripple currents. Any parasitic resistance in the filter components results in loss of power and lowers the efficiency.

The ft2920 does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. By eliminating the output filter, a smaller, less costly, and more efficient solution can be accomplished.

Because the frequency of the ft2920 output is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimum performance, use a speaker with a series inductance greater than 10uH. Typical 4Ω speakers exhibit series inductances in the range from 10μH to 47uH.

EMI Reduction

The ft2920 does not require an LC output filter for the connections from the amplifier to the speaker. However, additional EMI suppression can be made by use of a ferrite bead filter comprising a ferrite bead and a capacitor, as shown in Figure 25. Choose a ferrite bead with low DC resistance (DCR) and high impedance (100Ω ~ 330Ω) at high frequencies (>100MHz). The current flowing through the ferrite bead must be also taken into consideration. The effectiveness of ferrites can be greatly aggravated at much lower than the rated current values. Choose a ferrite bead with a rated current no less than 2A for an 8Ω load and 3A for a 4Ω load. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Choose a capacitor less than 1nF based on EMI performance. Place each ferrite bead filter tightly together and individually close to VOP and VON pins.

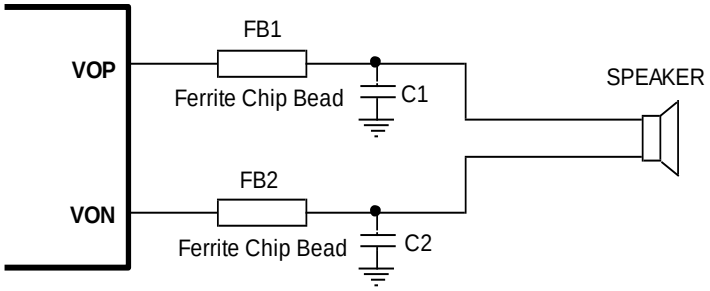


Figure 25: Ferrite Bead Filter to Reduce EMI

Class-D Output Snubber Circuit

For applications where the speaker load resistance is 4Ω or less, it may become necessary to add a snubber circuit across the two output pins, VOP and VON, to prevent the device from accelerated deterioration or abrupt destruction due to excessive inductive flybacks that are induced on fast output switching or by an over-current or short-circuit condition. Additionally, the snubber circuit can further lower EMI emissions of the Class-D outputs.

Figure 26 shows a simple RC snubber circuit with suggested values of R=4.7Ω in series with C=4.7nF. Note that the design of the RC snubber circuit is specific to each application and must take into account the parasitic reactance of the system board to reach proper values of R and C. Evaluate and ensure that the voltage spikes (overshoots and undershoots) at VOP and VON on the actual system board are within their absolute maximum ratings. Pay close attention to the layout of the RC snubber circuit to be tight and individually close to VOP and VON pins respectively.

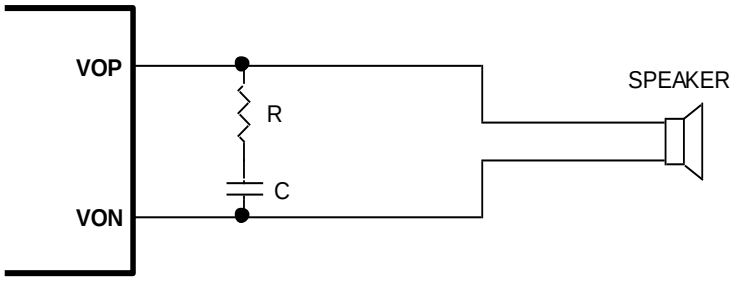


Figure 26: Class-D Output RC Snubber Circuit

Input Capacitor (C_{IN})

Input DC decoupling capacitors are recommended for audio inputs. The input DC decoupling capacitors remove the DC bias from audio inputs. The input capacitor C_{IN} and the total input resistance (R_{IN} + 15kΩ) form a highpass filter with the corner frequency, f_C, determined by 5.

$$f_C = 1 / [2 \times \pi \times (R_{IN} + 37.5k\Omega) \times C_{IN}] \quad \text{for GAIN=Low}$$
$$f_C = 1 / [2 \times \pi \times (R_{IN} + 25k\Omega) \times C_{IN}] \quad \text{for GAIN=High} \qquad (5)$$
$$f_C = 1 / [2 \times \pi \times (R_{IN} + 15k\Omega) \times C_{IN}] \quad \text{for GAIN=Unconnected}$$

R_{IN} is the external input resistance for a specific voltage gain. Note that the variation of the actual input resistance will affect the voltage gain proportionally. Thus choose R_{IN} with a tolerance of 2% or better.

Choose C_{IN} such that f_C is well below the lowest frequency of interest. Setting it too high affects the amplifier's low-frequency response. Consider an example where the specification calls for A_V=26dB with the GAIN pin grounded and a flat frequency response down to 20Hz. In this example, R_{IN}=0Ω and C_{IN} is calculated to be about 0.21μF; thus 0.22μF, as a common choice of capacitance, can be chosen for C_{IN}.

Note that any mismatch in capacitance between two audio inputs will cause a mismatch in the corner frequencies. Severe mismatch may also cause turn-on pop noise, PSRR, CMRR performance. Thus choose capacitors with a tolerance of ±2% or better.

Furthermore, the type of the input capacitor is crucial to audio quality. For best audio quality, use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

Supply Decoupling Capacitors (C_{VBAT}, $C_{PVDDL/R}$, C_{AVDD}, C_{BVDD})

Sufficient decoupling of the power supplies is crucial for audio amplifiers to ensure high efficiency, low distortion, and low EMI. Place a 1μF low-ESR ceramic capacitor (C_{VBAT}) in close proximity to the VBAT pin. Furthermore, add a small decoupling resistor (R_{VBAT}) of 10Ω between the system power supply and the VBAT pin, minimizing the detrimental effect of high battery current ripples on the detection of battery voltage.

Place a 1μF low-ESR ceramic capacitor (C_{PVDD}) individually close to each PVDD pin.

Place a 1μF low-ESR ceramic capacitor (C_{AVDD}, C_{BVDD}) individually close to AVDD and BVDD pins respectively. This choice of capacitors and the placement of C_{AVDD} and C_{BVDD} help minimize higher frequency transients, spikes, or digital hash on the supply line. Furthermore, add a small decoupling resistor (R_{AVDD}) of 10Ω between AVDD and PVDD pins, preventing high frequency transients of PVDD from interfering with on-chip linear amplifiers.

PRINTED CIRCUIT BOARD (PCB) LAYOUT GUIDELINES

Ground Plane - It is required to use a solid metal plane with sufficiently wide area as a central ground connection (GND) for ft2920. All ground pins (AGND, PGND, and PGNDB) are directly shorted to the ground plane.

Supply Decoupling capacitors – The supply decoupling capacitors (C_{VBAT}, C_{PVDD}, C_{AVDD}, and C_{BVDD}) should be placed as individually close to VBAT, PVDD, AVDD, and BVDD pins as possible.

Boost Regulator Input Capacitor - Place the supply input capacitor (C_S) in close proximity to the inductor. They should be on the same layer of the system board with ft2920.

Boost Regulator Inductor & Schottky Diodes - Place the inductor and Schottky diodes tightly together and in close proximity to the LX pins. They should be on the same layer of the system board with ft2920.

Boost Regulator Snubber Circuit - Place the snubber circuit (R_{LX} and C_{LX}) tightly together and in close proximity to the LX pins. They should be on the same layer of the system board with ft2920.

Boost Regulator Output Capacitors - Place the output capacitors (C_{PVOUT}) in close proximity to the Schottky diodes.

Ferrite Bead Filter - The ferrite bead filters of the Class-D amplifiers' outputs should be placed as individually close to audio output pins, VOP and VON, as possible for optimum EMI performance. Keep the current loop from each of the audio outputs through the ferrite bead and the capacitor and back to PGND as short and tight as possible.

Power Dissipation - The maximum output power of ft2920 can be severely limited by its thermal dissipation capability. To ensure the device operates properly and reliably at maximum output power without incurring over-temperature shutdown, the following guidelines are given for optimization of its thermal dissipation capability:

- Fill both top and bottom layers of the system board with solid GND metal traces.
- Solder the thermal pad directly onto a grounded metal plane.

- Place lots of equally-spaced VIAs underneath the thermal pad connecting the top and bottom layers of GND. The VIAs are connected to a solid metal plane on the bottom layer of the board.
- Reserve wide and uninterrupted areas along the thermal flow on the top layer, i.e., no wires cutting through the GND layer and obstructing the thermal flow.
- Place all the passive devices (Inductor, Schottky diodes, and Input/output capacitors) of the boost regulator tightly together and on the same layer of the board with ft2920.
- Avoid using VIAs for traces carrying high current.

TYPICAL APPLICATION CIRCUITS

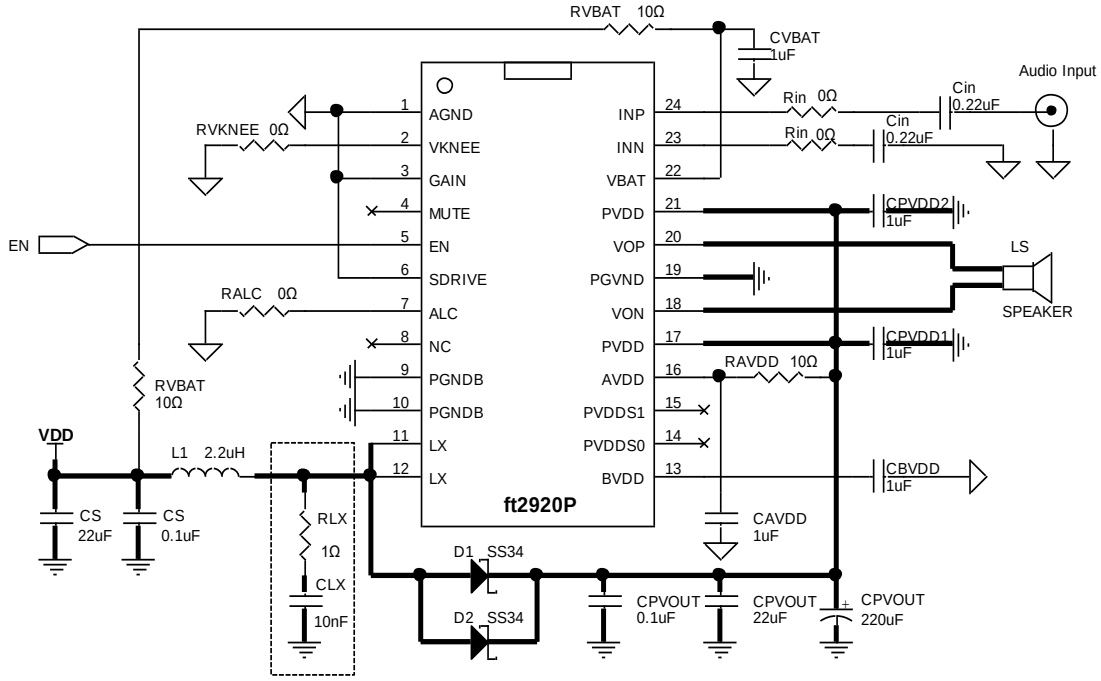


Figure 27: Single-Ended Audio Input with PVDD at 8.0V in ALC-1 Mode

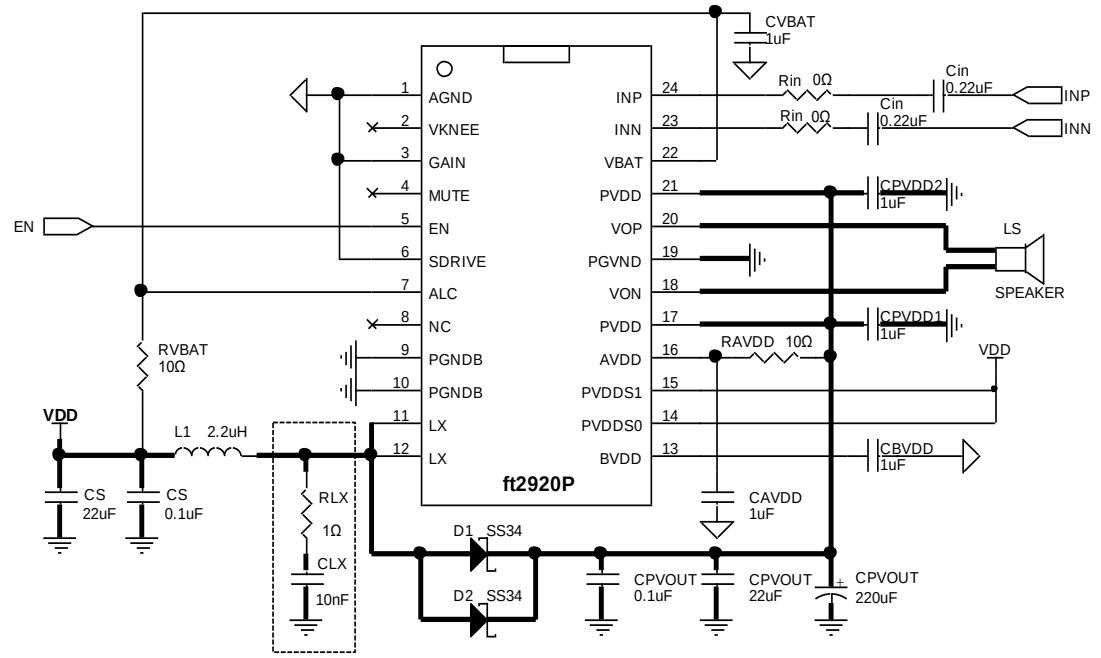


Figure 28: Differential Audio Inputs with PVDD at 7.4V in Non-ALC Mode

Note: The bold lines indicate high current paths and their respective traces are required to be as wide and short as possible on the system board for optimum performance in maximum output power, power efficiency, THD+N, and EMI emissions.

TYPICAL APPLICATION CIRCUITS

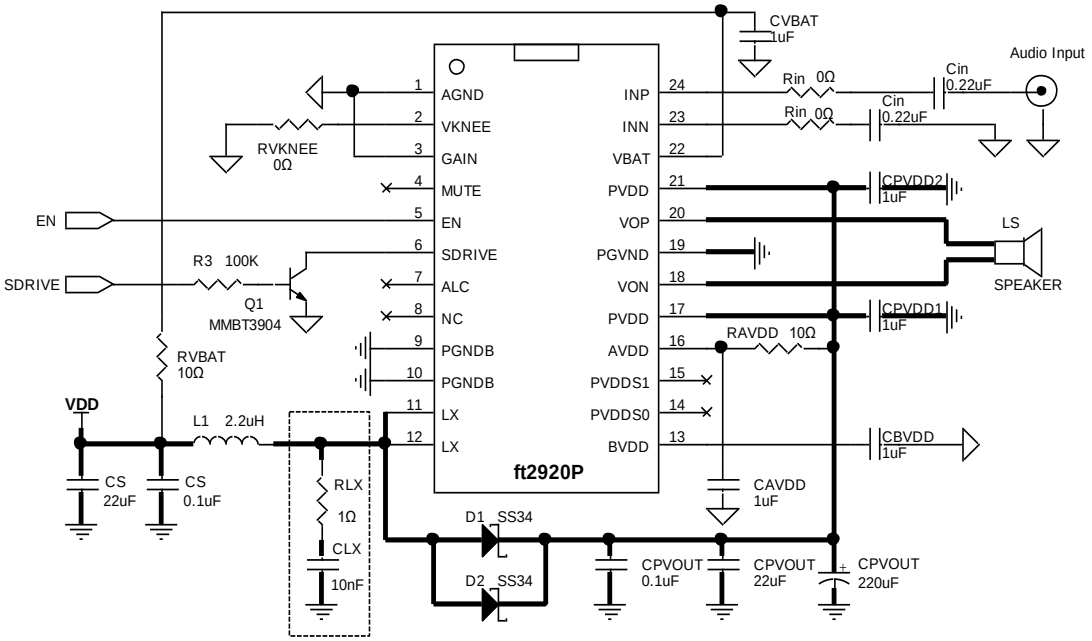


Figure 29: Single-Ended Audio Input with PVDD at 8.0V and SDRIVE Control in ALC-2 Mode

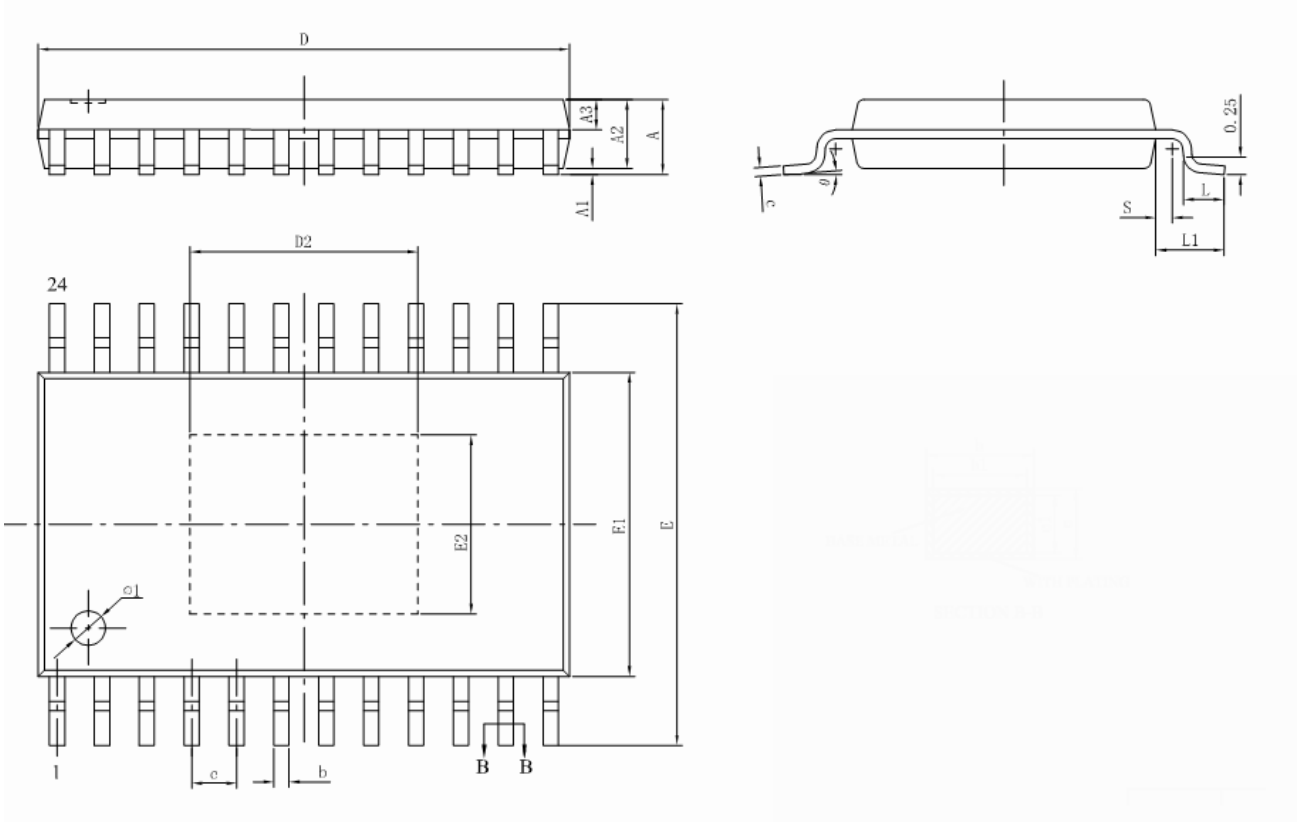
SDRIVE > 1.2V: Normal Mode - High Efficiency and High Power Operation

SDRIVE < 0.4V: Boost Disabled Mode - Low EMI and Low Power Operation

Note: The bold lines indicate high current paths and their respective traces are required to be as wide and short as possible on the system board for optimum performance in maximum output power, power efficiency, THD+N, and EMI emissions.

PHYSICAL DIMENSIONS

TSSOP-24L PACKAGE OUTLINE DIMENSIONS



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
S	0.20	—	—
Ø1	Ø0.8X0.05~0.10DP		
θ	0	—	8°

Unit: mm

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