ft2705

2X10W Class-D Stereo Audio Power Amplifier with Automatic Level Control

GENERAL DESCRIPTION

The ft2705 is a highly efficient 2X10W Class-D stereo audio power amplifier with automatic level control (ALC). It operates with a wide range of supply voltages from 4.5V to 8.8V in either dual bridge-tied-load (BTL) or parallel bridge-tied-load (PBTL) configuration. With a supply voltage at 8.8V, the ft2705 can deliver 10W per channel into a pair of 4Ω speakers in dual BTL configuration (stereo mode), or 14W into a single 3Ω speaker in PBTL configuration (mono mode), with 10% THD+N.

The ft2705 features ALC to constantly monitor and safeguard the audio outputs against the supply voltage, preventing output clipping distortion, excessive power dissipation, or speaker over-load. Once an over-level condition is detected in either channel, the ALC lowers the voltage gain of both audio amplifiers together to eliminate output clipping distortion while maintaining a maximum dynamic range of the audio outputs allowed for the supply voltage. In ALC mode, with a supply voltage at 8.8V, the ft2705 can deliver 7.7W per channel into a pair of 4Ω speakers in stereo mode, or 11W into a single 3Ω speaker in mono mode, with THD+N less than 0.5%.

As a filterless Class-D stereo audio amplifier, the ft2705 features high efficiency (up to 88%), high PSRR (70dB at 1kHz), and low EMI emissions, which reduce design and manufacturing complexities, lower system cost and PCB space.

In ft2705, comprehensive protection features against various operating faults ensure its safe and reliable operation.

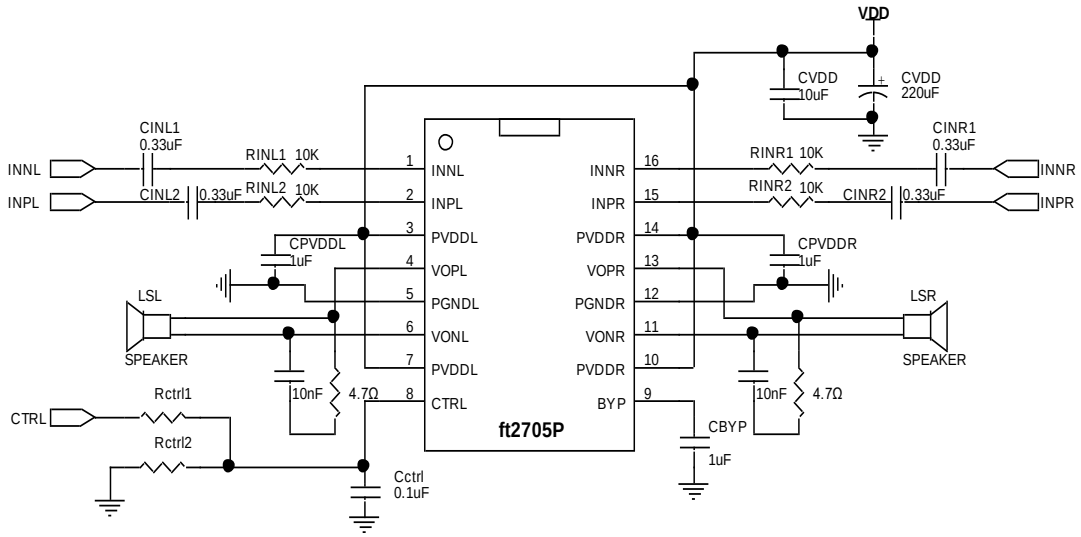
FEATURES

- Wide supply voltage range from 4.5V to 8.8V
- Automatic level control to eliminate output clipping
- Optional mono mode for low-impedance audio speakers in PBTL configuration
- Maximum output power in Non-ALC mode
  (V_{DD}=8.8V, f=1kHz, THD+N=10%)
  14W (3Ω+33μH load in PBTL configuration)
  10W/Ch (4Ω+33μH load)
  5.6W/Ch (8Ω+33μH load)
- ALC output power in ALC Mode
  (V_{DD}=8.8V, f=1kHz, THD+N<0.5%)
  11W (3Ω+33μH load in PBTL configuration)
  7.7W/Ch (4Ω+33μH load)
  4.3W/Ch (8Ω+33μH load)
- Low THD+N: 0.06%
  (V_{DD}=8.8V, f=1kHz, 4Ω+33μH, Po=5.0W)
- High efficiency up to 88%
- High PSRR: 70dB at 1kHz
- Wide ALC dynamic range: 10dB
- Maximum voltage gain: 32dB
- Under-voltage lockout protection
- Over-temperature shutdown protection
- Auto-recovering over-current protection
- Available in SOP-16L package

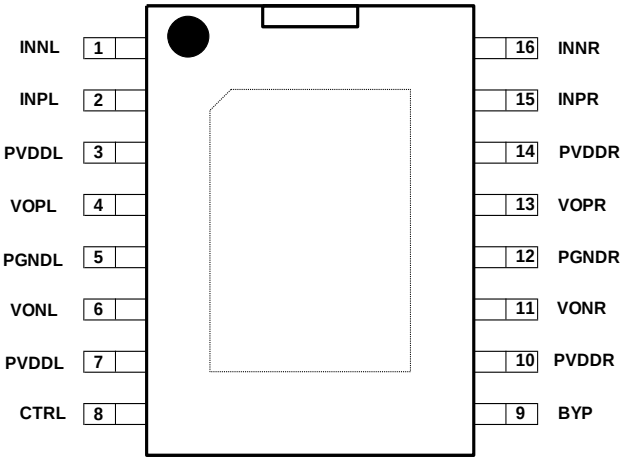
APPLICATIONS

- Blue Tooth Speakers
- Portable & Plug-In Consumer Electronics
- TV/Monitors

TYPICAL APPLICATION CIRCUIT



PIN CONFIGURATION AND DESCRIPTION



ft2705P (TOP VIEW)

NAME	PIN #	TYPE	DESCRIPTION
INNL	1	AI	Left-channel inverting audio input terminal.
INPL	2	AI	Left-channel non-inverting audio input terminal.
PVDDL	3, 7	P	Power supply for the left-channel power amplifier's output stage. Connect directly to the system power supply VDD and add a 1μF capacitor for decoupling.
VOPL	4	AO	Left-channel non-inverting audio output terminal.
PGNDL	5	G	Power ground for the left-channel power amplifier's output stage. Connect to the system ground GND.
VONL	6	AO	Left-channel inverting audio output terminal.
CTRL	8	DI	**Mode Control** (Active High) with a 300kΩ internal pulldown resister to ground.
BYP	9	AO	Common-mode bias for audio inputs. Connect to a 1μF capacitor for decoupling.
PVDDR	10, 14	P	Power supply for the right-channel power amplifier's output stage. Connect directly to the system power supply VDD and add a 1μF capacitor for decoupling.
VONR	11	AO	Right-channel inverting audio output terminal.
PGNDR	12	G	Power ground for the right-channel power amplifier's output stage. Connect to the system ground GND.
VOPR	13	AO	Right-channel non-inverting audio output terminal.
INPR	15	AI	Right-channel non-inverting audio input terminal. Connect to ground for mono mode.
INNR	16	AI	Right-channel inverting audio input terminal. Connect to ground for mono mode.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ft2705P	-40°C to +85°C	SOP-16L

REVISION HISTORY

Initial Release 1.0 (May, 2015)

Changed from Initial 1.0 (May, 2015) to Revision 1.1 (December, 2016)

1. Changed the absolute maximum rating of the supply voltage from 9.2V to 9V.
2. Changed the recommended maximum operating voltage from 9V to 8.8V.
3. Changed input capacitors (C_{INL1}, C_{INL2}, C_{INR1}, and C_{INR2}) from 1.0μF to 0.33μF in Typical Application Circuits.
4. Changed the minimum load resistance in PBTL configuration from 2.6Ω to 2.0Ω.
5. Revised Table 5, Typical Voltage Gain Settings & Input Resistor Values for Various Input Levels.

Changed from Revision 1.1 (December, 2016) to Revision 1.2 (January, 2017)

1. Added snubber circuits across audio outputs VOPL/R and VONL/R in Figure 1, 31, 32, and 32.

Changed from Revision 1.2 (January, 2017) to Revision 1.3 (April, 2017)

1. Revised Table 5, Typical Voltage Gain Settings & Input Resistor Values for Various Input Levels.
2. Revised Figure 30 - Class-D Output RC Snubber Circuit.
3. Changed the minimum load resistance in PBTL configuration from 2.0Ω to 2.4Ω for the supply voltage at 8.8V.
4. Changed the absolute maximum rating of the supply voltage from 9V to 9.2V.
5. Updated Typical Application Circuit Diagram on the first page.
6. Updated Typical Application Circuits in Figure 31, 32, and 33.

Changed from Revision 1.3 (April, 2017) to Revision 1.4 (June, 2017)

1. Added Electrical Characteristics of Po, THD+N, and η for speaker loads at R_L=2Ω+10μH.

Changed from Revision 1.4 (June, 2017) to Revision 1.5 (November, 2017)

1. Changed $C_{PVDDL/R}$ from 10μF to 1μF.
2. Added C_{VDD} of 10μF//220μF onto the system power supply.
3. Updated Typical Application Circuit on Page 1.
4. Updated Figure 31, 32, and 33 on Page 24.

ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	VALUE
Supply voltage, V_{DD} @ PVDDL/R	-0.3V to 9.2V
INNL/R, INPL/R, CTRL, BYP	-0.3V to 5.5V
All other Pins	-0.3V to V_{DD}+0.3V
Storage Temperature	-65°C to +150°C
ESD Ratings-Human Body Model (HBM)	2000V
Junction Temperature	150°C
Maximum Soldering Temperature (@10 second duration)	260°C

Note 1: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may damage the device or affect device reliability.

POWER DISSIPATION RATINGS (Note 2, 3)

PACKAGE	$T_A \leq +25°C$	$T_A = +70°C$	$T_A = +85°C$	Θ_{JA}
SOP-16L	3.1W	2.0W	1.7W	40°C/W

Note 2: The thermal pad of the package must be directly soldered onto a grounded metal island (as a thermal sink) on the system board.
Note 3: The power dissipation ratings are for a two-side, two-plane printed circuit board (PCB).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}	PVDDL/R		4.5		8.8	V
Minimum Load Resistance	R_L	Stereo Mode		3.2	4.0		Ω
		Mono Mode	V_{DD}=8.8V	2.4	3.0		Ω
			V_{DD}=8.4V	2.0	2.4		Ω
Audio Input Resistor	R_{IN}	@ INNL/R, INPL/R		0		62	kΩ
Audio Input Capacitor	C_{IN}	@ INNL/R, INPL/R		0.1		1.0	μF
Operating Mode Control Input Voltage	V_{CTRL}	Shutdown				0.4	V
		ALC Mode		1.1	1.25	1.4	V
		Non-ALC Mode		1.6			V
Operating Junction Temperature	T_J			-40		125	°C
Ambient Temperature	T_A			-40		85	°C

Note 4: The peak supply voltage including its tolerance over various operating conditions must not exceed its absolute-maximum-rated value (9.2v). Exposure to absolute-maximum-rated supply voltage may damage the device or affect device reliability permanently. For applications where the system supply voltage might momentarily exceed the rating, it is highly recommended to add an external diode in series with the system power supply to ensure the peak supply voltage not exceeding the absolute maximum rating. The added diode must be rated for a current no less than 4A and a reverse breakdown voltage no less than 15V.

Note 5: For applications where the supply voltage is higher than 8.4V, it is recommended to add a RC snubber circuit across VOPL/R and VONL/R pins to lower overshoot voltages (above VDD) and undershoot voltages (below GND), preventing permanent damage to the device for applications with long speaker wires.

IMPORTANT APPLICATION NOTES

1. For enhanced audio performance, it is recommended to use differential inputs from the audio source for ft2705. In single-ended input applications, the unused audio input of ft2705 should be AC-grounded at the audio source. The impedances seen at the two differential inputs should be substantially the same.
2. The ft2705 requires adequate power supply decoupling to ensure its optimum operation and performance in the output power, efficiency, distortion, and EMI emissions. Place each decoupling capacitors individually as close as possible to the device's PVDDL/R pins.
3. The ft2705 is a high performance, high power, Class-D stereo audio amplifier with an exposed thermal pad underneath the package. The thermal pad should be directly soldered onto a ground plane as a thermal sink for proper power dissipation. Failure to do so may result in the device prematurely going into thermal shutdown.
4. It is strongly recommended to add a ground plane (GND) for ft2705 on the system board.
5. Use a simple ferrite bead filter for further EMI suppression, as shown in Figure 29. Choose a ferrite bead with a rated current no less than 3A for applications with load resistances less than 4Ω. Also, place respective ferrite beard filters as individually close to VOPL/R and VONL/R pins as possible.
6. To enhance long-term reliability, it is highly recommended to add a simple RC snubber circuit, as shown in Figure 30, across the two audio outputs, VOPL/R and VONL/R, of each individual channel to prevent the device from accelerated deterioration or abrupt destruction due to excessive inductive flybacks that are induced on fast output switching or by an over-current or short-circuit condition.
7. Do not short audio outputs (VOPL/R and VONL/R) directly to ground (PGNDL/R) or the supply voltage (PVDDL/R) as this might damage the device permanently, particularly when the supply voltage is higher than 8.4V.

FUNCTIONAL BLOCK DIAGRAM

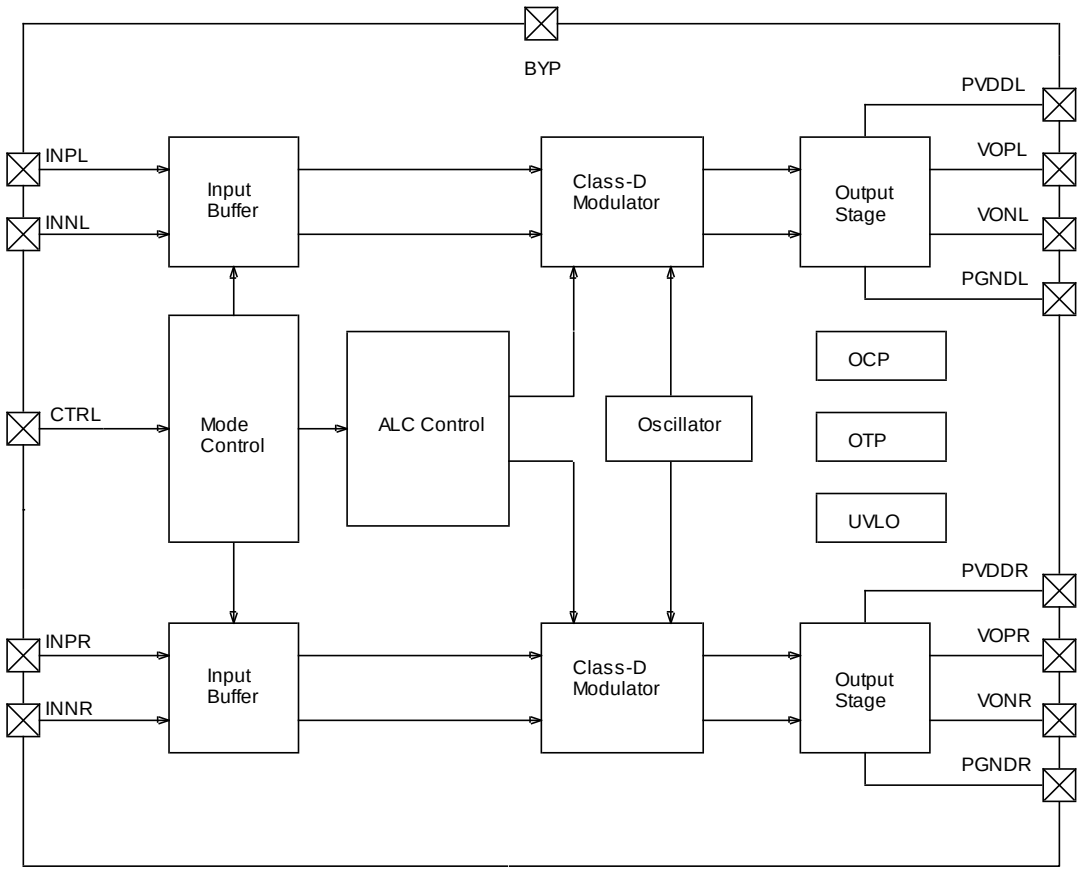


Figure 1: Simplified Functional Block Diagram of ft2705

TEST SETUP FOR ELECTRICAL & PERFORMANCE CHARACTERISTICS

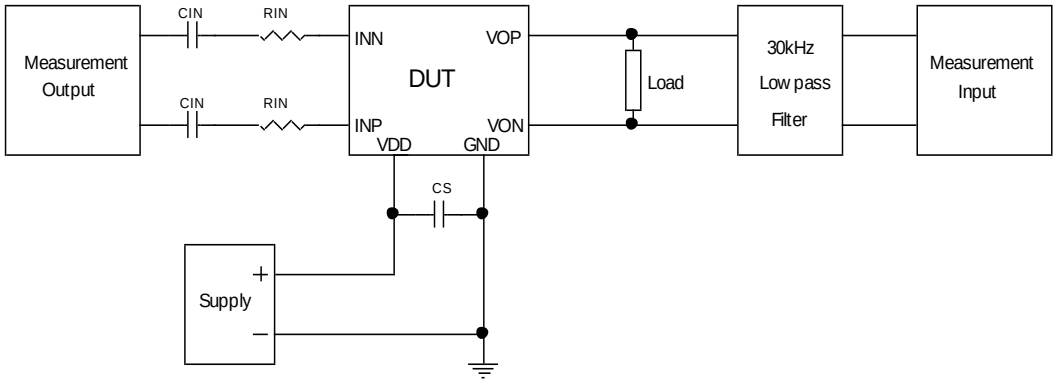


Figure 2: Test Setup Diagram for ft2705

All parameters specified in Electrical and Typical Performance Characteristics sections are measured according to the conditions:

1. The two differential inputs are shorted for common-mode input voltage measurement. All other parameters are taken with input resistors R_{IN}=10kΩ and input capacitors C_{IN}=0.33μF, unless otherwise specified.
2. The supply decoupling capacitors C_{PVDDL}=1μF and C_{PVDDR}=1μF is placed close to their individual pins.
3. A 33μH inductor was placed in series with the load resistor to emulate a speaker load for all AC and dynamic parameters.
4. The 33kHz lowpass filter is added even if the analyzer has an internal lowpass filter. An RC lowpass filter (100Ω, 47nF) is used on each output for the data sheet graphs.

ELECTRICAL CHARACTERISTICS

V_{DD}=8.8V, f=1kHz, Stereo Mode, Load=4Ω+33μH, C_{IN}=0.33μF, R_{IN}=10kΩ, C_{BYP}=1μF, $C_{PVDDL/R}$=1μF, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage	PVDDL/R	4.5		8.8	V
V_{UVLOUP}	Power-up Threshold Voltage	V_{DD} from Low to High		3.2		V
V_{UVLODN}	Power-off Threshold Voltage	V_{DD} from High to Low		2.9		V
V_{BYP}	Common-mode Bias Voltage	V_{DD}=8.8V	2.7	3.0	3.3	V
I_{VDD}	Supply Quiescent Current Inputs AC-Grounded No Load	V_{DD}=8.8V	12	16	20	mA
		V_{DD}=7.2V	10	13	16	mA
		V_{DD}=6.5V	9	12	15	mA
	Supply Quiescent Current Inputs AC-Grounded No Load (PBTL Configuration)	V_{DD}=8.8V	11	15	19	mA
		V_{DD}=7.2V	9	12	15	mA
		V_{DD}=6.5V	8	11	14	mA
I_{SD}	Shutdown Current	CTRL Low		10	20	μA
V_{CTRL}	Operating Mode Control Threshold Voltage	Shutdown Mode			0.4	V
		ALC Mode	1.1		1.4	V
		Non-ALC Mode	1.6			V
V_{MONO}	Mono Mode Threshold Voltage	@ INNR and INPR			0.4	V
R_{CTRL}	Pulldown Resistor to Ground	@ CTRL		300		kΩ
T_{OTP}	Over-Temperature Threshold			160		°C
T_{HYS}	Over-Temperature Hysteresis			20		°C
CLASS-D AMPLIFIER						
$P_{O, MAX}$ (R_L=3Ω)	THD+N=10%, Non-ALC Mode (PBTL Configuration)	V_{DD}=8.8V		14		W
		V_{DD}=7.2V		9.6		W
		V_{DD}=6.5V		7.8		W
	THD+N=1%, Non-ALC Mode (PBTL Configuration)	V_{DD}=8.8V		11.5		W
		V_{DD}=7.2V		7.7		W
		V_{DD}=6.5V		6.2		W
$P_{O, MAX}$ (R_L=4Ω)	THD+N=10%, Non-ALC Mode	V_{DD}=8.8V		10		W/Ch
		V_{DD}=7.2V		6.7		W/Ch
		V_{DD}=6.5V		5.5		W/Ch
	THD+N=1%, Non-ALC Mode	V_{DD}=8.8V		8.0		W/Ch
		V_{DD}=7.2V		5.4		W/Ch
		V_{DD}=6.5V		4.4		W/Ch
$P_{O, MAX}$ (R_L=8Ω)	THD+N=10%, Non-ALC Mode	V_{DD}=8.8V		5.6		W/Ch
		V_{DD}=7.2V		3.8		W/Ch
		V_{DD}=6.5V		3.1		W/Ch
	THD+N=1%, Non-ALC Mode	V_{DD}=8.8V		4.6		W/Ch
		V_{DD}=7.2V		3.0		W/Ch
		V_{DD}=6.5V		2.5		W/Ch
$P_{O, ALC}$ (R_L=3Ω)	ALC Mode (PBTL Configuration)	V_{DD}=8.8V, V_{IN}=0.30V_{RMS}		11		W
		V_{DD}=7.2V, V_{IN}=0.24V_{RMS}		7.4		W
		V_{DD}=6.5V, V_{IN}=0.22V_{RMS}		6.0		W

ELECTRICAL CHARACTERISTICS (Cont'd)

V_{DD}=8.8V, f=1kHz, Stereo Mode, Load=4Ω+33μH, C_{IN}=0.33μF, R_{IN}=10kΩ, C_{BYP}=1μF, $C_{PVDDL/R}$=1μF, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$P_{O,ALC}$ (R_L=4Ω)	ALC Mode	V_{DD}=8.8V, V_{IN}=0.30V_{RMS}		7.7		W/Ch
		V_{DD}=7.2V, V_{IN}=0.24V_{RMS}		5.2		W/Ch
		V_{DD}=6.5V, V_{IN}=0.22V_{RMS}		4.2		W/Ch
$P_{O,ALC}$ (R_L=8Ω)	ALC Mode	V_{DD}=8.8V, V_{IN}=0.30V_{RMS}		4.3		W/Ch
		V_{DD}=7.2V, V_{IN}=0.24V_{RMS}		2.8		W/Ch
		V_{DD}=6.5V, V_{IN}=0.22V_{RMS}		2.4		W/Ch
THD+N (R_L=3Ω)	V_{DD}=8.8V, Non-ALC Mode (PBTL Configuration)	Po=6.5W		0.08		%
	V_{DD}=8.8V, ALC Mode (PBTL Configuration)	Po=11W, V_{IN}=0.30V_{RMS}		0.5		%
THD+N (R_L=4Ω)	V_{DD}=8.8V, Non-ALC Mode	Po=5.0W		0.06		%
	V_{DD}=8.8V, ALC Mode	Po=7.7W, V_{IN}=0.30V_{RMS}		0.4		%
THD+N (R_L=8Ω)	V_{DD}=8.8V, Non-ALC Mode	Po=2.5W		0.04		%
	V_{DD}=8.8V, ALC Mode	Po=4.3W, V_{IN}=0.30V_{RMS}		0.3		%
A_V	Overall Voltage Gain	R_{IN}=10kΩ		28		dB
R_{IN}	Input Resistance	@ INNL/R, INPL/R		15		kΩ
$R_{O,SD}$	Output Resistance in Shutdown	@ INNL/R, INPL/R with CTRL Low		2.5		kΩ
V_{OS}	Output Offset Voltage	No Load		±10		mV
V_N	Idle-Channel Noise	A_V=25dB (R_{IN}=20kΩ), Inputs AC-Grounded, A-weighted		130		μV_{RMS}
η	Power Efficiency	V_{DD}=8.8V, Po=11W, R_L=3Ω		85		%
		V_{DD}=8.8V, Po=7.7W, R_L=4Ω		88		%
		V_{DD}=8.8V, Po=4.3W, R_L=8Ω		89		%
PSRR	Power Supply Rejection Ratio	f=1kHz		70		dB
CMRR	Common Mode Rejection Ratio	f=1kHz		65		dB
SNR	Signal-to-Noise Ratio	A_V=25dB (R_{IN}=20kΩ), Maximum Output (5.6V_{RMS}), A-weighted		92		dB
Crosstalk	Channel Separation	Po=5.0W, f=1kHz		80		dB
T_{STUP}	Startup Time			160		ms
T_{SD}	Shutdown Mode Settling Time			20		ms
f_{SW}	PWM Output Carrier Frequency			375		kHz
I_{LIMIT}	Over-Current Limit	Dual BTL Configuration		3.3		A/Ch
		PBTL Configuration		5.0		A
AUTOMATIC LEVEL CONTROL (ALC)						
A_{MAX}	Maximum ALC Attenuation			10		dB
T_{ATTACK}	ALC Attack Time			20		ms
$T_{RELEASE}$	ALC Release Time			500		ms
FADE-IN & FADE-OUT						
T_{FADEIN}	Fade-In Time			20		ms
$T_{FADEOUT}$	Fade-Out Time			20		ms

ELECTRICAL CHARACTERISTICS (Cont'd)

V_{DD}=7.4V, f=1kHz, Mono Mode, Load=2Ω+10μH, C_{IN}=0.33μF, R_{IN}=10kΩ, C_{BYP}=1μF, $C_{PVDDL/R}$=1μF, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$P_{O, MAX}$	Maximum Output Power	Non-ALC Mode, THD+N=10%		14		W
		Non-ALC Mode, THD+N=1%		11		W
$P_{O, ALC}$	ALC Output Power	ALC Mode, V_{IN}=0.30V_{RMS}		10.5		W
THD+N	Total Harmonic Distortion + Noise	Non-ALC Mode, Po=10W		0.1		%
		ALC Mode, V_{IN}=0.30V_{RMS}		0.5		%
η	Power Efficiency	ALC Mode, V_{IN}=0.30V_{RMS}		78		%

V_{DD}=8.4V, f=1kHz, Mono Mode, Load=2Ω+10μH, C_{IN}=0.33μF, R_{IN}=10kΩ, C_{BYP}=1μF, $C_{PVDDL/R}$=1μF, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$P_{O, MAX}$	Maximum Output Power	Non-ALC Mode, THD+N=10%		18		W
		Non-ALC Mode, THD+N=1%		14		W
$P_{O, ALC}$	ALC Output Power	ALC Mode, V_{IN}=0.30V_{RMS}		13.5		W
THD+N	Total Harmonic Distortion + Noise	Non-ALC Mode, Po=12W		0.1		%
		ALC Mode, V_{IN}=0.30V_{RMS}		0.4		%
η	Power Efficiency	ALC Mode, V_{IN}=0.30V_{RMS}		78		%

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD}=8.8V, f=1kHz, Stereo Mode, Load=4Ω+33μH, C_{IN}=0.33μF, R_{IN}=10kΩ, C_{BYP}=1μF, $C_{PVDDL/R}$=1μF, T_A=25°C, unless otherwise specified.

List of Typical Performance Characteristics

DESCRIPTION	CONDITIONS	FIGURE #
Output Power vs. Supply Voltage	R_L=3Ω+33μH, ALC (V_{IN}=0.30V_{RMS}) & Non-ALC Modes (PBTL Configuration)	3
	R_L=4Ω+33μH, ALC (V_{IN}=0.30V_{RMS}) & Non-ALC Modes	4
	R_L=8Ω+33μH, ALC (V_{IN}=0.30V_{RMS}) & Non-ALC Modes	5
Output Power vs. Input Voltage	R_L=3Ω+33μH, ALC & Non-ALC Modes (PBTL Configuration)	6
	R_L=4Ω+33μH, ALC & Non-ALC Modes	7
	R_L=8Ω+33μH, ALC & Non-ALC Modes	8
Efficiency vs. Output Power	R_L=3Ω+33μH, Non-ALC Mode (PBTL Configuration)	9
	R_L=4Ω+33μH, Non-ALC Mode	10
	R_L=8Ω+33μH, Non-ALC Mode	11
THD+N vs. Output Power	R_L=4Ω+33μH, Non-ALC Mode	12
THD+N vs. Input Voltage	R_L=4Ω+33μH, ALC & Non-ALC Modes	13
THD+N vs. Input Frequency	R_L=4Ω+33μH, ALC Mode, Po=5.0W	14
PSRR vs. Frequency	R_L=4Ω+33μH, Inputs AC-Grounded	15
Crosstalk vs. Frequency	R_L=4Ω+33μH, Vo=2.0V_{RMS}, R-CH to L-CH	16
Quiescent Current vs. Supply	Inputs AC-Grounded, No Load, ALC Mode	17
ALC Attack & Release Time	V_{IN}=0.20V_{RMS} ~ 0.63V_{RMS}, R_L=4Ω+33μH, ALC Mode	18
Output Startup Waveforms	R_L=4Ω+33μH, Vin=0.10V_{RMS}, ALC Mode	19
Output Shutdown Waveforms	R_L=4Ω+33μH, Vin=0.10V_{RMS}, ALC Mode	20

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

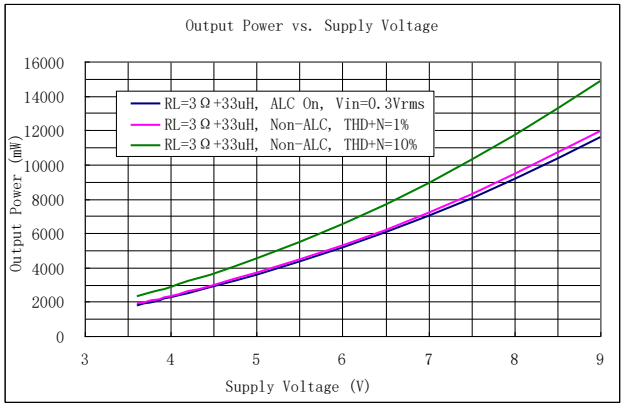


Figure 3: Output Power vs. Supply Voltage

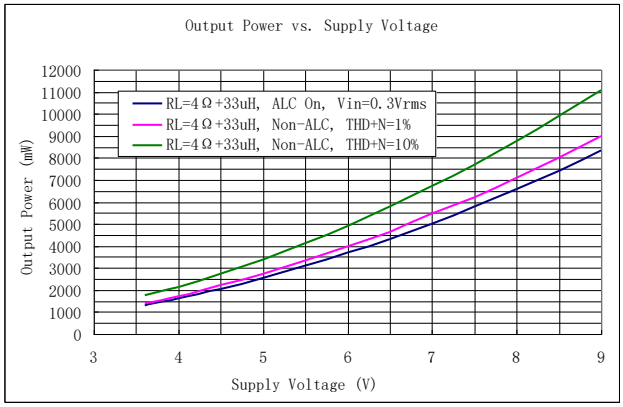


Figure 4: Output Power vs. Supply Voltage

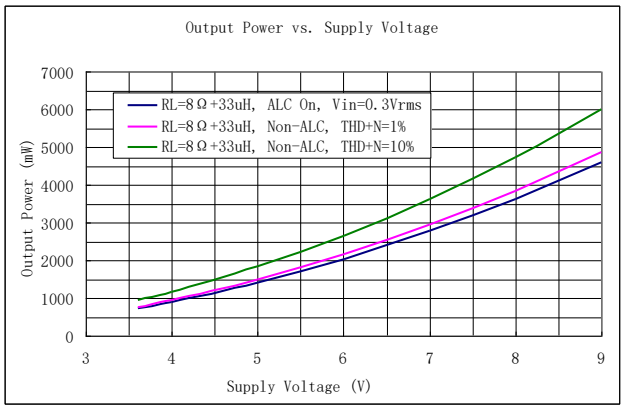


Figure 5: Output Power vs. Supply Voltage

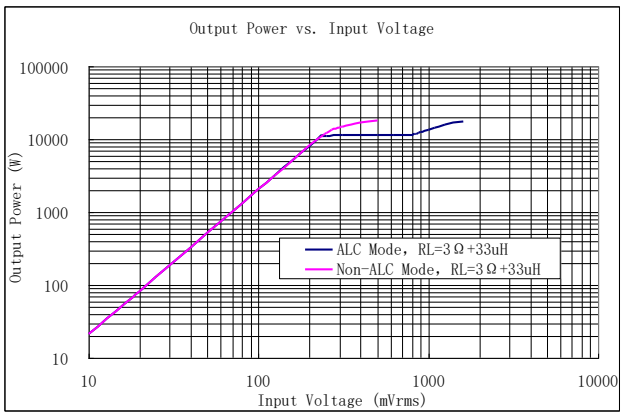


Figure 6: Output Power vs. Input Voltage

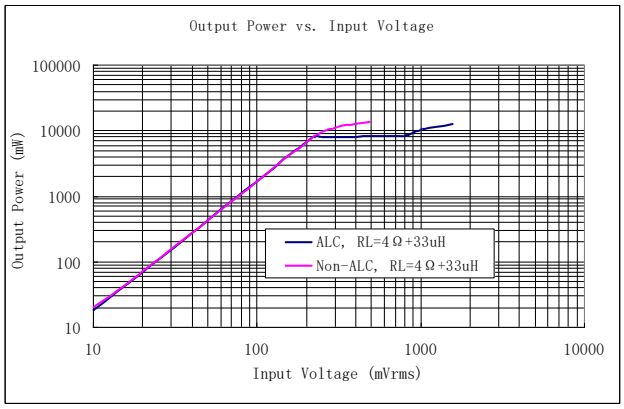


Figure 7: Output Power vs. Input Voltage

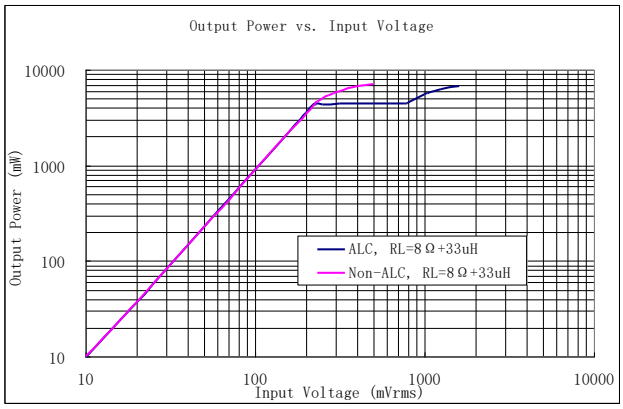


Figure 8: Output Power vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

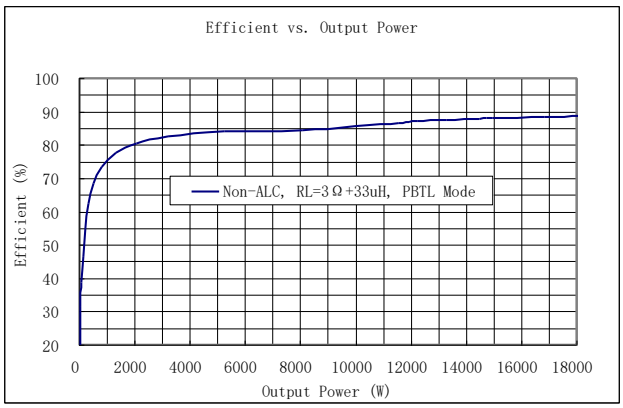


Figure 9: Efficiency vs. Output Power

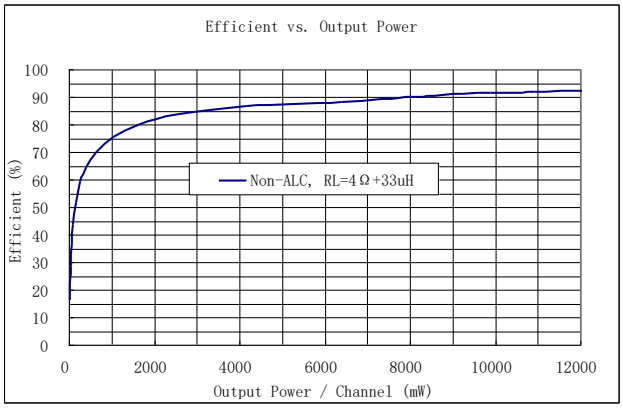


Figure 10: Efficiency vs. Output Power

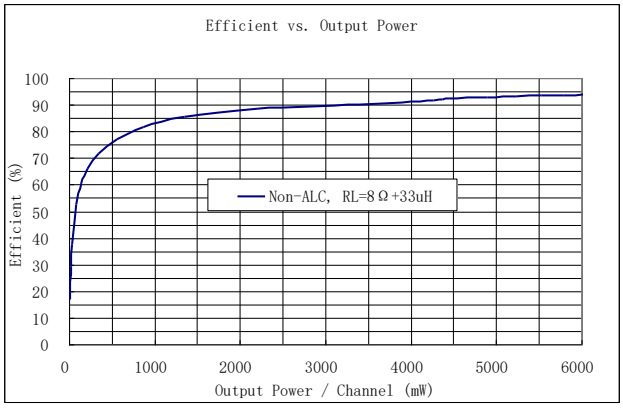


Figure 11: Efficiency vs. Output Power

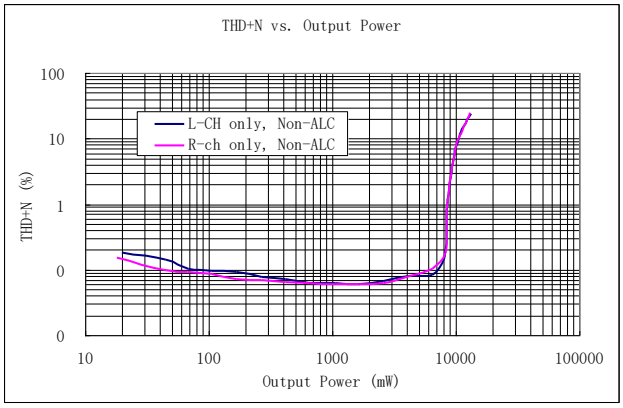


Figure 12: THD+N vs. Output Power

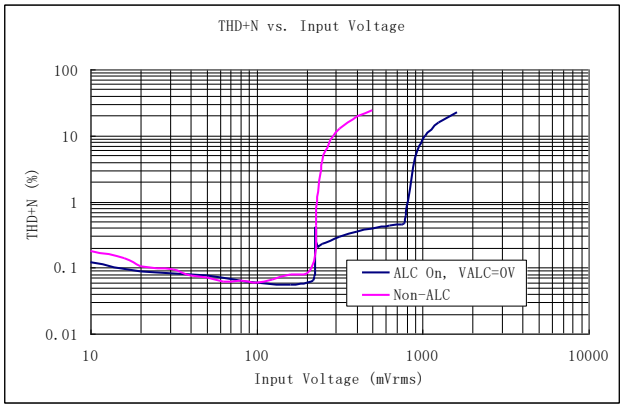


Figure 13: THD+N vs. Input Voltage

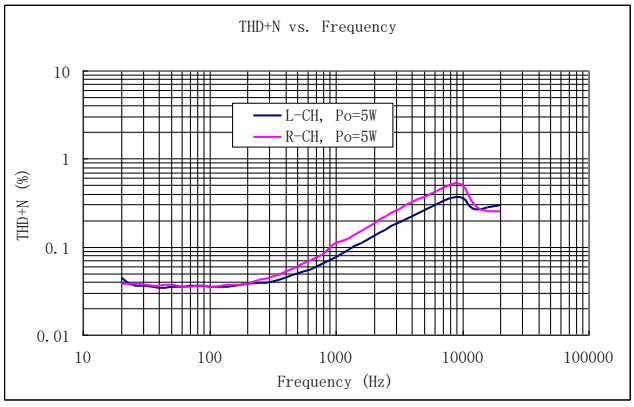


Figure 14: THD+N vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

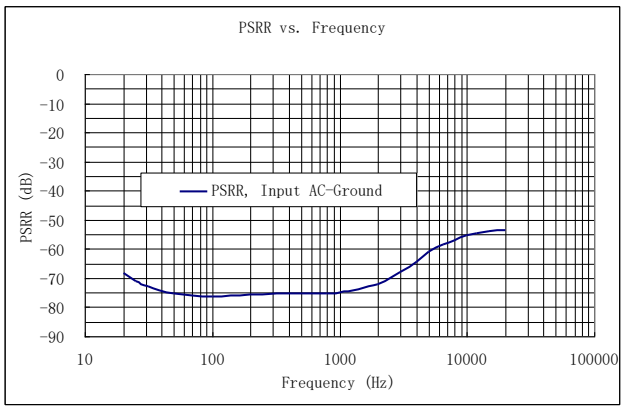


Figure 15: PSRR vs. Frequency

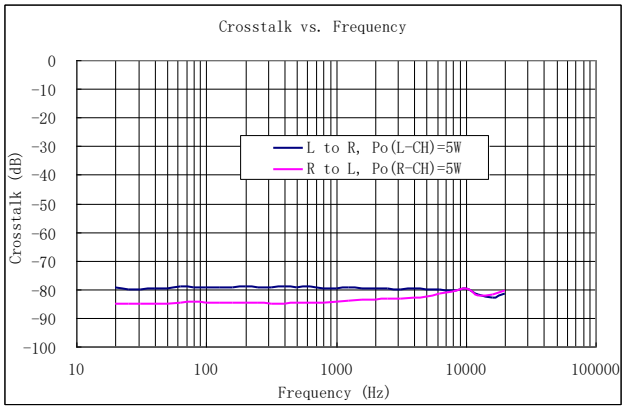


Figure 16: Crosstalk vs. Frequency

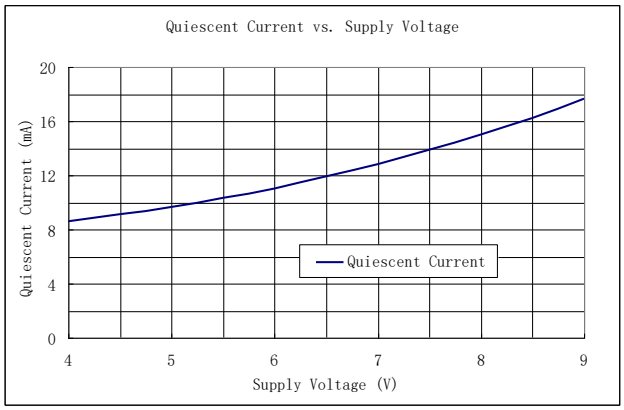


Figure 17: Quiescent Current vs. Supply Voltage

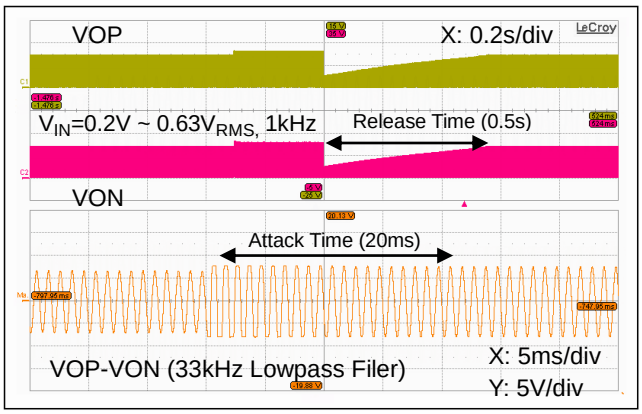


Figure 18: ALC Attack & Release Time

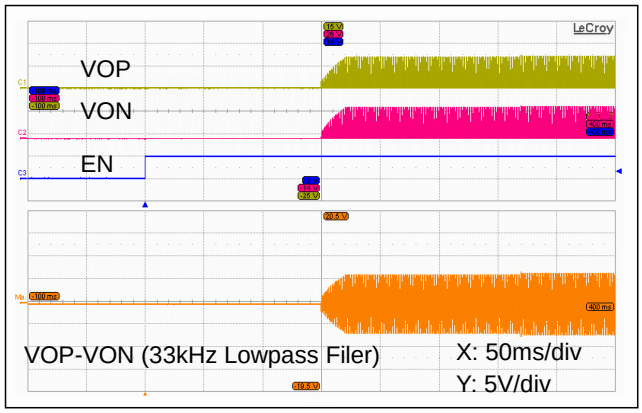


Figure 19: (VOP-VON) Startup Waveforms

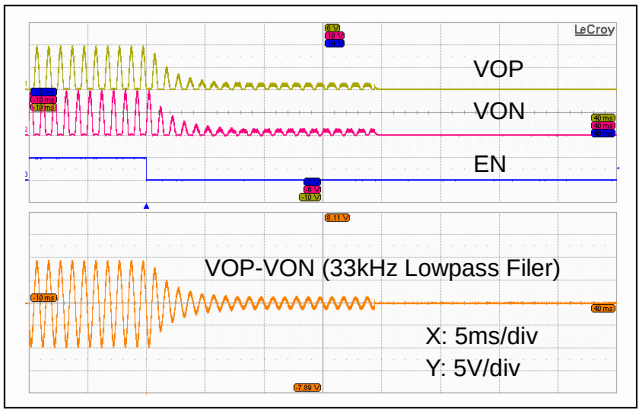


Figure 20: (VOP-VON) Shutdown Waveforms

APPLICATION INFORMATION

The ft2705 is a highly efficient 2X10W Class-D stereo audio power amplifier with automatic level control (ALC). It operates with a wide range of supply voltages from 4.5V to 8.8V in either dual bridge-tied-load (BTL) or parallel bridge-tied-load (PBTL) configuration. With a supply voltage at 8.8V, the ft2705 can deliver 10W per channel into a pair of 4Ω speakers in dual BTL configuration (stereo mode), or 14W into a single 3Ω speaker in PBTL configuration (mono mode), with 10% THD+N.

In ft2705, two operating modes, i.e., ALC and Non-ALC, are available that can be selected via the CTRL pin. The Non-ALC mode configures the device in a conventional Class-D operation, where the output power is maximized without ALC operation. In ALC mode, the ft2705 constantly monitors and safeguards the audio outputs against the supply voltage, preventing output clipping distortion, excessive power dissipation, or speaker over-load. Once an over-level condition is detected in either channel, the ALC lowers the voltage gain of both audio amplifiers together to eliminate output clipping distortion while maintaining a maximum dynamic range of the audio outputs allowed for the supply voltage. In ALC mode, with a supply voltage at 8.8V, the ft2705 can deliver 7.7W per channel into a pair of 4Ω speakers in stereo mode, or 11W into a single 3Ω speaker in mono mode, with THD+N less than 0.5%.

As a filterless Class-D audio amplifier, the ft2705 features high efficiency (up to 88%), high PSRR (70dB at 1kHz), and low EMI emissions, which reduce design and manufacturing complexities, lower system cost and PCB space. These features make ft2705 an ideal audio solution for portable and plug-in consumer electronic devices.

As specifically designed for portable applications, the ft2705 incorporates a shutdown mode to minimize the power consumption by holding the CTRL pin to ground. It also includes comprehensive protection features against various operating faults such as over-current, short-circuit, over-temperature, or under-voltage for a safe and reliable operation.

AUTOMATIC LEVEL CONTROL (ALC)

The automatic level control is to maintain the audio output signals for a maximum voltage swing without distortion when an excessive input that may cause output clipping is applied. With the ALC function, the ft2705 lowers the gain of the amplifier to an appropriate value such that the clipping at the outputs is substantially eliminated. It also eliminates the clipping of the output signal due to the reduction of the power-supply voltage.

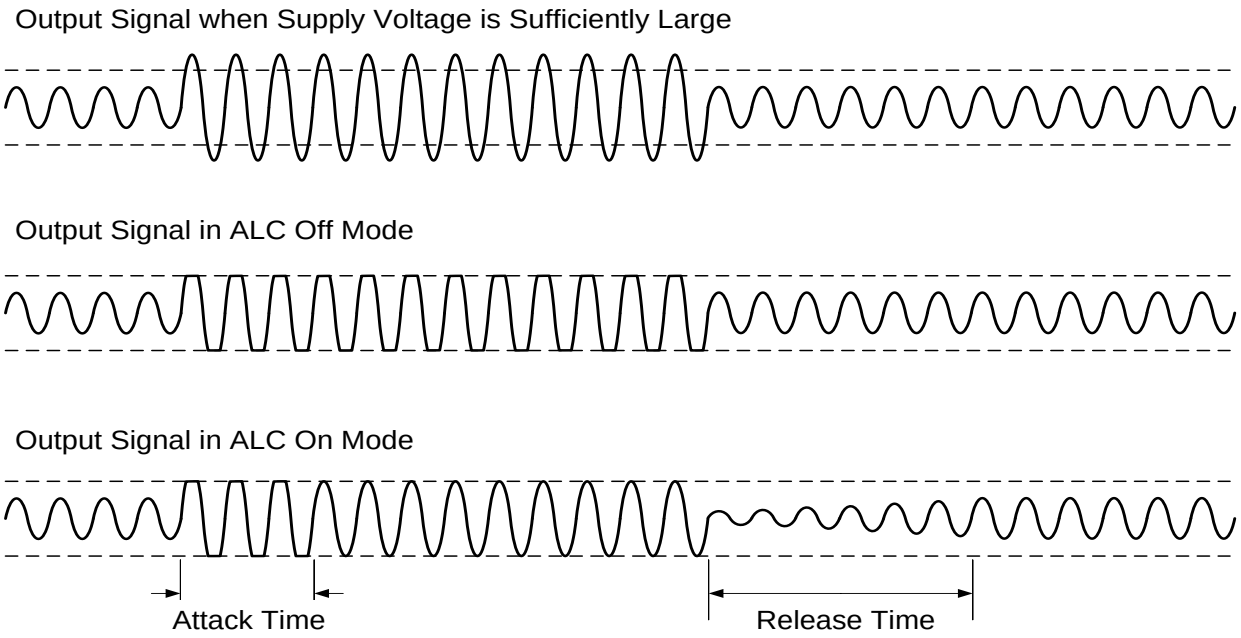


Figure 21: Automatic Level Control Diagram

The attack time and release time of the ALC are shown in Table 1. The attack time is defined as the time interval required for the gain to fall to its steady-state gain less 3dB approximately, assumed that a sufficiently large input signal is applied. The release time is the time interval required for the amplifier to exit out of the present mode of operation.

Attack Time (ms)	Release Time (ms)
20	500

Table 1: Attack Time & Release Time

OPERATING MODE CONTROL

As described in Table 2, depending upon the voltage V_{CTRL} at the CTRL pin, the ft2705 can be configured in one of the three operating modes. If V_{CTRL} is set less than 0.4V, the ft2705 is in shutdown mode. If V_{CTRL} is set in the range between 1.1V and 1.4V, the ft2705 operates in ALC mode, where the ft2705 constantly monitors and safeguards the audio outputs of both channels against the applied supply voltage. Once an over-level condition is detected in either channel, the ALC lowers the voltage gain of both audio amplifiers proportionally to eliminate output clipping. If V_{CTRL} is set higher than 1.6V, the ft2705 operates in Non-ALC mode, where the ft2705 operates as a conventional Class-D amplifier without ALC function.

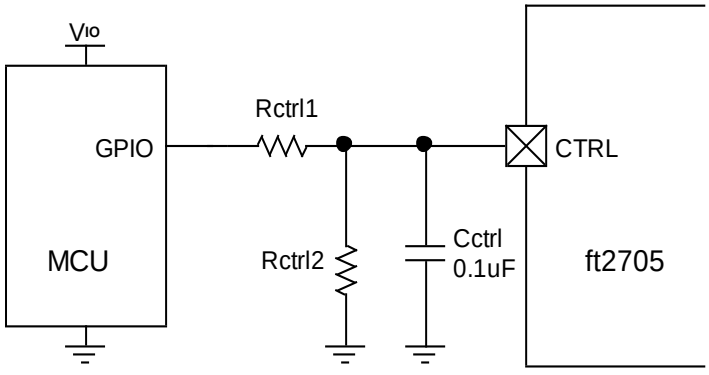
The ALC mode of operation can be chosen for the applications where the audio quality is one of major design considerations and the output clipping must be substantially eliminated. On the contrary, the Non-ALC operation can be chosen for the applications where a maximum audio loudness is much desired.

Voltage @ CTRL	Operating Mode
$V_{CTRL} \leq 0.4V$	Shutdown
$1.1V \leq V_{CTRL} \leq 1.4V$	ALC
$V_{CTRL} \geq 1.6V$	Non-ALC

Table 2: Operating Mode Control

An example of setting the ALC mode of operation by a host processor or microcontroller is shown in Figure 22. As depicted in the figure, two external resistors (R1, R2 with 1% accuracy) connected to the CTRL pin and a GPIO port from the host is used to set the voltage at the CTRL pin. It is recommended to add a ceramic capacitor ($\geq$0.1uF) to the CTRL pin to smooth out the mode transition as well as to minimize noise interference.

In the table of Figure 22, “H” indicates a high-level output voltage (V_{IO}) at the host’s I/O port. “L” indicates a low-level output voltage at the port. To generate a proper voltage at the CTRL pin for a specific mode of operation, the GPIO port is required to have sufficient pulldown capabilities. Also, the ground of the host must be at the same potential as that of ft2705. Furthermore, the voltage at the CTRL pin is a function of the supply voltage (V_{IO}) applied onto the host.



GPIO	Operating Mode
H	ALC
L	Shutdown

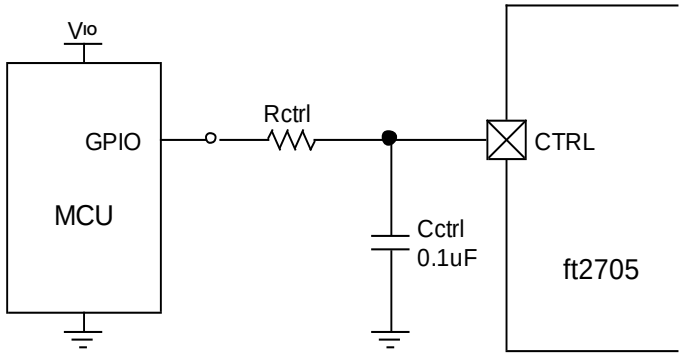
Figure 22: CTRL Setup Circuit Diagram for ALC Mode of Operation

Table 3 defines typical resistor values that can be used to set up proper CTRL voltages for various supply voltages at V_{IO}.

V_{IO} (V)	1.8	2.8	3.0	3.3	4.2	5.0
R1 (kΩ)	10	12	20	24	22	30
R2 (kΩ)	22	10	15	15	10	10

Table 3: Typical Resistor Values for CTRL Setup Circuit

For applications where Non-ALC operation is desired, the CTRL circuit diagram shown in Figure 22 can be further simplified as shown in Figure 23. In this case, one external resistor (Rctrl) and one GPIO port are used to set the voltage at the CTRL pin. The value of the resistor is chosen such that the resulting RC time constant (≥1ms) will provide sufficient noise rejection at the CTRL pin.



GPIO	Operating Mode
H	Non-ALC
L	Shutdown

Figure 23: CTRL Setup Circuit Diagram for Non-ALC Mode of Operation

VOLTAGE GAIN SETTING

In ft2705, the voltage gain of the audio amplifier can be externally adjusted by inserting external input resistors, R_{IN}, in series with the input capacitors, as depicted in Figure 24 and 25. In both figures, it is required that C_{IN} = C_{INL1} = C_{INL2} = C_{INR1} = C_{INR2}, R_{IN} = R_{INL1} = R_{INL2} = R_{INR1} = R_{INR2}.

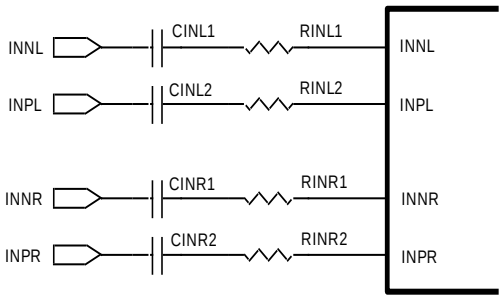


Figure 24: Gain Setting (Differential Inputs)

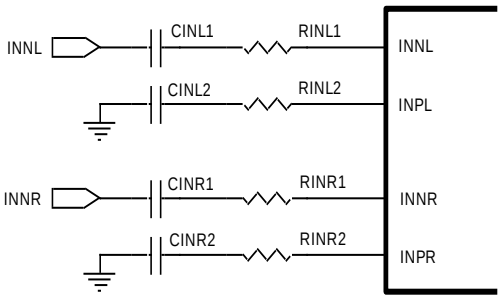


Figure 25: Gain Setting (Single-Ended Inputs)

The value of R_{IN} (in kΩ) for a given voltage gain can be calculated by Equation 1, where A_V is the voltage gain of the audio amplifier.

$$A_V = \frac{625}{R_{IN} + 15} \qquad (1)$$

Table 4 shows suitable resistor values of R_{IN} that can be used for various voltage gains.

R_{IN} (kΩ)	10	16	20	24	30	36	39	47	56	62
A_V (dB)	28	26	25	24	23	22	21	20	19	18

Table 4: External Input Resistor Values Required for Various Voltage Gains

The choice of the voltage gain will strongly influence the loudness and quality of audio sounds. In general, the higher the voltage gain is, the louder the sound is perceived. However an excessive voltage gain may cause audio outputs to be severely clipped for high-level (loud) audio sounds. On the other hand, an unusually low gain may cause relatively low-level (quite) sounds soft or inaudible. Thus it is crucial to choose a proper voltage gain for well balanced audio quality.

The voltage gain is chosen based upon various system-level considerations including the supply voltage, the dynamic range of audio sources and speaker loads, and the desired sound effects. As a general guideline, the voltage gain can be simply expressed in Equation 2. In the equation, $V_{IN, MAX}$ (in V_{RMS}) is the maximum input level from the audio source, VDD (in volts) is the supply voltage, and α is the design parameter, which ranges from 0.65 to 2.2. The higher α is, the higher the average output power (louder) is, with some degree of compression for high-level audio sounds.

$$A_V = \frac{\alpha \times VDD}{V_{IN, MAX}} \qquad (2)$$

As an example, Table 5 shows the voltage gains for various input levels and VDD settings with α at about 1.0. In the table, R_{IN} is the external input resistor in series with the input capacitor.

VDD (V)	$V_{IN, MAX}$ (V_{RMS})	R_{IN} (kΩ)	A_V (V/V)	A_V (dB)	$P_{O, ALC}$ (W) with 4Ω+33μH Load
8.8	0.3	10	25	28	7.7
	0.5	20	18	25	
	0.7	36	12	22	
	1.0	62	8	18	
7.2	0.3	16	20	26	5.2
	0.5	33	13	22	
	0.7	47	10	20	
6.5	0.3	20	18	25	4.2
	0.5	36	12	22	
	0.7	56	9	19	

Table 5: Typical Voltage Gain Settings & Input Resistor Values for Various Input Levels

MONO MODE (PBTL CONFIGURATION)

The ft2705 features an optional mono mode that allows the left and right channels to operate in parallel BTL configuration, delivering 14W into a single 3Ω speaker. To operate ft2705 in mono mode, connect the INNR and INPR pins (pin 15 and 16) directly to ground (no decoupling capacitors). In mono mode, as shown in Figure 26, an audio input signal applied to the left channel (pin 1 and 2) is routed to the H-bridge of both channels. Note that it is intended for the mono mode to be configured strictly by the hardware connection. Leaving either INNR or INPR pin unconnected while the audio outputs VOPL/R and VONL/R are wired together in PBTL configuration can trigger an over-current or thermal overload protection or both. The mono mode is configured by the following arrangement:

- Connect INPR and INNR pins directly to ground (no decoupling capacitors).
- Apply an audio signal to the left-channel inputs (INPL and INNL pins).
- Connect VOPL to VONL together as one terminal of the speaker and connect VOPR to VONR together as the other terminal of the speaker. Use heavy PCB traces as close as possible to the device.
- Place the speaker between the left and right-channel outputs.

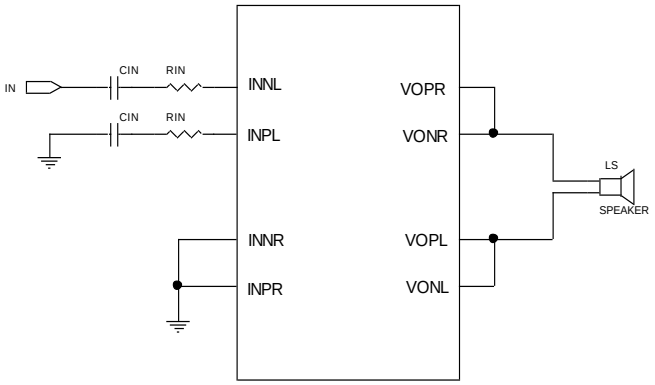


Figure 26: Application Circuit of ft2705 in Mono Mode for PBTL Configuration

VOLUME FADE-IN & FADE-OUT

The volume fade-in/out function operates when the CTRL toggles. This function is used to reduce intermittent sound considerably and eliminate uncomfortable feeling.

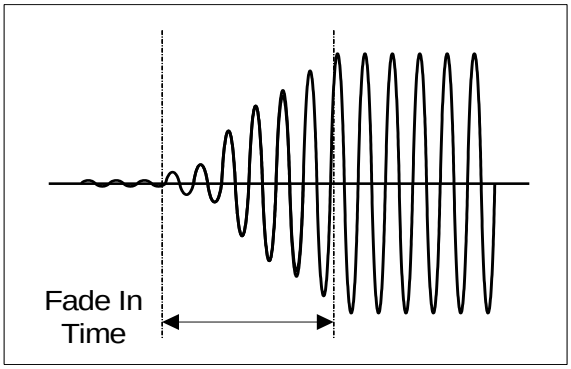


Figure 27: Fade-In Waveform

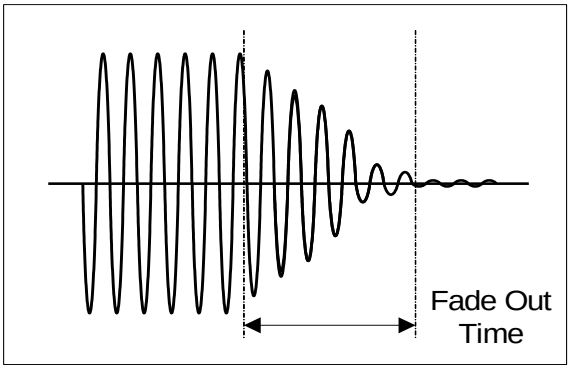


Figure 28: Fade-Out Waveform

BYP PIN

A reference voltage is internally generated and provided to the BYP pin as the common-mode voltage bias of internal analog circuitry. It is required to decouple BYP with a low equivalent-series-resistance (ESR) ceramic capacitor of 1µF to ground for low distortion and high PSRR operation.

SHUTDOWN AND STARTUP

The ft2705 employs the CTRL pin to minimize power consumption while it is not in use. When the CTRL pin is pulled to ground, the ft2705 is forced into shutdown mode, where all the analog circuitry is de-biased and the supply current is thus reduced to less than 20µA, and the differential outputs are shorted to ground through an internal resistor (2.5kΩ) individually. Once in shutdown mode, the CTRL pin must remains low for at least 20ms (T_{SD}), the shutdown settling time, before it can be brought high again. When the CTRL pin is asserted high, the device exits out of shutdown mode and enters into either ALC or Non-ALC mode after the startup time (T_{STUP}) of 160ms.

Note that an internal pulldown resistor of 300kΩ is integrated onto the CTRL pin. Furthermore, shutdown mode is the state when the power supply is first applied to the device. Whenever possible, it is recommended to assert the CTRL pin high to exit the device out of shutdown mode only after the device is properly powered up. Also, place the amplifiers in shutdown mode prior to removing the power supply voltage for best power-off pop performance.

CLICK-AND-POP SUPPRESSION

The ft2705 features comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces any audible transients internal to the device. When entering into shutdown, the differential

audio outputs VOPL/R and VONL/R ramp down to ground quickly and simultaneously.

PSRR ENHANCEMENT

With a dedicated pin, BYP, for the common-mode voltage bias and an external holding capacitor onto the pin, the ft2705 achieves a PSRR, 70dB at 1kHz.

PROTECTION MODES

The ft2705 incorporates various protection functions against possible operating faults for a safe and reliable operation. It includes Under-voltage Lockout (UVLO), Over-Current Protection (OCP), and Over-Temperature Shutdown (OTSD).

Under-Voltage Lockout (UVLO)

The ft2705 incorporates a circuitry to detect a low supply voltage for a safe and reliable operation. When the supply voltage is first applied, the ft2705 will remain inactive until the supply voltage exceeds 3.2V (V_{UVLU}). When the supply voltage is removed and drops below 2.9V (V_{UVLD}), the ft2705 enters into shutdown mode immediately.

Over-Temperature Shutdown (OTSD)

When the die temperature exceeds a preset threshold, the device enters into the over-temperature shutdown mode, where the differential audio outputs VOPL/R and VONL/R are pulled to ground through on-chip resistors individually. The device will resume normal operation once the die temperature returns to a lower temperature, which is about 20°C lower than the threshold.

Over-Current Protection (OCP)

During operation, the outputs of the Class-D amplifiers are constantly monitored for any over-current and/or short-circuit conditions. When a short-circuit condition between two differential outputs or differential outputs to the supply voltage or ground, the output stage of the respective Class-D amplifier is immediately forced into high impedance state. Once the fault condition persists over a prescribed period, the ft2705 then enters into the shutdown mode and remains in this mode for about 40ms (T_{OCP}), the over-current recovery time. When the shutdown mode times out, the ft2705 will initiate another start-up sequence and then check if the short-circuit condition has been removed. If the fault condition is still present, the ft2705 will repeat itself for the process of a startup followed by detection, qualification, and shutdown. It is so-called the hiccup mode of operation. Once the fault condition is removed, the ft2705 automatically restores to its normal mode of operation.

Although the output stages of the Class-D audio amplifiers can withstand a short between VOPL/R and VONL/R, do not short audio outputs (VOPL/R and VONL/R) directly to ground (PGNDL/R) or the supply voltage (PVDDL/R) as this might damage the device permanently, particularly when the supply voltage is higher than 8.4V.

CLASS-D AUDIO AMPLIFIER

The Class-D audio amplifiers in the ft2705 operate in much the same way as traditional Class-D amplifiers and similarly offer much higher power efficiency than Class-AB amplifiers. The high efficiency of Class-D operation is achieved by the switching operation of the output stage of the amplifier. The power loss associated with the output stage is limited to the conduction and switching loss of the power switches, which are much less than the power loss associated with a linear output stage in Class-AB amplifiers.

Fully Differential Amplifier

The ft2705 includes a pair of fully differential amplifiers with differential inputs and outputs. The fully differential amplifiers ensure that the differential output voltages are equal to the differential input voltages time the amplifier gain. Although the ft2705 supports for single-ended inputs, differential inputs are much preferred for applications where the environment can be noisy in order to ensure maximum SNR.

Low-EMI Filterless Output Stage

Traditional Class-D audio amplifiers require for the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. The ft2705 applies an edge-rate control circuitry to reduce EMI emission, while maintaining high power efficiency.

Filterless Design

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filter adds cost, increases the solution size of the amplifier, and can adversely affect efficiency and THD+N performance. The traditional PWM scheme uses large differential output swings (twice of the supply voltage) and causes large ripple currents. Any parasitic resistance in the filter components results in loss of power and lowers the efficiency.

The ft2705 does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. By eliminating the output filter, a smaller, less costly, and more efficient solution can be accomplished.

Because the frequency of the ft2705 output is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimal performance, use a speaker with a series inductance greater than 10μH. Typical 4Ω speakers exhibit series inductances in the range from 10μH to 47μH.

Ferrite Bead EMI Filter

The ft2705 does not require an LC output filter for short connections from the amplifier to the speaker. However, additional EMI suppression can be made by use of a simple ferrite bead filter comprising a ferrite bead and a capacitor, as shown in Figure 29. Choose a ferrite bead with low DC resistance (DCR) and high impedance (100Ω ~ 220Ω) at high frequencies (>100MHz). The current flowing through the ferrite bead must be also taken into consideration. The effectiveness of ferrites can be greatly aggravated at much lower than the rated current values. Choose a ferrite bead with a rated current value no less than 3A. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Choose a capacitor less than 1nF based on EMI performance. Place each ferrite bead filter tightly together and individually close to VOPL/R and VONL/R pins, respectively.

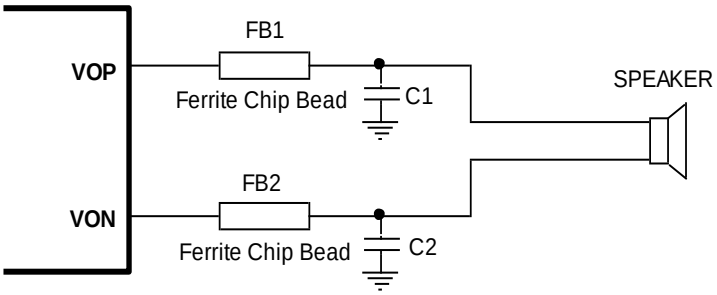


Figure 29: Ferrite Bead Filter to Reduce EMI

Class-D Output RC Snubber Circuit

For applications where the power supplies are rated more than 8.4V or the speaker load resistances less than 4Ω, it may become necessary to add an RC snubber circuit across the two output pins, VOPL/R and VONL/R, of each individual channel to prevent the device from accelerated deterioration or abrupt destruction due to excessive inductive flybacks that are induced on fast output switching or by an over-current or short-circuit condition. The snubber circuit can also lower EMI emission of Class-D outputs.

Figure 30 shows a simple RC snubber circuit with suggested values of R_3=4.7Ω in series with C_3=10nF. Note that the design of the RC snubber circuit is specific to each design and must take into account the parasitic reactance of the system board to reach proper values of R_3 and C_3. Evaluate and ensure that the voltage spikes (overshoots and undershoots) at VOPL/R and VONL/R on the actual system board are within their absolute

maximum ratings. Pay close attention to the layout of the RC snubber circuit to be tight and individually close to VOPL/R and VONL/R pins, respectively.

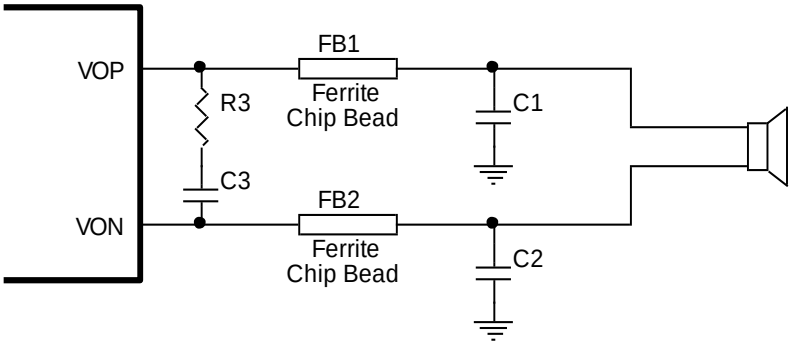


Figure 30: Class-D Output RC Snubber Circuit

Supply Decoupling Capacitor (C_{PVDDL}, C_{PVDDR})

As a high performance Class-D audio power amplifier, the ft2705 requires sufficient decoupling of the power supply to ensure its high efficiency, low distortion, and low EMI. Sufficient power supply coupling also prevents oscillations for long lead lengths between the amplifier and the speakers. It is highly recommended to use a solid ground plane GND on the system board to reduce parasitic resistances and inductances of the ground.

For best audio quality and reliability, place a 1µF low-ESR ceramic capacitor ($C_{PVDDL/R}$) individually close to PVDDL/R pins respectively. In tandem with each 1µF capacitor, add a small, good quality, low-ESR ceramic capacitor of 0.047µF, within 2mm of the PVDDL/R pins, for high-frequency filtering and EMI reduction.

Input Resistors (R_{INL1}, R_{INL2}, R_{INR1}, R_{INR2})

In ft2705, individual 15kΩ input resistors are internally integrated onto INPL/R and INNL/R pins, respectively. Internal input resistors bring such benefits as fewer variations on PSRR and minimum turn-on pop noise since on-chip resistors tend to match well. Additional input resistors can be externally added onto INPL/R and INNL/R pins respectively for specific voltage gains. The value of external input resistors must be included for the calculation of overall voltage gain, as described in Equation 3, as well as the selection of proper input capacitors, as described in Equation 4. As shown in Equation 3, the external input resistors attenuate the original voltage gain by the ratio of $R_{INTERNAL}$ / (R_{IN}+$R_{INTERNAL}$).

$$A_V = A_{V0} \times [R_{INTERNAL} / (R_{IN}+R_{INTERNAL})] \quad (3)$$

where A_{V0} = 42 (32dB) and $R_{INTERNAL}$ = 15kΩ

Input Capacitors (C_{INL1}, C_{INL2}, C_{INR1}, C_{INR2})

The input DC decoupling capacitors are recommended to bias the incoming audio inputs to a proper DC level. The input capacitor C_{IN}, in conjunction with the amplifier input resistance (including both internal 15kΩ and external resistor R_{IN}, if any) forms a highpass filter that removes the DC bias of the audio inputs. The corner frequency, f_C, of the highpass filter is given by Equation 4.

$$f_C = 1 / [2 \times \pi \times (R_{IN} + 15k\Omega) \times C_{IN}] \quad (4)$$

where $C_{IN} = C_{INL1} = C_{INL2} = C_{INR1} = C_{INR2}$ and $R_{IN} = R_{INL1} = R_{INL2} = R_{INR1} = R_{INR2}$

R_{IN} is the external input resistance for a specific voltage gain. Note that the variation of the actual input resistance will affect the voltage gain proportionally. Choose R_{IN} with a tolerance of 2% or better.

Choose C_{IN} such that f_C is well below the lowest frequency of interest. Setting it too high affects the amplifiers' low-frequency response. Consider an example where the specification calls for A_V=28dB and a flat frequency response down to 20Hz. In this example, R_{IN}=10kΩ and C_{IN} is calculated to be about 0.32µF; thus 0.33µF, as a common choice of capacitance, can be chosen for C_{IN}.

Note that any mismatch in resistance or capacitance between two audio inputs will cause a mismatch in the

corner frequencies. Severe mismatch may also cause turn-on pop noise, PSRR, CMRR performance. Choose C_{IN} with a tolerance of ±2% or better.

Furthermore, the type of the input capacitor is crucial to audio quality. For best audio quality, use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies. Other factors, including the constraints of the overall system such as the physical size of the speakers, are to be considered when designing the input filter.

PRINTED CIRCUIT BOARD (PCB) LAYOUT

Decoupling capacitors – Place the decoupling capacitors C_{PVDDDL} and C_{PVDDR} as individually close to PVDDL and PVDDR pins as possible. Large bulk power supply decoupling capacitors should be placed close to the ft2705. Also, place the decoupling capacitor C_{BYP} as close to BYP pin as possible.

Grounding – Use a ground plane with sufficiently wide area on the system board. The PGNDL/R pins must be directly connected to the ground plane GND. Also, the thermal pad underneath the package must be directly soldered to the ground plane.

Ferrite Bead EMI Filter – The ferrite EMI filters should be placed tightly together and individually close to their respective audio output pins, VOPL/R and VONL/R, for the best EMI performance. Keep the current loop, traversing from each individual audio output through the ferrite bead and the filter capacitor and back to PGNDL/R, as tight and short as possible.

Class-D Output RC Snubber – Place RC snubber circuits tightly together and as close as possible to the audio output pins, VOPL/R and VONL/R.

TYPICAL APPLICATION CIRCUITS

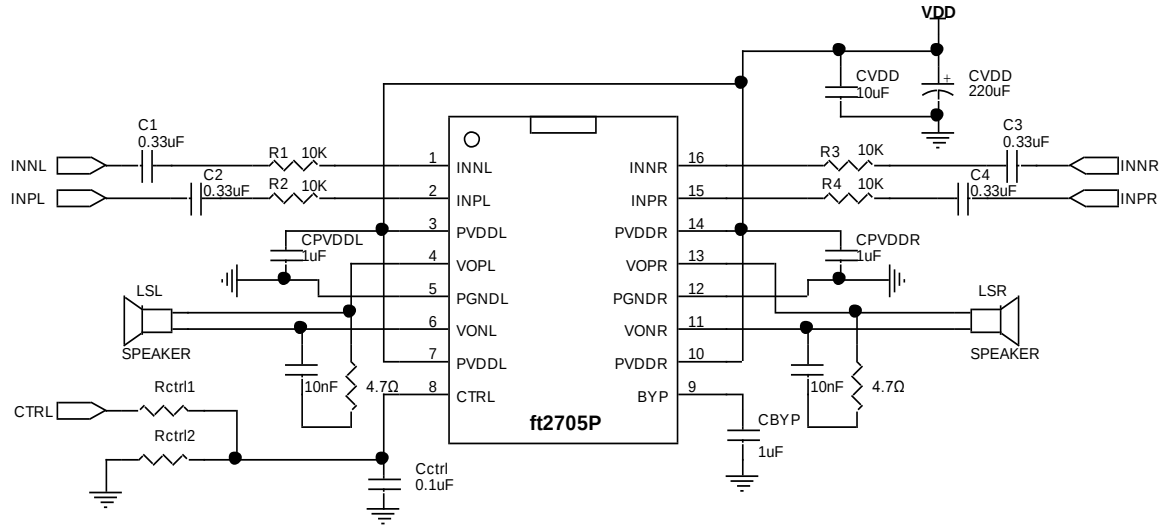


Figure 31: Differential Inputs in Dual BTL Configuration with ALC

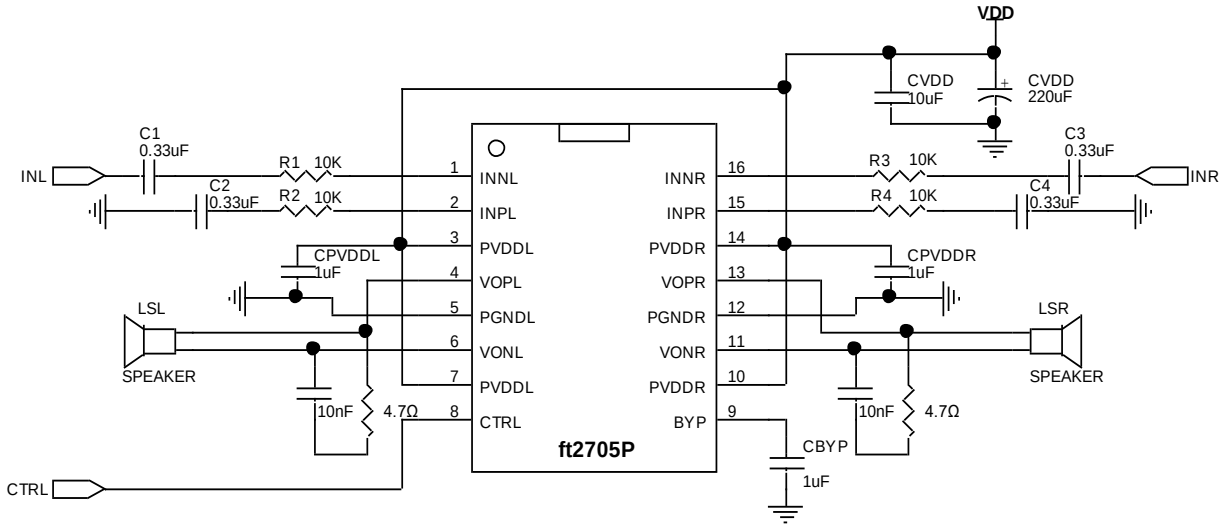


Figure 32: Single-Ended Inputs in Dual BTL Configuration without ALC

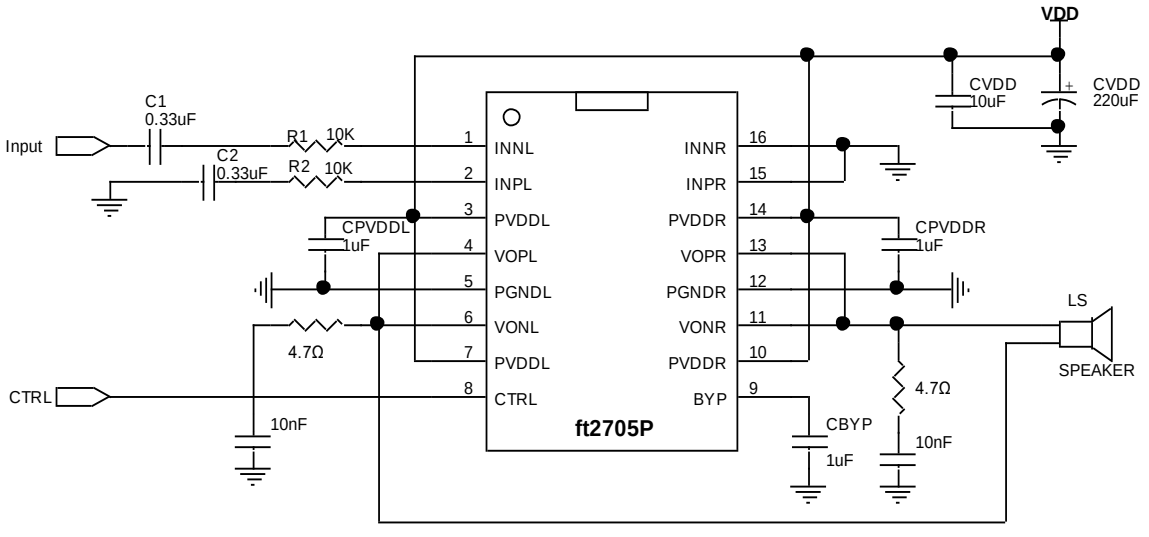
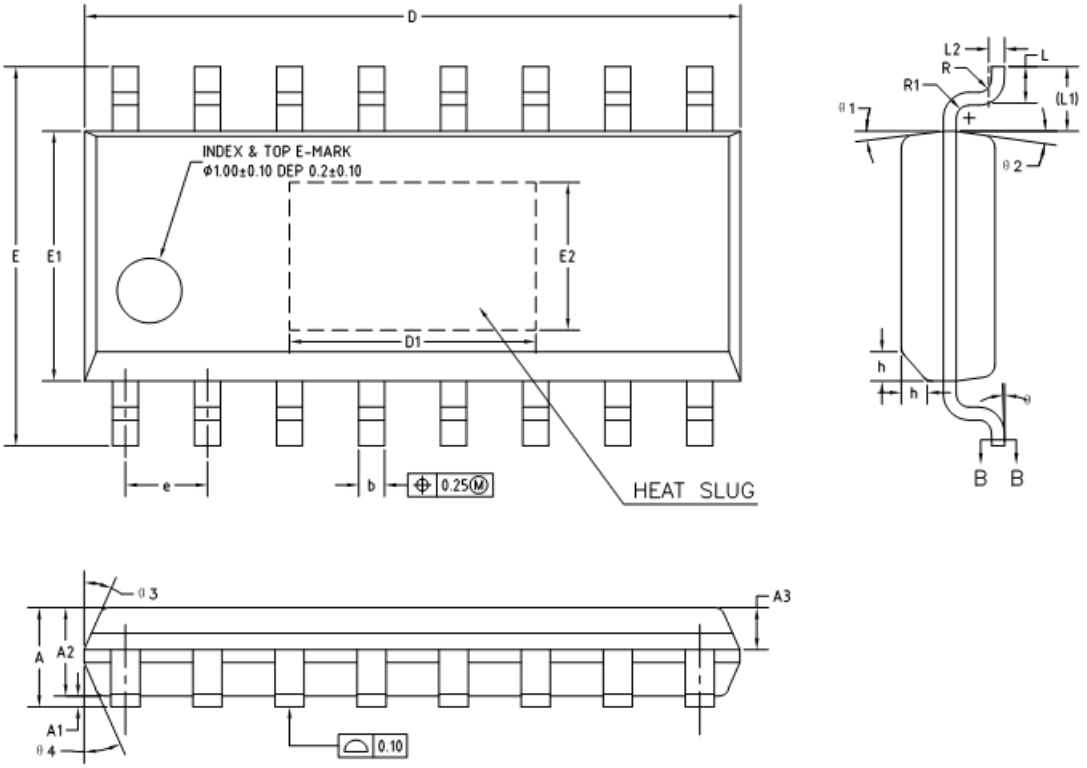


Figure 33: Single-Ended Input in PBTL Configuration without ALC

PHYSICAL DIMENSIONS

SOP-16L PACKAGE OUTLINE DIMENSIONS



SYMBOL		MIN	NOM	MAX
A		1.35	1.52	1.70
A1		0.02	0.07	0.12
A2		1.35	1.45	1.55
A3		0.55	0.65	0.75
D		9.86	9.96	10.06
D1	OPTION1	3.30	3.81	4.00
	OPTION2	3.70	4.06	4.20
E		5.80	6.00	6.20
E1		3.80	3.90	4.00
E2	OPTION1	1.78	2.29	2.50
	OPTION2	1.70	2.08	2.20
e		1.17	1.27	1.37
L		0.45	0.60	0.80
L1		1.04REF		
L2		0.25BSC		
R		0.07	–	–
R1		0.07	–	–
h		0.30	0.40	0.50
θ		0°	–	8°
θ 1		6°	8°	10°
θ 2		6°	8°	10°
θ 3		5°	7°	9°
θ 4		5°	7°	9°

Unit: mm

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