# FSUSB242

# Type-C USB Port Protection Switch

### Features

- Fully USB Data Port Protection
- $V_{DD}$ 0 V– 5.5 V (12 V DC tolerant)
- –18 V to +20 V DC Tolerance on HSD± Port
- ±25 V IEC 61000–4–5 Surge Protection w/o External TVS
- $V_{DD}$ Operating Range, 2.7 V–5.5 V
- HSD RON: 5 Ω Typical
- $C_{ON}$ = 5 pF Typical
- Wide –3 dB Bandwidth: > 720 MHz
- Low Power Operation: $I_{CC}$ < 10 μA (Typical)
- Over Voltage Protection: 3.6 V & 4.5 V

### Typical Applications

- Smartphones
- Tablets
- Laptops

### Safety Mechanisms Highlight

- 3.6 V & 4.5 V OVP Trip Point
- ±25 V Surge Protection without Need for External TVS

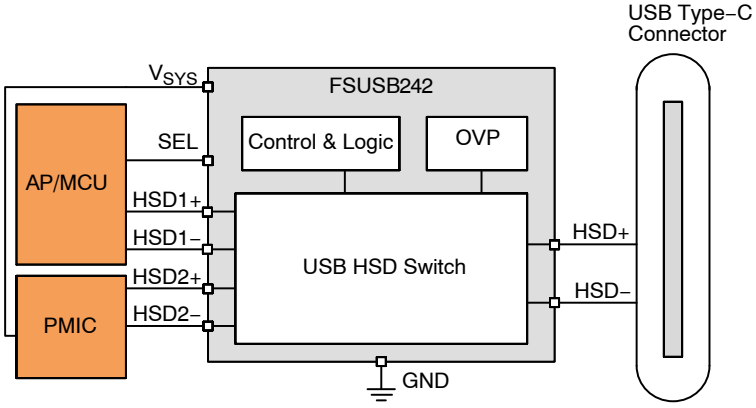


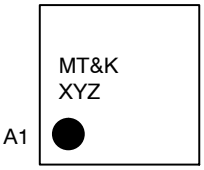

**Figure 1. Application Schematic**

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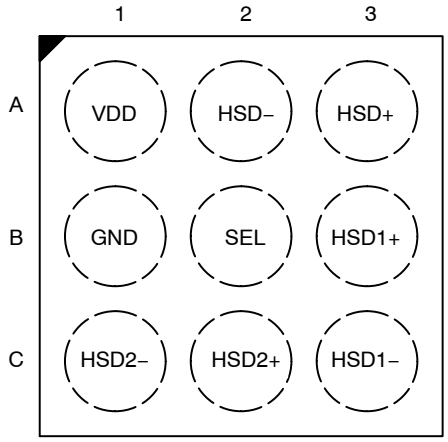
**WLCSP9 1.20 × 1.20**
**CASE 567UL**

### MARKING DIAGRAM




MT = Specific Device Code
&K = 2 Digit Lot Run Code
X = Year
Y = 2 Week Data Code
Z = Plant Code

### PIN CONNECTION




TOP Through View

### ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

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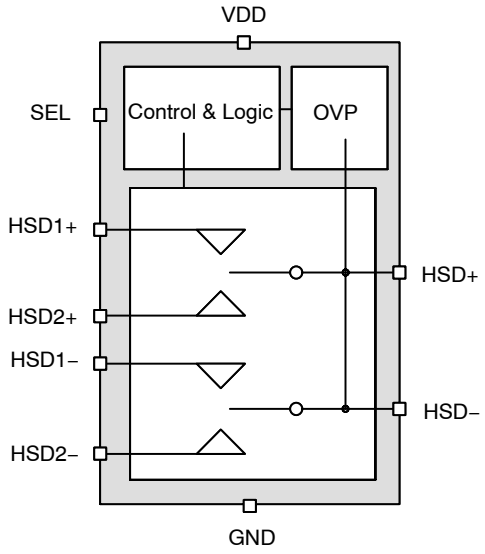



**Figure 2. Simplified Block Diagram**

**Table 1. PIN FUNCTION DESCRIPTION**

| CSP Bump | Name | Type | Description |
|---|---|---|---|
| A1 | VDD | Power | Supply Power |
| B1 | GND | Ground | Ground |
| A3 | HSD+ | Data | Common High Speed Data Bus |
| A2 | HSD− | Data | Common High Speed Data Bus |
| B3 | HSD1+ | Data | Multiplexed High Speed Data Port 1 |
| C3 | HSD1− | Data | Multiplexed High Speed Data Port 1 |
| C2 | HSD2+ | Data | Multiplexed High Speed Data Port 2 |
| C1 | HSD2− | Data | Multiplexed High Speed Data Port 2 |
| B2 | SEL | I/O | Tri−Input HSD Switch Select & /OE |

**Table 2. SWITCH TRUTH TABLE CONFIGURATION**

| VDD | SEL | Switch Configuration |
|---|---|---|
| UVLO | X | Switch off High impedance |
| Valid | 0 | HSD+ = HSD1+, HSD− = HSD1− |
| Valid | 1 | HSD+ = HSD2+, HSD− = HSD2− |
| Valid | Float/High−Z | Switch Disable High impedance |

## APPLICATION INFORMATION

### Over Voltage Protection

Over voltage protection turns the switch off if the inputs HSD+/HSD− rise above the over voltage trip threshold.

### Under Voltage Lockout

The under−voltage lockout on $V_{DD}$ pin turns the switch off if the $V_{DD}$ voltage drops below the lockout threshold. With the SELpin active, the input voltage rising above the UVLO threshold releases the lockout and enables the switch.

### Tri−State Input Control Pin (SEL)

The SEL pin can be tri−stated to disable the switch to save power, there are a few ways to achieve this. If the SEL pin is controlled by GPIO in the system, if the GPIO pin has a High−Z state where the impedance of the High−Z state is larger then 2.5 MΩ the switch will recognize the High−Z state and disable the switch. If the system does not have GPIO that supports High−Z state, the user can utilize 2 MOSFETs or a Logic Device to achieve the same result.

*For GPIO*

The SEL pin function below:

- If the input is pulled up with less than 50 kΩ it will be considered as Logic High
- If the input is pulled down with less than 50 kΩ it will be consider as Logic Low
- If the input is pulled up or down with more 2.5 MΩ it will be consider as float/High−Z

### System Timing Diagram

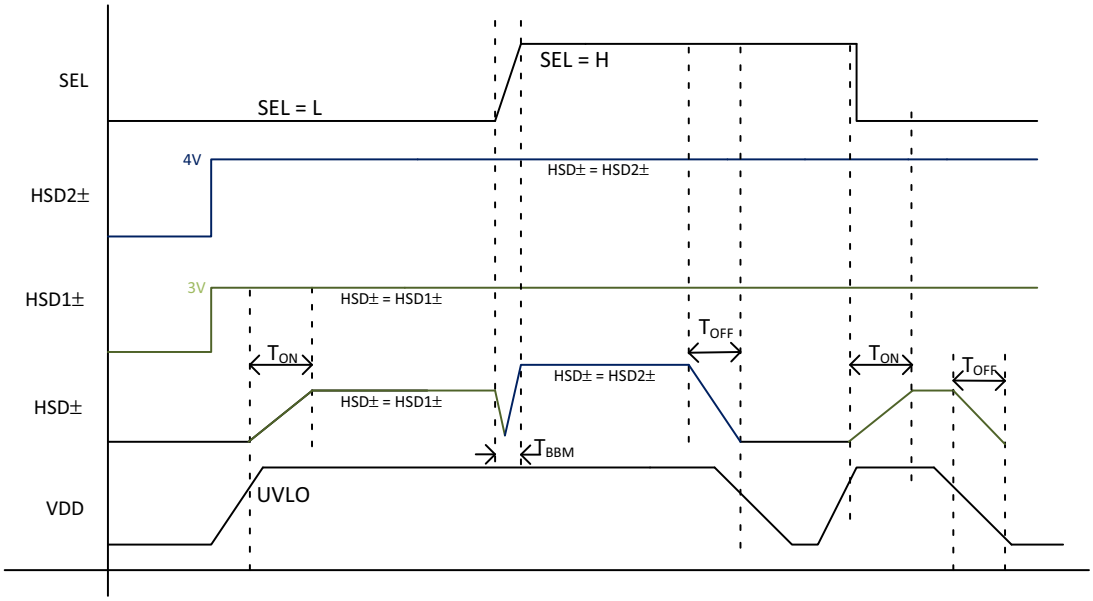



**Figure 3. System Timing Plot**

**System Block Diagrams**

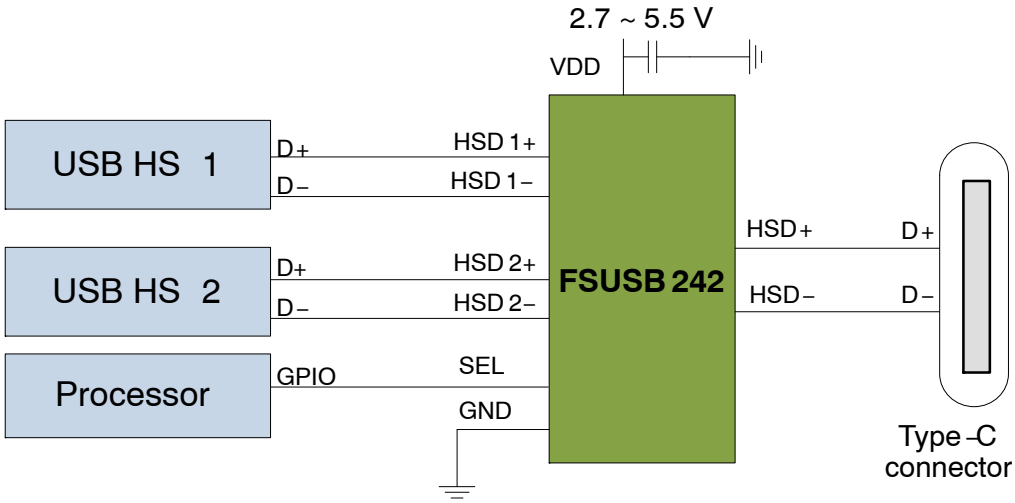



**Figure 4. Application of 2x USB HS interface**

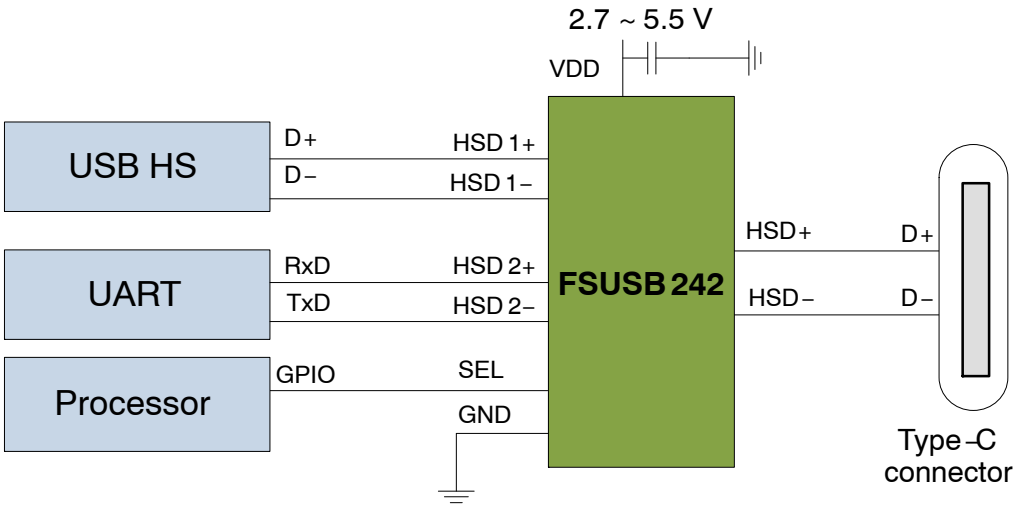



**Figure 5. Application of UART and USB HS interface**

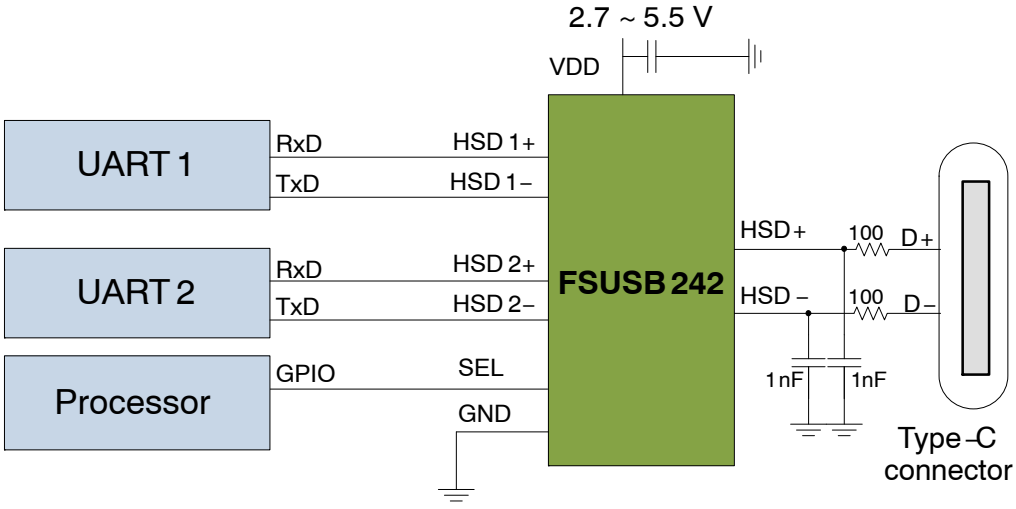



**Figure 6. Application of 2x UART interface**

When 2x UART signals are switched over FSUSB242, both 100 ohm series resistor and 1 nF bypass capacitors are recommended in the common switch path as above. If FSUSB242 is used to switch USB and UART signals, connect UART signals to HSD1.

**USB High Speed Eye Diagram**

*$V_{DD}$ = 5.5 V HSD to HSD1 Path*

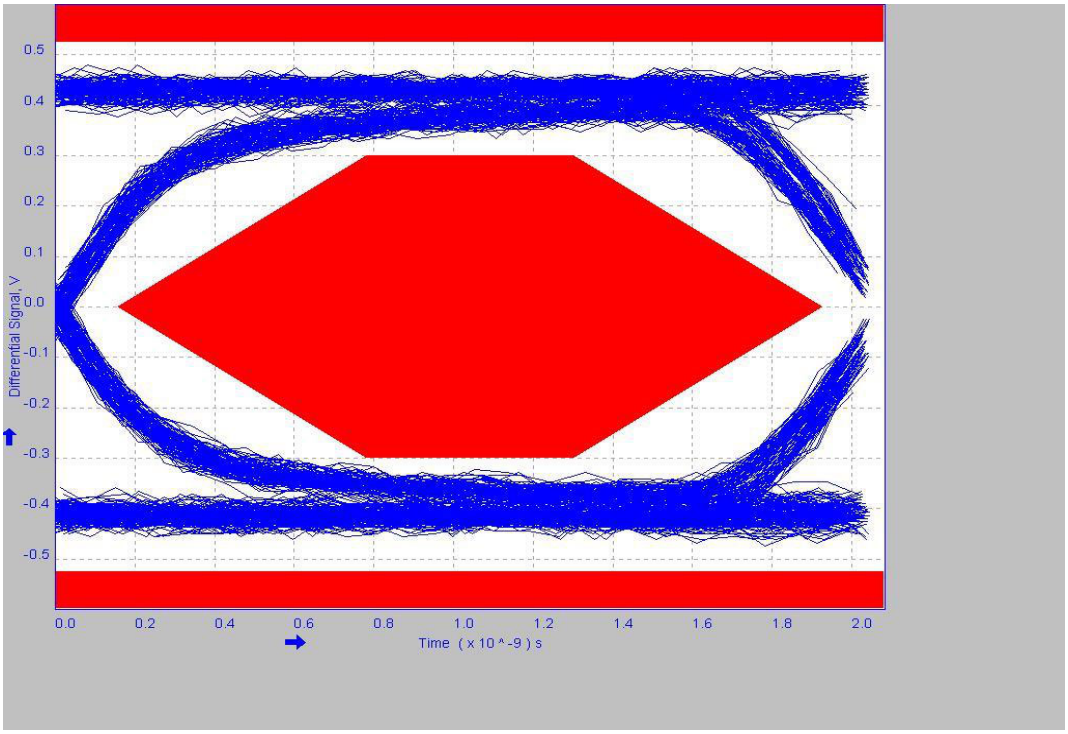



**Figure 7. HS USB Eye @ $V_{DD}$ = 5 V**

*$V_{DD}$ = 2.7 V HSD to HSD2 Path*

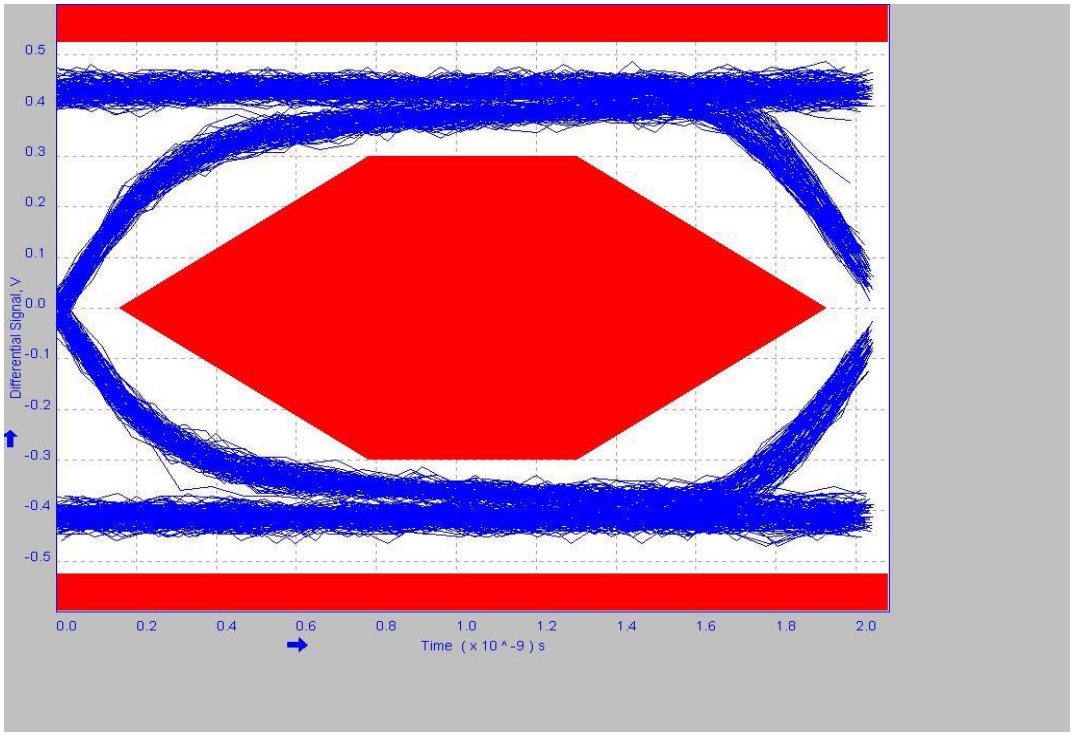



**Figure 8. HS USB Eye @ $V_{DD}$ = 2.7 V**

**Table 3. ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage from $V_{DD}$ | | | −0.5 | 12.0 | V |
| $V_{SW}$ | DC Input voltage tolerance for HSD±, to GND | | | −18 | 20 | V |
| | DC Input voltage tolerance for HSD1±, HSD2± to GND | | | −1.2 | 6 | V |
| $V_{CONTROL}$ | DC Input Voltage (SEL) | | | −0.5 | 6 | V |
| $I_{SW}$ | DC HSD Switch Current | | | | 100 | mA |
| $I_{IK}$ | DC Input Diode Current | | | −50 | | mA |
| $T_{STORAGE}$ | Storage Temperature Range | | | −65 | +150 | °C |
| $T_J$ | Maximum Junction Temperature | | | | +150 | °C |
| $T_L$ | Lead Temperature (Soldering, 10 seconds) | | | | +260 | °C |
| ESD | IEC 61000−4−2 System ESD (Note 1) | Connector Pins (HSD±) | Air Gap | 15 | | kV |
| | | | Contact | 8 | | |
| | Human Body Model, JEDEC JESD22−A114 | Power to GND | | 2 | | kV |
| | | Internal Pin to GND (HSD1±, HSD2±) | | 2 | | |
| | | External Pin to GND (HSD±) | | 14 | | |
| | Charged Device Model, JEDEC LESD22−C101 | All Pins | | 1 | | |
| | IEC 61000−4−5 Surge Protection | HSD±, to GND | | ±25 | | V |
| | | $V_{DD}$ to GND | | +12 | | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. System level test that depends on end system for actual performance. These tests results are with external TVS protection. These specs are listed as general guidelines for expected performance in actual system and do not guarantee listed performance.

**Table 4. RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 2.7 | 4.2 | 5.5 | V |
| $V_{SW1}$ | HSD1 Switch I/O Signal Swing Voltage (Note 2) | −0.5 | | 3.6 | V |
| $V_{SW2}$ | HSD2 Switch I/O Signal Swing Voltage (Note 2) | −0.5 | | 4.5 | V |
| $I_{CCSW}$ | Maximum HSD Switch Continuous Current | | | 75 | mA |
| $V_{CNTRL}$ | Control Input Voltage (SEL) | −0.5 | | $V_{DD}$ | V |
| $T_A$ | Operating Temperature | −40 | | +85 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. The switch swing voltage is based on the OVP trip level, and when OVP triggers the switch will be disabled to protect the host and no longer in the standard operating condition, once over voltage is removed the device will automatically recover back to normal condition.

**Table 5. DC ELECTRICAL CHARACTERISTICS**

(Unless otherwise specified: Recommended $T_A$ and $T_J$ temperature ranges. All typical values are at $T_A$ = 25°C and $V_{DD}$ = 4.2 V unless otherwise specified.)

| Symbol | Characteristic | $V_{DD}$ (V) | Conditions | $T_A$ = −40 to +85°C, $T_J$ = −40 to +125°C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| **BASIC OPERATION DEVICE** | | | | | | | |
| $I_{CC}$ | Quiescent Supply Current | 2.7 to 5.5 | WLCSP: /OE = H & L, $I_{OUT}$ = 0 | | 10 | | μA |
| $I_{OFF}$ | Power−Off Leakage Current | 0 | $V_{SWHSD1}$ = 0 V to 3.6 V, $V_{SWHSD2}$ = 0 V to 4.5 V | −3 | | 3 | μA |

**Table 5. DC ELECTRICAL CHARACTERISTICS** (continued)
(Unless otherwise specified: Recommended $T_A$ and $T_J$ temperature ranges. All typical values are at $T_A$ = 25°C and $V_{DD}$ = 4.2 V unless otherwise specified.)

| Symbol | Characteristic | $V_{DD}$ (V) | Conditions | $T_A$ = −40 to +85°C, $T_J$ = −40 to +125°C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| **BASIC OPERATION DEVICE** | | | | | | | |
| $I_{IN}$ | Control Input Leakage | 2.7 to 5.5 | $V_{CNTRL}$ = 0 V to $V_{DD}$ | −2 | | 4 | μA |
| $I_{OZ}$ | Off State Leakage | 2.7 to 5.5 | HSD± ≥ 0 V, HSD1±, HSD2± ≤ 3.6 V | −3 | | 5 | μA |
| **BASIC OPERATION HSD SWITCH** | | | | | | | |
| $R_{ON}$ | HSD Path On Resistance | 2.7 to 5.5 | $I_{OUT}$ = 8 mA, $V_{SW}$ = 0 V to 0.4 V | | 5 | | Ω |
| $\Delta R_{ON}$ | HSD Path Delta $R_{ON}$ | 2.7 to 5.5 | $I_{OUT}$ = 8 mA, $V_{SW}$ = 0 V to 0.4 V | | 0.15 | | Ω |
| $V_{IH}$ | SEL Input Voltage High | 2.7 to 5.5 | | 1.3 | | | V |
| $V_{IM}$ | SEL Input Voltage Middle (Note 3) | 2.7 to 5.5 | | 0.8 | | 1.0 | V |
| $V_{IL}$ | SEL Input Voltage Low | 2.7 to 5.5 | | | | 0.5 | V |
| Zfloat | Impedance to VDD or GND detected as a Float including $V_{DD}$ = 0 | 2.7 to 5.5 | | 2.5 | | | MΩ |
| $V_{OV_TRIP1}$ | Input OVP Lockout for HSD1 (FSUSB242UCX) | 2.7 to 5.5 | $V_{HSD±}$ Rising, SEL = 0 | 3.6 | 3.8 | 4.0 | V |
| | | | $V_{HSD±}$ Falling, SEL = 0 | 3.3 | 3.5 | | |
| | Input OVP Lockout for HSD1 (FSUSB242UCXF45) | 2.7 to 5.5 | $V_{HSD±}$ Rising, SEL = 0 | 4.5 | 4.7 | 4.9 | V |
| | | | $V_{HSD±}$ Falling, SEL = 0 | 4.2 | 4.4 | | |
| $V_{OV_TRIP2}$ | Input OVP Lockout for HSD2 | 2.7 to 5.5 | $V_{HSD±}$ Rising, SEL = 1 | 4.5 | 4.7 | 4.9 | V |
| | | | $V_{HSD±}$ Falling, SEL = 1 | 4.2 | 4.4 | | |
| $V_{OV_TRIP3_F45}$ (Note 4) | Input OVP Lockout for both HSD1 and HSD2 | 2.7 to 5.5 | $V_{HSD±}$ Rising | 4.5 | 4.7 | 4.9 | V |
| | | | $V_{HSD±}$ Falling | 4.2 | 4.4 | | |
| $V_{OV_HYS}$ | Input OVP Hysteresis | 2.7 to 5.5 | | | 0.3 | | V |
| $V_{NV_TRIP}$ | Input Negative Voltage Lockout | 2.7 to 5.5 | $V_{HSD±}$ Falling | | −1.0 | | V |
| | | | $V_{HSD±}$ Rising | | −0.7 | | |
| $V_{NV_HYS}$ | Input OVP Hysteresis | 2.7 to 5.5 | | | 0.3 | | V |
| $V_{CL}$ | Clamping Voltage | 2.7 to 5.5 | $V_{HSD±} \geq V_{OV_TRIP}$ | | 4.5 | | V |
| $V_{UVLO}$ | Under−Voltage Lockout | | $V_{DD}$ Rising | | 2.4 | 2.7 | V |
| | | | $V_{DD}$ Falling | | 2.3 | | |
| TSD | Thermal Shutdown (Note 3) | | Shutdown Threshold | | 150 | | °C |
| | | | Return from Shutdown | | 130 | | |
| | | | Hysteresis | | 20 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Guaranteed by characterization or Design, not production tested.

4. FSUSB242F45UCX OVP threshold.

**Table 6. AC ELECTRICAL CHARACTERISTICS**

(Unless otherwise specified: Recommended $T_A$ and $T_J$ temperature ranges. All typical values are at $T_A$ = 25°C and $V_{DD}$ = 4.2 V unless otherwise specified.)

| Symbol | Characteristic | $V_{DD}$ (V) | Conditions | $T_A$ = −40 to +85°C, $T_J$ = −40 to +125°C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| **HSD SWITCH TIMING PARAMETER** | | | | | | | |
| $t_{OVP}$ | OVP Response Time (Note 53) | 2.7 to 5.5 | $I_{OUT}$ = 8 mA, $C_L$ = 5 pF, $R_L$ = 50 Ω, $V_{HSD±}$ = 3.3 V to 4.9 V | | 0.35 | | μs |
| $t_{ON}$ | Turn−On Time, SEL to Output | 2.7 to 5.5 | $R_L$ = 50 Ω, $C_L$ = 5 pF | | 0.1 | | ms |
| $t_{OFF}$ | Turn−Off Time, SEL to Output | 2.7 to 5.5 | $R_L$ = 50 Ω, $C_L$ = 5 pF, $V_{SW}$ = 0.8 V | | 0.2 | | μs |
| $t_{PD}$ | Propagation Delay (Note 5) | 2.7 to 5.5 | $R_L$ = 50 Ω, $C_L$ = 5 pF, $V_{SW}$ = 0.8 V | | 1.3 | | ns |
| $t_{BBM}$ | Break−Before−Make (Note 5) | 2.7 to 5.5 | $R_L$ = 50 Ω, $C_L$ = 5 pF, $V_{SW1}$ = $V_{SW2}$ = 0.8 V | | 50 | | μs |
| $t_{SK(P)}$ | Skew of Opposite Transitions of the Same Output (Note 5) | 2.7 to 5.5 | $V_{SW}$ = 0.2 $Vdiff_{PP}$, $R_L$ = 50 Ω, $C_L$ = 5 pF | | 35 | | ps |
| $t_J$ | Total Jitter (Note 5) | 2.7 to 5.5 | $V_{SW}$ = 0.2 $Vdiff_{PP}$, $R_L$ = 50 Ω, $C_L$ = 5 pF, $t_R$ = $t_F$ = 500 ps (10−90%) @ 480 Mbps (PRBS = $2^{15}$ − 1) | | 250 | | ps |
| **HSD± SWITCH CAPACITANCE** | | | | | | | |
| $C_{IN}$ | Control Pin Input Capacitance (Note 5) | 0 | | | 1.5 | | pF |
| $C_{ON}$ | HSD± On Capacitance (Note 5) | 2.7 to 5.5 | SEL = L/H, f = 240 MHz | | 4 | | |
| $C_{OFF}$ | HSD± Off Capacitance (Note 5) | 2.7 to 5.5 | SEL = Float, f = 240 MHz | | 3 | | |
| **HSD SWITCH BANDWIDTH** | | | | | | | |
| BW | −3dB SDD21 Bandwidth (Note 5) | 2.7 to 5.5 | $R_L$ = 50 Ω, $C_L$ = 0 pF | | 1000 | | MHz |
| | | | $R_L$ = 50 Ω, $C_L$ = 5 pF | | 550 | | MHz |
| **HSD SWITCH AC PARAMETER** | | | | | | | |
| $O_{IRR}$ | Off Isolation (Note 5) | 2.7 to 5.5 | $R_L$ = 50 Ω, f = 240 MHz | | −35 | | dB |
| Xtalk | Non−Adjacent Channel Crosstalk (Note 5) | 2.7 to 5.5 | $R_L$ = 50 Ω, f = 240 MHz | | −40 | | dB |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Guaranteed by characterization or Design, not production tested.

## TEST DIAGRAMS

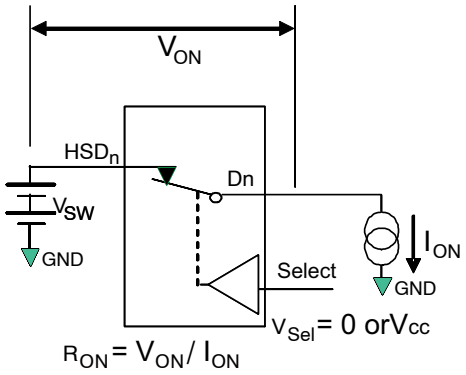
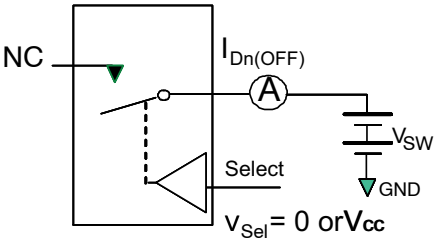
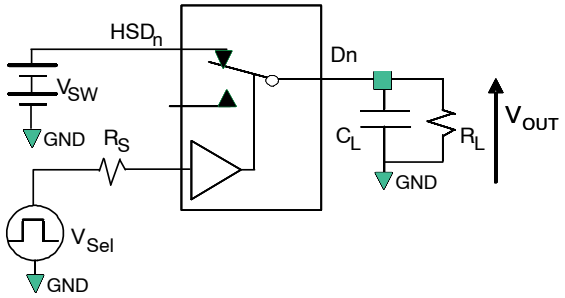



**Figure 9. On Resistance**




**Each switch port is tested separately

**Figure 10. Off Leakage**




$R_L$, $R_S$, and $C_L$ are functions of the application environment (see AC Tables for specific values)
$C_L$ includes test fixture and stray capacitance.

**Figure 11. AC Test Circuit Load**

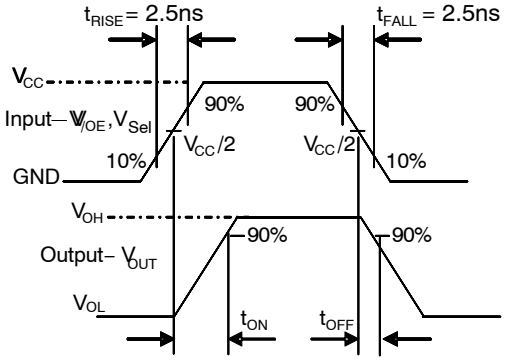



**Figure 12. Turn–On / Turn–Off Waveforms**

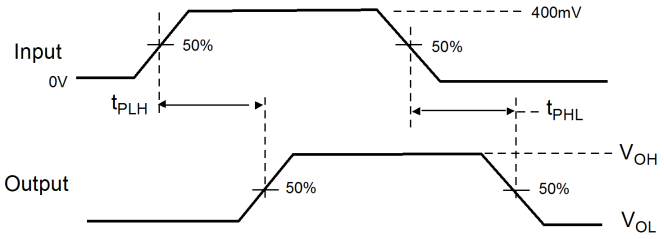



**Figure 13. Propagation Delay ($t_R t_F$ – 500 ps)**

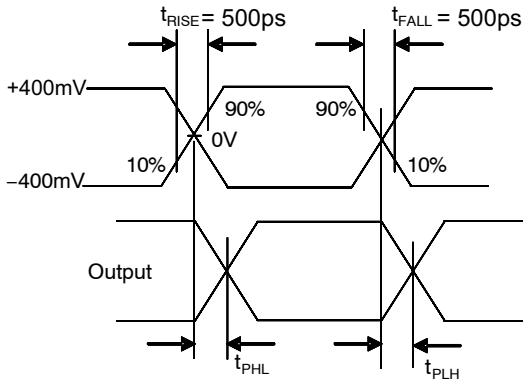
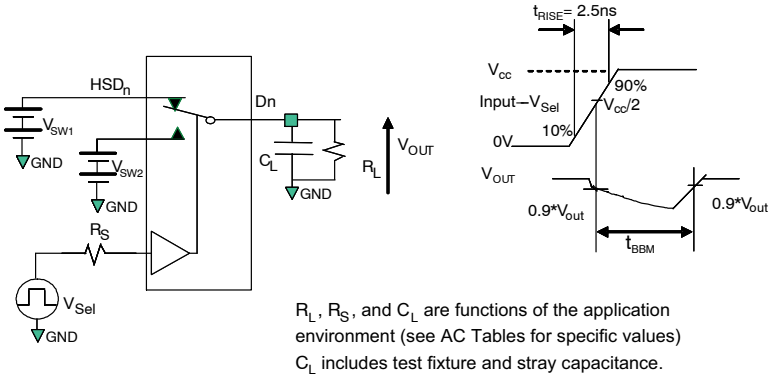


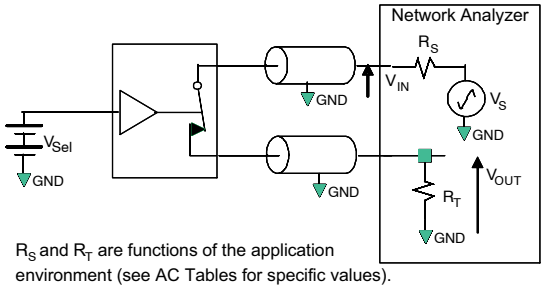

**Figure 14. Intra-Pair Skew Test $t_{SK(P)}$**

## TEST DIAGRAMS (Continued)



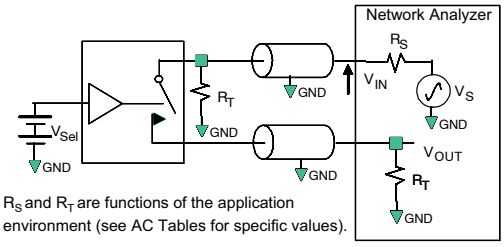

$R_L$, $R_S$, and $C_L$ are functions of the application environment (see AC Tables for specific values)
$C_L$ includes test fixture and stray capacitance.

**Figure 15. Break−Before−Make Interval Timing**




$R_S$ and $R_T$ are functions of the application environment (see AC Tables for specific values).

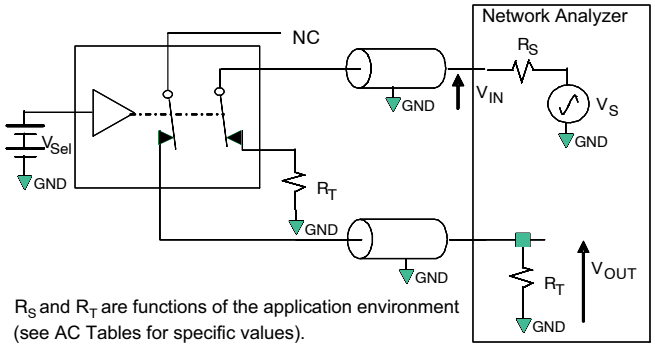
**Figure 16. Bandwidth**




$R_S$ and $R_T$ are functions of the application environment (see AC Tables for specific values).

Off isolation = 20 Log ($V_{OUT}$ / $V_{IN}$)

**Figure 17. Channel Off Isolation**




$R_S$ and $R_T$ are functions of the application environment (see AC Tables for specific values).

Crosstalk = 20 Log ($V_{OUT}$ / $V_{IN}$)

**Figure 18. Non-Adjacent Channel-to-Channel Crosstalk**

## TEST DIAGRAMS (Continued)

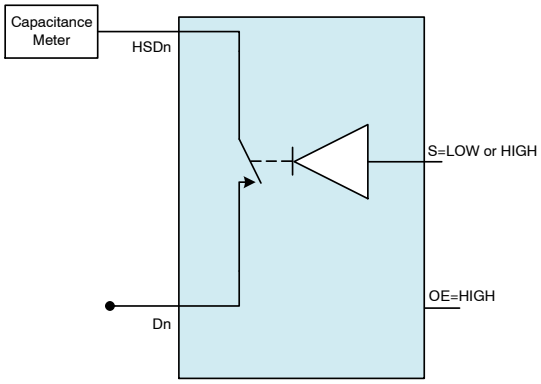



**Figure 19. Channel Off Capacitance**

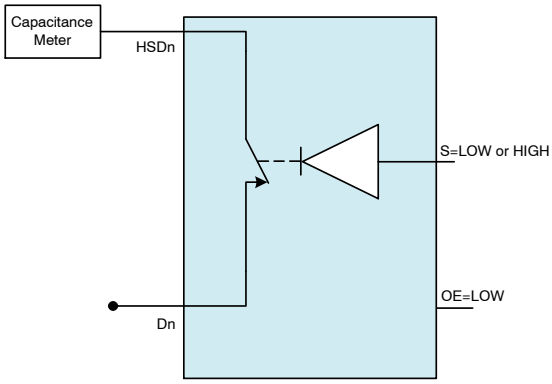



**Figure 20. Channel On Capacitance**

## ORDERING INFORMATION

**Table 7. AVAILABLE PART NUMBERS**

| Part Number | Device Code | Operating Temperature Range | Package | Packing Method† |
|---|---|---|---|---|
| FSUSB242UCX | MT | −40 to 85°C | 9−Ball WLCSP (1.20 x 1.20 mm) | Tape and Reel |
| FSUSB242F45UCX | MU | −40 to 85°C | 9−Ball WLCSP (1.20 x 1.20 mm) | Tape and Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

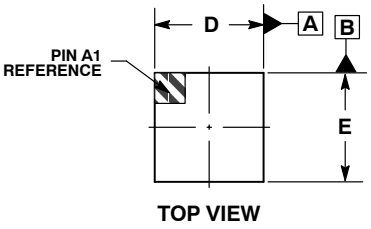
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

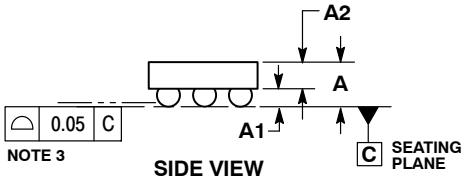
**WLCSP9, 1.2x1.2x0.48**
CASE 567UL
ISSUE A

SCALE 4:1

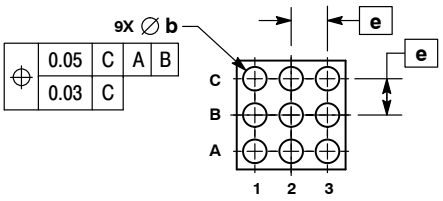
DATE 07 JUL 2017




TOP VIEW




SIDE VIEW

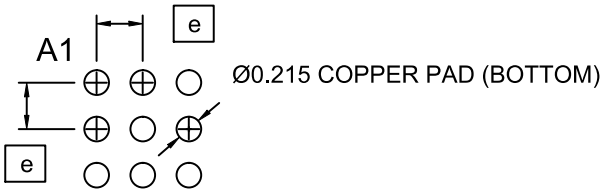



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.450 | 0.488 | 0.526 |
| A1 | 0.176 | 0.196 | 0.216 |
| A2 | 0.274 | 0.292 | 0.310 |
| b | 0.24 | 0.26 | 0.28 |
| D | 1.14 | 1.20 | 1.26 |
| E | 1.14 | 1.20 | 1.26 |
| e | 0.40 BSC | | |

**RECOMMENDED SOLDERING FOOTPRINT* (NSMD PAD TYPE)**




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | | |
|---|---|---|---|
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| **DESCRIPTION:** | **WLCSP9, 1.2x1.2x0.48** | | **PAGE 1 OF 1** |

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