FSES0765RG

Green Mode Fairchild Power Switch (FPS™) for CRT Monitors

Features

- Burst Mode Operation to Reduce the Power Consumption in Standby Mode
- External Pin for Synchronization
- Wide Operating Frequency Range up to 130kHz
- Internal Startup Circuit
- Low Operating Current (Max:6mA)
- Pulse by Pulse Current Limiting
- Over Voltage Protection (Auto Restart Mode)
- Over Load Protection (Auto Restart Mode)
- Abnormal Over Current Protection (Auto Restart Mode)
- Internal Thermal Shutdown (Auto Restart Mode)
- Under Voltage Lockout
- Internal High Voltage SenseFET (650V)

Application

- CRT Monitor

Description

FSES0765RG is a Fairchild Power Switch (FPS) specially designed for off-line SMPS of CRT monitors with minimal external components. This device combines a current mode PWM controller with a high voltage power SenseFET in a single package. The PWM controller features an integrated oscillator to be synchronized with the external sync signal, under voltage lockout, optimized gate driver and temperature-compensated precise current sources for the loop compensation. This device also includes various fault protection circuits such as over voltage protection, over load protection, abnormal over current protection and over temperature protection. Compared with discrete MOSFET and PWM controller solutions, FPS can reduce total cost, component count, size and weight while simultaneously increasing efficiency, productivity and system reliability. This device is well suited for cost effective CRT-monitor power supplies.

OUTPUT POWER TABLE(3)		
PRODUCT	230VAC ±15%(2)	85-265VAC
	Open Frame(1)	Open Frame(1)
FSES0765RG	90 W	70 W

Notes:

1. Maximum practical continuous power in an open frame design at 50°C ambient.
2. 230 VAC or 100/115 VAC with doubler.
3. The maximum output power can be limited by the junction temperature

Typical Circuit

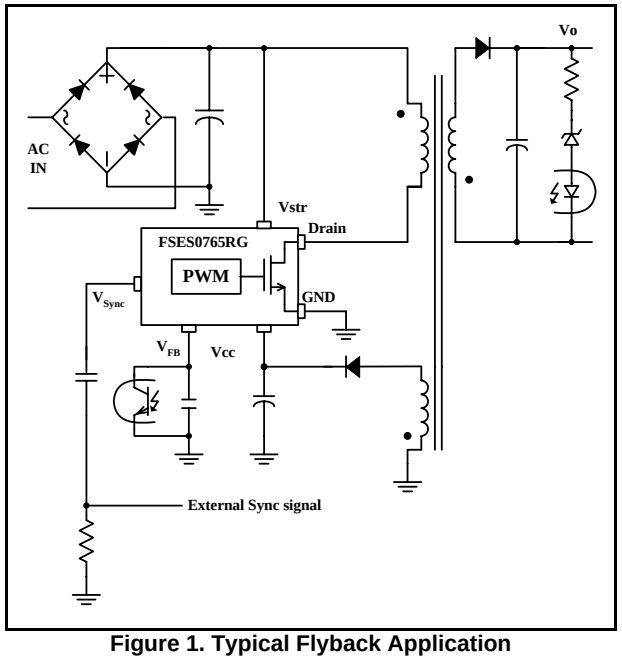


Figure 1. Typical Flyback Application

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Internal Block Diagram

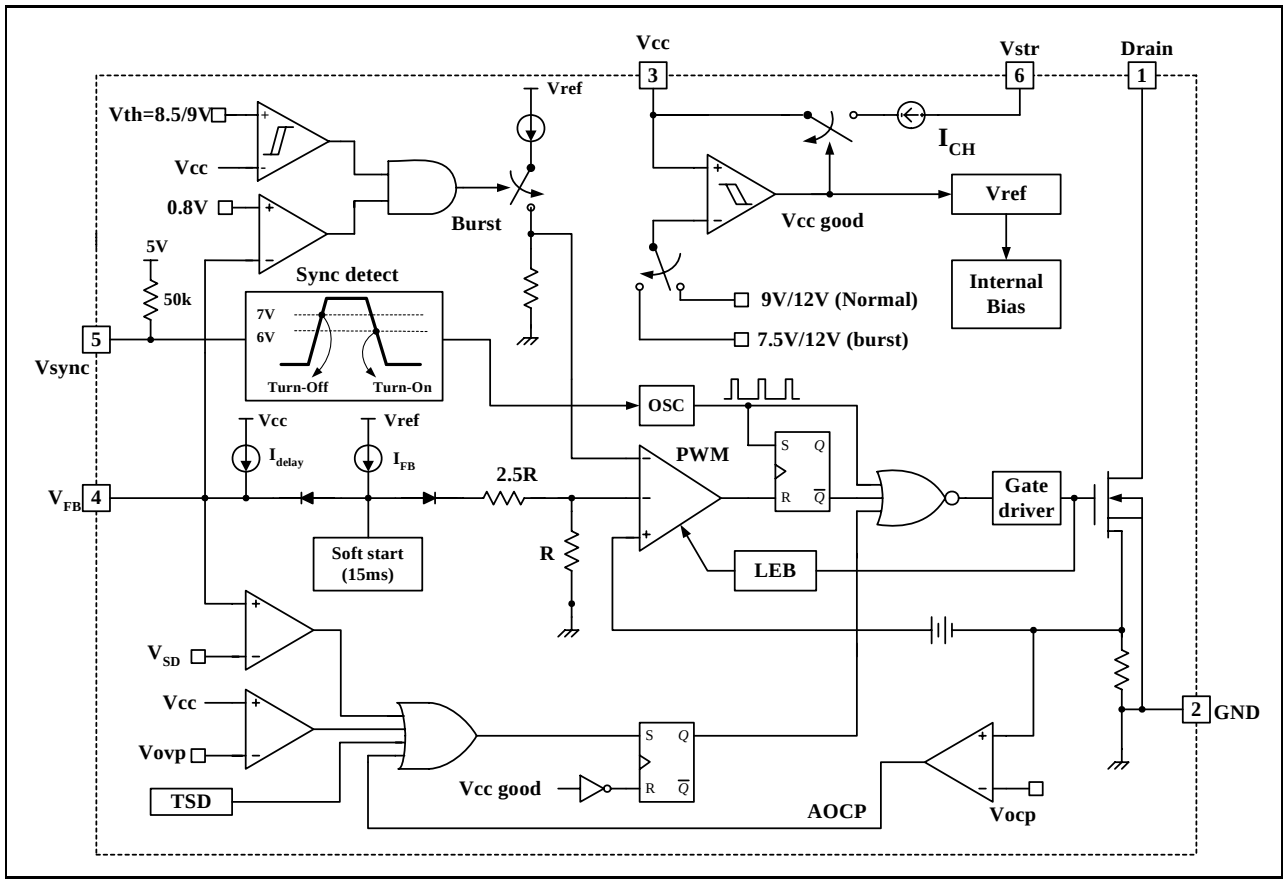


Figure 2. Functional Block Diagram of FSES0765RG

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	Drain	This pin is the high voltage power SenseFET drain connection.
2	GND	This pin is the control ground and the SenseFET source.
3	Vcc	This pin is the positive supply input. This pin provides the internal operating current for both start-up and steady-state operation.
4	Vfb	This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 7.5V, the over load protection triggers resulting in shutdown of the FPS.
5	Vsync	This pin is for synchronized switching. For proper synchronization, a pulse signal should be applied on this pin. The internal MOSFET is turned on being synchronized by the falling edge of this signal.
6	Vstr	This pin is connected directly to the high voltage DC link. At startup, the internal high voltage current source supplies the internal bias and charges the external capacitor that is connected to the Vcc pin. Once Vcc reaches 12V, the internal current source is disabled.

Pin Configuration

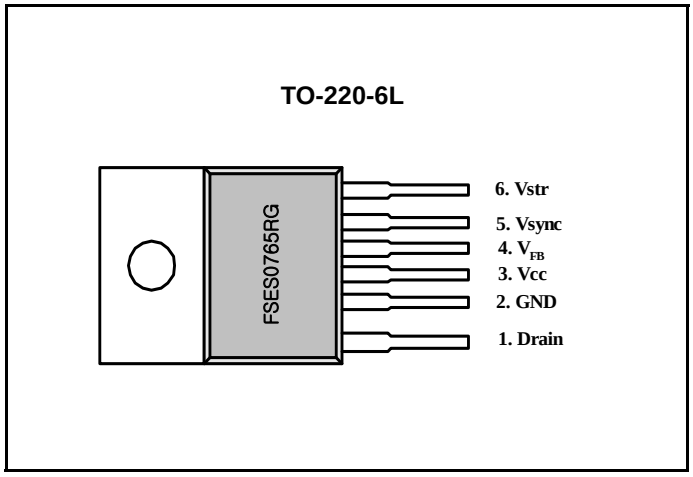


Figure 3. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain Voltage	V_{DS}	650	V
Vstr Voltage	Vstr	650	V
Drain Current Pulsed(1)	I_{DM}	15	A
Continuous Drain Current (Tc = 25°C, with infinite heat sink)	I_D	7	A
Continuous Drain Current (T_C=100°C, with infinite heat sink)	I_D	4.5	A
Single pulsed Avalanche Energy (2)	E_{AS}	570	mJ
Supply Voltage	V_{CC}	20	V
Analog Input Voltage Range	V_{sync}	-0.3 to 13	V
	V_{FB}	-0.3 to 10	V
Total Power Dissipation (Tc = 25°C , with infinite heat sink)	P_D	145	W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	-25 to +85	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C
Thermal Resistance	Rthjc	0.86	°C/W
Drain to PKG Breakdown Voltage (3)	BVpkg	3500	V
ESD Capability, HBM Model (All pins except Vstr and Vfb)	-	2.0	kV
ESD Capability, Machine Model (All pins except Vstr and Vfb)	-	300	V

Notes:

1. Repetitive rating: Pulse width limited by maximum junction temperature
2. Lm=21mH, Vdd=50V, Rg=25Ω, starting Tj=25°C
3. 60Hz AC

Electrical Characteristics (Continued)

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SENSEFET SECTION						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	650	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max, Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS}= 0.8*Max., Rating V_{GS} = 0V, T_C = 85°C	-	-	300	μA
Static Drain-source on Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 2.3A	-	1.4	1.6	Ω
Output Capacitance	Coss	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	-	100	130	pF
UVLO SECTION						
Vcc Start Threshold Voltage	V_{START}	V_{FB}=5V	11	12	13	V
Vcc Stop Threshold Voltage (Normal operation)	V_{STOP}	V_{FB}=5V	8.5	9	9.5	V
Vcc Stop Threshold Voltage (Burst operation)	V_{BSTOP}	V_{FB}=0V	7	7.5	8	V
OSCILLATOR SECTION						
Initial Frequency	F_{OSC}	V_{FB}=5	18	20	22	kHz
Voltage Stability	F_{STABLE}	11V ≤ Vcc ≤ 18V	0	1	3	%
Maximum Duty Cycle	D_{MAX}	V_{FB}=5	48	55	62	%
Minimum Duty Cycle	D_{MIN}	-	-	0	-	%
FEEDBACK SECTION						
Feedback Source Current (Normal operation)	I_{FB}	V_{FB} = 0V, Vcc=15V	0.7	0.9	1.1	mA
Feedback Source Current (Burst operation)	I_{BFB}	V_{FB} = 0V, Vcc=8.7V	70	100	130	uA
Feedback Voltage Threshold to Stop Switching	V_{OFF}	0V ≤ V_{FB} ≤ 0.4V	0.2	0.3	0.4	V
Shutdown Feedback Voltage	V_{SD}	V_{FB} ≥ 6.9V	7	7.5	8	V
Shutdown Delay Current	I_{DELAY}	V_{FB} = 4V	1.6	2	2.4	μA
PROTECTION SECTION						
Over Voltage Protection	V_{OVP}	Vcc ≥ 17V	18	19	20	V
Over Current Protection Threshold Voltage(1)	V_{AOCP}	-	0.9	1.0	1.1	V
Thermal Shutdown Temp(2)	T_{SD}	-	140	-	-	°C

Note:

1. These parameters, although guaranteed in design, are tested only in EDS (wafer test) process.
2. These parameters, although guaranteed in design, are not tested in mass production.

Electrical Characteristics (Continued)

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sync SECTION						
Low Sync Threshold Voltage	V_{SL}	Vcc=15V, V_{FB}=5V	5.6	6	6.4	V
High Sync Threshold Voltage	V_{SH}		6.5	7	7.5	V
Sync blanking time	T_{SYB}		3	5	7	us
BURST MODE SECTION						
Burst Mode Enable Feedback Voltage	V_{BFB}	Vcc=8.5V	0.7	0.8	0.9	V
Burst Mode Peak Current Limit (1)	I_{BPK}	Vcc=8.8V, V_{FB}=0V	0.45	0.6	0.75	A
Switching Frequency in Burst Mode	F_{SB}	Vcc=8.8V, V_{FB}=0V	40	50	60	kHz
Vcc High Threshold Voltage in Burst Mode	VccH		8.6	9	9.4	V
Vcc Low Threshold Voltage in Burst Mode	V_{ccL}		8.1	8.5	8.9	V
SOFTSTART SECTION						
Soft start Time (1)	T_{SS}	V_{FB}=4V	10	15	20	ms
CURRENT LIMIT(SELF-PROTECTION)SECTION						
Peak Current Limit (2)	I_{LIM}	Vcc=15V, V_{FB}=5V	3.52	4	4.48	A
TOTAL DEVICE SECTION						
Startup Charging Current	I_{CH}	V_{STR}=650V, Vcc=0V	1.2	1.5	1.8	mA
Operating Supply Current (3)						
- In normal operation	I_{OP}	Vcc=15V, V_{FB}=5V	-	3.5	6	mA
- In burst mode	I_{OB}	Vcc=8.7V, V_{FB}=0V	-	1.5	3	mA

Note:

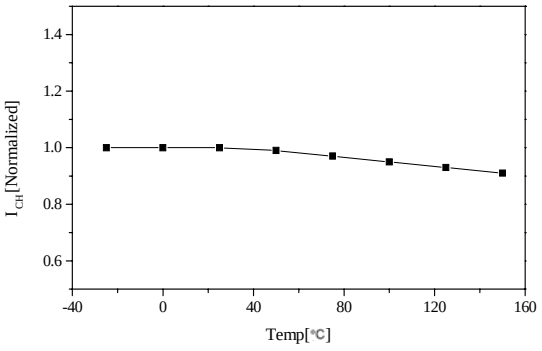
1. These parameters, although guaranteed in design, are tested only in EDS (wafer test) process.
2. These parameters indicate the Inductor current.
3. These parameters apply to the current flowing into the control IC.

Comparison of FS6S0765RC, FS8S0765RC and FSES0765RG

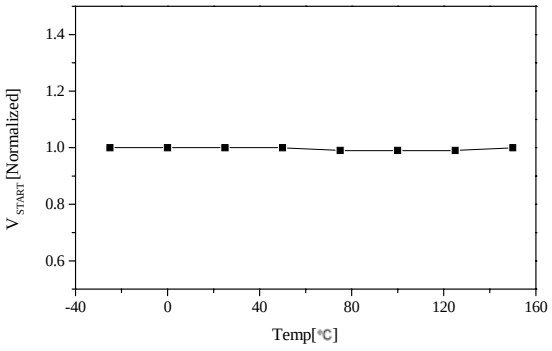
Function	FS6S0765RC	FS8S0765RC	FSES0765RG
Startup Resistor	Required Istart=170uA (max)	Required Istart=80uA (max)	Not Required (Internal startup circuit)
Operating Supply Current	15mA (max)	15mA (max)	6mA (max) : Normal mode 3mA (max) : Burst mode
Control Method	SSR	PSR	SSR
Vcc OVP Threshold	30V	37V	20V
Vcc Hysteresis Level in Burst Mode	11/12V	11/12V	8.5/9V
Soft Start	With external capacitor	With external capacitor	Internal soft-start (15ms)
Switching Frequency in Burst Mode	50kHz	40kHz	50kHz
Current Peak in Burst Mode	0.6A	0.6A	0.6A

Electrical Characteristics

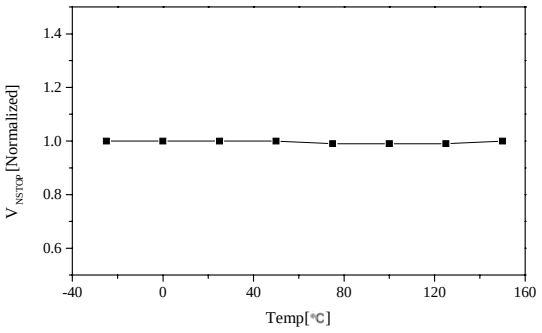
(These characteristic graphs are normalized at Ta= 25°C)



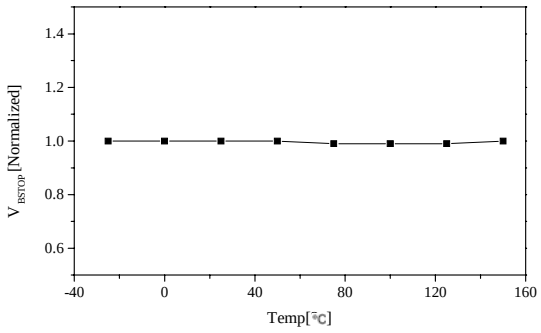
Start Up Charging Current vs. Temp.



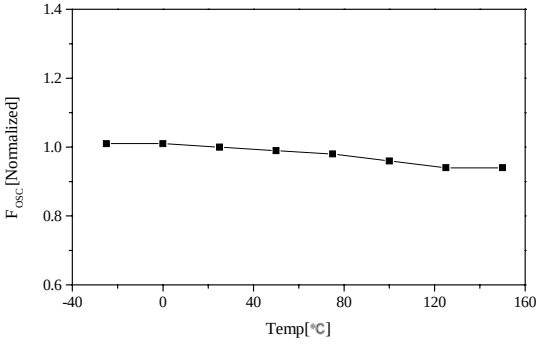
Vcc Start Voltage vs. Temp.



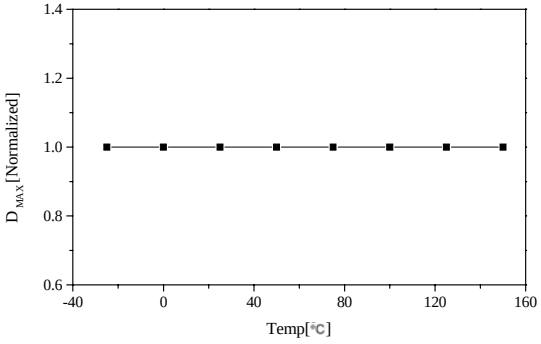
Normal Mode Vcc Stop Voltage vs. Temp.



Burst Mode Vcc Stop Voltage vs. Temp.



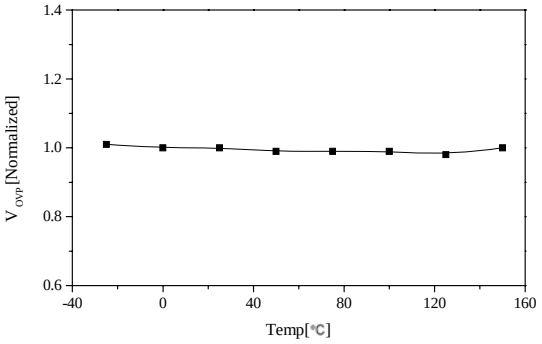
Initial Frequency vs. Temp.



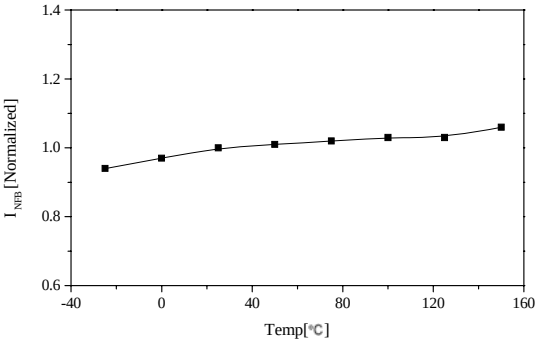
Maximum Duty Cycle vs. Temp.

Electrical Characteristics

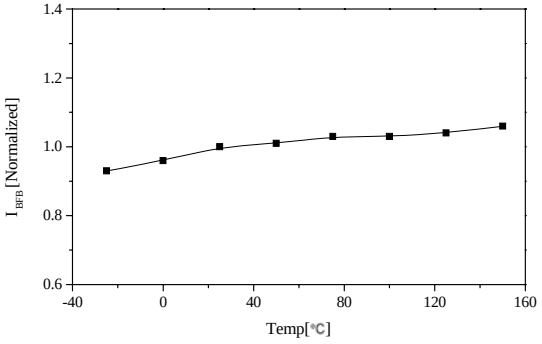
(These characteristic graphs are normalized at Ta= 25°C)



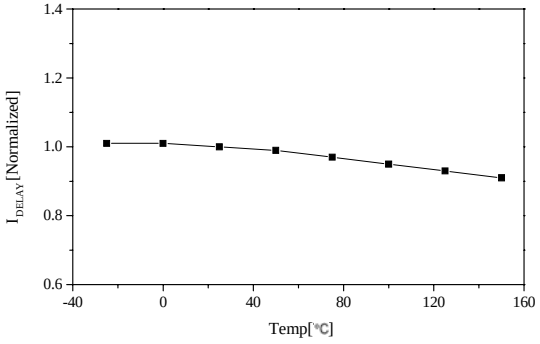
OVP Threshold Voltage vs. Temp.



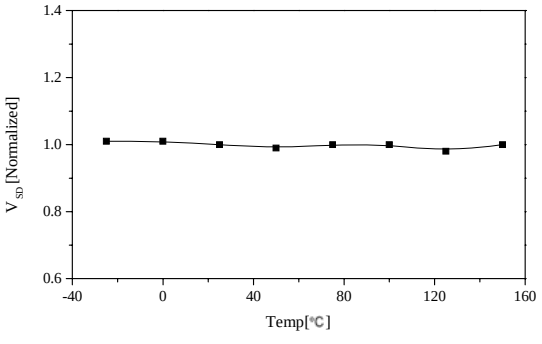
Normal Mode Feedback Current vs. Temp.



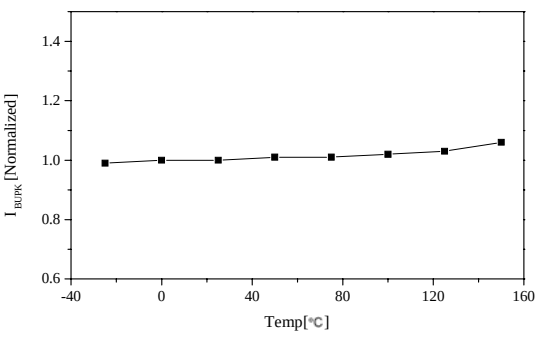
Burst Mode Feedback Current vs. Temp.



Feedback Delay Current vs. Temp.



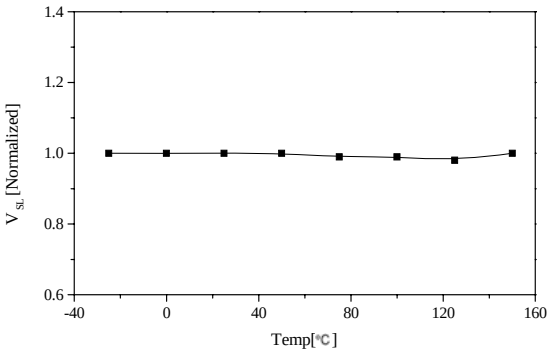
OLP Threshold Voltage vs. Temp.



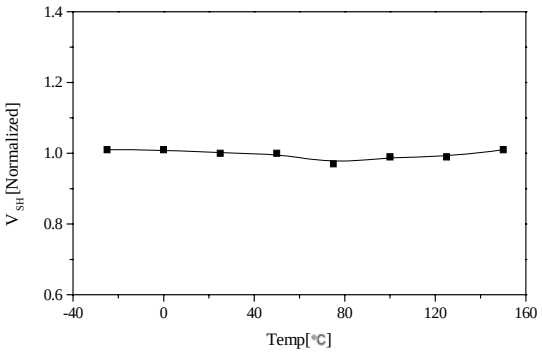
Burst Mode Peak Drain Current vs. Temp.

Electrical Characteristics

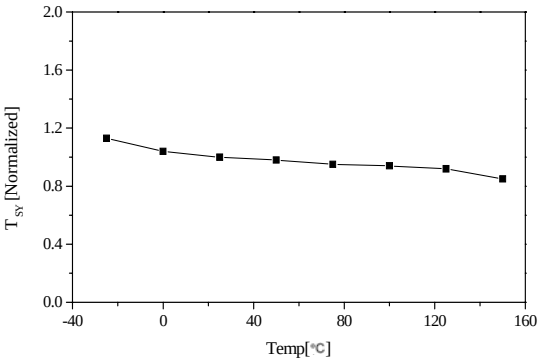
(These characteristic graphs are normalized at Ta= 25°C)



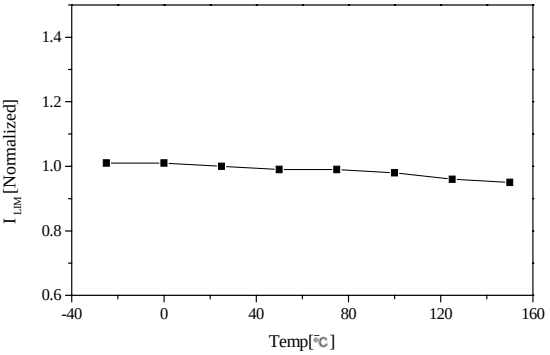
Low Sync Threshold Voltage vs. Temp.



High Sync Threshold Voltage vs. Temp.



Sync Blanking Time vs. Temp.



Pulse-by-Pulse Current Limit vs. Temp.

Functional Description

1. **Startup** : In previous generations of Fairchild Power Switches (FPS^{TM}) the Vcc pin had an external start-up resistor to the DC input voltage line. In this generation the startup resistor is replaced by an internal high voltage current source. At startup, an internal high voltage current source supplies the internal bias and charges the external capacitor (C_{Vcc}) that is connected to the Vcc pin as illustrated in figure 4. When Vcc reaches 12V, the FPS begins switching and the internal high voltage current source is disabled. Then, the FPS continues its normal switching operation and the power is supplied from the auxiliary transformer winding unless Vcc goes below the stop voltage of 9V.

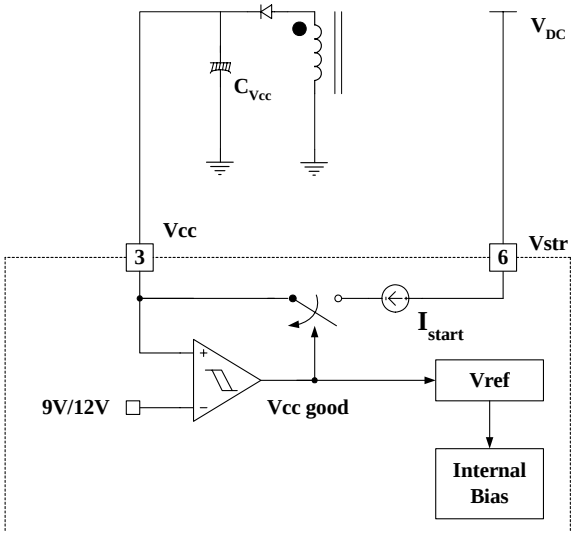


Figure 4. Internal Startup Circuit

2. Feedback Control : FSES0765RG employs current mode control, as shown in figure 5. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the Rsense resistor plus an offset voltage makes it possible to control the switching duty cycle. When the reference pin voltage of the KA431 exceeds the internal reference voltage of 2.5V, the H11A817A LED current increases, thus pulling down the feedback voltage and reducing the duty cycle. This event typically happens when the input voltage is increased or the output load is decreased.

2.1 Pulse-by-pulse Current Limit: Because current mode control is employed, the peak current through the Sense FET is limited by the inverting input of the PWM comparator (Vfb*) as shown in figure 5. Assuming that the 0.9mA current source flows only through the internal resistor (2.5R +R= 2.8 kΩ), the cathode voltage of diode D2 is about 2.5V. Since diode D1 is blocked when the feedback voltage (Vfb) exceeds 2.5V, the maximum voltage of the cathode of D2 is clamped at this voltage, thus clamping Vfb*. Therefore, the peak value of the SenseFET current is limited.

2.2 Leading Edge Blanking (LEB) : At the instant the internal Sense FET is turned on, there usually exists a high current spike through the Sense FET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the Rsense resistor would lead to incorrect feedback operation in the current mode PWM control. To counter this effect, the FPS employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (T_{LEB}) after the Sense FET is turned on.

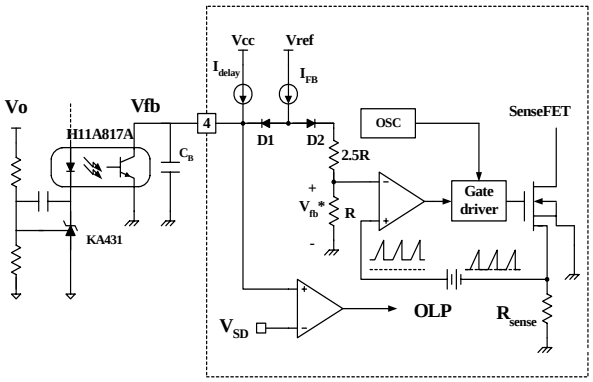


Figure 5. Pulse Width Modulation (PWM) Circuit

3. Protection Circuits : The FSES0765RG has several self protective functions such as over load protection (OLP), abnormal over current protection (AOCP), over voltage protection (OVP) and thermal shutdown (TSD). Because these protection circuits are fully integrated into the IC without requiring external components, the reliability can be improved without increasing cost. Once the fault condition occurs, switching is terminated and the Sense FET remains off. This causes Vcc to fall. When Vcc reaches the UVLO stop voltage, 9V, the protection is reset and the internal high voltage current source charges the Vcc capacitor via the Vstr pin. When Vcc reaches the UVLO start voltage,12V, the FPS resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated (see figure 6).

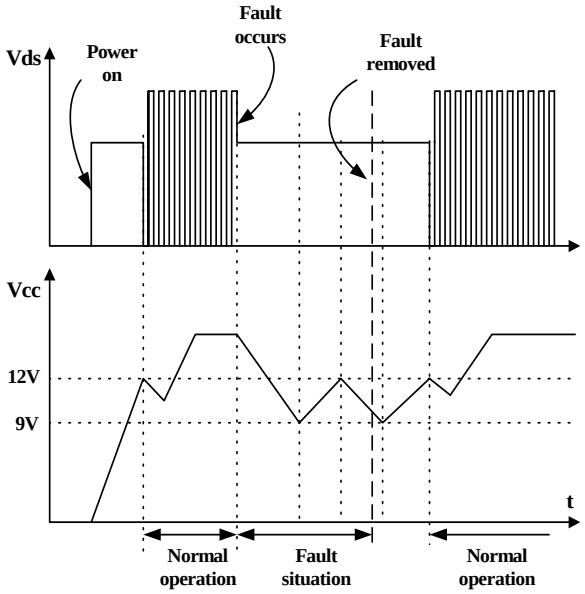


Figure 6. Auto restart operation

3.1 Over Load Protection (OLP) : Overload occurs when the load current exceeds a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated in order to protect the SMPS. However, even when the SMPS is in the normal operation, the over load protection circuit can be activated during the load transition. In order to avoid this undesired operation, the over load protection circuit is designed to be activated after a specified time to determine whether it is a transient or overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the Sense FET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes beyond this maximum power, the output voltage (Vo) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (Vfb). If Vfb exceeds 2.5V, D1 is blocked and the 2uA current source (I_{delay}) starts to charge C_B slowly up to Vcc. In this condition, Vfb continues increasing until it reaches 7.5V, then the switching operation is terminated as shown in figure 7. The delay time for shutdown is the time required to charge C_B from 2.5V to 7.5V with 2uA. In general, a 10 ~ 50 ms delay time is typical for most applications.

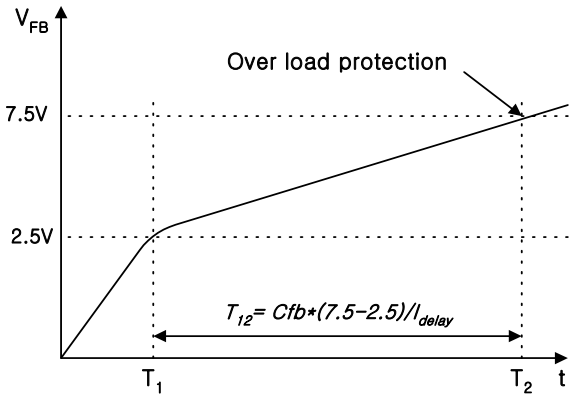


Figure 7. Over Load Protection

3.2 Abnormal Over Current Protection (AOCP) : Even though the FPS has OLP (Over Load Protection) and current mode PWM feedback, these protections are not enough to protect the FPS when a secondary side diode short or a transformer pin short occurs. The FPS has an internal AOCP (Abnormal Over Current Protection) circuit, as shown in figure 8. When the gate turn-on signal is applied to the power Sense FET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is then compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the reset signal is applied to the latch, resulting in the shutdown of SMPS.

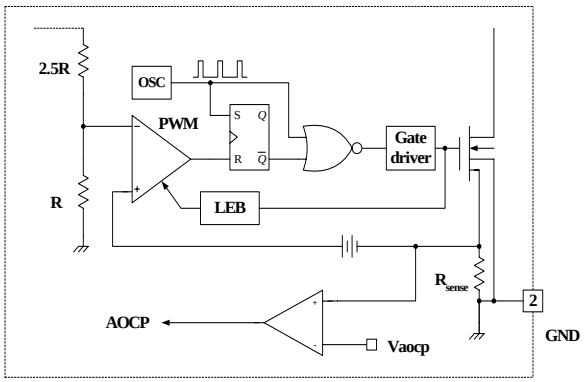


Figure 8. AOCP Block

3.3 Over Voltage Protection (OVP) : If the secondary side feedback circuit malfunctions or a solder defect causes an open in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then, Vfb climbs up in a manner similar to the over load situation, forcing the preset maximum current to be supplied to the SMPS until the over load protection is activated. Because more energy than required is provided to the output, the output voltage may

exceed the rated voltage before the over load protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. In general, Vcc is proportional to the output voltage and the FPS uses Vcc instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, an OVP circuit is activated resulting in the termination of the switching operation. In order to avoid undesired activation of OVP during normal operation, Vcc should be designed to be below 19V.

3.4 Thermal Shutdown (TSD) : The Sense FET and the control IC are built in one package. This makes it easy for the control IC to detect the heat generation from the Sense FET. When the temperature exceeds approximately 150°C, the thermal shutdown is activated.

4. Synchronization : Since the FSES0765RG is designed for CRT Monitor applications, this device has a synchronization function to minimize the screen noise. The MOSFET is turned on being synchronized to the external synchronization signal as shown in figure 9. In order to reduce voltage stress on the secondary side rectifier, a double pulse prevention function is included as well. The MOSFET's turn-on is inhibited for 5us after the MOSFET is turned off in order to eliminate a double pulse situation.

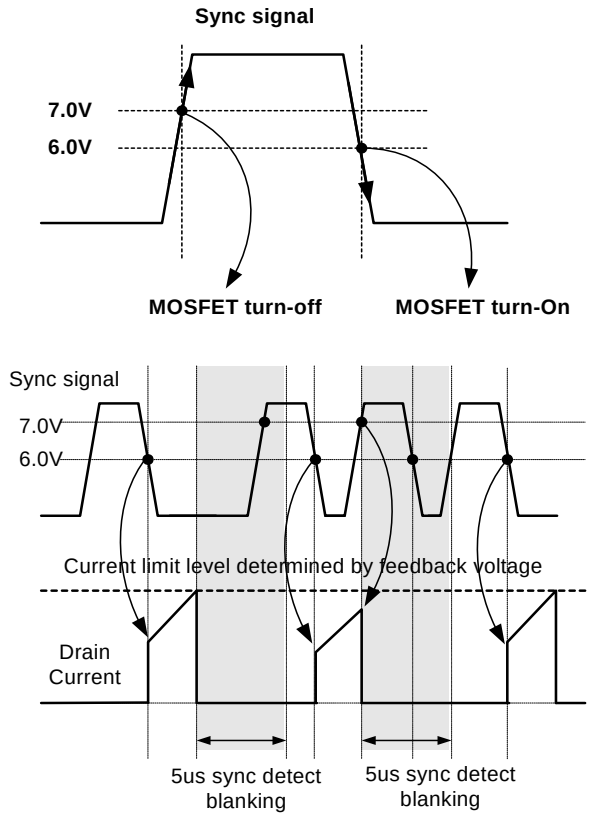


Figure 9. Synchronization Operation

5. Soft Start : The FPS has an internal soft start circuit that slowly increases the PWM comparator's inverting input voltage together with the Sense FET current during startup. The typical soft start time is 15ms. The pulse width to the power switching device progressively increases to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors also progressively increases with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode during startup.

6. Burst operation : In order to minimize the power consumption in the standby mode, the FSES0765RG employs burst operation. Once FSES0765RG enters into burst mode, effective switching frequency and all output voltages are reduced. Figure 10 shows the typical feedback circuit to force the FSES0765RG to enter burst operation. In normal operation, the picture on signal is applied and the transistor Q_1 is turned on, which de-couples R_3 and D1 from the feedback network. Therefore, only V_{o1} is regulated by the feedback circuit in normal operation and determined by R_1 and R_2 as

$$V_{o1}^{norm} = 2.5 \cdot \left(\frac{R_1 + R_2}{R_2}\right)$$

In standby mode, the picture on signal is disabled and the transistor Q_1 is turned off, which couples R_3 and D_1 to the reference pin of KA431. Then, the voltage on the reference pin of KA431 is higher than 2.5V and the current through the opto coupler increases, which increases the current through the opto LED. This pulls down the feedback voltage (V_{FB}) of FPS and forces FPS to stop switching until Vcc drops to 8.5V. When Vcc reaches 8.5V, the FPS starts switching with a switching frequency of 50kHz and a peak drain current of 0.6A until Vcc reaches 9V. When Vcc reaches 9V, the switching operation is terminated again until Vcc reduces to 8.5V.

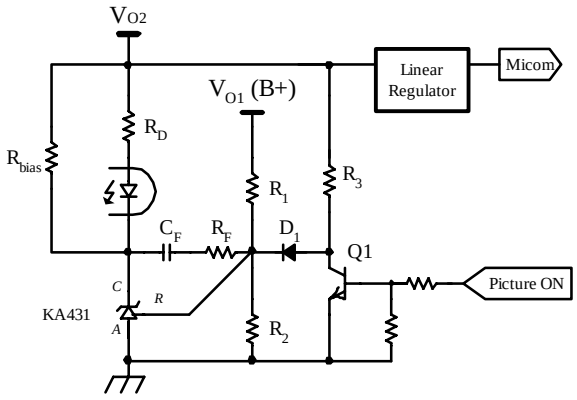


Figure 10. Typical feedback Circuit for FPS Burst Operation

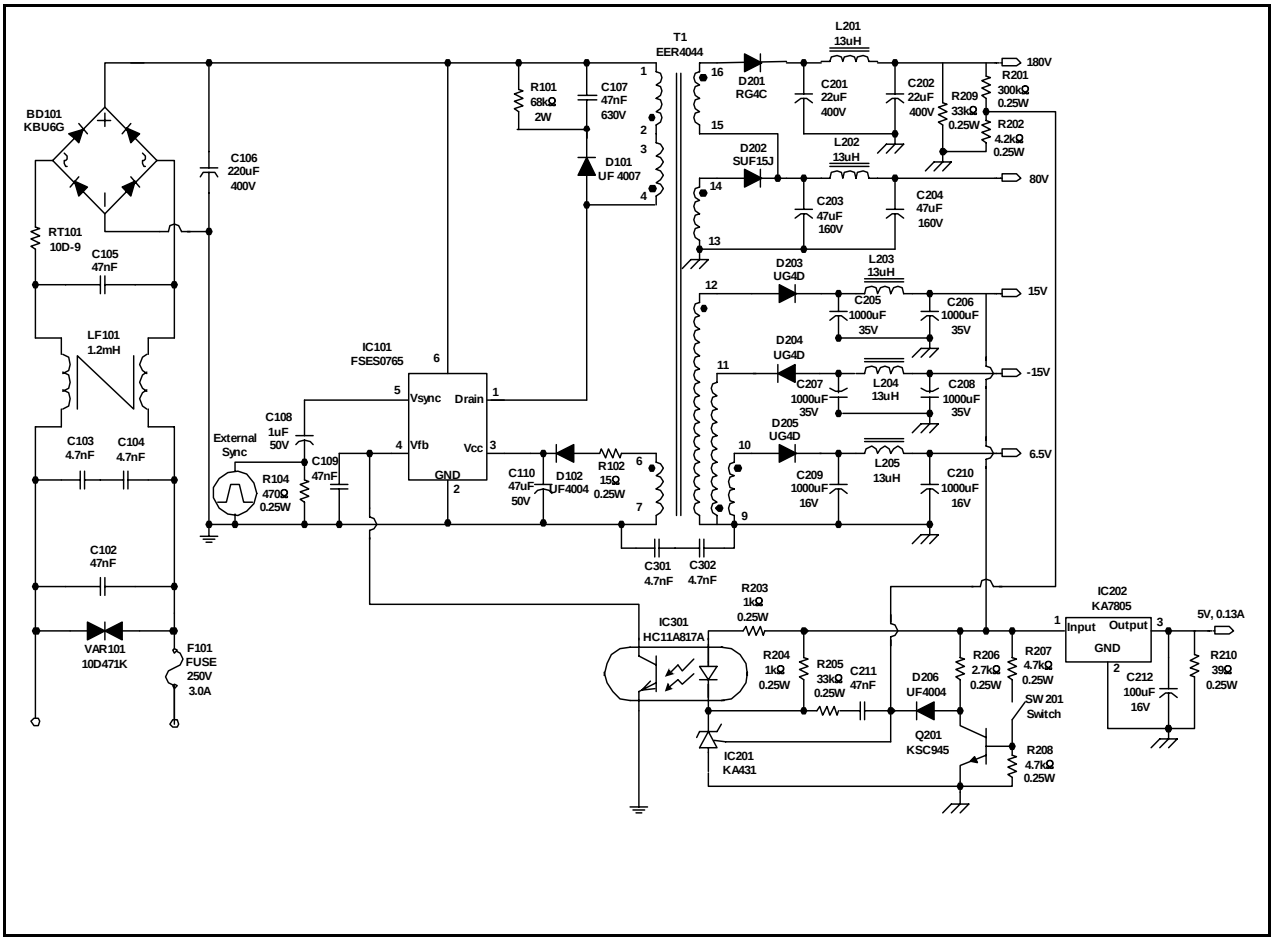
Typical application Circuit

Application	Output power	Input voltage	Output voltage (Max current)
CRT-Monitor	64W	Universal input (85-265Vac)	80V (0.15A) 50V (0.70A) 14V (0.8A) -14V (0.3A) 6.5V (0.3A)

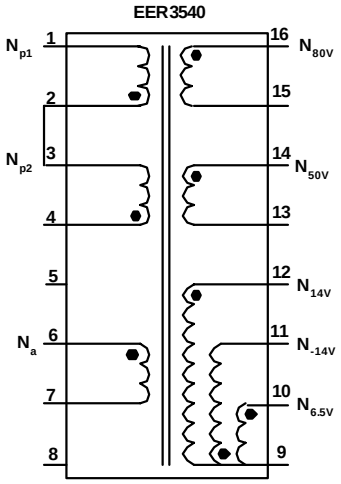
Features

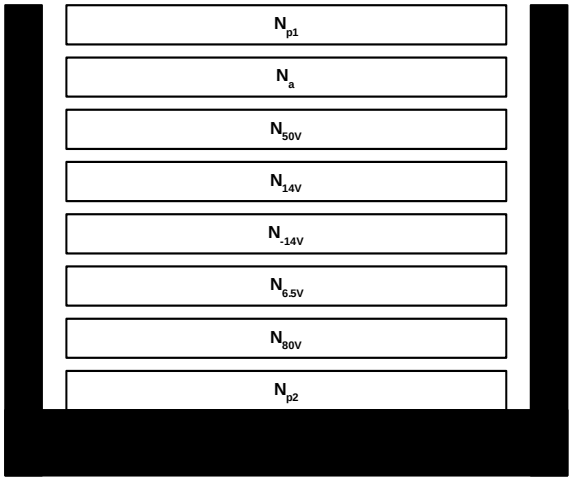
- High efficiency (>80% at 85Vac input)
- Synchronized switching
- Low standby mode power consumption (<1W)
- Low component count
- Enhanced system reliability through various protection functions
- Internal soft-start (15ms)

1. Schematic



2. Transformer Schematic Diagram





3.Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
N_{p2}	2 - 1	$0.3^{\phi} \times 2$	20	Center Winding
N_{80V}	16 - 15	$0.3^{\phi} \times 1$	10	Center Winding
$N_{6.5V}$	10 - 9	$0.3^{\phi} \times 2$	3	Center Winding
N_{-14V}	9 - 11	$0.3^{\phi} \times 1$	5	Center Winding
N_{14V}	12 - 9	$0.3^{\phi} \times 2$	6	Center Winding
N_{50V}	14 - 13	$0.3^{\phi} \times 3$	22	Center Winding
N_{a}	6 - 8	$0.2^{\phi} \times 1$	8	Center Winding
N_{p1}	4 - 3	$0.3^{\phi} \times 2$	20	Center Winding

4.Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 4	420uH ± 5%	1kHz, 1V
Leakage Inductance	1 - 4	5uH Max	2^{nd} all short

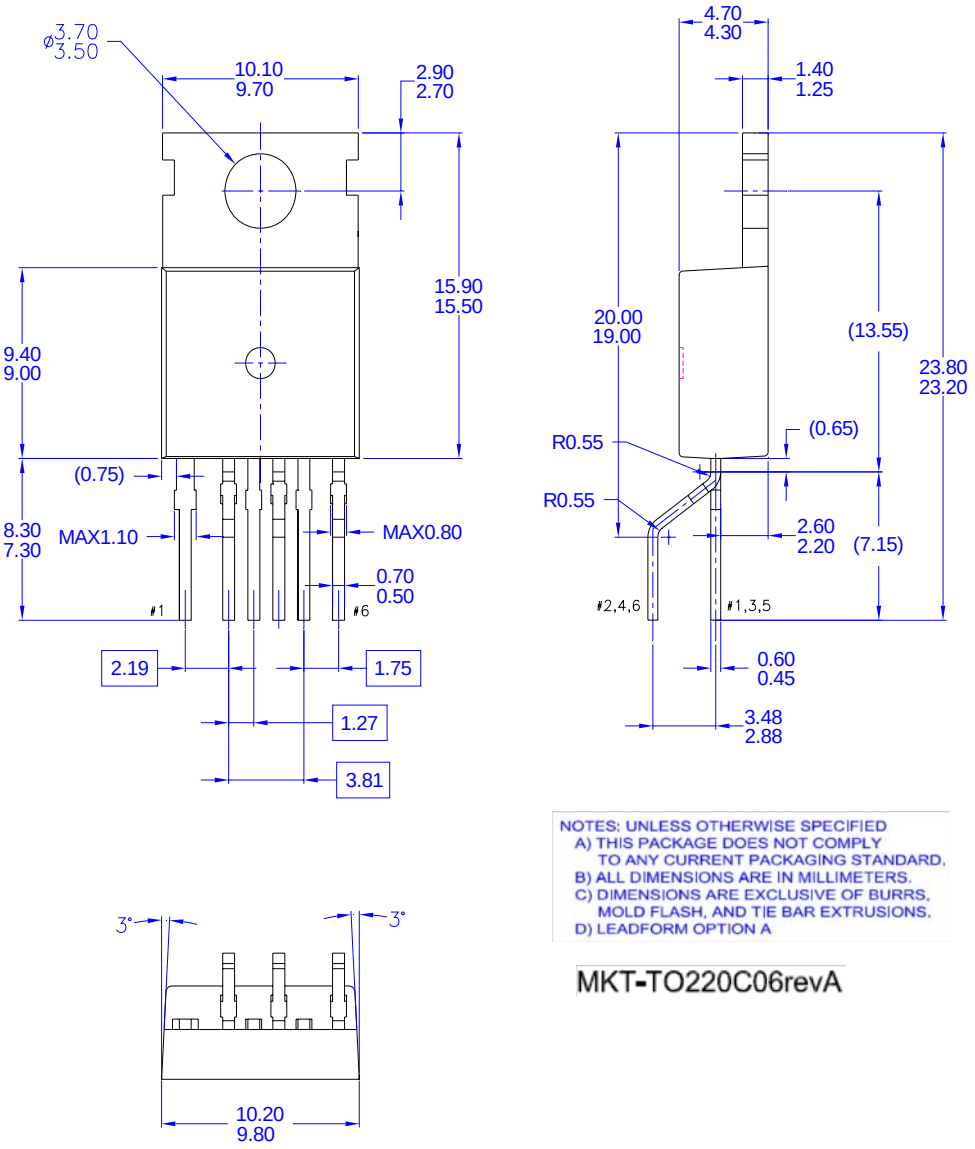
5. Core & Bobbin

Core : EER 3540
Bobbin : EER3540
Ae : 107 mm^2

Package Dimensions

Dimensions in Millimeters

TO-220-6L(Forming)



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D) LEADFORM OPTION A

MKT-TO220C06revA

Ordering Information

Product Number	Package	Marking Code	BVdss	$R_{ds(ON)}$ Max.
FSES0765RGWDTU	TO-220-6L(Forming)	ES0765R	650V	1.6 Ω

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