FSDL0365RN, FSDM0365RN

Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged Sense FET
- Consumes only 0.65W at 240VAC & 0.3W load with Advanced Burst-Mode Operation
- Frequency Modulation for low EMI
- Precision Fixed Operating Frequency
- Internal Start-up Circuit
- Pulse by Pulse Current Limiting
- Abnormal Over Current Protection
- Over Voltage Protection
- Over Load Protection
- Internal Thermal Shutdown Function
- Auto-Restart Mode
- Under Voltage Lockout
- Low Operating Current (3mA)
- Adjustable Peak Current Limit
- Built-in Soft Start

Applications

- SMPS for VCR, SVR, STB, DVD & DVCD
- SMPS for Printer, Facsimile & Scanner
- Adaptor for Camcorder

Description

The FSDx0365RN(x stands for L, M) are integrated Pulse Width Modulators (PWM) and Sense FETs specifically designed for high performance offline Switch Mode Power Supplies (SMPS) with minimal external components. Both devices are integrated high voltage power switching regulators which combine an avalanche rugged Sense FET with a current mode PWM control block. The integrated PWM controller features include: a fixed oscillator with frequency modulation for reduced EMI, Under Voltage Lock Out (UVLO) protection, Leading Edge Blanking (LEB), optimized gate turn-on/turn-off driver, Thermal Shut Down (TSD) protection, Abnormal Over Current Protection (AOCP) and temperature compensated precision current sources for loop compensation and fault protection circuitry. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSDx0365RN reduce total component count, design size, weight and at the same time increase efficiency, productivity, and system reliability. Both devices are a basic platform well suited for cost effective designs of flyback converters.

OUTPUT POWER TABLE				
PRODUCT	230VAC ±15%(3)		85-265VAC	
	Adapter(1)	Open Frame(2)	Adapter(1)	Open Frame(2)
FSDL321	11W	17W	8W	12W
FSDH321	11W	17W	8W	12W
FSDL0165RN	13W	23W	11W	17W
FSDM0265RN	16W	27W	13W	20W
FSDH0265RN	16W	27W	13W	20W
FSDL0365RN	19W	30W	16W	24W
FSDM0365RN	19W	30W	16W	24W
FSDL0165RL	13W	23W	11W	17W
FSDM0265RL	16W	27W	13W	20W
FSDH0265RL	16W	27W	13W	20W
FSDL0365RL	19W	30W	16W	24W
FSDM0365RL	19W	30W	16W	24W

Table 1. Notes: 1. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient. 2. Maximum practical continuous power in an open frame design at 50°C ambient. 3. 230 VAC or 100/115 VAC with doubler.

Typical Circuit

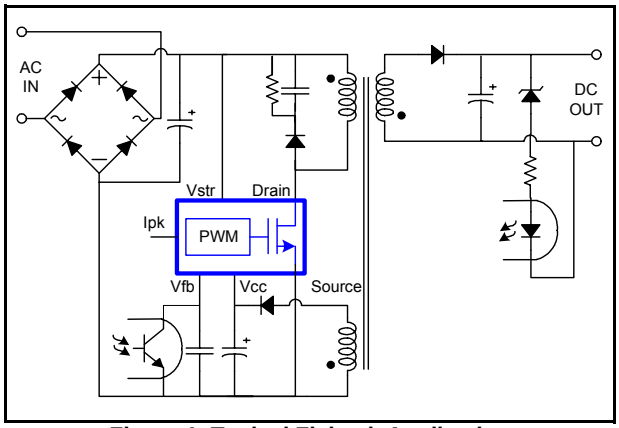


Figure 1. Typical Flyback Application

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Internal Block Diagram

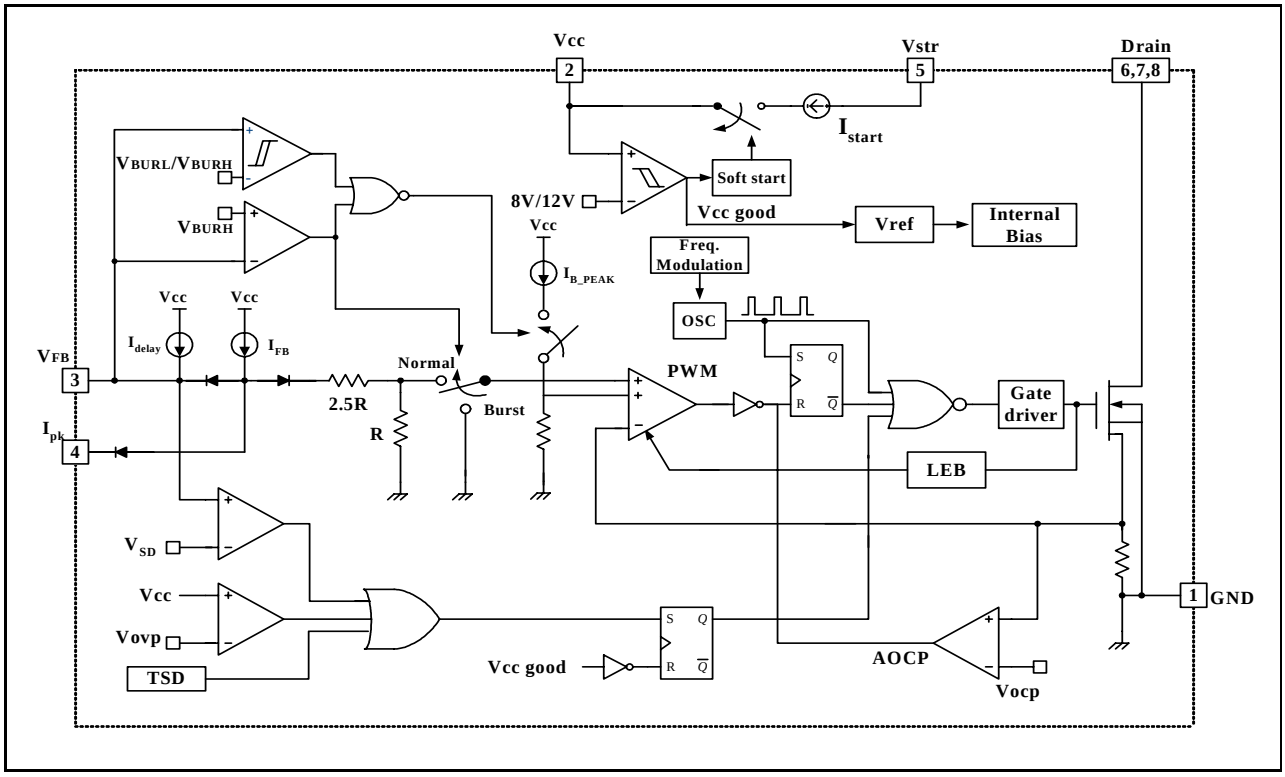


Figure 2. Functional Block Diagram of FSDx0365RN

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	GND	Sense FET source terminal on primary side and internal control ground.
2	Vcc	Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during startup (see Internal Block Diagram section). It is not until Vcc reaches the UVLO upper threshold (12V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	Vfb	The feedback voltage pin is the non-inverting input to the PWM comparator. It has a 0.9mA current source connected internally while a capacitor and optocoupler are typically connected externally. A feedback voltage of 6V triggers over load protection (OLP). There is a time delay while charging between 3V and 6V using an internal 5uA current source, which prevents false triggering under transient conditions but still allows the protection mechanism to operate under true overload conditions.
4	Ipk	Pin to adjust the current limit of the Sense FET. The feedback 0.9mA current source is diverted to the parallel combination of an internal 2.8kΩ resistor and any external resistor to GND on this pin to determine the current limit. If this pin is tied to Vcc or left floating, the typical current limit will be 2.15A.
5	Vstr	This pin connects directly to the rectified AC line voltage source. At start up the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the Vcc reaches 12V, the internal switch is disabled.
6, 7, 8	Drain	The Drain pin is designed to connect directly to the primary lead of the transformer and is capable of switching a maximum of 650V. Minimizing the length of the trace connecting this pin to the transformer will decrease leakage inductance.

Pin Configuration

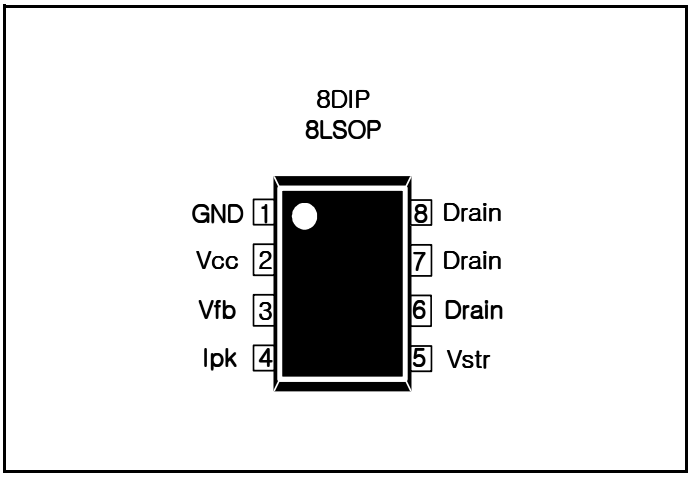


Figure 3. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Drain Current Pulsed(1)	I_{DM}	12.0	A_{DC}
Single Pulsed Avalanche Energy(2)	E_{AS}	127	mJ
Maximum Supply Voltage	$V_{CC,MAX}$	20	V
Analog Input Voltage Range	V_{FB}	-0.3 to V_{SD}	V
Total Power Dissipation	P_D	1.56	W
Operating Junction Temperature.	T_J	+150	°C
Operating Ambient Temperature.	T_A	-25 to +85	°C
Storage Temperature Range.	T_{STG}	-55 to +150	°C

Note:

1. Repetitive rating: Pulse width limited by maximum junction temperature
2. L = 51mH, starting Tj = 25°C
3. L = 13μH, starting Tj = 25°C
4. Vsd is shutdown feedback voltage (see Protection Section in Electrical Characteristics)

Thermal Impedance

Parameter	Symbol	Value	Unit
8DIP			
Junction-to-Ambient Thermal	θ_{JA}(1)	85.74	°C/W(3)
Junction-to-Case Thermal	θ_{JC}(2)	30.38	°C/W

Note:

1. Free standing with no heatsink.
2. Measured on the GND pin close to plastic interface.
3. Soldered to 0.36 sq. inch(232mm2), 2 oz.(610g/m2) copper clad.

Electrical Characteristics

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sense FET SECTION						
Startup Voltage (Vstr) Breakdown	BV_{STR}	V_{CC}=0V, I_D=1mA	650	-	-	V
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=50μA	650	-	-	V
Off-State Current (Max.Rating =660V)	I_{DSS}	V_{DS}=660V, V_{GS}=0V	-	-	50	μA
		V_{DS}=0.8Max.Rating, V_{GS}=0V, T_C=125°C	-	-	200	μA
On-State Resistance(1)	$R_{DS(ON)}$	V_{GS}=10V, I_D=0.5A	-	3.6	4.5	Ω
Input Capacitance	C_{ISS}	V_{GS}=0V, V_{DS}=25V, F=1MHz	-	315	-	pF
Output Capacitance	C_{OSS}		-	47	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	9	-	pF
Turn On Delay Time	$T_{D(ON)}$	V_{DS}=325V, I_D=1.0A (Sense FET switching time is essentially independent of operating temperature)	-	11.2	-	ns
Rise Time	T_R		-	34	-	ns
Turn Off Delay Time	$T_{D(OFF)}$		-	28.2	-	ns
Fall Time	T_F		-	32	-	ns
CONTROL SECTION						
Output Frequency	F_{OSC}	**FSDM0365R**	61	67	73	KHz
Output Frequency Modulation	F_{MOD}		±1.5	±2.0	±2.5	KHz
Output Frequency	F_{OSC}	**FSDL0365R**	45	50	55	KHz
Output Frequency Modulation	F_{MOD}		±1.0	±1.5	±2.0	KHz
Frequency Change With Temperature(2)	-	-25°C ≤ Ta ≤ 85°C	-	±5	±10	%
Maximum Duty Cycle	D_{MAX}		71	77	83	%
Minimum Duty Cycle	D_{MIN}		0	0	0	%
Start threshold voltage	V_{START}	V_{FB}=GND	11	12	13	V
Stop threshold voltage	V_{STOP}	V_{FB}=GND	7	8	9	V
Feedback Source Current	I_{FB}	V_{FB}=GND	0.7	0.9	1.1	mA
Internal Soft Start Time	$T_{S/S}$	V_{FB}=4V	10	15	20	ms
BURST MODE SECTION						
Burst Mode Voltages	V_{BURH}	-	0.4	0.5	0.6	V
	V_{BURL}	-	0.25	0.35	0.45	V
PROTECTION SECTION						
Drain to Source Peak Current Limit	I_{OVER}	Max. inductor current	1.89	2.15	2.41	A

Current Limit Delay(3)	T_{CLD}		-	500	-	ns
Thermal Shutdown	T_{SD}	-	125	140	-	°C
Shutdown Feedback Voltage	V_{SD}		5.5	6.0	6.5	V
Over Voltage Protection	V_{OVP}		18	19	-	V
Shutdown Feedback Delay Current	I_{DELAY}	V_{FB}=4V	3.5	5.0	6.5	μA
Leading Edge Blanking Time	T_{LEB}		200	-	-	ns
TOTAL DEVICE SECTION						
Operating Current	I_{OP}	V_{CC}=14V	1	3	5	mA
Start Up Current	I_{START}	V_{CC}=0V	0.7	0.85	1.0	mA
Vstr Supply Voltage	V_{STR}	V_{CC}=0V	35	-	-	V

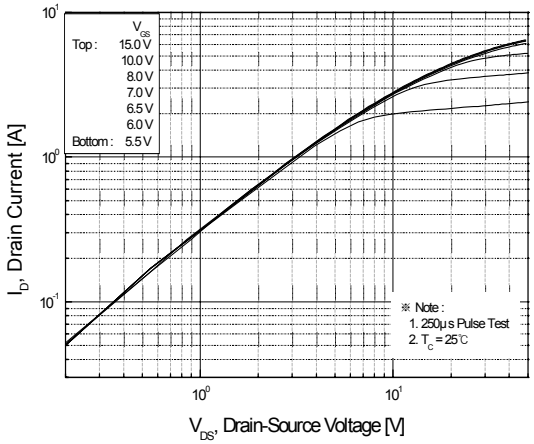
Note:

1. Pulse test: Pulse width ≤ 300uS, duty ≤ 2%
2. These parameters, although guaranteed, are tested in EDS (wafer test) process
3. These parameters, although guaranteed, are not 100% tested in production

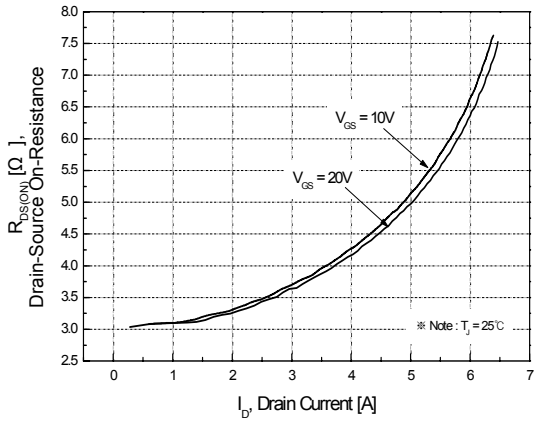
Comparison Between KA5x0365RN and FSDx0365RN

Function	KA5x0365RN	FSDx0365RN	FSDx0365RN Advantages
Soft-Start	not applicable	15mS	• Gradually increasing current limit during soft-start further reduces peak current and voltage component stresses • Eliminates external components used for soft-start in most applications • Reduces or eliminates output overshoot
External Current Limit	not applicable	Programmable of default current limit	• Smaller transformer • Allows power limiting (constant over-load power) • Allows use of larger device for lower losses and higher efficiency.
Frequency Modulation	not applicable	±2.0KHz @67KHz ±1.5KHz @50KHz	• Reduced conducted EMI
Burst Mode Operation	not applicable	Yes-built into controller	• Improve light load efficiency • Reduces no-load consumption • Transformer audible noise reduction
Drain Creepage at Package	1,02mm	7.62mm	• Greater immunity to arcing as a result of build-up of dust, debris and other contaminants

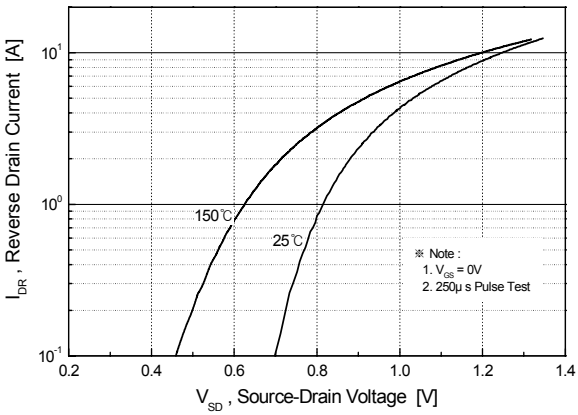
Typical Performance Characteristics (Sense FET part)



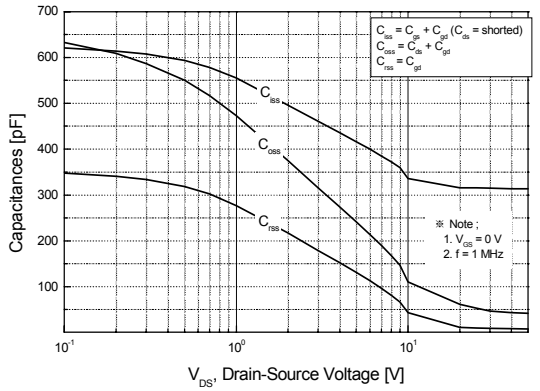
Output Characteristics



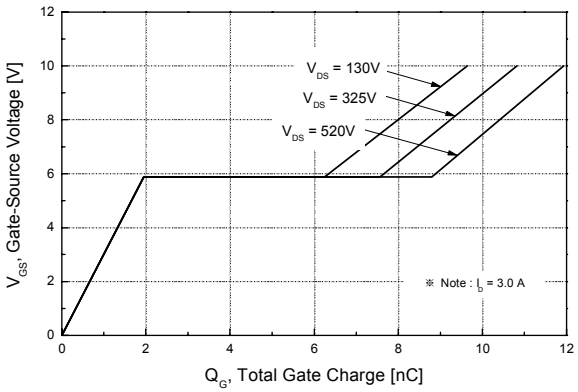
On-Resistance vs. Drain Current



Source-Drain Diode Forward Voltage

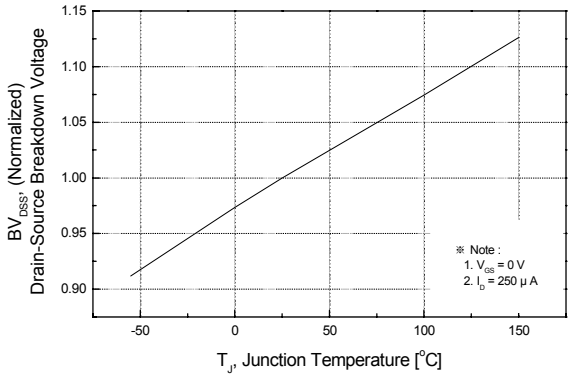


Capacitance vs. Drain-Source Voltage

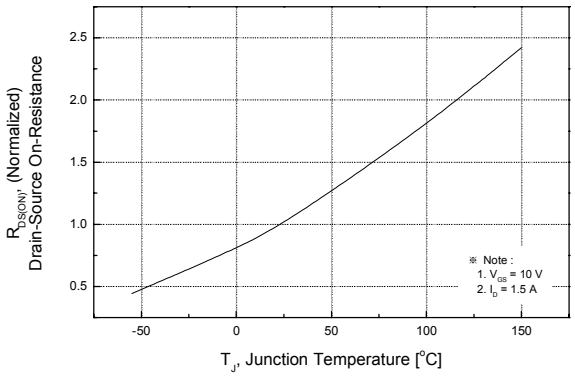


Gate Charge vs. Gate-Source Voltage

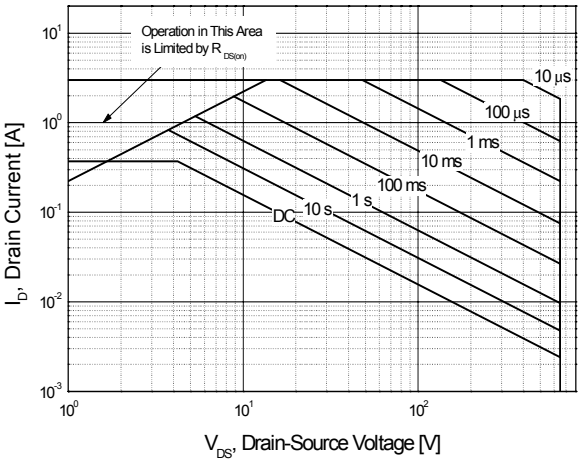
Typical Performance Characteristics (Continued)



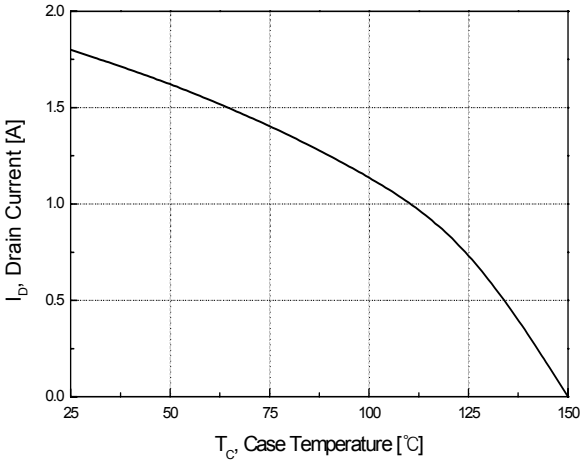
Breakdown Voltage vs. Temperature



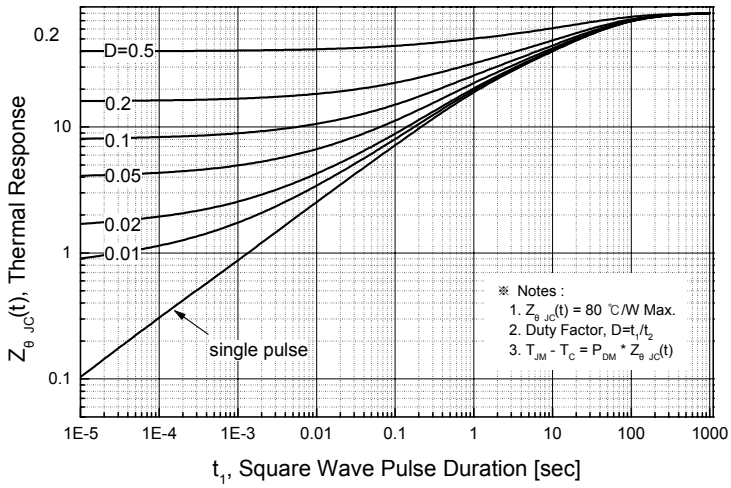
On-Resistance vs. Temperature



Max. Safe Operating Area



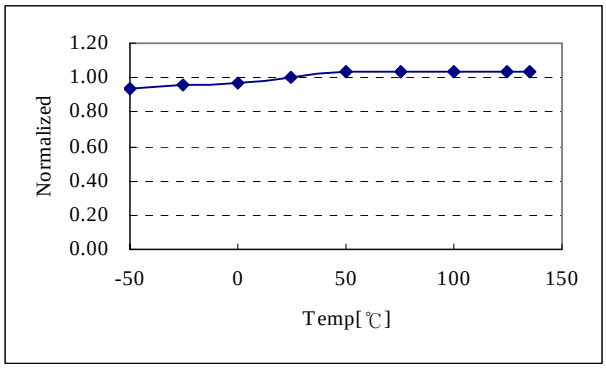
Max. Drain Current vs. Case Temperature



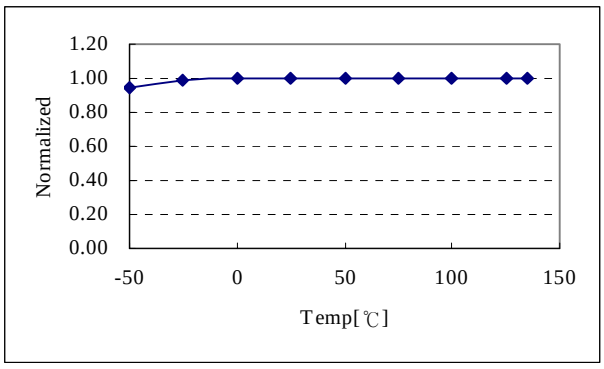
Thermal Response

Typical Performance Characteristics (Control Part)

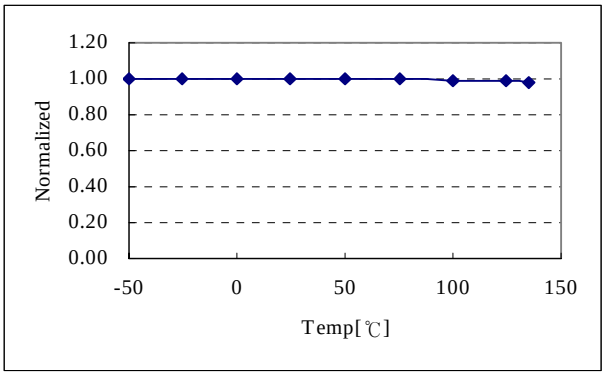
(These characteristic graphs are normalized at Ta = 25°C)



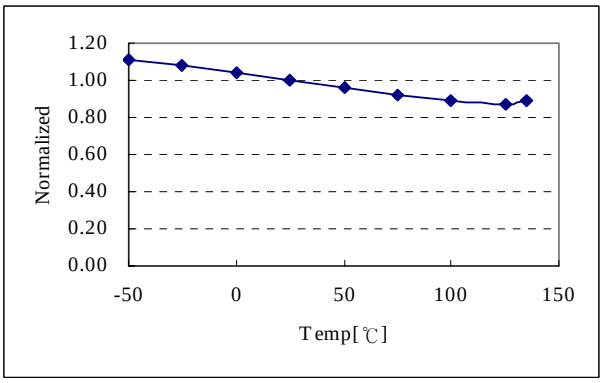
Operating Frequency (Fosc)



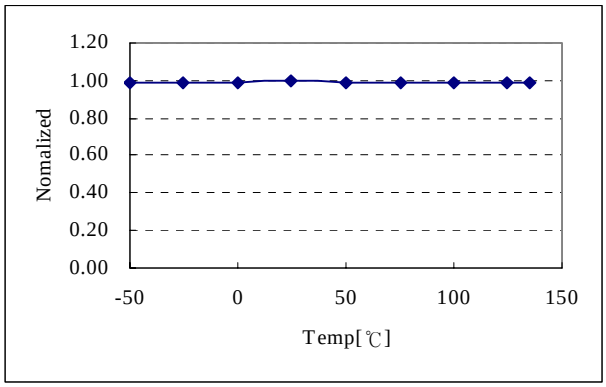
Frequency Modulation (FMOD)



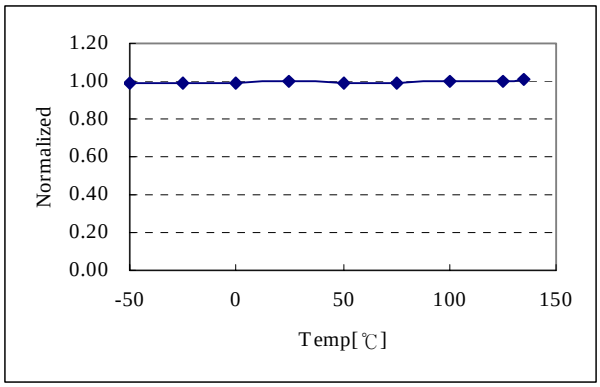
Maximum duty cycle (Dmax)



Operating supply current (Iop)

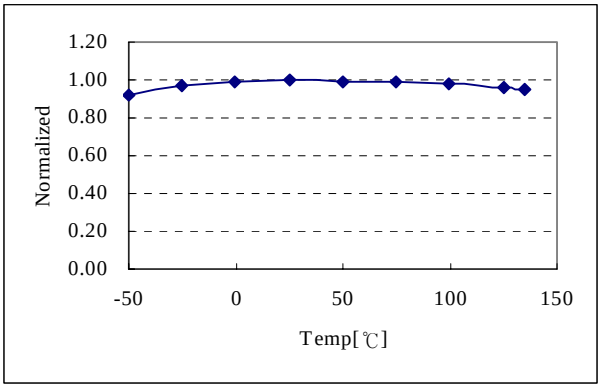


Start Threshold Voltage (Vstart)

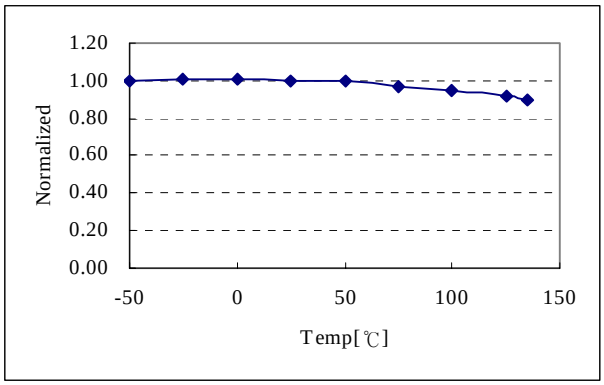


Stop Threshold Voltage (Vstop)

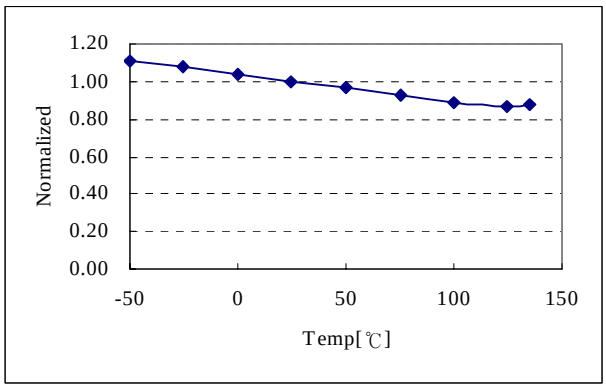
Typical Performance Characteristics (Continued)



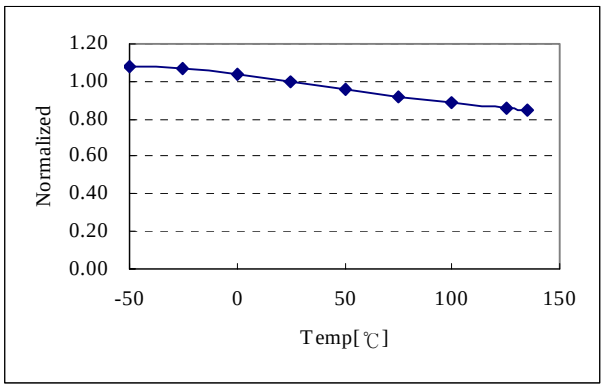
Feedback Source Current (Ifb)



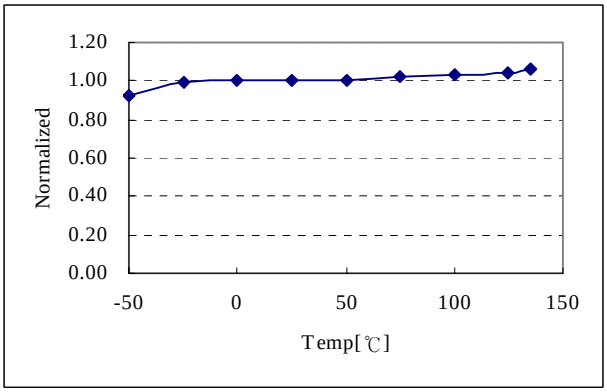
Peak current limit (Iover)



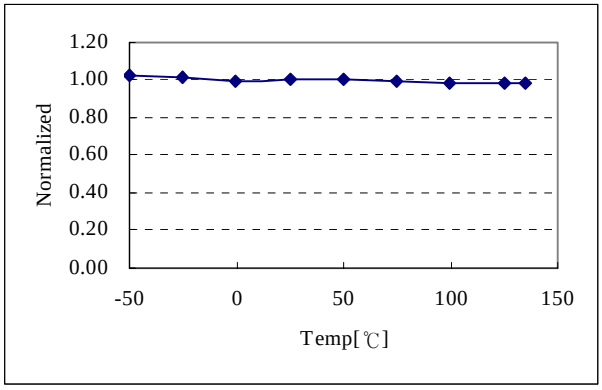
Start up Current (Istart)



J-FET Start up current (Istr)



Burst peak current (Iburst)



Over Voltage Protection (Vovp)

Functional Description

1. Startup : In previous generations of Fairchild Power Switches (FPS) the Vstr pin had an external resistor to the DC input voltage line. In this generation the startup resistor is replaced by an internal high voltage current source and a switch that shuts off when 15mS goes by after the supply voltage, Vcc, gets above 12V. The source turns back on if Vcc drops below 8V.

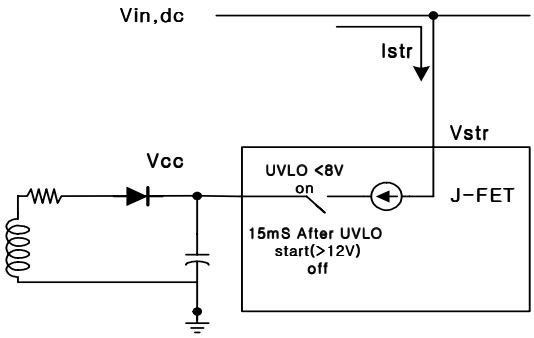


Figure 4. High voltage current source

2. Feedback Control : The FSDx0365RN employs current mode control, shown in figure 5. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the Rsense resistor plus an offset voltage makes it possible to control the switching duty cycle. When the reference pin voltage of the KA431 exceeds the internal reference voltage of 2.5V, the H11A817A LED current increases, thus pulling down the feedback voltage and reducing the duty cycle. This event typically happens when the input voltage is increased or the output load is decreased.

3. Leading edge blanking (LEB) : At the instant the internal Sense FET is turned on, there usually exists a high current spike through the Sense FET, caused by the primary side capacitance and secondary side rectifier diode reverse recovery. Excessive voltage across the Rsense resistor would lead to incorrect feedback operation in the current mode PWM control. To counter this effect, the FPS employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (T_{LEB}) after the Sense FET is turned on.

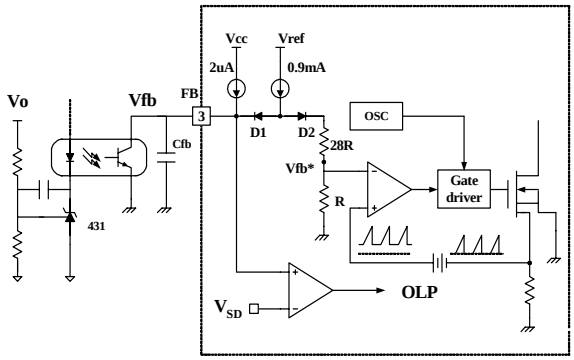
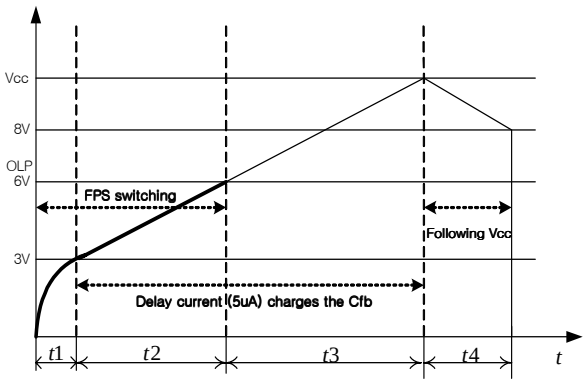


Figure 5. Pulse width modulation (PWM) circuit

4. Protection Circuit : The FPS has several protective functions such as over load protection (OLP), over voltage protection (OVP), abnormal over current protection (AOCP), under voltage lock out (UVLO) and thermal shutdown (TSD). Because these protection circuits are fully integrated inside the IC without external components, the reliability is improved without increasing cost. Once the fault condition occurs, switching is terminated and the Sense FET remains off. This causes Vcc to fall. When Vcc reaches the UVLO stop voltage, 8V, the protection is reset and the internal high voltage current source charges the Vcc capacitor via the Vstr pin. When Vcc reaches the UVLO start voltage,12V, the FPS resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated.

4.1 Over Load Protection (OLP) : Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated in order to protect the SMPS. However, even when the SMPS is in the normal operation, the over load protection circuit can be activated during the load transition. In order to avoid this undesired operation, the over load protection circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation. In conjunction with the Ipk current limit pin (if used) the current mode feedback path would limit the current in the Sense FET when the maximum PWM duty cycle is attained. If the output consumes more than this maximum power, the output voltage (Vo) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (Vfb). If Vfb exceeds 3V, the feedback input diode is blocked and the 5uA Idelay current source starts to charge Cfb slowly up to Vcc. In this condition, Vfb continues increasing until it reaches 6V, when the switching operation is terminated as shown in figure 6. The delay time for shutdown is the time required to charge Cfb from 3V to 6V with 5uA.



$$t1 = -\frac{1}{RC_{fb}} In(1-\frac{V(t1)}{R}); V(t1) = 3V, R = 2.8K\Omega, C_{fb} = C_{fb_fig.2}$$

$$t2 = C_{fb}\frac{(V(t1+t2)-V(t1))}{I_{delay}}; I_{delay} = 5uA, V(t1+t2)-V(t1) = 3V$$

Figure 6. Over load protection

4.2 Thermal Shutdown (TSD) : The Sense FET and the control IC are integrated, making it easier for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 140°C, thermal shutdown is activated.

4.3 Abnormal Over Current Protection (AOCP) :

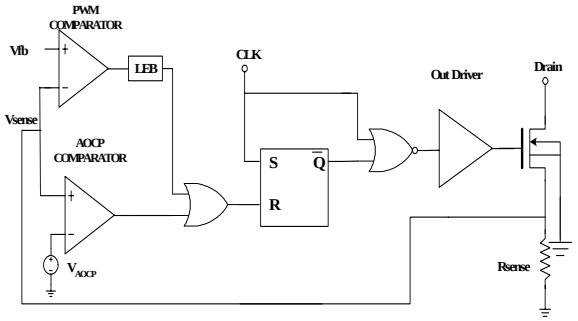
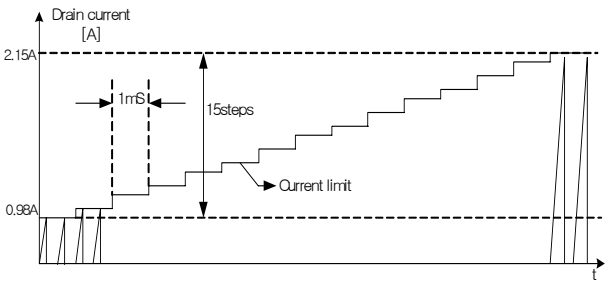


Figure 7. AOCP Function & Block

Even though the FPS has OLP (Over Load Protection) and current mode PWM feedback, these are not enough to protect the FPS when a secondary side diode short or a transformer pin short occurs. In addition to start-up, soft-start is also activated at each restart attempt during auto-restart and when restarting after latch mode is activated. The FPS has an internal AOCP (Abnormal Over Current Protection) circuit as shown in figure 7. When the gate turn-on signal is applied to the power Sense FET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is then compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, pulse by pulse AOCP is triggered regardless of uncontrollable LEB time. Here, pulse by pulse AOCP stops Sense FET within 350nS after it is activated.

4.4 Over Voltage Protection (OVP) : In case of malfunction in the secondary side feedback circuit, or feedback loop open caused by a defect of solder, the current through the opto-coupler transistor becomes almost zero. Then, Vfb climbs up in a similar manner to the over load situation, forcing the preset maximum current to be supplied to the SMPS until the over load protection is activated. Because excess energy is provided to the output, the output voltage may exceed the rated voltage before the over load protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. In general, Vcc is proportional to the output voltage and the FPS uses Vcc instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, OVP circuit is activated resulting in termination of the switching operation. In order to avoid undesired activation of OVP during normal operation, Vcc should be properly designed to be below 19V.

5. Soft Start : The FPS has an internal soft start circuit that increases the feedback voltage together with the Sense FET current slowly after it starts up. The typical soft start time is 15msec, as shown in figure 8, where progressive increments of Sense FET current are allowed during the start-up phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode.



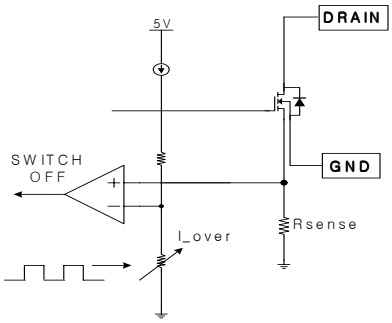


Figure 8. Soft Start Function

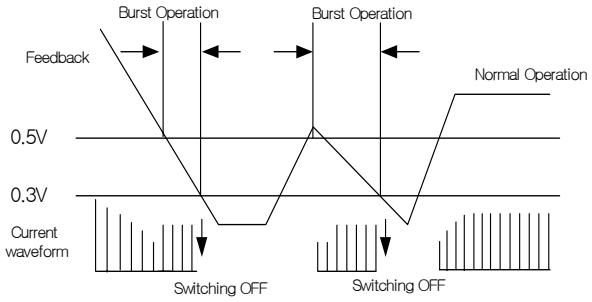


Figure 10. Circuit for Burst Operation

6. Burst operation : In order to minimize power dissipation in standby mode, the FPS enters burst mode operation.

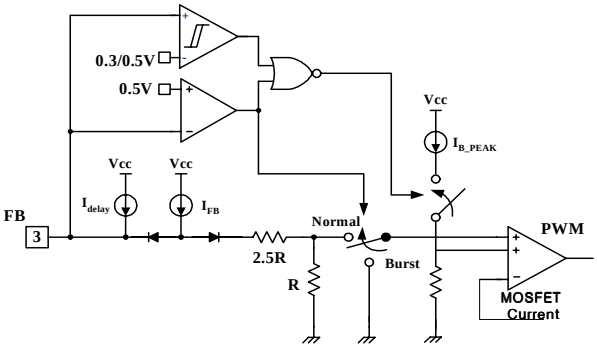


Figure 9. Circuit for Burst operation

As the load decreases, the feedback voltage decreases. As shown in figure 10, the device automatically enters burst mode when the feedback voltage drops below VBURH(500mV). Switching still continues but the current limit is set to a fixed limit internally to minimize flux density in the transformer. The fixed current limit is larger than that defined by Vfb = VBURH and therefore, Vfb is driven down further. Switching continues until the feedback voltage drops below VBURL(300mV). At this point switching stops and the output voltages start to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes VBURH(500mV) switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the power Sense FET thereby reducing switching loss in Standby mode.

7. Frequency Modulation : EMI reduction can be accomplished by modulating the switching frequency of a switched power supply. Frequency modulation can reduce EMI by spreading the energy over a wider frequency range than the band width measured by the EMI test equipment. The amount of EMI reduction is directly related to the depth of the reference frequency. As can be seen in Figure 11, the frequency changes from 65KHz to 69KHz in 4mS for the FSDM0265RN. Frequency modulation allows the use of a cost effective inductor instead of an AC input mode choke to satisfy the requirements of world wide EMI limits.

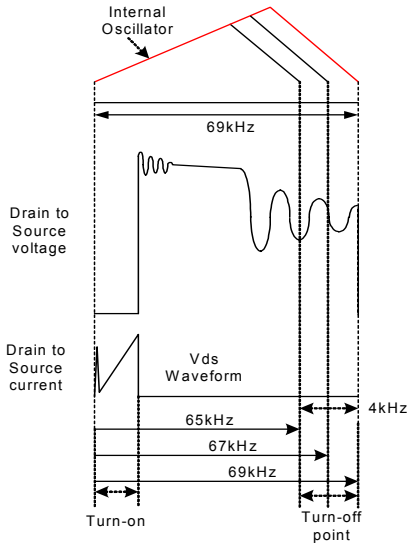


Figure 11. Frequency Modulation Waveform

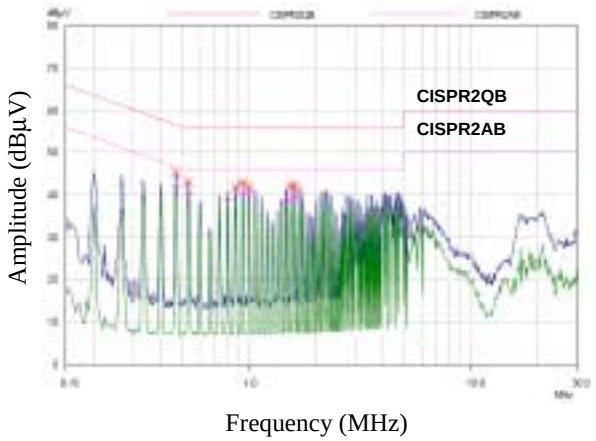


Figure 12. KA5-series FPS Full Range EMI scan(67KHz, no Frequency Modulation) with DVD Player SET

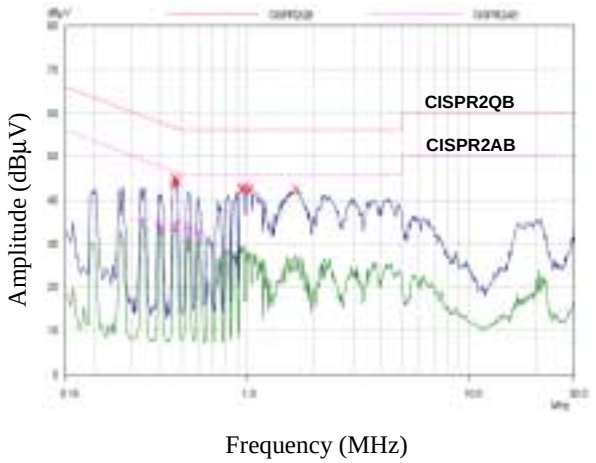


Figure 13. FSDX-series FPS Full Range EMI Scan (67KHz, with Frequency Modulation) with DVD Player SET

8. Adjusting Current limit function: As shown in fig 14, a combined 2.8KΩ internal resistance is connected into the non-inverting lead on the PWM comparator. A external resistance of Y on the current limit pin forms a parallel resistance with the 2.8KΩ when the internal diodes are biased by the main current source of 900uA.

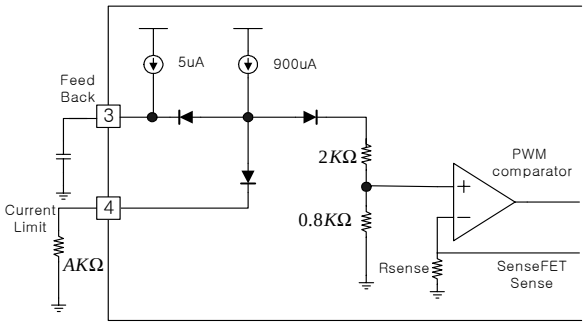


Figure 14. Peak current adjustment

For example, FSDx0265RN has a typical Sense FET current limit (IOVER) of 2.15A. The Sense FET current can be limited to 1A by inserting a 2.8kΩ between the current limit pin and ground which is derived from the following equations:

2.15: 1 = 2.8KΩ : XKΩ ,

X = 1.3KΩ,

Since X represents the resistance of the parallel network, Y can be calculated using the following equation:

Y = X / (1 - (X/2.8KΩ))

Typical application circuit

1. Set Top Box Example Circuit (20W Output Power)

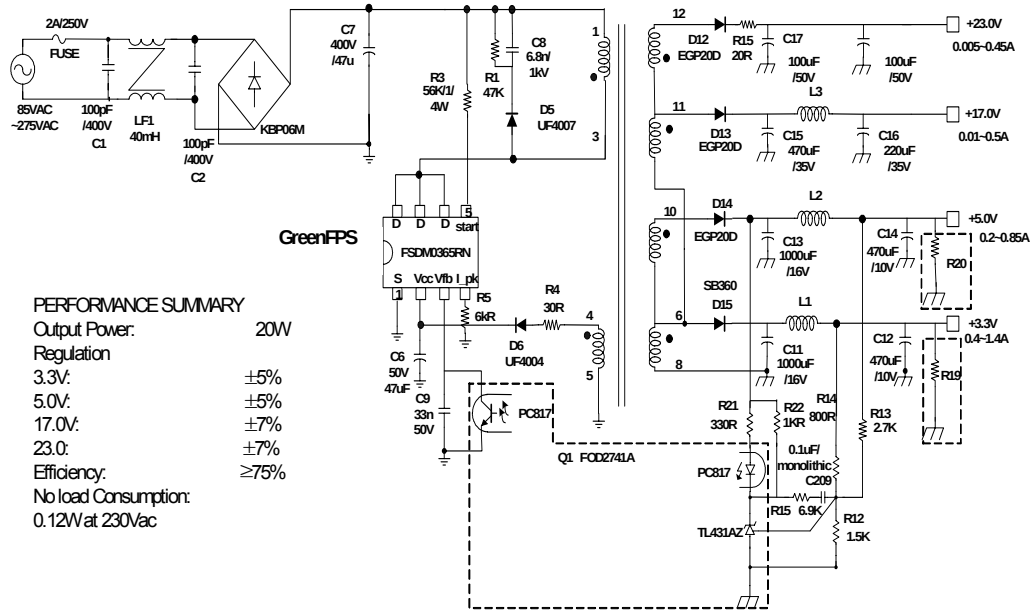


Figure15. 20W multiple power supply using FSDM0365RN

Multiple Output, 20W, 85-265VAC Input Power supply: Figure 15 shows a multiple output supply typical for high end set-top boxes containing high capacity hard disks for recording or LIPS(LCD Inverter Power Supply) for 15" LCD monitor. The supply delivers an output power of 20W cont./24 W peak (thermally limited) from an input voltage of 85 to 265 VAC. Efficiency at 20W, 85VAC is ≥75%.

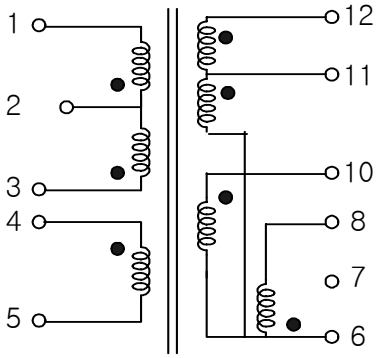
The 3.3 V and 5 V outputs are regulated to ±5% without the need for secondary linear regulators. DC stacking (the secondary winding reference for the other output voltages is connected to the anode of D15. For more accuracy, connection to the cathode of D15 will be better.) is used to minimize the voltage error for the higher voltage outputs. Due to the high ambient operating temperature requirement typical of a set-top box (60 °C) the FSDL0165RN is used to reduce conduction losses without a heatsink. Resistor R5 sets the device current limit to limit overload power.

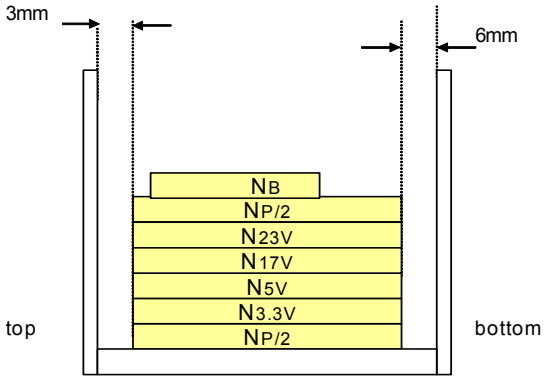
Leakage inductance clamping is provided by R1 and C8, keeping the DRAIN voltage below 650 V under all conditions. Resistor R1 and capacitor C8 are selected such that R1 dissipates power to prevent rising of DRAIN Voltage caused by leakage inductance. The frequency modulation feature of FSDL0165RN allows the circuit shown to meet CISPR2AB with simple EMI filtering (C1, LF1 and C2) and the output grounded. The secondaries are rectified and smoothed by D12, D13, D14,and D15. Diode D15 for the 3.4V output is a Schottky diode to maximize efficiency. Diode D14 for the 5 V output is a PN type to center the 5 V output at 5 V. The 3.3 V and 5 V output voltage require two capacitors in parallel to meet the ripple current requirement. Switching noise filtering is provided by L3, L2 and L1. Resistor R15 prevents peak charging of the lightly loaded 23V output. The outputs are regulated by the reference (TL431) voltage in secondary. Both the 3.3 V and 5 V outputs are sensed via R13 and R14. Resistor R22 provides bias for TL431and R21 sets the overall DC gain. Resistor R21, C209, R14 and R13 provide loop compensation.

2. Transformer Specification

1. TRANSFORMER SPECIFICATION

- **SCHEMATIC DIAGRAM (TRANSFORMER)**





2. WINDING SPECIFICATION

NO.	PIN(S → F)	WIRE	TURNS	WINDING METHOD
NP/2	3 → 2	0.25 Φ × 1	22	SOLENOID WINDING
N3.3V	6 → 8	0.3 Φ × 8	2	STACK WINDING
N5V	10 → 6	0.3 Φ × 2	1	STACK WINDING
N16V	11 → 6	0.3 Φ × 4	7	SOLENOID WINDING
N23V	12 → 11	0.3 Φ × 2	3	SOLENOID WINDING
NP/2	2 → 1	0.25 Φ × 1	22	SOLENOID WINDING
NB	4 → 5	0.25 Φ × 1	10	CENTER WINDING

3. ELECTRIC CHARACTERISTIC

CLOSURE	PIN	SPEC.	REMARKS
INDUCTANCE	1 - 3	800uH ± 10%	1KHz, 1V
LEAKAGE L	1 - 3	15uH MAX.	2nd ALL SHORT

4. BOBBIN & CORE.

CORE: EER2828
BOBBIN: EER2828

Layout Considerations

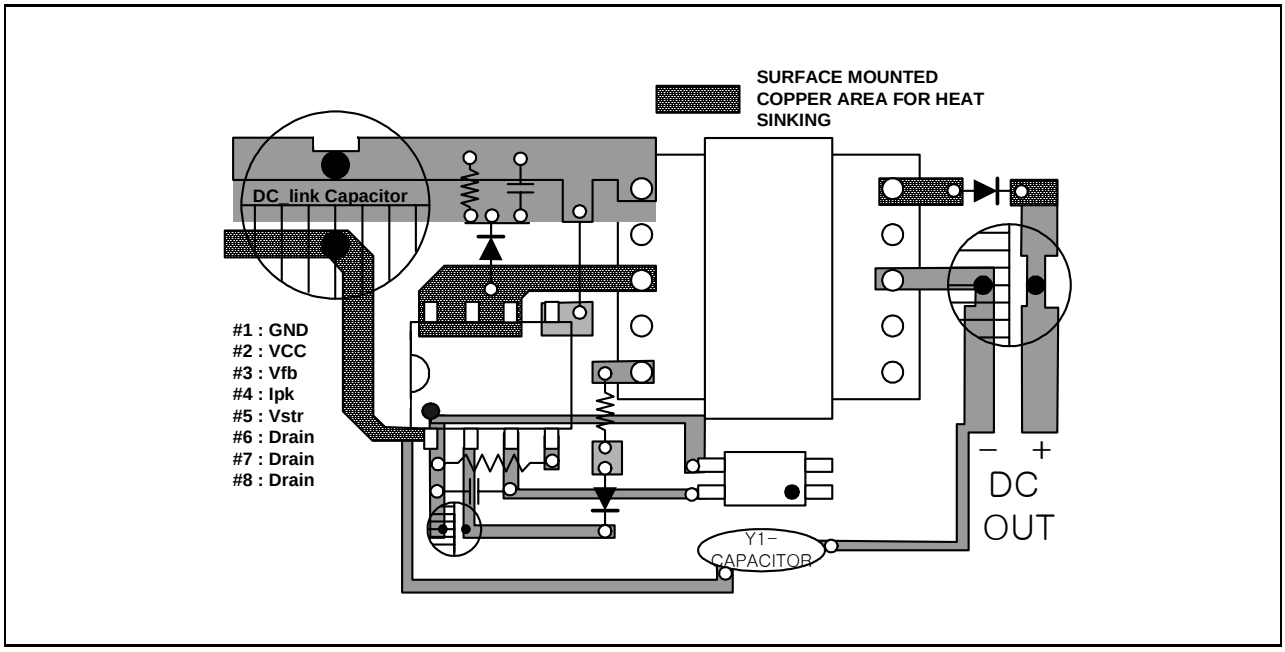
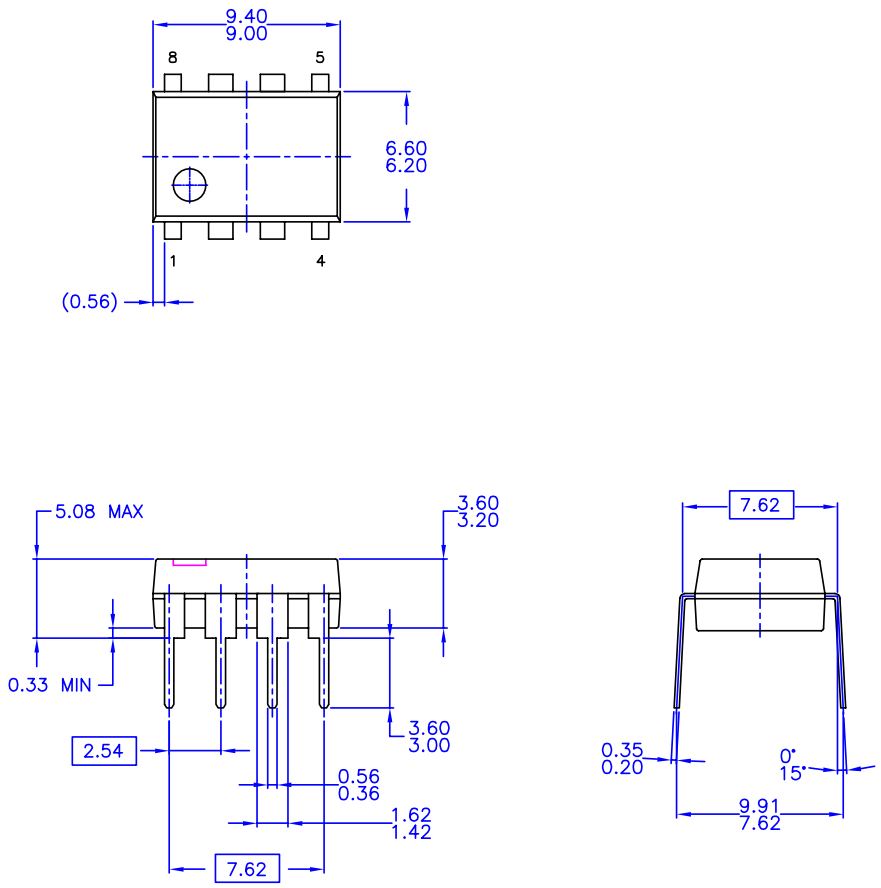


Figure 15. Layout Considerations for FSDx0365RN using 8DIP

Package Dimensions

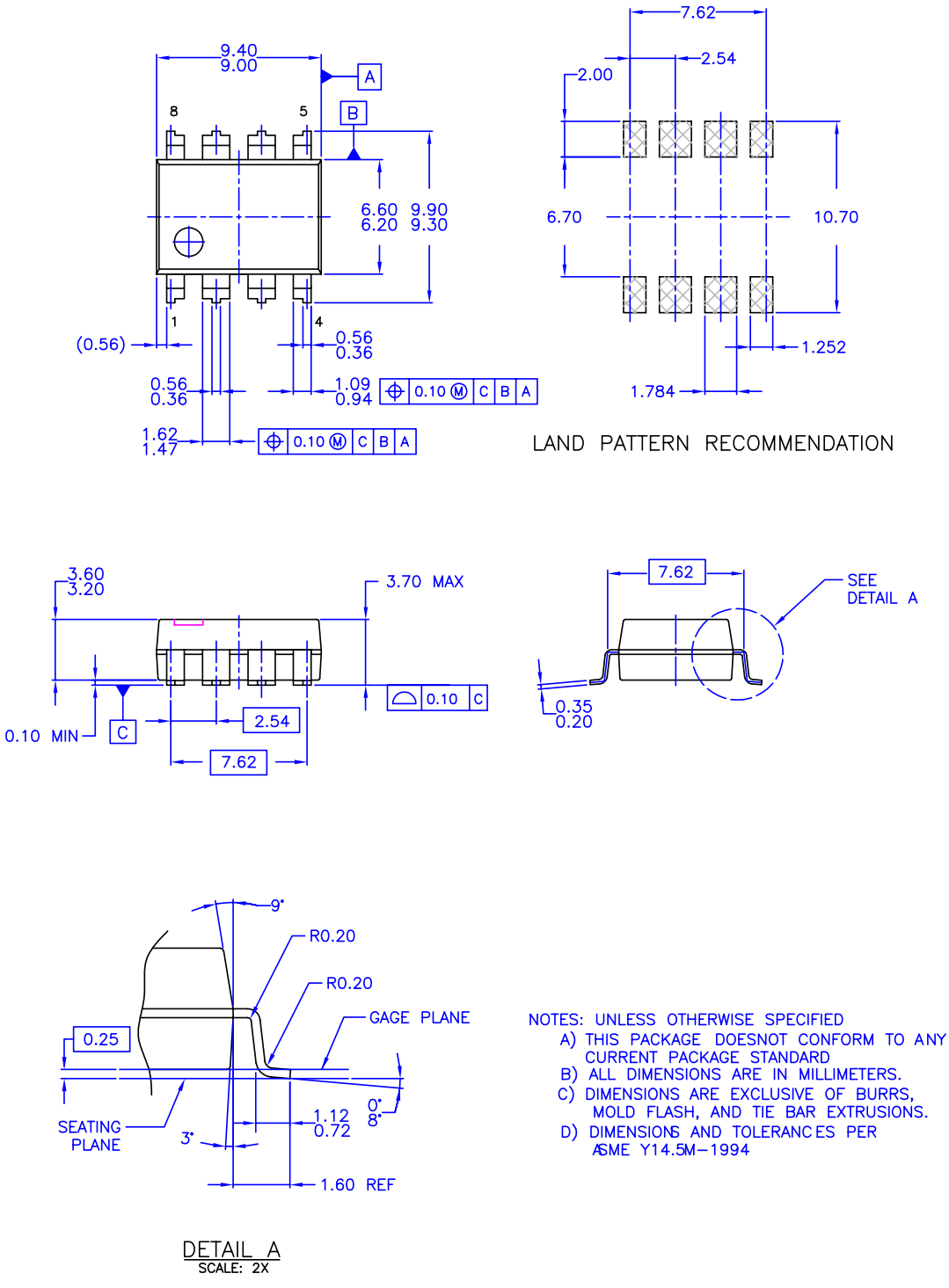
8DIP



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

Package Dimensions (Continued)

8LSOP



Ordering Information

Product Number	Package	Marking Code	BV_{DSS}	F_{OSC}	$R_{DS(on)}$
FSDM0365RN	8DIP	DM0365R	650V	67KHz	3.6Ω
FSDL0365RN	8DIP	DL0365R	650V	50KHz	3.6Ω
FSDM0365RL	8LSOP	DM0365R	650V	67KHz	3.6Ω
FSDL0365RL	8LSOP	DL0365R	650V	50KHz	3.6Ω

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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