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May 2013

FSA2257
Low R_{ON}, Low-Voltage Dual SPDT Bi-Directional Analog Switch

Features

- Maximum 1.15 Ω On Resistance (R_{ON}) at 4.5 V V_{CC}
- 0.3 Ω Maximum R_{ON} Flatness at +5 V V_{CC}
- Space-Saving MicroPak™
- Broad V_{CC} Operating Range: 1.65 V to 5.50 V
- Fast Turn-On and Turn-Off Time
- Break-Before-Make Enable Circuitry
- Over-Voltage Tolerant TTL-Compatible Control Input

Applications

- Cell Phone
- PDA
- Mobile Devices

Description

The FSA2257 is a high-performance bi-directional dual Single-Pole/Double-Throw (SPDT) analog switch. This switch can be configured as either a multiplexer or a de-multiplexer by select pins. The device features ultra-low R_{ON} of 1.3 Ω maximum at 4.5 V V_{CC} and operates over the wide V_{CC} range of 1.65 V to 5.50 V. The device is fabricated with submicron CMOS technology to achieve fast switching speeds and is designed for break-before-make operation. The select input is TTL-level compatible.

Ordering Information

Part Number	Package Number	Top Mark	Package Description	Packing Method
FSA2257L10X	MAC10A	EP	10-Lead MicroPak™, 1.6 x 2.1 mm	5000 Units Tape and Reel
FSA2257MTCX	MCT14	FSA2257	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4 mm Wide	2500 Units Tape and Reel
FSA2257MUX	MUA10A	FSA 2257	10-Lead Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0 mm	4000 Units Tape and Reel

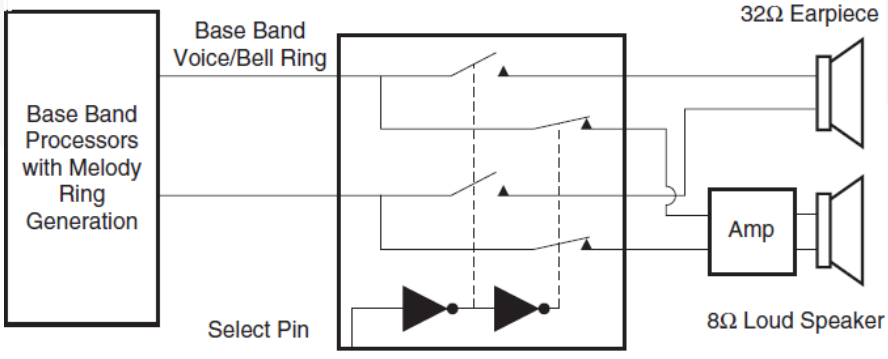

Figure 1. Block Diagram

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Pin Configurations

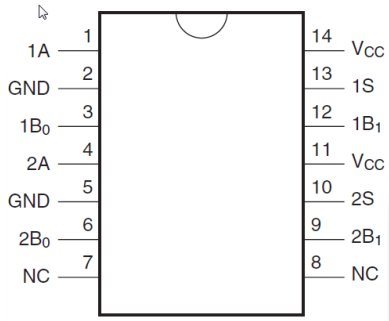

Figure 2. Pin Assignments for TSSOP (Top View)

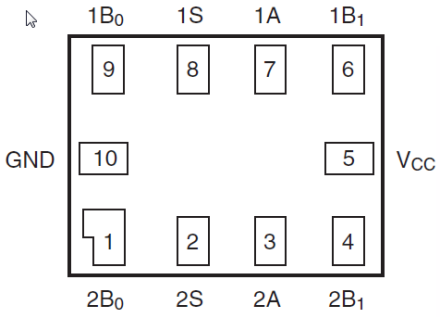

Figure 3. MicroPak™ Pad Assignments (Top View)

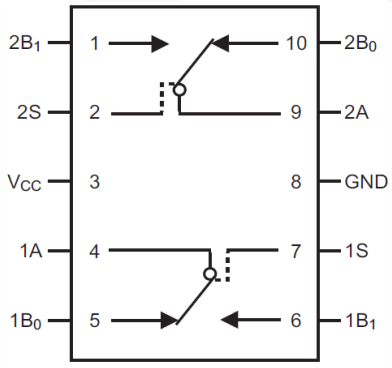

Figure 4. Pin Assignments for MSOP (Top View)

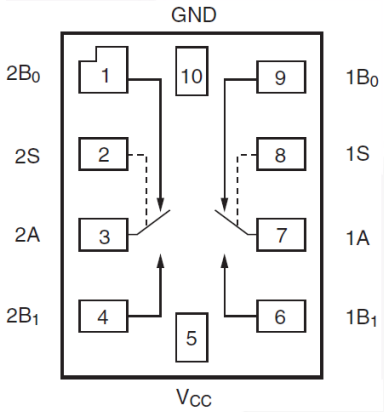

Figure 5. Analog Symbols (Top Through View)

Pin Definitions

Pin# TSSOP	Pin# MicroPak™	Pin # MSOP	Name	Description
1	7	4	1A	Data Ports
2,5	10	8	GND	Ground
3	9	5	$1B_0$	Data Ports
4	3	9	2A	Data Ports
6	1	10	$2B_0$	Data Ports
7,8			NC	No Connect
9	4	1	$2B_1$	Data Ports
10	2	2	2S	Control Inputs
11,14	5	3	V_{CC}	Power Supply
12	6	6	$1B_1$	Data Ports
13	8	7	1S	Control Inputs

Truth Table

Control Input (S)	Function
Low Logic Level	B_0 connected to A
High Logic Level	B_1 connected to A

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	6.0	V
V_{SW}	DC Switch Voltage[1]		-0.5	V_{CC} + 0.5	V
V_{IN}	DC Input Voltage[1]		-0.5	6.0	V
I_{IK}	Input Diode Current		-50		mA
	Switch Current			200	
	Peak Switch Current (Pulsed at 1 ms duration, <10% duty cycle)			400	
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature			+150	°C
T_L	Lead Temperature (Soldering, 10 seconds)			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		8000	V
		Charged Device Model, JESD22-C101		2000	

Note:
1. Input and output negative ratings may be exceeded if input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.65	5.50	V
V_{CNTRL}	Control Input Voltage[2]	0	V_{CC}	V
V_{SW}	Switch Input Voltage	0	V_{CC}	V
T_A	Operating Temperature	-40	+85	°C

Note:
2. Unused control input must be held HIGH or LOW and it must not float.

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DC Electrical Characteristics

Typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC}(V)	T_A=+25°C			T_A=-40°C to +85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	Input Voltage High		1.8 to 2.7				1.0		V
			2.7 to 3.6				2.0		
			4.5 to 5.5				2.4		
V_{IL}	Input Voltage Low		1.8 to 2.7					0.4	V
			2.7 to 3.6					0.6	
			4.5 to 5.5					0.8	
I_{IN}	Control Input Leakage	V_{IN}=0 V to V_{CC}	2.7 to 3.6				-1.0	1.0	µA
			4.5 to 5.5				-1.0	1.0	
$I_{NO(OFF)}$, $I_{NC(OFF)}$	Off Leakage Current of Port B_0 and B_1	A=1 V, 4.5 V, B_0 or B_1=1 V, 4.5 V	5.5	-2		2	-20	20	nA
$I_{A(ON)}$	On Leakage Current of Port A	A=1 V, 4.5V, B_0 or B_1=1 V,4.5 V or Floating	5.5	-4		2	-40	40	nA
R_{ON}	Switch On Resistance MicroPak[3]	I_{OUT}=100 mA, B_0 or B_1=1.5 V	1.8		4.6				Ω
			2.7		2.6	4.0		4.3	
		I_{OUT}=100 mA, B_0 or B_1=3.5 V	4.5		0.95	1.15		1.30	
	Switch On Resistance MSOP/TSSOP[3]	I_{OUT}=100 mA, B_0 or B_1=1.5 V	2.7		2.8			4.5	
		I_{OUT}=100 mA, B_0 or B_1=3.5 V	4.5		1.5			2.3	
ΔR_{ON}	On Resistance Matching Between Channels MicroPak [4]	I_{OUT}=100 mA, B_0 or B_1=3.5 V	4.5		0.06	0.12		0.15	Ω
	On Resistance Matching Between Channels MSOP / TSSOP[4]		4.5		0.7			0.3	
$R_{FLAT(ON)}$	On Resistance Flatness[5]	I_{OUT}=100 mA, B_0 or B_I =0 V, 0.75 V,1.5 V	1.8		3.0				Ω
			2.7		1.4				
		I_{OUT}=100 mA, B_0 or B_I =0 V, 1 V, 2 V	4.5		0.2	0.3		0.4	
I_{CC}	Quiescent Supply Current	V_{IN}=0 V or V_{CC}, I_{OUT}=0 V	3.6		0.1	0.5		1.0	µA
			5.5		0.1	0.5		1.0	

Notes:

3. On resistance is determined by the voltage drop between A and B pins at the indicated current through the switch.
4. $\Delta R_{ON} = R_{ONmax} – R_{ONmin}$ measured at identical V_{CC}, temperature, and voltage.
5. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.

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AC Electrical Characteristics

Typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC}(V)	T_A=+25°C			T_A=-40°C to +85°C		Unit	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{ON}	Turn-On Time	B_0 or B_1=1.5 V, R_L=50 Ω, C_L=35 pF	1.8 to 2.7		75				ns	Figure 6
			2.7 to 3.6			50		60		
		B_0 or B_1=3.0 V, R_L=50 Ω, C_L=35 pF	4.5 to 5.5			35		40		
t_{OFF}	Turn-Off Time	B_0 or B_1=1.5 V, R_L=50 Ω, C_L=35 pF	1.8 to 2.7		20				ns	Figure 6
			2.7 to 3.6			20		30		
		B_0 or B_1=3.0 V, R_L=50 Ω, C_L=35 pF	4.5 to 5.5			15		20		
t_{BBM}	Break-Before-Make Time	B_0 or B_1=1.5 V, R_L=50 Ω, C_L=35 pF	2.7 to 3.6				1		ns	Figure 7
		B_0 or B_1=3.0 V, R_L=50 Ω, C_L=35 pF	4.5 to 5.5		20		1			
Q	Charge Injection	C_L=1.0 nF, V_{GEN}=0 V, R_{GEN}=0 Ω	2.7 to 3.6		20				pC	Figure 9
			4.5 to 5.5		10					
OIRR	Off Isolation	f=1 MHz, R_L=50 Ω	2.7 to 3.6		-70				dB	Figure 8
			4.5 to 5.5		-70					
Xtalk	Crosstalk	f=1 MHz, R_L=50 Ω	2.7 to 3.6		-75				dB	Figure 8
			4.5 to 5.5		-75					
BW	-3 db Bandwidth	R_L=50 Ω	2.7 to 3.6		200				MHz	Figure 11
			4.5 to 5.5		200					
THD	Total Harmon Distortion	R_L=600 Ω, V_{IN}=0.5 V_{PP} f=20 Hz to 20 kHz	2.7 to 3.6		0.002				%	Figure 12
			4.5 to 5.5		0.002					

Capacitance

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25°C			Unit	Figure
				Min.	Typ.	Max.		
C_{IN}	Control Pin Input Capacitance	f=1 MHz	0		3.5		pF	Figure 10
C_{OFF}	B Port Off Capacitance	f=1 MHz	4.5		12.0		pF	Figure 10
C_{ON}	A Port On Capacitance	f=1 MHz	4.5		40.0		pF	Figure 10

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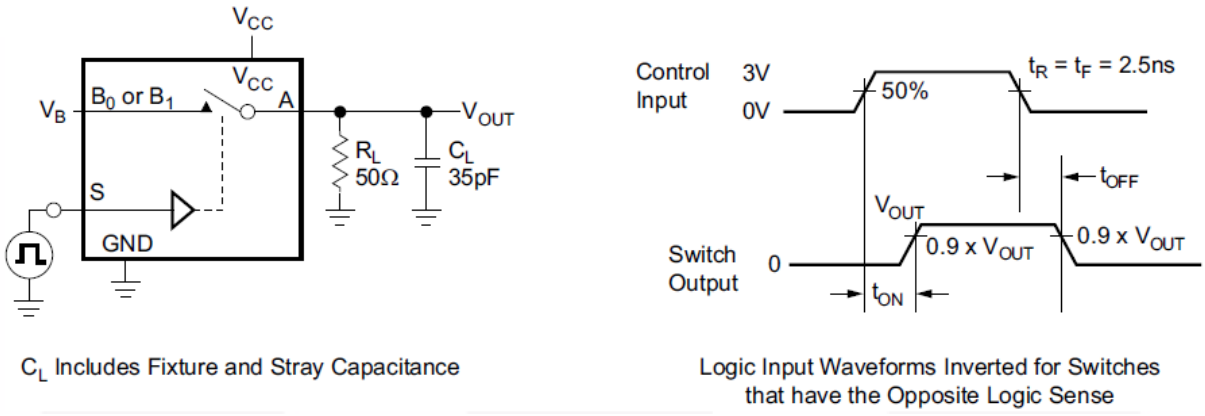
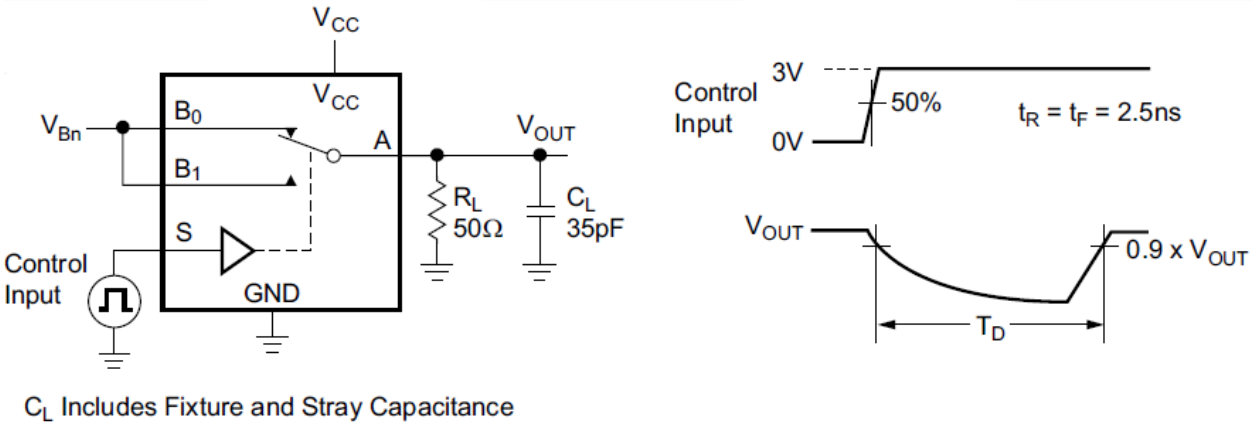
AC Loadings and Waveforms



C_L Includes Fixture and Stray Capacitance

Logic Input Waveforms Inverted for Switches that have the Opposite Logic Sense

Figure 6. Turn On / Off Timing



C_L Includes Fixture and Stray Capacitance

Figure 7. Break Before Make Timing

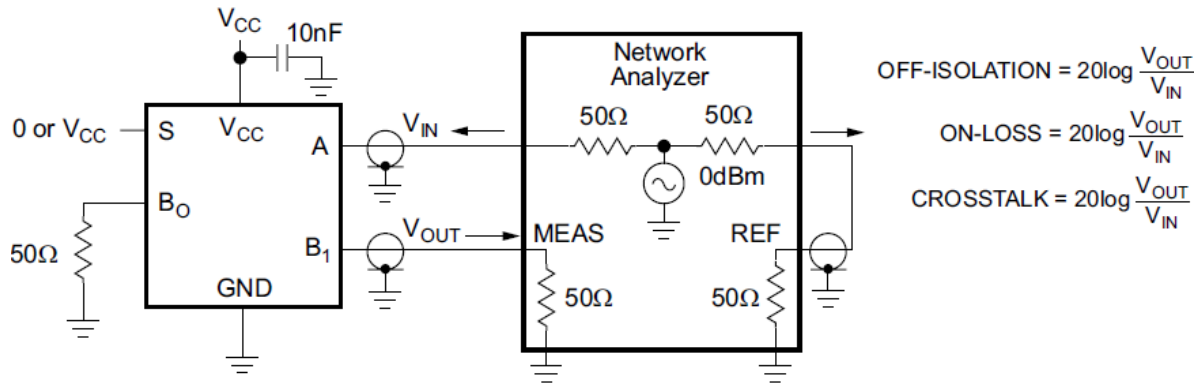


Figure 8. Off Isolation and Crosstalk

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AC Loadings and Waveforms (Continued)

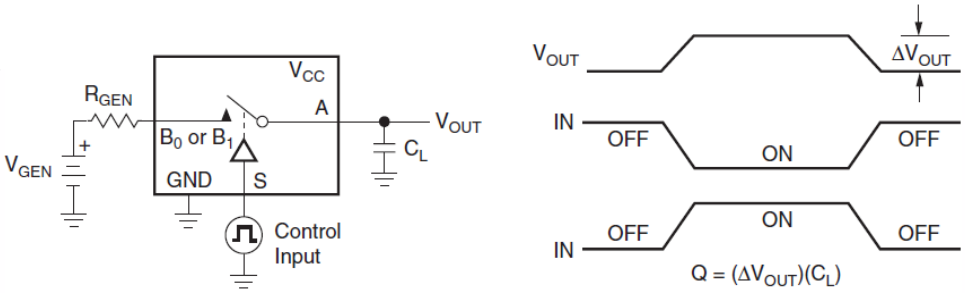

Figure 9. Charge Injection

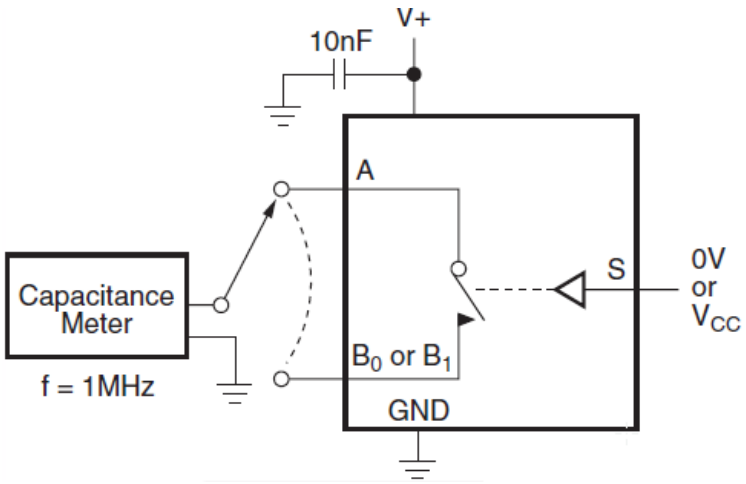

Figure 10. On / Off Capacitance Measurement Setup

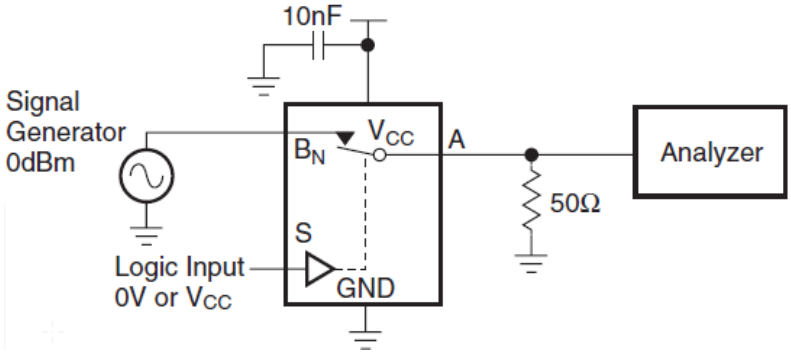

Figure 11. Bandwidth

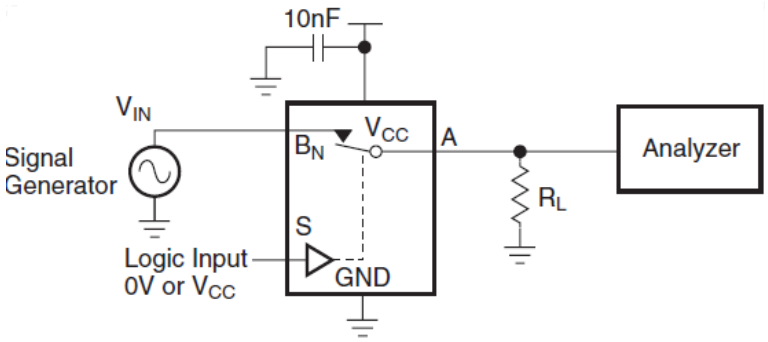

Figure 12. Harmonic Distortion

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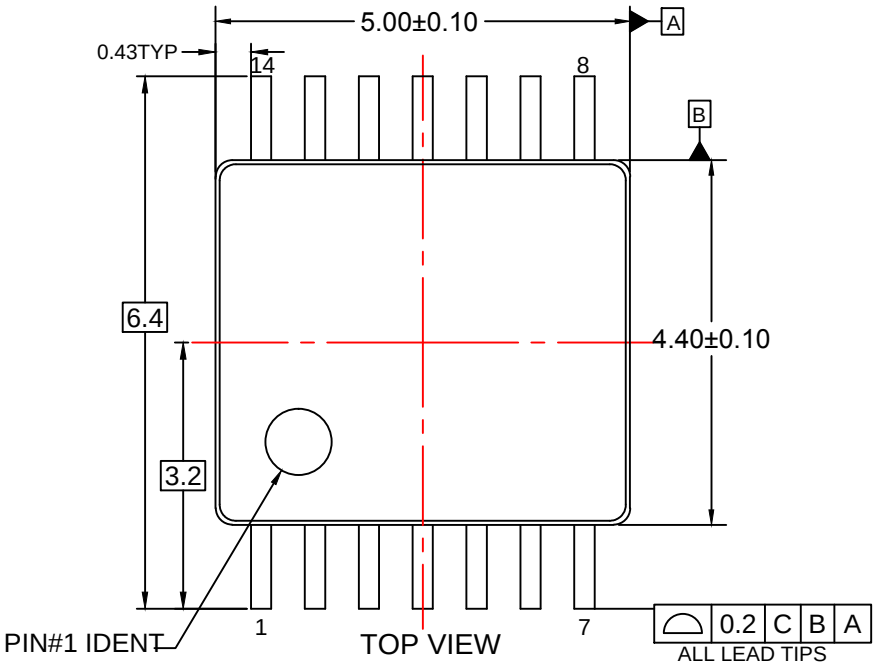
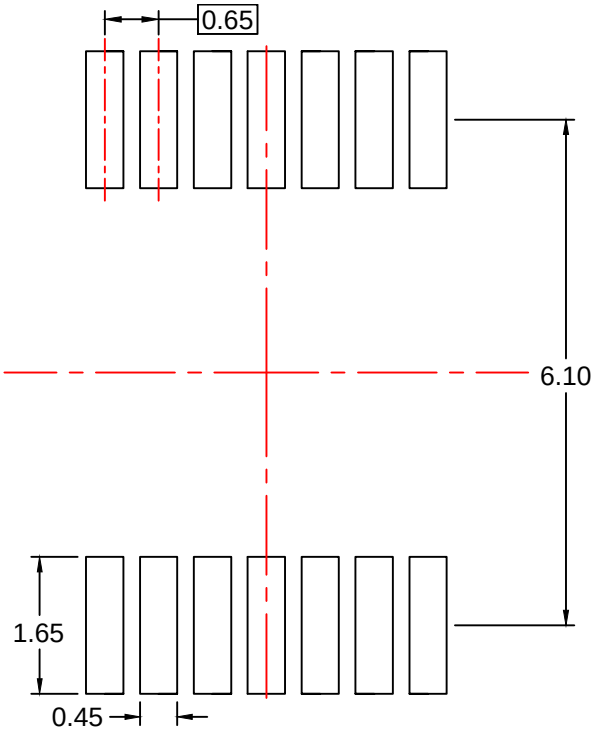
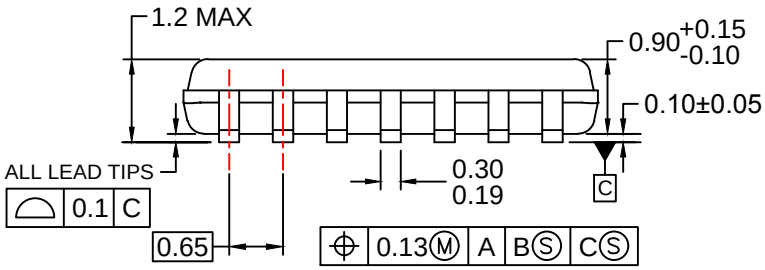


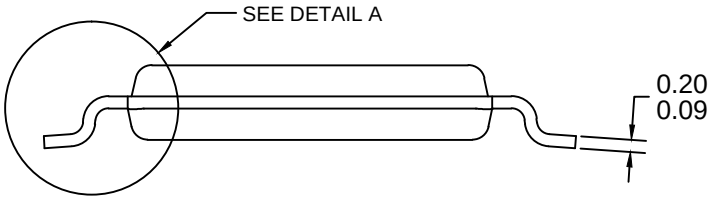
TOP VIEW

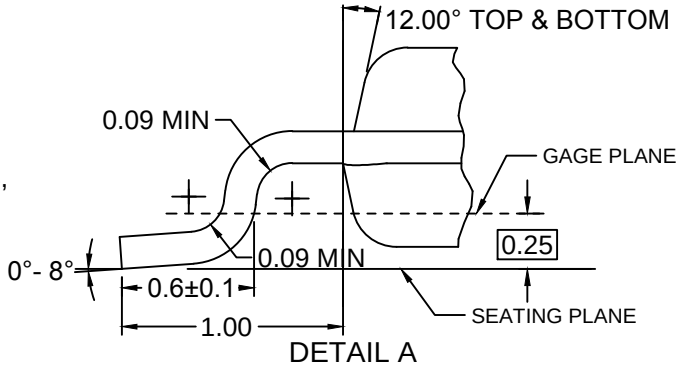


RECOMMENDED LAND PATTERN



FRONT VIEW





DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.

E. LANDPATTERN STANDARD: SOP65P640X110-14M.

F. DRAWING FILE NAME: MKT-MTC14rev7.

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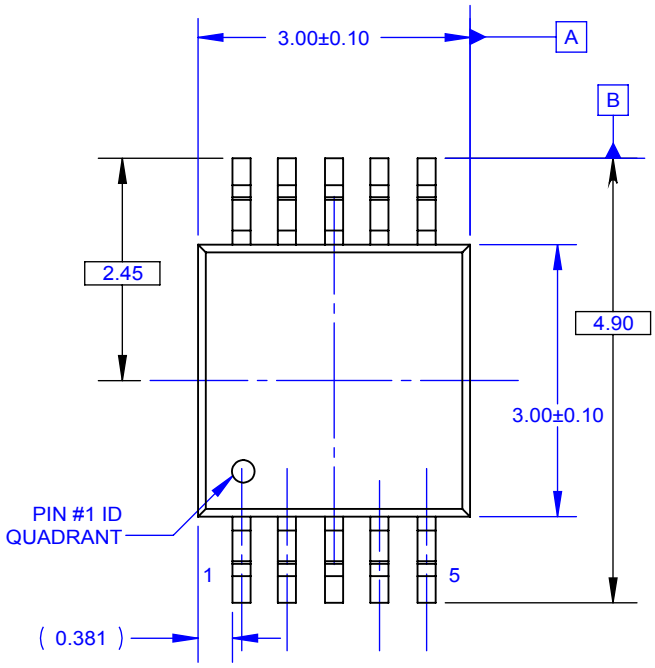
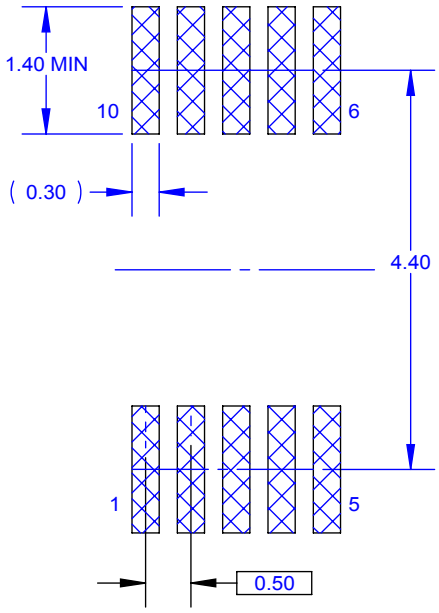
REVISIONS

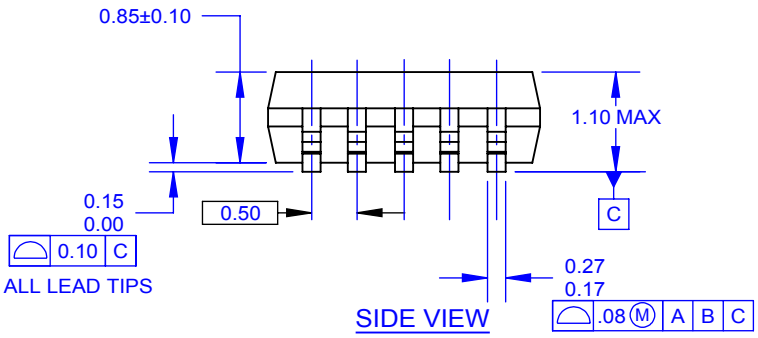
NBR	DESCRIPTION	DATE	BY/APP'D
B	REDREW FORMER NSC DWG	07JUN2006	H.ALLEN
2	* REMOVE SITE ADDRESS AND CHANGE REVISION TO NUMERICAL & CHANGED LAND PATTERN TO IPC. * CHANGE LEAD WIDTH FROM 0.27MAX TO 0.33MAX. * REMOVE DATE OF JEDEC REVISION	20AUG2009	KHLEE/FSSZ
3	* REVERT LEAD WIDTH TO 0.27MAX.	24SEP2009	KHLEE/FSSZ



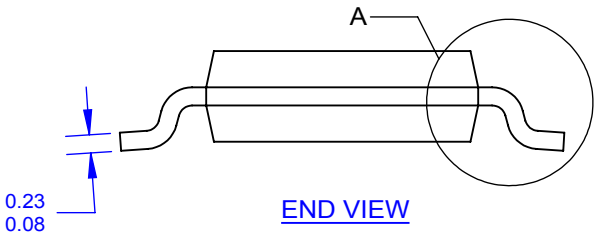
TOP VIEW



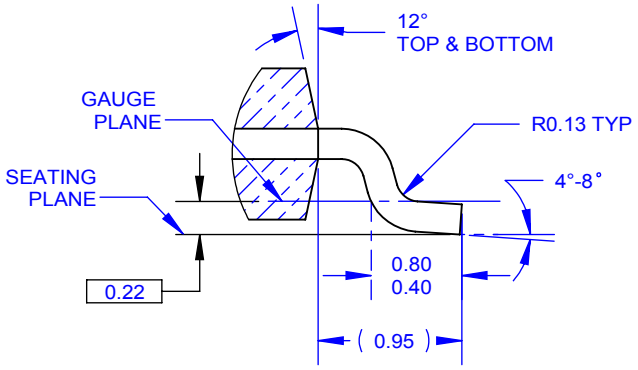
LAND PATTERN RECOMMENDATION



SIDE VIEW



END VIEW



DETAIL A
SCALE 20 : 1

NOTES: UNLESS OTHERWISE SPECIFIED

A. THIS PACKAGE CONFORMS TO JEDEC MO-187 VARIATION BA.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES AS PER ASME Y14.5-1994.
E. LAND PATTERN AS PER IPC7351#SOP50P490X110-10AN
F. FILE NAME: MKT-MUA10AREV3

APPROVALS	DATE
DRAWN: BOBOY MALDO	24SEP09
CHECKED: KH LEE	
APPROVED: BY HUANG	
APPROVED: HOWARD ALLEN	

PROJECTION [MM] INCH

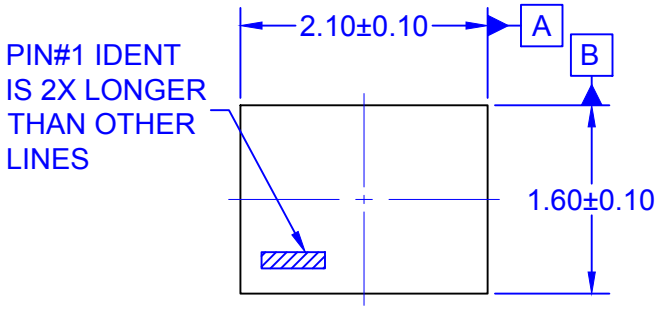
FAIRCHILD SEMICONDUCTOR TM

10LD, MSOP, JEDEC MO-187, 3.0MM WIDE

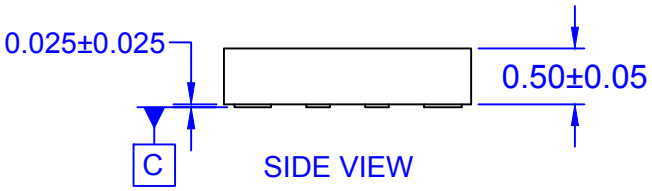
SCALE	SIZE	DRAWING NUMBER	REV
1:1	N/A	MKT-MUA10A	3

FORMERLY: N/A

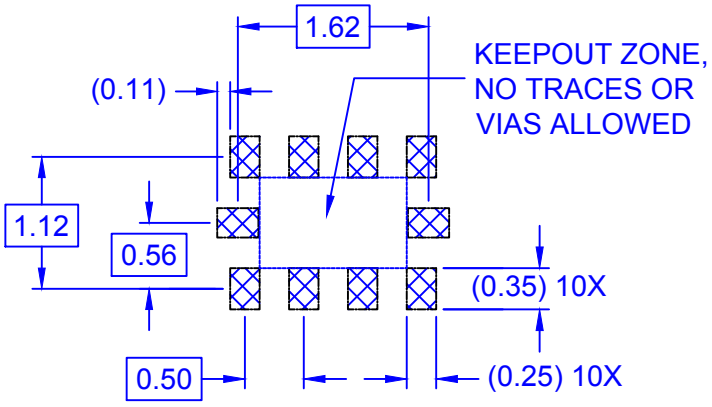
SHEET : 1 OF 1



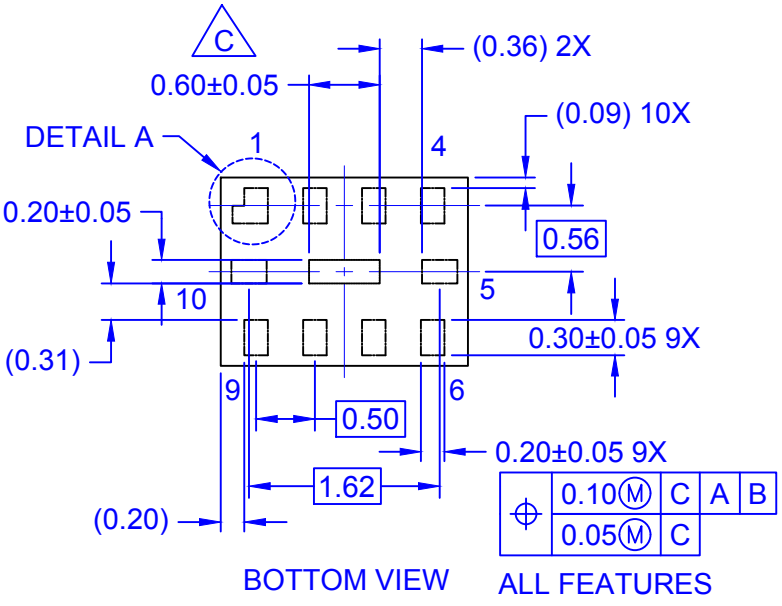
TOP VIEW



SIDE VIEW

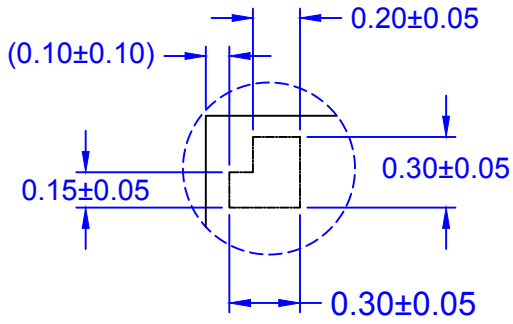


RECOMMENDED LAND PATTERN



BOTTOM VIEW

ALL FEATURES



DETAIL A
SCALE 2:1

NOTES:

A. PACKAGE CONFORMS TO JEDEC REGISTRATION MO-255, VARIATION UABD.

B. DIMENSIONS ARE IN MILLIMETERS.

C. PRESENCE OF CENTER PAD IS PACKAGE SUPPLIER DEPENDENT. IF PRESENT IT IS NOT INTENDED TO BE SOLDERED AND HAS A BLACK OXIDE FINISH.

D. DRAWING FILENAME: MKT-MAC10ArevG.

E. DIMENSIONS WITHIN ( ) ARE UNCONTROLLED.

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