Datasheet

FS970X

5,000/50,000 counts DMM analog front end.

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1. General Description

FS970X is a series of Digital Multi-function Meter (DMM) front-end chip. The core is a high resolution Σ-Δ ADC, combined with function network, operation amplifier, comparator, digital filter, crystal oscillator circuit, digital control logic and micro processor interface.

FS970X ADC includes not only high-resolution output to achieve accurate measurement, but high-speed ADC output to display the bar graph of digital meter and to measure +/- peak hold.

Combined with a micro processor, FS970X can function as an auto-range DMM to measure DC/AC voltage, DC/AC current, resistance, frequency, peak hold and diode, etc. In addition, it includes several sets of programmable ADC direct input to expand product applicability (such as pressure function, temperature function, etc.…)

There are two operation amplifiers built in FS970X to act as high impedance buffer and DC/AC converter when measuring AC voltage. These two amplifiers are with other functions as well even not acting as DC/AC converter. One of them can be connected to external resistor to build a x10 amplify circuit. The reading from the x10 signal into the ADC can still be of accuracy due to the excellent noise immunity of the amplifier.

Chip	Max. resolution (counts)/ output (Hz)	Speed output (HZ) / resolution (counts)	DC Voltage	DC Current	AC Buffer	AC/DC Converter	X 10 path	Resistor	Capacitor	Frequency counter	Peak hold	Diode testing	Voltage regulator	ADP input
FS9701B	5000 / 5	640 / 500	√	√	√	√	√	√	√	√	√	√	√	5
FS9704B	80000 / 5	640 / 800	√	√	√	√	√	√	√	√	√	√	√	5

Chart 1. FS970X A/B series chips

There are two different versions of FS970X with different specifications and functions. With the same micro processor FSμP01 chip (programs), customers can easily and quickly develop different levels of DMM.

2. Features

General Features (FS9701A/B as an example)

1) Built-in high resolution Δ-Σ ADC
2) 5,000 counts, high-resolution low-speed input, 5 times / sec.
3) 500 counts, low resolution, high-speed input, 640 times / sec.
4) Built-in voltage regulator with 9V input, ±3.2V output
5) Under DC voltage, power consumption is under 1.2mA
6) Standby saving mode
7) Low battery detection
8) Good CMRR at 50/60HZ
9) Built-in crystal oscillator circuit
10) 2.5 kHz beeper driver

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11) Standard 4-bit parallel interface to directly connect to micro processor port
12) 4 programmable ADC direct input channel
13) 64 PIN LQFP package

Measurement Range (FS9701B as an example)

1) 500.0 mV, 50.00mVDC voltage, high impedance input.
2) 0.5000V, 5.000 V, 50.00 V, 500.0 V and 1000 V DC voltage
3) 500.0 uA, 5.000 mA, 50.00mA, 500.0 mA, 5.000 A, and 10.00 A DC current
4) 500.0 Ω, 5.000 KΩ, 50.00 KΩ, 500.0 KΩ, 5.000 MΩ and 50.00 MΩ resistance
5) 0.5000V, 5.000 V, 50.00 V, 500.0 V and 1000 V AC voltage
6) 500.0 uA, 5.000 mA, 50.00mA, 500.0 mA, 5.000 A, and 10.00 A AC current
7) 10.00 nF, 100.0 nF, 1.000 uF,10.00 uF, and 100.0 uF capacitor
8) 50.00 Hz, 500.0 Hz, 5.000 Khz, 50.00 Khz, 500.0 Khz, and 5.000 Mhz frequency.
9) Diode forward bias voltage test, with maximum forward voltage of 2V
10) 1 mS above peak hold detector

3. Ordering Information

Product Number	Package Type
FS9701B	64-pin LQFP
FS9704B	64-pin LQFP
FS9701B-GCE	Green 64-pin LQFP
FS9704B-GCE	Green 64-pin LQFP

4. Electrical Characteristics

(VBAT = 9V, VSS = 0V, T_A=+25℃, unless otherwise indicated)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Zero Input Reading	V_{IN}=0V, 500mV Scale	-1	0	1	Counts
Zero Reading Drift	V_{IN}=0V, 0℃<T_A<+70℃				μV/℃
Linearity (Max. deviation from best straight line fit)	500mV Scale	-2	0	2	Counts
Input Common-Mode Rejection Ratio	V_{CM}=±1V, V_{IN}=0V, 500mV Scale			120	μV/V
Input Common-Mode Voltage Range	V_{IN}=0V, 500mV Scale, ±12 Counts	-1		1	V
Noise (p-p Value not Exceeding 95% of Time)	V_{IN}=0V, 500mV Scale		0	1	Counts
Rollover Error (Difference in reading for equal positive and negative inputs near Full Scale)	-V_{IN}=+V_{IN}=500.00mV	0	1	5	Counts
Input Leakage Current	V_{IN}=0V		1	10	pA
Scale Factor Temperature Coefficient	V_{IN}=500.00mV, 0℃<T_A<+70℃		7.5		ppm/℃
Analog Ground Voltage (With respect to VSS)			3.2		V
Analog Supply Voltage (With respect to VSS)			6.2		V
Digital Supply Voltage (With respect to VSS)			5		V
Analog Ground Source Capability	ΔV_O=-0.1V		20		μA
Analog Ground Sink Capability	ΔV_O=0.1V		3		mA
Analog Supply Source Capability	ΔV_O=0.1V		60		mA
VBAT		7	9		V

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PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Low Battery Detection Voltage		6.7	6.8	6.9	V
VBAT Operating Current	V_{IN}=0, 500mV Scale		960		μA
	R_{IN}=1KΩ, 500Ω Scale		3000		
Sleep Current			10	30	μA
ADC Current	V_{IN}=0		660		μA
ACOP Current	V_{IN}=0		170		μA
Comparator Current	V_{IN}=0.5V DC		14		μA
OSRC Source Capability	ΔV_O=-0.1V, 500Ω Scale		600		μA
Bandwidth of ACOP					Hz
DC Gain of ACOP					dB
Bandwidth of Comparator	V_{IN}=600mV_{P-P} SIN		15M		Hz
	V_{IN}=40mV_{rms} SIN		500K		
Hysteresis of Comparator	ENSCHMT=1		0.2		V
ACBUF Linearity Error	Gain=1				
(R_L=10MΩ, C_L=30pF)	V_{IN}=0.4V_{rms}, 100KHz SIN		0.25		%
	V_{IN}=0.4V_{rms}, 50KHz SIN		0.05		
	V_{IN}=0.4V_{rms}, 20KHz SIN		0.01		
	V_{IN}=0.4V_{rms}, 10KHz SIN calibration		-		
	V_{IN}=0.4V_{rms}, 50Hz SIN		0.0025		
(R_L=10KΩ, C_L=30pF)	V_{IN}=0.4V_{rms}, 100KHz SIN		0.23		
	V_{IN}=0.4V_{rms}, 50KHz SIN		0.045		
	V_{IN}=0.4V_{rms}, 20KHz SIN		0.005		
	V_{IN}=0.4V_{rms}, 10KHz SIN calibration		-		
	V_{IN}=0.4V_{rms}, 50Hz SIN		0.07		
ACBUF Linearity Error	Gain=10				
(R_L=10MΩ, C_L=30pF)	V_{IN}=0.04V_{rms}, 20KHz SIN		4.3		%
	V_{IN}=0.04V_{rms}, 10KHz SIN		1.14		
	V_{IN}=0.04V_{rms}, 5KHz SIN		0.27		
	V_{IN}=0.04V_{rms}, 1KHz SIN calibration		-		
	V_{IN}=0.04V_{rms}, 50Hz SIN		0		
(R_L=10KΩ, C_L=30pF)	V_{IN}=0.04V_{rms}, 20KHz SIN		4.4		
	V_{IN}=0.04V_{rms}, 10KHz SIN		1.14		
	V_{IN}=0.04V_{rms}, 5KHz SIN		0.27		
	V_{IN}=0.04V_{rms}, 1KHz SIN calibration		-		
	V_{IN}=0.04V_{rms}, 50Hz SIN		0.05		
RCTOP Linearity Error	V_{IN}=0.2V_{rms}, 100Hz SIN calibration				
	V_{IN}=0.2V_{rms}, 10KHz SIN		2.5		%
Switch Resistance:					
SW1			240		Ω
SW2			700		
SW3			2K		
Parasitic Capacitance				12	pF
Digital Output High	I_{OUT}=-1mA		5		V
Digital Output Low	I_{OUT}=1mA		25		mV
Digital Input High					V
Digital Input Low					V

Note 1: If you wanna know OP-AMP Specifications, you can read attachment (1).

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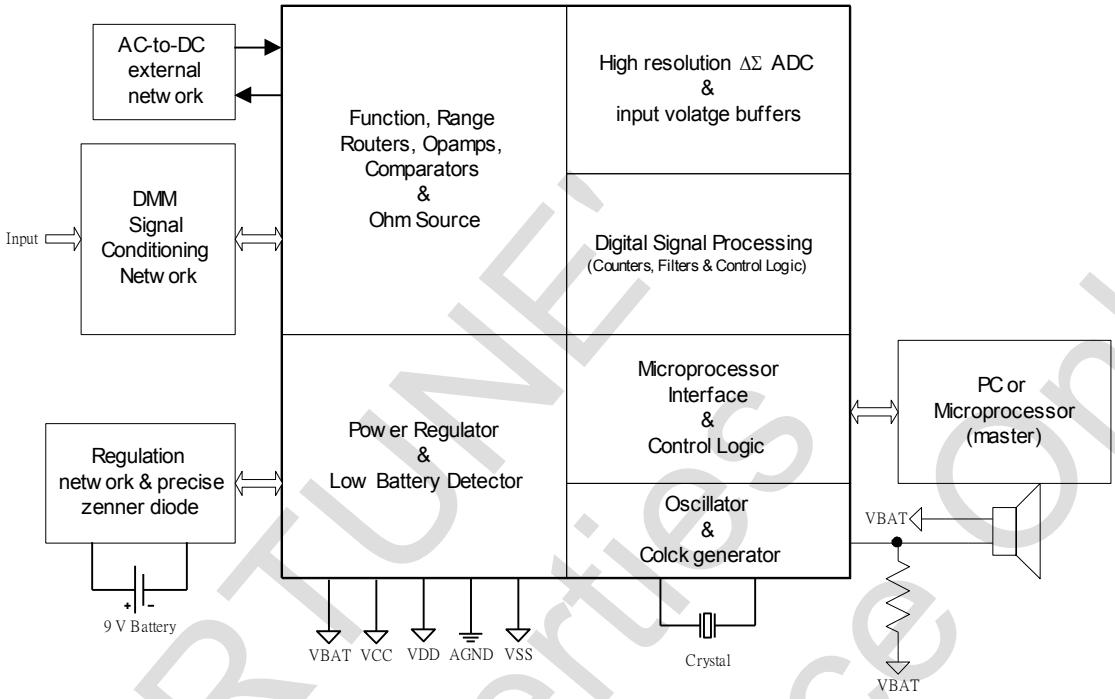
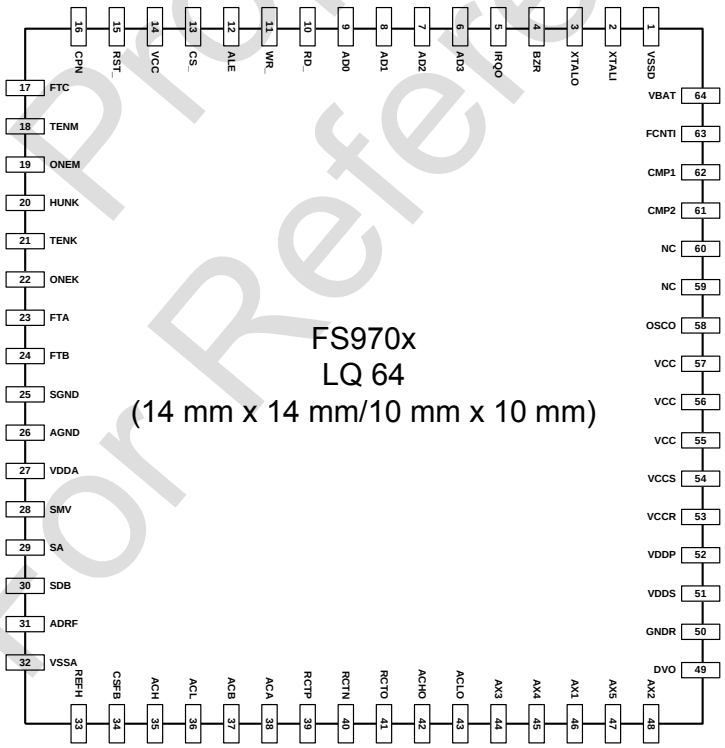
5. Block-diagram



6. Packaging & Pins

LQFP 64 Pin Definition



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Pin Description

64 PIN LQFP pin	Pin Type	Symbol	Description
1	DPI	VSSD	Global Ground（-3.2 V）.
2-3	DIO	XTALI,XTALO	The terminals of crystal oscillator circuit
4	DO	BZR	The Output terminal of BUZZER function
5	DO	IRQO	The Interrupt output terminal when updating data
6-9	DIO	AD<3:0>	The I/O ports of Address and Data Lines
10	DI	RD_	When Active_low, read values from FS970X
11	DI	WR_	When Active_low, write values to FS970X
12	DI	ALE	When Active_Hi, AD<3:0> acts as address line
13	DI	CS_	When Active_low, enable FS970X interface
14	DPI	VCC	Digital power supply（+1.8 V）
15	DI	RST_	Reset all the registers to “0” when Active_low
16	AIO	CPN	The connector of the compensation capacitor at ACV function
17	AIO	FTC	The terminal of pre-filter capacitor
18-22	AIO	TENM,ONEM,HUNK,TENK,ONEK	The terminal of resistors of router
23-24	AIO	FTA,FTB	The terminal of pre-filter capacitor
25	AI	SGND	The sensing point of analog ground
26	API	AGND	Analog ground（0 V）
27	API	VDDA	Positive analog power supply（+3.0 V）
28	AIO	SMV	The input of DCmV function
29	AIO	SA	The terminal of current function
30	AIO	SDB	The negative terminal of reference under resistance measurement
31	AI	ADRF	The input of the voltage reference of ADC
32	API	VSSA	Negative analog power supply（-3.2 V）.
33	AI	REFH	The output of Zener diode
34	AIO	CSFB	The terminal of Zener diode function
35-36	AIO	ACH, ACL	The output terminals of AC-to-DC function
37-38	AIO	ACB, ACA	The connection of AC buffer OPAMP
39-40	AIO	RCTP, RCTN	The terminal of OPAMP of AC-to-DC function
41	AIO	RCTO	The output terminal of OPAMP of AC-to-DC function
42-43	AIO	ACHO, ACLO	The output terminals of rectify function of AC-to-DC measurement
44-48	AIO	AX1-AX5	The input terminal of ADC
49	AO	DVO	The output terminal SDV through an analog switch control
50	APO	GNDR	The analog ground of internal voltage regulator (0 V).
51	PO	VDDS	The output terminal VDD through an analog switch control
52	PI	VDDP	The power supply of regulator (+3.0 V)
53	DPO	VCCR	The output of regulator（+1.8 V）
54	DPO	VCCS	The output terminal VCC through an analog switch control
55-57	DOI	VCC	Digital power supply（+1.8 V）
58	DO	OSCO	The output of crystal oscillator circuit (the output frequency can be programmable)
59-61		NC	No use.
62	DO	CMP1	The output of comparator
63	DI	FCNTI	The input terminal of frequency counter
64	P	VBAT	The terminal of battery

1) D – (Digital)
2) A – (Analog)
3) P – (Power)
4) O – (Output)
5) I – (Input)
6) For example, DIO stands for Digital Input and Output pin.

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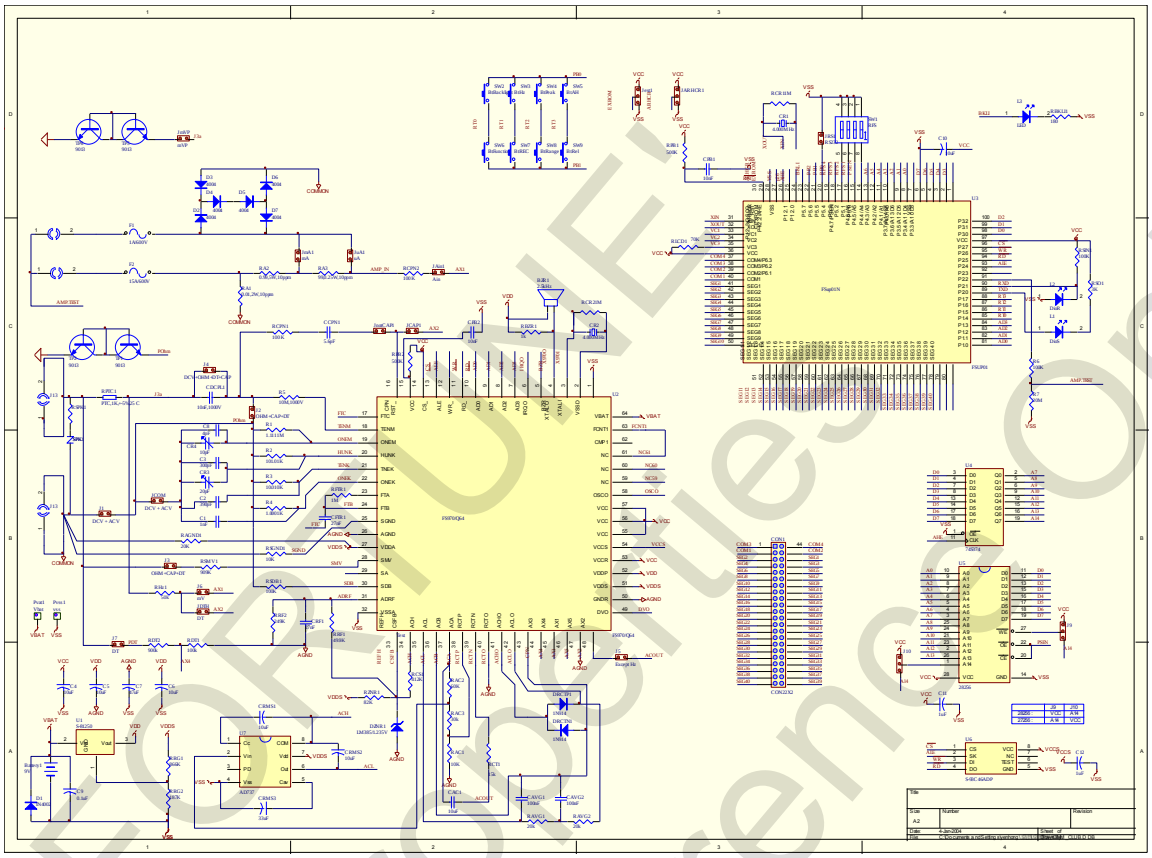
7. Typical Application Circuit



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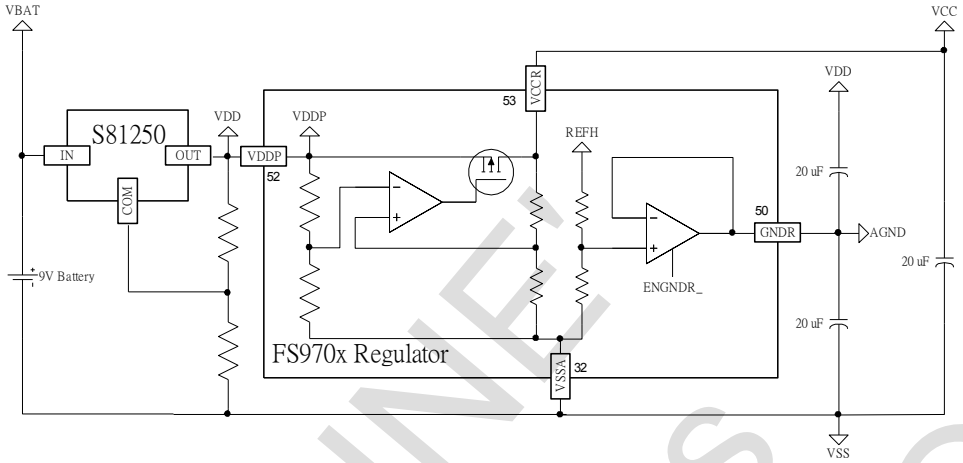
8. Regulator



Graph 1. FS970X Regulator Block-diagram

FS970X Regulator, as shown in Graph 1, needs to be connected with a S81250 low-cost regulator to convert the battery voltage above 6.8V to VDD voltage of approx. 6.3V. There are two functions of VDD power: one is the positive voltage (negative voltage to be VSSA) of analog circuit (or regulator), and the other is as the reference voltage of regulators.

The power of the digital circuit in the chip is supplied by VCC. The digital signal ground is VSSD. The digital signal ground VSSD and negative supply of analog circuit VSSA in the chip are connected by chip foundation of thousand ohms.

As shown in Graph 1, the FS970X regulator circuit refers respectively to the voltage of VDDP and REFH; at the same time, adjusting to the voltage of VCCR, GNDR and VSS to supply the chip. If VSS is set to be 0V, the voltage of VCCR and GNDR will be 5V and 3.2V. This analog supply can directly supply AD737 to enable the meter to measure the true root mean square of AC signal.

The supply source of FS970X can be selected by users, either from the chip itself or from external connection. The analog supply within the chip is provided by VDDA, AGND and VSSA. Thus, directly feeding the output of regulator VCCR, GNDR and VSS into VCC, AGND and VSSA will supply the chip itself. If the system has its own supply, it can be connected directly to VCC, AGND and VSSA, instead of using VCCR and GNDR.

The power consumption of analog is static DC current, with an equivalent DC power consumption. The major reason that will affect this DC power consumption is the change between each function. The power consumption of FS970X analog parts is designed to be under 1.2mA and the digital parts under 0.5mA.

To be even more stringent on power consumption design under saving mode, connecting the chip's analog supply VDDA to VDDS will reduce the idle VDDA consumption to 0 under saving mode. For details about VDDS, please see 5.3.

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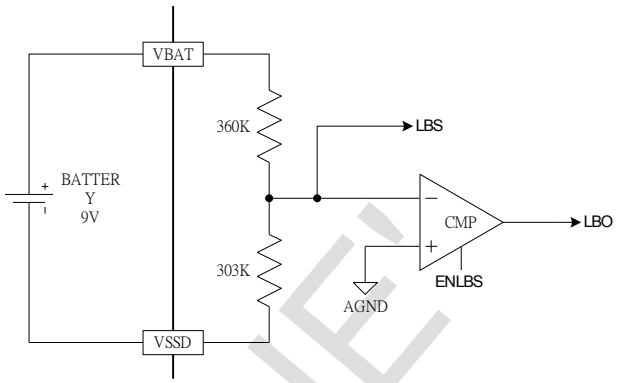
Low Voltage Detector



Graph 2 Low Voltage Detector

Low voltage detector is shown as Graph 2. After the voltage of VBAT is divided as LBS by resistor, it will flow into low voltage detector. The output of the detector is LBO, used to judge whether the battery voltage VBAT is lower than 6.8V. If it's lower than 6.8V, the output is "Hi", meaning that it needs a battery change. Before reading LBO, set ENLBS to "Hi". After approx. 0.1 ms, pull it back to "L" to read LBO.

The voltage of LBS can flow into ADC, controlled by ADC multiplexers. It can also be directly measured by ADC. The battery voltage is calculated as Formula 1.

Formula 1 ..... $V_{BAT} \approx \frac{17}{8} \times V_{LBS}$

Under saving mode, setting ENGNDR_ (MISC2<1>) to "H" will turn off GNDR in order to save power consumption.

Saving Mode

In FS970X, all the power-consumption related circuits, except for VCCR generator, can be turned off by FS970X registers to save power. The power-consumption related control signals and components are shown in Chart 2.

If all of the FS970X components are turned off, only VCCR regulator will still be running. This keeps the chip power consumption under 10 uA.

According to the setup in Chart 2, the power consumption of VDDA may drift. Therefore, aside from the setup procedures in Chart 2, the supply of VDDA should come from VDDS considering the saving mode. By doing so, S81250 will be the only component that consumes power under saving mode.

Register	Control circuit	Saving mode value	Related power consumption circuit
RGD>3:0>	MODE<3:0>	000x	Fixed voltage generator
SRF<7:6>	SOSR<1:0>	00	Ohm power supply
SCP<0>	CMPEN1	0	Comparator

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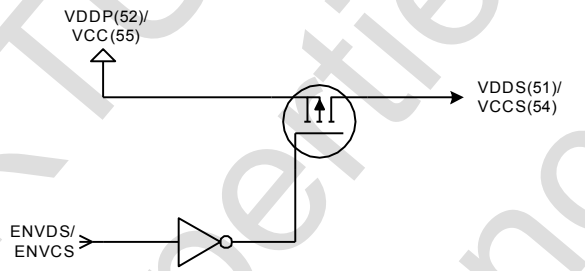
AFT<6>	RCTEN	0	Full-wave retifier
AFT<4>	ACEN	0	AC buffer
ADG<7>	ENAD	0	ADC
SETADC<7:6>	ENVDS, ENVCS	00	On/off power output
MISC1<4>	ENOSCO_	1	OSCO output
MISC1<3>	ENXTL_	1	Crystal oscillator circuit
MISC2<1>	ENGNDR_	1	AGND voltage regulator

Chart 2. Saving Mode Setup.

On/Off Power Output



Graph 3 On/Off power output.

VDDS and VCCS are the on/off power output of VDDP and VCC. The circuit is shown in Graph 3. VDDP/VCC flows into PMOS, output from VDDS/VCCS. PMOS on/off status is controlled by ENVDS/ ENVCS. When set under 0 and 1, PMOS is respectively under open/close status.

Connecting VDDA to VDDS under saving mode, this will decrease VDDA power consumption to 0.

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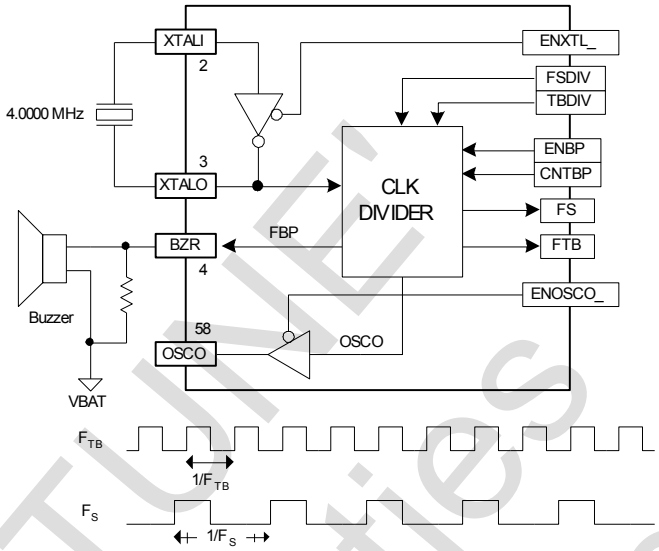
9. Clock and Buzzer Generator

Clock Generator



Graph 4 Clock Generator.

Clock generator is shown in Graph 4. It can be connected to a 4.000 MHz crystal oscillator to produce 4.000 MHz clock frequency. It can then be divided to FS, FTB, and FBP frequencies by a divider. Among these, FS is used by ADC. (please refer to 8.4 for details.) FTB is used by digital circuits, such as the reference frequency of frequency counter (please refer to section 9.1). FBP is used by buzzer to initiate buzzing.

FTB and FS are respectively controlled by ENXTAL_. TBDIV and FSDIV. The true value Chart is shown in Chart 3:

ENXTAL_	TBDIV	F_{TB}	FSDIV	F_S
L	L	1.0000 MHz	L	166.67 kHz
L	L	1.0000 MHz	H	83.33 kHz
L	H	125.0 kHz	L	166.67 kHz
L	H	125.0 kHz	H	83.33 kHz
H	X	0, (L)	X	0, (L)

Chart 3. FTB / FS generator true value Chart.

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Buzzer Generator

FBP generator is controlled by ENBP. CNTBP and CMP1. The true value Chart is shown in Chart 4.

ENBP	CNTBP	CMP1	F_{BP}
H	X	X	2.6 kHz
L	L	X	0, (L)
L	X	L	0, (L)
X	H	H	2.6 kHz

Chart 4. FBP true value Chart

The output of buzzer, BZR, is an open drain output. It can be connected to an external pull-up resistor to pull the “Hi” output to the required voltage. When ENBP is “Hi” or CMP1 and CNTBP are both “Hi”, BZR will produce approx. 2.6 kHz square-wave output to initiate buzzer. ENBP and CNTBP can be set up directly by digital interface while the value of CMP1 is related to the measurement status. Please refer to Function Network for details.

When ENOSCO_=0, the square-wave output of OSCO is fixed to be 2.000 MHz. When ENOSCO_=1,the fixed output is 0. This will save VCC power consumption.

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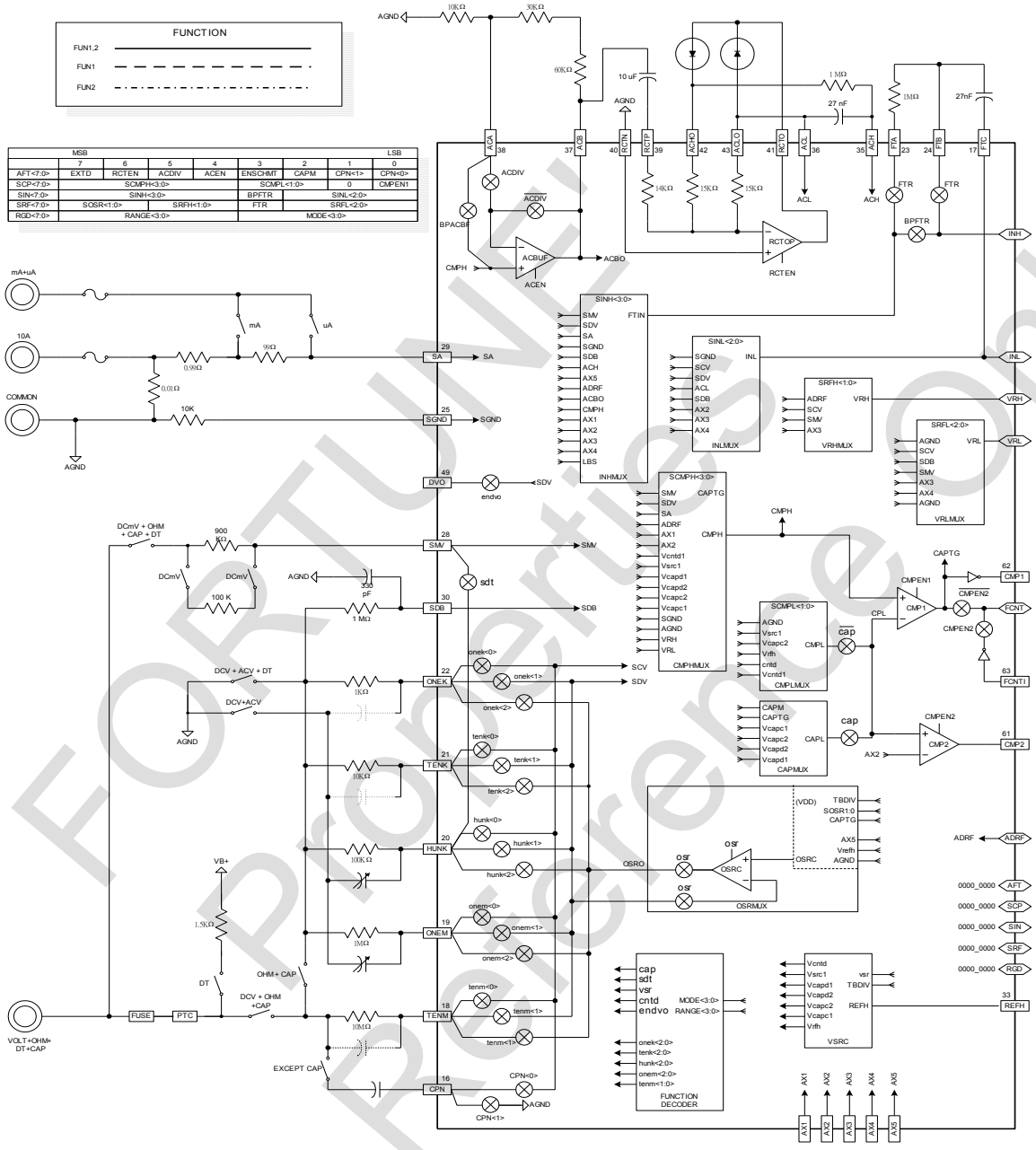
10. Function Network



Graph 5. FS970X function network diagram

Function Network, as shown in Graph 5, includes six major parts: function decoder, area network switch, fixed voltage generator, Ohm power supply, multiplexers and pre-filter, operation amplifier and comparator.

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Function Decoder

Function decoder includes two set of input – MODE and RANGE. RANGE controls area network switch to determine measurement range, and MODE controls the function network signal to determine measurement mode.

As shown in Chart 5, the setup of register MODE3:0 (represents MODE<3:0>) can decode the control signals such as cap. Sdt. Vsr. Cntd and endvo. It also controls the measurement mode and operation status of function network.

When High Bandwidth AC is capable of processing AC signal more than 1 MHz, SDV can be the direct output of SDV. Refer to section 7.5.1 for details.

Measurement Mode	MODE3:0	cap	sdt	vsr	cntd	endvo
DCmV, DCV, ACV, and PKH	0000	0	0	0	0	0
DIODE	0001	0	1	0	0	0
High Bandwidth AC	0011	0	0	1	0	1
Resistor x, Continuity	100x	0	0	1	1	0
Capacitor x	101x	1	0	1	0	0

Chart 5 Control of Measurement mode .

As shown in Chart 6, area network switch is controlled by both MODE3:0 and RANGE3:0. The four bits in RANGE directly controls network resistor path: 1k , 10k , 100k , and 1M At the same time, the path of 10M can be determined by

Formula 2 $$e = a + b + c + d = \bar{f}$$

Under Range Divider mode, area network becomes decay network. It controls area network on/off status to determine different measurement range according to the setup of RANGE3:0. Under Resistor mode, area network will become the reference resistor initiated by appropriate returned Ω supply. It selects different reference resistor to determine different measurement range according to the setup of RANGE3:0. Resistor I or II represent respectively whether reference resistor is parallel with the 10 MΩ resistor. Under Capacitor mode, area network becomes charge/discharge resistor with power supply. Capacitor I or II also represent whether charge/discharge resistor is parallel with 10 MΩ resistor.

Range Mode	MODE3:0	RANGE3:0	onek2:0	tenk2:0	hunk2:0	onem2:0	tenm1:0
Range Divider	00xx	abcd	0aa	0bb	0cc	0dd	0e
Resistor I	1000	abcd	aaa	Bbb	ccc	ddd	f1
Resistor II	1001	abcd	aaa	Bbb	ccc	ddd	ff
Capacitor I	1010	abcd	aaa	Bbb	ccc	ddd	f1
Capacitor II	1011	abcd	aaa	Bbb	ccc	ddd	ff

Chart 6 Decay network switch.

FORTUNE Properties For Reference Only

10..1 Area Network Switch

Combining area network switch to an external high-precision resistor becomes a measurement network. It transfers the signal of the sensor into suitable voltage range for ADC and measures the signal. The function decoder controls the measurement range and on/off status. See Graph 5 and Section 7.1 for details.

Take DC5V as an example, using Chart 6 as reference, setting MODE3:0=0000 and RANGE=0001 will make onek2:0=tenk2:0=hunk2:0=000, onem2:0=011, and tenm1:0=01. When corresponding this value to the area network of the low-left corner of Graph 5, all the switches are under open status except for tenm<0>, onem<1>, and onem<2>. Thus, connecting to an external resistor network will make up a ten-times decay circuit to achieve the decay function required by DC5V.

Fixed Voltage Generator

When under capacity measuring, short testing, and resistor measuring, all the required power supply is provided by this block.

The output of this block includes Vcntd, Vsrc1, Vcapd1, Vcapd2, Vcapc2, Vcapc1, and Vrfh. The output voltage is controlled by vsr and TBDIV, as shown below. Vsr comes from the decoding of MODE3:0 input by function decoder. TBDIV can be directly set up by register.

INPUT		OUTPUT						
vsr	TBDIV	Vrfh	Vcapc1	Vcapc2	Vcapd2	Vcapd1	Vsrc1	Vcntd
1	0	1.2 V	0.8 V	0.64 V	0.56 V	0.4 V	0.16 V	0.04 V
1	1	3.1 V	1.58 V	1.65 V	1.45 V	1.52 V	0.4 V	0.1 V
0	x	0 V	0 V	0 V	0 V	0 V	0 V	0 V

Chart 7. Voltage output of fixed voltage generator.

When TBDIV=0, the block refers to the voltage of REFH, as shown in Chart 7, REFH=1.2V. And if REFH = 0.6V, the voltage generated are 0.6V, 0.4 V, 0.32 V, 0.28 V, 0.2 V, 0.08 V, and 0.02 V. When TBDIV=1, it refers to the voltage of VDD, as shown in Chart 7, which is the voltage output of VDD voltage being 3.1 V under normal condition.

Vrfh is the reference voltage of ohm power supply when measuring resistance and capacity. Vcapc1 and Vcapd1 are respectively the reference voltage of charge/discharge comparator Vcapc1 (charging) and Vacpd1 (discharging) when measuring capacity. Vcapc2 and Vcapd2 are the second set of reference voltage of charge/discharge comparator. According to the measuring capacity range, one set of the reference voltage can be selected by CAPM setup of register. (See Chart 14 for details). Vcntd is the reference voltage of comparator under short testing. There is no special function of Vsrc1, users can customize it according to their needs.

FORTUNE Properties For Reference Only

Ω Power Supply

Ω power supply flows directly into decay network, providing voltage as shown in Chart 8. Among them, **cap** is determined by function decoder. When cap=0, it's not under capacity measuring mode. For DMM application, it represents resistance measurement. At this time, the output of Ω is controlled by SOSR1:0, as shown in Chart 8. SOSR1:0 can be set up by register.

When cap = 1, it's under capacity measuring mode. At this time, the output of Ωpower supply is irrelevant to SOSR1:0, but controlled by TBDIV and CAPTG. When TBDIV = 0, Vrfh is approx. 1.2 V, and the charge/discharge voltage is approx.1.2V. When TBDIV=1, Vrfh is approx. 3.1 V (VDD), and the charge/discharge voltage is also approx. 3.1 V. This improves the charge/discharge speed of capacity measuring. CAPTG is the output of comparator CMP1. It controls the charge/discharge selection of Ω power supply to the measuring capacity.

When output is VDD, theΩvoltage is the voltage on the pins, which will be affected by on/off resistors on the path so the real voltage of the load will be affected by the load.

When output is other than VDD, the on/off resistor can be ignored because operation amplifier is high gain and negative feedback. The real voltage of the load affected by the load can be ignored as well. Under all kinds of output, the maximum power is approx. ±1.2mA.

INPUT				OUTPUT
cap	TBDIV	CAPTG	SOSR1:0	OSRO
0	x	x	00	high impendence
0	x	x	01	AX5
0	x	x	10	Vrfh
0	x	x	11	VDD
1	0	0	Xx	Vrfh (REFH)
1	0	1	Xx	AGND
1	1	0	Xx	Vrfh (VDD)
1	1	1	Xx	AGND

Chart 8 Ω power supply true-value Chart

FORTUNE Properties For Reference Only

Multiplexers and pre-filter

Through multiplexers such as INHMUX, INLMUX, VRHMUX and VRLMUX, selectable ADC signals are FTIN, INL, VRH, and VRL. FTIN and INL first flow through a RC pre-filter, and then into full differential amplifier input INH and INL of ADC. At the same time, they can bypass the RC pre-filter and flow directly into ADC through BPFTR and FTR.

Each output path is directly controlled by registers. Details are shown in Chart 9, Chart 10, Chart 11 and Chart 12.

Name	SMV	SDV	SA	SGND	SDB	ACH	AX5	ADRF
SINH	0000	0001	0010	0011	0100	0101	0110	0111
Name	ACBO	CMPH	AX1	AX2	AX3	AX4	LBS	NA
SINH	1000	1001	1010	1011	1100	1101	1110	NA

Chart 9 FTIN multiplexers setup

Name	SGND	SCV	SDV	ACL	SDB	AX2	AX3	AX4
SINL	000	001	010	011	100	101	110	111

Chart 10 INL multiplexers setup.

Name	ADRF	SDV	SMV	AX3
SRFH	00	01	10	11

Chart 11 VRH multiplexers setup.

Name	AGND	SCV	SDB	SMV	AX3	AX4	AGND
SRFL	000	001	010	011	100	101	110

Chart 12 VRL multiplexers setup.

The signal into the comparator can be selected by comparator multiplexers – CMPMUX. The path is controlled by registers as well, as show below.

Name	SMV	SDV	SA	ADRF	AX1	AX2	Vcntd	Vsrc1
SCMPH	0000	0001	0010	0011	0100	0101	0110	0111
Name	Vcapd1	Vcapd2	Vcapc2	Vcapc1	SGND	AGND	VRH	VRL
SCMPH	1000	1001	1010	1011	1100	1101	1110	1111

Chart 13 CMPH multiplexers setup.

FORTUNE Properties For Reference Only

CPL is the negative input of CMP1, controlled by cap, cntd, SCMPL1:0, CAPM, and CAPTG. Details are shown in Chart 14.

When cap=0 and cntd=0, the output of CPL is irrelevant to CAPM and CAPTG. It is directly selected by SCMPL1:0.

When cap=0 and cntd=1, it's under short testing mode. The output of CPL is fixed to be Vcntd.

When cap=1, it's under capacitor measuring mode. At this time, the output of CPL is irrelevant to cntd and SCMPL1:0. When CAPM=0, it means low and medium capacity measuring. The output of CPL is controlled by CAPTG; they are Vcapc1 and Vcapd1. When CAPM=1, it means high capacity measuring. The output of CPL is controlled by CAPTG. They are Vcapc2 and Vcapd2.

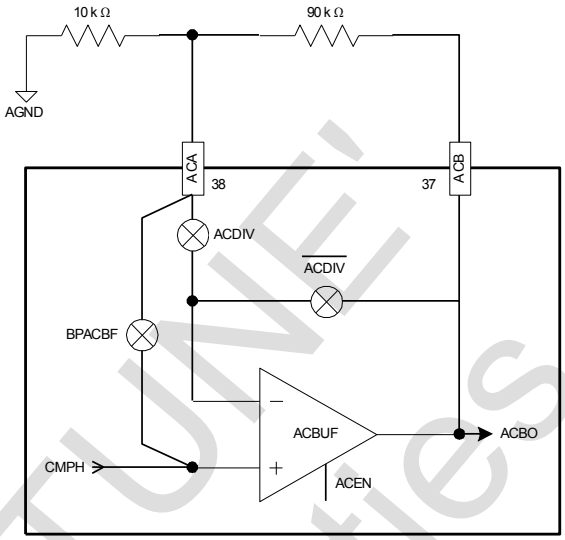
I N P U T	cap	0	0	0	0	0	1	1	1	1
	cntd	0	0	0	0	1	x	x	X	x
	SCMPL1:0	00	01	10	11	xx	xx	xx	Xx	xx
	CAPM	x	x	X	x	x	0	0	1	1
	CAPTG	x	x	X	x	x	0	1	0	1
OUTPUT	CPL	AGND	Vsrc1	Vcapc2	Vrfh	Vcntd	Vcapc1	Vcapd1	Vcapc2	Vcapd2

Chart 14 CPL multiplexers setup.

FORTUNE Properties For Reference Only

Operation Amplifier and Comparator

The block composed by operation amplifier and comparator include AC buffer block, full-wave rectifiers block, and comparator block.



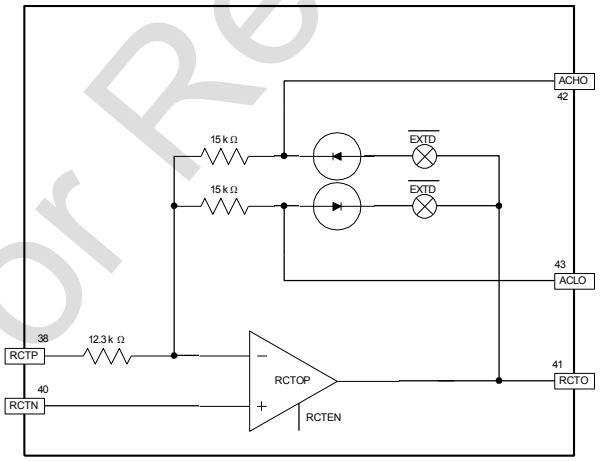
Graph 6. AC buffer block.

As shown in Graph 6, buffer block is controlled by ACBUF and ACDIV. It becomes a gain network when connecting with an external resistor. Whether ACBUF works or not can be directly controlled by ACEN. When ACEN=0, it turns off the buffer and the output becomes high impedance.

Signal enters through CMPH, and flows out from ACBO or the 37th pin ACB. ACDIV can at the same time controls the gain. If ACDIV=0, the gain of the buffer is 1. If ACDIV=1, the gain of the buffer is determined by the external network resistor. In Typical Application Circuit, the gain becomes 10.

When the gain is 1, the 100 kHz side wave flowing through the buffer will be reduced to lower than 0.5%. The bandwidth of AC is limited by the frequency response of full-wave rectifier.

If the signal bandwidth is higher than100 kHz, let BPACBF=1, it will change the output source to the 38th pin (ACA) instead of AC buffer.

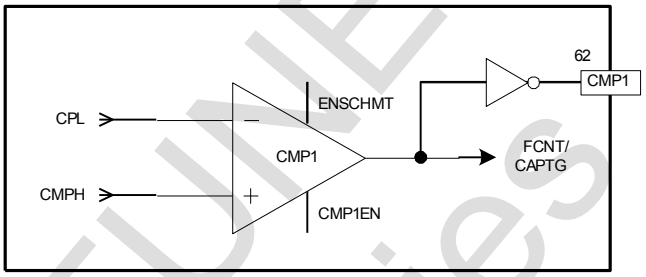


Graph 7. Full-wave rectifier switch block

FORTUNE Properties For Reference Only

As shown in Graph 7, the AC signal, inputting from RCTP and going through the rectifier, will obtain a full differential amplifier signal from ACHO and ACLO. It will then be connected to an external RC low-pass filter network to do the arithmetic average. The result value, a absolute average AC/DC voltage, then flows into ADC and displays.

The full-wave rectifier of FS970X has built in the required resistor. And the rectifier diode is controlled by EXTD to select built-in or externally connected. When EXTD=0, it means that the bandwidth of the built-in diode is 3kHz under precision of 1%. When EXTD=1, it means that the bandwidth of the external diode using 1N914 is 10kHz under precision of 1%. It can increases the bandwidth of the rectifier if using faster diode or adding a high-frequency compensation circuitry of full-wave rectifier. The enable capability of the rectifier is controlled by RCTEN. When RCTEN is Lo, turning off the operation amplifier will save power consumption.



Graph 8. Comparator Block-diagram.

As shown in Graph 8, comparator CMP1 can directly set the enable action of control register CMPEN1. And the Schmidt trigger function of the comparator can be selected by enable ENSCHMT. When ENSCHMT=0, the comparator has no delay, suitable for capacity measurement. When ENSCHMT=1, the comparator has the delay voltage of approx. $0.1V_{RMS,}$ suitable for frequency measurement.

The negative input is CPL, as shown in Chart 14. The positive input is CMPH, as shown in Chart 13. The output flows directly into frequency counter through FCNT or controls the charge/discharge function of capacity measurement by CAPTG (as shown in Chart 14)It can also be transferred through Pin 62 (SMP 1)by a reverser or the logic value can be obtained by the control register. (as shown Chart 18).

10..1 Bandwidth of AC Signal

According to section 7.5，When providing appropriate frequency compensation to decay network, FS970X chip can directly process the AC signal under the frequency of approx. 100 kHz.

If the bandwidth of AC signal is over 100 kH, the AD buffer ACBUF of FS970X will be unable to process. Thus, setting BPACBF=1, the high-frequency signal will bypass the AC buffer, and flow out directly from ACA, as shown in the upper left corner of Graph .

However, when the bandwidth of the signal is higher than 1 MHz, if the signal flows from SDV, through CMPHMUX to ACA, the on/off resistor and parastic capact on the path will decay the high-frequency signal dramatically, causing problems to frequency response.

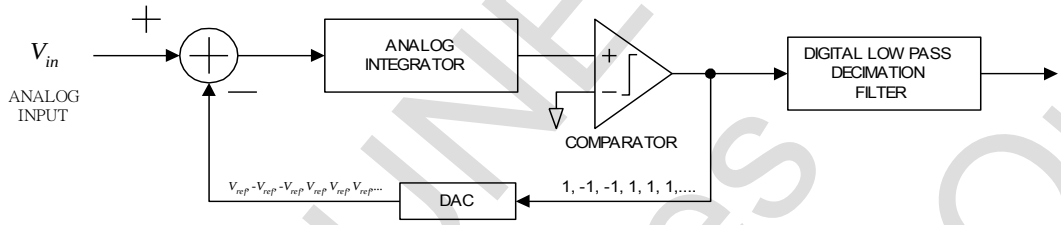
Therefore, when processing AC signal higher than 1 MHz, setting MODE3:0=0011 will make endvo=1. At this time, the signal of SDV, through the CMOS switch controlled by endvo, flows directly out from DVO, as shown in the upper left corner of Graph 5.

FORTUNE Properties For Reference Only

11. Analog to Digital Converter (ADC)

The operating theory of Σ-Δ ADC

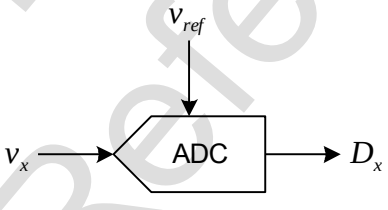
This high-resolution ADC adapts the modulation of delta and sigma. It samples the consecutive analog input signal by the sampling frequency of far higher frequency width input signal. It will then be converted into one-bit code by the modulation of delta and sigma. It then filters the high-frequency noise of Σ-Δ converter by the digital filter in the chip. It becomes high-resolution digital coding to be applied in high-resolution DMM. Besides, this kind of converter only performs a 1-bit transfer on the analog-end; therefore, it's with better linear characteristics. The signal input and reference voltage input will be full differential amplifier input, with good CMRR, which can reject the common mode signal.



Graph 9. Σ-Δ ADC concept diagram.

As shown in Graph 9, Σ-Δ ADC includes an analog differentor , an integrator, and a comparator, a one-bit ADC and a digital low-pass filter. The analog input signal is taken from the consecutively sampled input, and deduct it directly from the expected voltage. The difference will then flow into analog integrator, then product a predicted digital by the comparator. It will then be converted to the expected voltage（$+V_{ref}$ or $-V_{ref}$ ）by ADC, reversely feed in to the integrator to get a stable negative feedback. The integrator has unlimited gain to DC; therefore, if the speed of change of input signal is far smaller than the speed of sampling, the average of the expected voltage signal of theΣ-Δ converter will be very close to the input signal. It's considered equivalent under certain resolution. Thus, the one-bit digital converted from the comparator is equal to the analog signal value $\pm V_{ref.}$ Therefore, take the one-bit digital and perform an arithmetical average by the digital filter to get a high-resolution Σ-Δ digital.

Transfer Function & Non-ideal affect



Graph10. ADC.

As shown in Graph 10, there are two sets of input and one set of output in ADC – voltage input v_x , reference voltage input v_{ref} , and ADC output D_x . The ideal transfer function is:

Formula 3..... $$D_x = G' \times \frac{v_x}{v_{ref}}$$

G' represents the gain value of the ADC.

However, the ADC in reality is not ideal. The relationship is:

Formula 4 ..... $$D_x = G' \times \frac{v_x + v_{os}}{v_{ref}} = G' \times \frac{v_x}{v_{ref}} + G' \times \frac{v_{os}}{v_{ref}}$$

FORTUNE Properties For Reference Only

$G^{'}$ and v_{os} represent respectively the gain and the offset voltage of ADC. They can both be affected during manufacturing, and vary every single chip

Under most of the applications of ADC, reference voltage is a fixed value V_{rrf}. ADC converts the variable voltage v_x into an equivalent value as V_{rrf}. Examples are AC/DC voltage measurement and AC/DC currency measurement of DMM. In this kind of application, reference voltage is fixed; thus, Formula 4 can be simplified as:

Formula 5..... $$D_x = G^{'} \times \frac{v_x}{V_{ref}} + D_{os}$$

D_{os} is a fixed value.

However, in the application of DMM, the most often used type of measurement of resistor is scale-type measurement. The reference voltage v_{ref} will vary with resistor, not a fixed value. Formula 5 will not reflect the actual situation, and needs to be modified as:

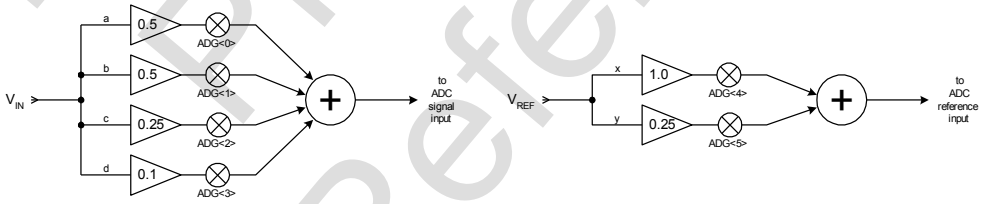
Formula 6.....

$$D_x = G^{'} \frac{v_x}{v_{ref}} + D_{os}(v_{ref}) = G^{'} \times \frac{R_x}{R_{ref}} + D_{os}(R_x)$$

Whereas, $D_{os}(v_{ref})$ is the function of reference voltage. In the application of the measurement of scale-type resistors, we will learn that $D_{os}(R_x)$ is related to resistor R_x.

FS970X includes two kinds of ADC output: high-resolution, low-speed and low-resolution, high-speed. Under high-resolution, low-speed output, the offset voltage has been eliminated. Its transfer function converts from the ideal linear from Formula 3. Under low-resolution, high-speed output, the offset voltage still exists. The transfer function comes from either Formula 5 or Formula 6, according to different condition. See Chapter 8 for details.

Function Gain Setup



Graph 11. FS970X Gain setup.

As shown in Graph 11, the input of FS970X ADC includes four different gain paths. They are independently controlled by ADG<3:0> (4 bits) of the register. The input of reference voltage includes two different gain paths. They are independently controlled by ADG<5:4>(2 bits) of the register. All the gain values are approximation. Precise gain values are only available after calibration.

FORTUNE Properties For Reference Only

With suitable gain option control, all kinds of measurement can be applied to the best dynamic range of ADC. Chart 15 shows the setup of three typical functions and ADG<5:0> in the application of DMM.

	1st function	2nd function	3rd function
ADG<5:0>	01_0011	11_0111	11_1000
Reference voltage gain (G_{REFi})	×1.0	×1.25	×1.25
Input voltage gain (G_{SIGi})	×1.0	×1.25	×0.1

Chart 15 970x Typical ADC function setup.

The measurement transfer functions of each function is:

Formula 7
$$D_x = \frac{G_{SIGi}}{G_{REFi}} \times \frac{v_x}{v_{ref}}$$

The reference voltage of each function and the gain approximation of the input voltage are shown in Chart 15. The actual precise gain value and offset voltage should be obtained from calibration.

Digital Filter

As shown in Graph 9, the 1-bit output from the comparator must go through a digital low-pass filter and perform calculation similar to arithmetic average to become a high-resolution multi-bit resolution. The transfer function of digital filter used by 970x is:

Formula 8
$$\left|H(f)\right| = \frac{1}{N^2}\left(\frac{\sin(N\pi f / f_S)}{\sin(\pi f / f_S)}\right)^2$$

Whereas, N is the number of the filter (TAP).

Assuming the sampling frequency of the ADC is 166kHz and the number of the filter is 16600, the frequency response Graph of the filter is shown as Graph 9. The first zero-point would be found at:

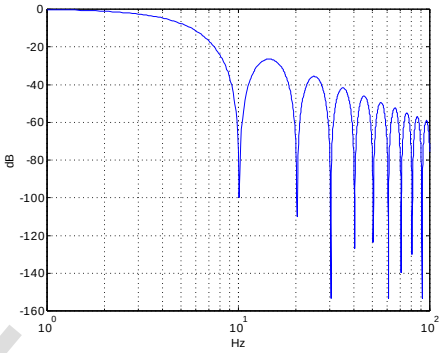
Formula 9
$$f_{Z1} = \frac{f_S}{N} = \frac{166000\ \text{Hz}}{16600} = 10\ \text{Hz}$$

Thereafter, all the integer multiple points of the first zero-point occur zero-point. The signal around the zero-point will be completely filtered out by the filter. So the frequency responses as shown in Graph 12, all have good suppressing effect to the noise of 50 Hz and 60 Hz. By the same token, assuming the sampling frequency is 83kHz, and the number of the filter is still 16600, then, the first zero-point position can be calculated as 5 Hz.

FORTUNE Properties For Reference Only

There are two this kind of programmable digital filters in FS970X, namely, COMB1 and COMB2. Their output is SUM1 and SUM2 respectively. The number of COMB1is higher, often used to measure high resolution. And the number of COMB2 is lower; its high-speed, low-resolution output can be used on peak-hold sampling and analog bar graph.

The numbers of COMB1 and COMB2 are both programmable. They can be set by TPS1 and TPS2 respectively, as shown in Chart 16. Taking the sampling frequency of 166.7 kHz as an example, the location of the first zero-point is calculated as Chart 17.



● Graph 12、Digital filter frequency response of 970x

The actual resolution of each status is defined by the actual measurement.

	COMB1（TPS1）		COMB2（TPS2）	
TPSX<1:0>	Number（N）	1st 0-point frequency（Hz）	Number（N）	1st 0-point frequency（Hz）
11	16384	10.17	256	651.17
10	8192	20.34	128	1302.34
01	4096	40.68	64	2604.68
00	2048	81.40	32	5209.38

Chart 16. Digital Filter number setup and 1st zero-point location（F_S=166.7 kHz）.

Because of the delay of the digital filter, the bandwidth of the signal pulse needs to be greater than four-times output period of the input signal of ADC. For example, when set TPS2 to 00, the output period of COMB2 will be:

Formula 10..... $\frac{1}{5209}\sec = 192\,\text{us}$.

Therefore, the pulse bandwidth of the input signal must be greater than $4 \times 192\,\text{us} = 0.769\,\text{ms}$ so that the value can be effectively converted by ADC. When the sampling frequency (FS) is 166.7 kHz, the output reading of SUM2 from COMB2 can detect to the smallest pulse bandwidth and TPS2, as shown in Chart 17.

TPS2<1:0>	00	01	10	11
Output frequency	5.2 kHz	2.6 kHz	1.3 kHz	0.65 kHz
Detectable smallest pulse bandwidth	0.769 ms	1.53 ms	3.06 ms	6.12 ms

Chart 17. The relationship between detectable smallest pulse bandwidth and TPS2.

FORTUNE Properties For Reference Only

Reading and operation of ADC

As described in 8.2, the circuitry of FS970X ADC might drift and causes an offset voltage because of manufacturing process. This might cause variance to the reading of ADC. To eliminate the offset variance, it's necessary to change the setup CYS<1:0> of register SETADC. There are three different working modes. These modes influence the reading and operation of high-resolution and low-resolution. They are described as below:

11..1 High-resolution, low-speed output

When CYS<1:0>=00, the input of ADC becomes short; then, we can read the negative value of offset voltage of ADC from SUM1.

When CYS<1:0>=11, the equivalent digit value of the voltage can be read from SUM1, as shown in Formula 5.

When CYS<1:0>=01, then, the reading value of SUM1 is equal to the ideal reading of linear ADC of the voltage. Its transfer function is shown as Formula 3. It can be used for all the measurement for high resolution.

When CYS<1:0>≠01, the output frequency of SUM1is the first zero-point frequency f_{Z1} of COMB1, as shown in Formula 9. When CYS<1:0> =01, the output frequency equals $f_{Z1}/2$.

11..2 Low-resolution, high-speed output

When CYS<1:0>=00, the input of ADC becomes short; then, we can read the negative value of offset voltage of ADC from SUM2. It can be used D_{os} self-calibration.

When CYS<1:0>=11, the equivalent digit value of the voltage can be read from SUM2, as shown in Formula 5. It can be used for peak-hold sampling measurement.

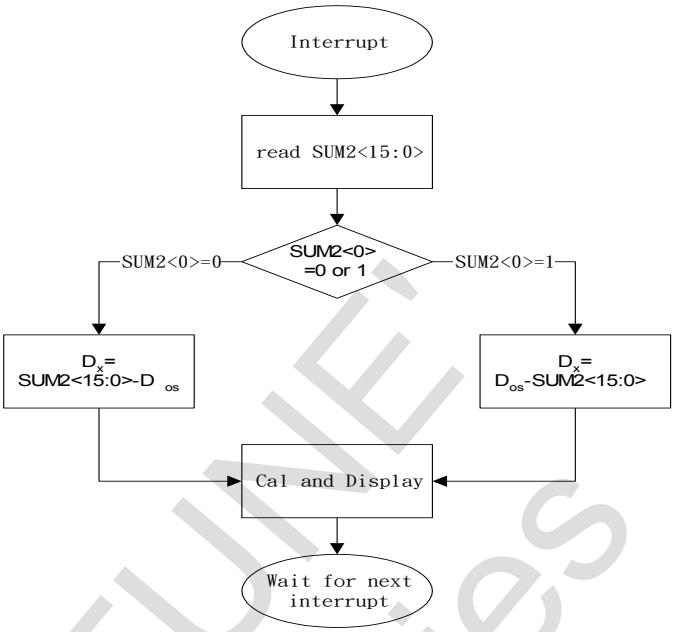
When CYS<1:0>=01, the transfer function of low resolution output SUM2 should become (a revision from Formula 5)

Formula 9.....

$$SUM2 = \left(G^{'} \times \frac{v_x}{V_{ref}} + D_{os} \right) \cdot \overline{SUM2<0>} + \left(D_{os} - G^{'} \times \frac{v_x}{V_{ref}} \right) \cdot SUM2<0>$$

The value of D_{os} can be read from SUM2 when power-on or turning the rotary, set CYS<1:0>=00. Therefore, the flow-Chart of operation and display of fast ADC output is shown as Graph 13. Whereas, D_x is the ideal ADC values of non-offset voltage, calculated from SUM2. It can be used for Bargraph display of all kinds of high resolution measurement.

FORTUNE Properties For Reference Only



Graph 13. The flow-Chart of operation and display of fast ADC output.

The output frequency of fast ADC is the same as the first zero-point frequency of COMB2. When sampling frequency f_S =166 kHz, if set TPS2<1:0>=11, then, the output frequency will be about 650 Hz.

11..3 Scale-type resistance measurement and Analog Bargraph

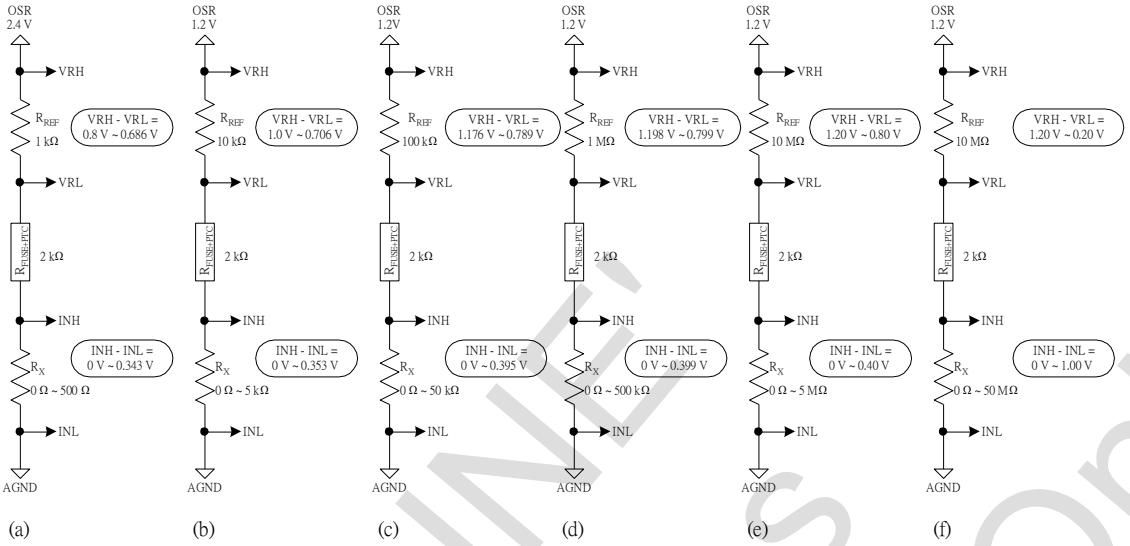
FS970X is equipped with fast ADC output SUM2. In the application of DMM, it can be used for Analog Bargraph display.

However, as shown in Formula 6, when performing the scale-type resistor measurement, the reference voltage of feeding ADC is no longer a constant value. Thus, the equivalent digital value D_{os} of the offset voltage is no longer a constant value, either. It varies with resistor. The method of deduction of D_{os} when performing the calculation, as described in Section 8.5.2, is no longer adequate.

As shown in Graph 14, the reference voltage below 5 MΩ varies between the range of 0.8 V~1.2 V. According to Formula 4, the D_{os} will vary dramatically, and cause problems to the Analog Bargraph.

Generally speaking, the Analog Bargraph display is approx. 50 digits. The accuracy requirement is not strict; thus, the problem can be solved by using section approximation. That is to say, when measuring the resistor, the operation of the Analog Bargraph can be processed under the following three conditions:

FORTUNE Properties For Reference Only



Graph 14. The converting voltage range of scale-type resistor measurement.

The 1st condition is low resistance under 5 kΩ. The D_{os} can be obtained by setting the reference voltage equivalent to 0.8 V. The 0.8 V can be generated by the fixed voltage generator in the chip. (as shown in Chart 7), through ACBUF output, connecting to AX3 and then into VRH. Or obtained through ACBUF, connecting to AX5, through Ωpower supply, and returning to VRH.

The 2nd condition is middle resistance between 50 kΩ ~ 5 MΩ. The D_{os} can be obtained by setting the reference voltage equivalent to 1.0 V. Under this condition, the D_{os} value, just like the other measuring D_{os} value, can be processed by the same parameter.

The 3rd condition is high resistance – 50 MΩ. Because the various range of the reference voltage is too great, the value of D_{os} can be easily use an approximate number. Therefore it can be obtained by reducing the Bargrapg display speed and using the reading of the high resolution output, or reduce the digit of the Bargraph to 10 or 20 digit.

By using the method illustrated in this section to set the reference voltage between 0.8 V and 1.0V when cut in the resistor file and calibrate the D_{os} of under 5 kΩ and 50 kΩ ~ 5 MΩ respectively. According to different measurement range to select different D_{os} . Then using the calculation shown in 8.5.2, we can complete the calculation of 50 digit of fast Bargraph display.

The Conversion of Digital Output & Equivalent Voltage

Take the high resolution digital output of FS970X, the output, SUM1<23:0>, is the compensation value of 2/24bits. Whereas, SUM1<23> is the symbol bit – "0" = positive, and "1" = negative. The floating point locates between SUM1<22> and SUM1<21>.

Assuming SUM1<23:0>=0010_1000_0000_0000_0000_0000, the equivalent floating point calculation is:

Formula 10

$$\begin{aligned} SUM1 &= 00.10\_1000\_0000\_0000\_0000\_0000 \\ &= 1\times 2^{-1} + 0\times 2^{-2} + 1\times 2^{-3} + 0\times 2^{-4} + 0\times 2^{-5} + \ldots\ldots + 0\times 2^{-22} \\ &= 0.5 + 0.125 = 0.625 \end{aligned}$$

Assuming SUM1<23:0>=1101_1111_1111_1111_1111_1111, the equivalent floating point calculation is:

FORTUNE Properties For Reference Only

Formula 11

$$\begin{aligned} SUM1 &= 11.01\_1111\_1111\_1111\_1111\_1111 \\ &= -(00.10\_0000\_0000\_0000\_0000\_0001) \\ &= -(1\times 2^{-1}+0\times 2^{-2}+0\times 2^{-3}+0\times 2^{-4}+.....+1\times 2^{-22} \\ &= -0.5000002384 \end{aligned}$$

As shown in Formula 3, when the gain $G^{'}$ equals the ideal value 1, the reference voltage V_{ref} equals 1.00000V. From the reading of ADC 0010_1000_0000_0000_0000_000, the voltage can be calculated as:

$$v_x = \frac{V_{ref}}{G^{'}} \times D_x = \frac{1.00000\ \mathrm{V}}{1} \times 0.625 = 0.62500\ \mathrm{V}.$$

When the reading of ADC is 1101_1111_1111_1111_1111_1111, the voltage can be calculated as:

$$v_x = \frac{V_{ref}}{G^{'}} \times D_x = \frac{1.00000\ \mathrm{V}}{1} \times -0.5000002384 = -0.50000\ \mathrm{V}.$$

However, in reality, the $G^{'}$ value affected by the drifting of the process, will not equal to 1.It will vary approx. $\pm 1\%$. At the same time, the reference voltage V_{ref}, affected by the reference power and dividing resistance, will not equal to 1.00000V. Therefore, the gain variances from the components have to be calibrated.

The different output code of different models

FS970X chip series has three models with different resolution, 5,000 digits, 20,000 digits, and 50,000 digits. The digit output codes are as follows:

In the 5,000 digits or 50,000 digits models, when the absolute value of SUM1, and the SUM1<21:18> is greater than 1010, then, the SUM1<21:18>will saturate to 1111. And the equivalent voltage of SUM1<21:18>=1010 will be approx. 0.625V.

In the 20,000 model, when the absolute value of SUM1, and the SUM1<21:18> is greater than 0101, then, the SUM1<21:18>will saturate to 1111. And the equivalent voltage of SUM1<21:18>=1010 will be approx. 0.3125V.

In the 5,000 digit model, the digital output of SUM1<5:1> is a constant 00000.

Other Control setting

ENAD(ADG<7>) is the enabling signal of ADC. It turns on the ADC when value =1, and turns off the ADC when value=0. It saves the power consumption setting the value to 0.

12. Digital Signal Process

Except digital filter, the digital signal process of FS970X includes frequency counter and peak-hold sampling process.

Frequency counter

The frequency counter of FS970X is composed of time-based counter and signal counter. The physical value of the target can be calculated from these two counters. The physical values of the target have signal frequency and duty cycle. It is determined by the DTON. It performs the frequency counter when setting it as “Lo” and performs duty cycle measurement when setting to as “Hi”.

When performing the frequency counter measurement, it needs the reference time pulse signal FTB, as shown

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in Graph 4. The frequency of the target can be obtained from the following formula:

Formula 12

$$F_{INSIG} = \frac{K_{SG}}{K_{TB}} \times F_{TB}$$

Whereas K_{SG} and K_{TB} are the values of signal counter and time-based counter respectively. F_{TB} is the frequency of reference signal, as shown in Chart 3. F_{INSIG} is the frequency of the target signal.

When performing the duty cycle measurement, the relationship between the duty cycle DT_{INSIG} and K_{SG} 和 K_{TB} is as follow:

Formula 13

$$DT_{INSIG} = \frac{K_{DT}}{K_{TB}} \times 100\%$$

You may have noticed that the value is independent from the reference time pulse frequency.

The reading process of frequency counter

Both controls of frequency measurement and duty cycle measurement are the motion of the frequency counter through FQRST_. When first setting FQRST_ to 0, and then resetting it to 1, it will trigger the action of frequency counter. It will complete the counting in approx. 0.2 seconds. It will also advice the microprocessor to read. After the reading of KTB and KSG, the value can be calculated from Formula 12 or Formula 13. Then, repeat the reset to get the new value of the next measurement, and so forth and so on.

However, whether processed by the interrupt or polling after the reset of the counter, the interrupt status bit is set to 1, meaning the counting is completed. However, when using the frequency counter of FS970X chip, and when entering the counter measurement, after the first reset, it should read the values of KTB and KSG. It doesn't need to process the values. Thereafter, it starts the reading process of the interrupt status bits.

Peak-hold sampling process

As shown in the Chart 17, the reading of the output value of fast ADC meets the requirement of positive negative peak-hold of pulse bandwidth measuring in a matter of naro-second. The peak-hold sampling logic of FS970X accepts the control of PKHRST. It uses the SUM 2 as an input. It composed of the positive-negative peak-hold comparison device and the positive-negative peak-hold register.

When PKHRST_ equals 0, the positive peak-hold register (POSPK) and the negative peak-hold register (NEGPK) will be reset to the most negative and positive value respectively.

When PKHRST is set to Hi, the digit comparison device will compare the value of SUM2 with the value of the positive peak-hold register (POSPK) and the negative peak-hold register (NEGPK). When the value of SUM2 is greater than the value of the positive peak-hold register, the value of the positive peak-hold register will be updated, otherwise it will remain the same. When the value of SUM2 is smaller than the value of the negative peak-hold register, the value of the negative peak-hold register will be updated, otherwise it will remain the same.

Therefore, after resetting the peak-hold sampling logic, set PKHRST_ equal 1, and the interrupt status digit of the peak-hold sampling to 1; then, read the values of POSPK and NEGPK registers. One can obtain the values of the measuring of positive peak-hold and negative peak-hold values.

Because the value of the peak-hold sampling device is derived from the value of SUM2, one should use Formula 5 to calculate the equivalent voltage value of the operator.

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13. Microprocessor interface

970x can directly connect to any microprocessor by CS_. WR_. RD_. ALE. AD3. AD2. AD1. AD0, and IRQO pins. It can also control read / write functions of registers, and handle interrupt.

Control register

The control registers are all 8-bit register, input-output port and for microprocessor to read and write. And the control register will be reset to the initial value of 0 when connecting to the RST_ pin of the chip.

The primary function of the control register is to provide the microprocessor to write to the control setting of the chip. Hence, it controls all the action of the chip. It can also read the value and for the use of detection.

		MSB								LSB
Block	Address	Name	7	6	5	4	3	2	1	0
Router	00	RGD<7:0>	RANGE<3:0>				MODE<3:0>			
	01	SIN<7:0>	SINH<3:0>				BPFTR	SINL<2:0>		
	02	SRF<7:0>	SOSR<1:0>		SRFH<1:0>		FTR	SRFL<2:0>		
	03	SCP<7:0>	SCMPH<3:0>				SCMPL<1:0>		CMPEN2	CMPEN1
	04	AFT<7:0>	EXTD	RCTEN	ACDIV	ACEN	ENSCHMT	CAPM	CPN<1>	CPN<0>
ADC	05	ADG<7:0>	ENAD	CPVR	ADG<5:0>					
	06	SETADC	ENVDS	ENVCS	CYS<1:0>		TPS2<1:0>		TPS1<1:0>	
MISC	07	MISC1<7:0>	ENBP	FSDIV	TBDIV	ENOSCO_	ENXTL_	DTON	FQRST_	PKHRST_
	08	MISC2<7:0>	ENCP_	CMP2	CMP1	LBO	CNTBP	BPACBF	ENGNDR_	ENLBS
INT	09	INTRG<7:0>	INSTA<3:0>				INTEN<3:0>			

Chart 18 . The corresponding address table of all control and interrupt register of the chip.

There are, in total, nine (9) 00~08 addresses of control line or register; as shown in Chart 18. The functions of each address are briefly illustrated in the Chart 19.

Register	Function	Reference
RGD<7>0>	Controls the on/off status of the measurement mode and decay network of function network	As described in Section 7.1
SIN<7:0>	Controls the path and the pre-filter of signal input amplifier of ADC	Chart 9 and Chart 10
SRF<5:0>	Controls the path and the pre-filter of reference voltage of ADC	Chart 11 and Chart 12
SRF<7:6>	Output option of Ω power supply	Chart 8
SCP<7:0>	Controls the path & enable control of the multiplexers at the front-end of comparator	Chart 13 and Chart 14
AFT<7:0>	The enable control of on/off status & operation amplifier in some function networks	Graph 5
AFT<3>	When ENSCHMT = 1, the Schmidt trigger function of enable comparator	Section 7.5
ADG<5:0>	The gain setting of ADC input	Section 8.3

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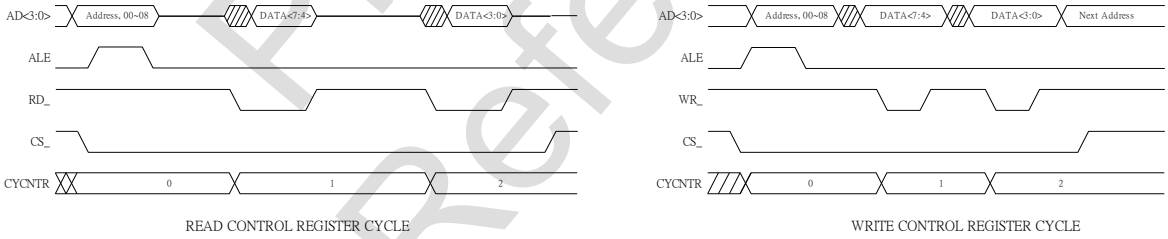
ADG<7:6>	Performance setting of ADC	Section 8.7
SETADC<7:6>	ENVDS & ENVCS, on/off power control setting	Section 5.3
SETADC<5:4>	CYS<1:0> elimination mode setting of offset voltage of ADC	Section 8.5
SETADC<3:0>	TPS1<1:0> and TPS2<1:0> the number of digital filter	Section 8.4
MISC1<7>	CNTBP and CMP1of ENBP and MISC2<3> determine the action of buzzer	Chart 4
MISC1<6:3>	Setting of clock generator controls the operating mode of capacity measurement	Chart 3, Chart 7 and Chart 8
MISC1<2:1>	DTON and FQRST_ are the counter mode of frequency counter and reset control	Section 9.1
MISC1<0>	PKHRST_ is the reset signal of peak-hold sampling circuitry	Section 9.2
MISC2<6:4>	Output of compactor and low voltage detector	Section 7.5 and 5.1
MISC2<2>	When equal 1, the signal of CMPH can directly input from ACA, without going through an AC buffer	Section 7.5.1
MISC2<1:0>	ENGNDR_ and ENLBS are the enable control of basic job offset voltage and low voltage detector.	5.1 and 5.2

Chart 19. The brief illustration of the function of each register in FS970X.

The read/write sequence of each control register is shown as Graph 15. Because of the data length is 8 bit, it requires consecutive two times for each read or write, first MSB, and then LSB（4 bits each）”0” when the next ALE occurred. Thus, it will start with MSB again when starting the next read/write sequence.



Graph 15. The read/write sequence of the control register.

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The interrupt process

The measurements can be read by the microprocessor interface are high-resolution output of ADC, the low resolution output of ADC, positive-negative peak-hold value, the output of frequency counter…etc. In any of the registers, each new value means new “event”. The chip, thru its IRQO pin, will send an interrupt signal to the microprocessor and request to process.

When microprocessor received an interrupt signal of negative-end trigger; means that some measuring registers in 970x chip has detected a new value. The microprocessor will then read the interrupt status register （INTSTA）, checking where the interrupt comes from. Chart 20 shows the corresponding event for each bit in the INSTA. The INTEN in Chart 20 controls whether a measuring event interrupt will occur.

INSTA	INSTA<3>	INSTA<2>	INSTA<1>	INSTA<0>
Event	Frequency counter output	+/- peak-hold value	Low-resolution ADC	High-resolution ADC
INTEN	INTEN<3>	INTEN<2>	INTEN<1>	INTEN<0>
Function	Corresponding IRQO enable	Corresponding IRQO enable	Corresponding IRQO enable	Corresponding IRQO enable

Chart 20. Interrupt status registers.

When microprocessor reads the register again, the interrupt bit will be reset to 0, and waiting for the new measurement to generate the interrupt again.

The interrupt status register INSTA<3:0> is a read-only register. The interrupt enable register INTEN<3:0> is a read/write register. The read/write sequences of both registers are the same as control register, as shown in Graph 15.

The flow-Chart of interrupt process are as follows:

1) When there’s a new value shown in the enable register, then set IRQO equal to 0, and keep it to 0.
2) When microprocessor receive this negative-end trigger, then read the interrupt status register.
3) After reading the status register, IRQO will be pulled back to1.
4) Check if the IRQO was pulled back to 1. If not, it means that it didn’t catch a negative end; then, it should read the interrupt status one more time.

When reading the instruction period of the interrupt register; the negative-end of the new interrupt might be lost. Therefore, by adding Step 4) will improve this problem.

In addition, whether the value of the interrupt status register has been updated in independent from interrupt enable register. That is to say, the interrupt enable register only affects IRQO output.

FORTUNE Properties For Reference Only

Measurement Registers

Address	Register	Function	Length of register	Times of reading
0A	KTB<23:0>	Output of time-based counter	24	6
0B	KSG<23:0>	Output of signal counter	24	6
0C	POSPK<15:0>	The up-most positive peak-hold register	16	4
0D	NEGPK<15:0>	The up-most negative peak-hold register	16	4
0E	SUM2<15:0>	Output of low-resolution ADC	16	4
0F	SUM1<23:0>	Output of high-resolution ADC	24	6

Chart 21. all measurement value registers in the chip.

All measurement registers and their corresponding address of FS970X are listed in Chart 21. There are six addresses in total. The length of each register varies. They are all output ports, and can only be read by microprocessor.

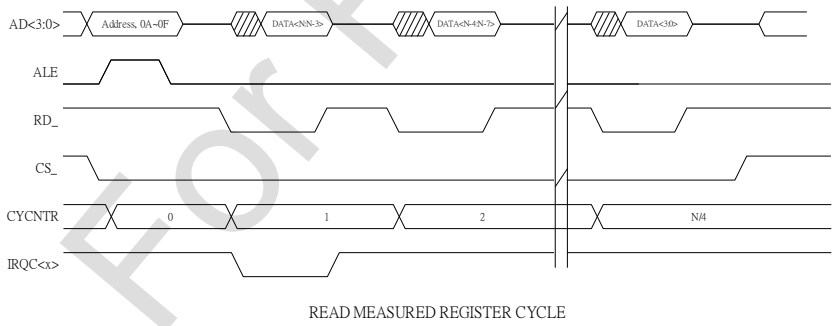
The reading clocks of the measurement register are shown in

Graph . When IRQC<x> is on the negative-end, it will clear the corresponding INSTA<x>. The number of readings of each new value has to be correct. Otherwise, read/write cycle counter CYCNTR will be cleared to 0 when ALE is “Hi”. The number of readings of each address varies with the length of each register, as shown in the last column of Chart 21.

When reading SUM1or SUM2, the first reading period (when CYCNTR=1), the low pulse width of RD_ must be greater than the sampling period of ADC. The other reading periods need only to be greater than 2 us. For example, when the sampling frequency of the ADC is 83.3 kHz, then, the first reading period of SUM1 and SUM2 must be greater than 12 us.

Regarding the frequency counter, what worth mentioning is when reading the value of the time-based counter, it will not clear the interrupt bit INSTA<3>. Only when reading the signal counter, its corresponding interrupt bit INSTA<3> can be cleared.

INSTA<2> will be cleared whether reading registers of the up-most positive peak-hold value or up-most negative peak-hold value.



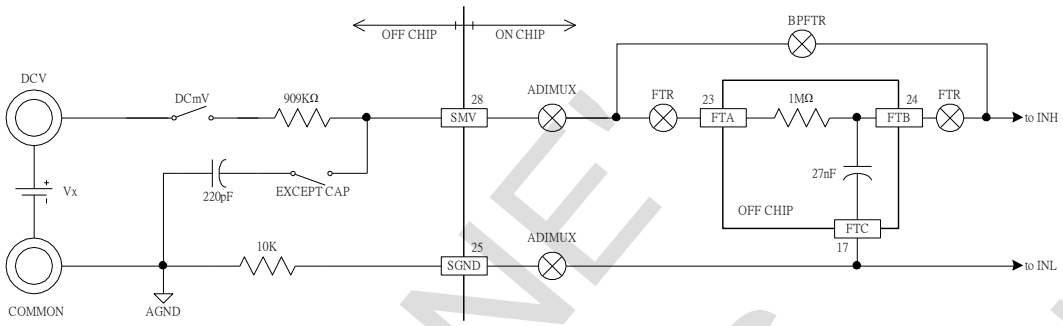
Graph 16. Reading sequence diagram of measuring registers.

FORTUNE Properties For Reference Only

14. Basic Measurement Application

DCmV

14..1 500 mV



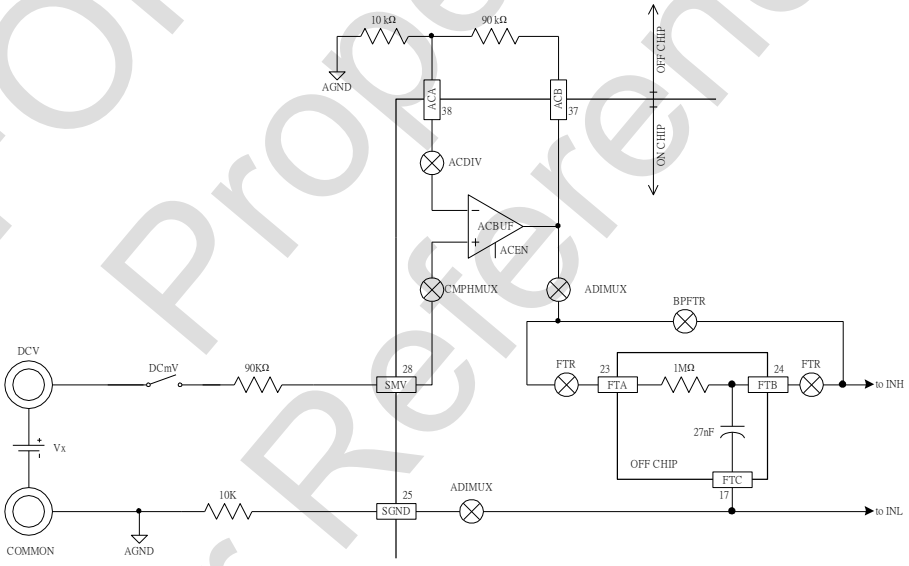
Graph 17. Function network diagram of 500 mV.

Address	00	01	02	03	04	05	06	07	08
Register	RDG	SIN	SRF	SCP	AFT	ADG	SETADC	MISC1	MISC2
Value	00h	00h	08h	00h	00h	93h	9Fh	00h	00h

Chart 22. 500 mV register setup.

Signal flows in SMV, through ADIMUX and pre-filter, into ADC.

14..2 50 mV



Graph 18. Function network diagram of 50 mV.

Address	00	01	02	03	04	05	06	07	08
Register	RDG	SIN	SRF	SCP	AFT	ADG	SETADC	MISC1	MISC2
Value	00h	80h	08h	00h	30h	93h	9Fh	00h	80h

Chart 23. 50 mV register setup.

Signal flows in from AMV, through a 10-times amplified gain network by ACBUF, and goes through a pre-filter before flowing into ADC.

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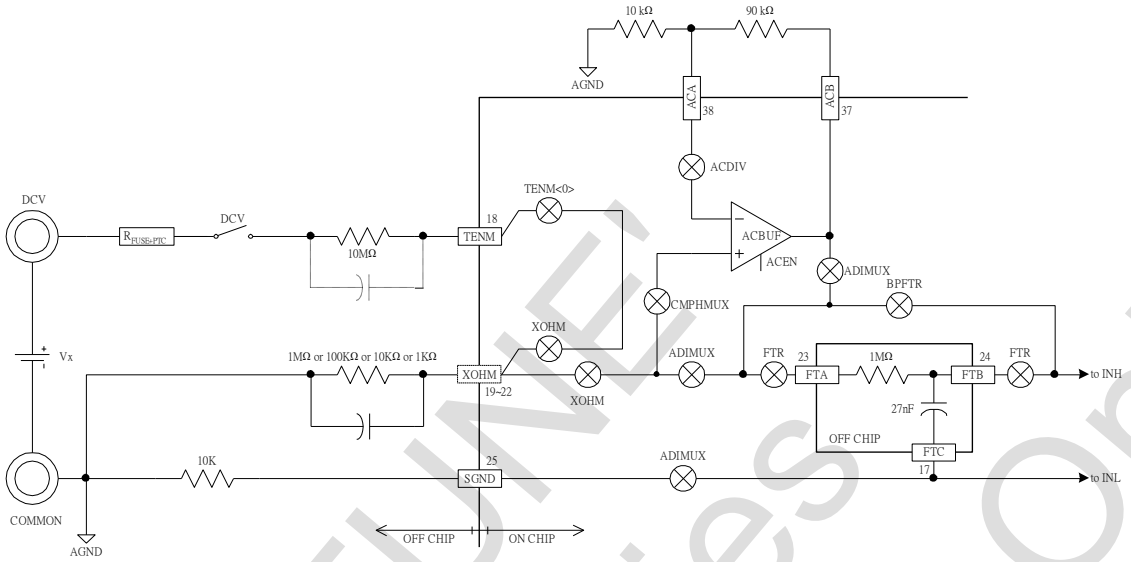
DC voltage



Graph 19. Function network diagram of DC voltage.

Address	00	01	02	03	04	05	06	07	08
Register	RDG	SIN	SRF	SCP	AFT	ADG	SETADC	MISC1	MISC2
0.5 V	10	80	08h	00h	30h	93h	9Fh	00h	80h
5V~1000V	x0h	10h	08h	00h	00h	93h	9Fh	00h	00h

Chart 24. DC voltage register setup.

Whereas, the value of RGD<7:4> is determined by function, as shown in Chart .

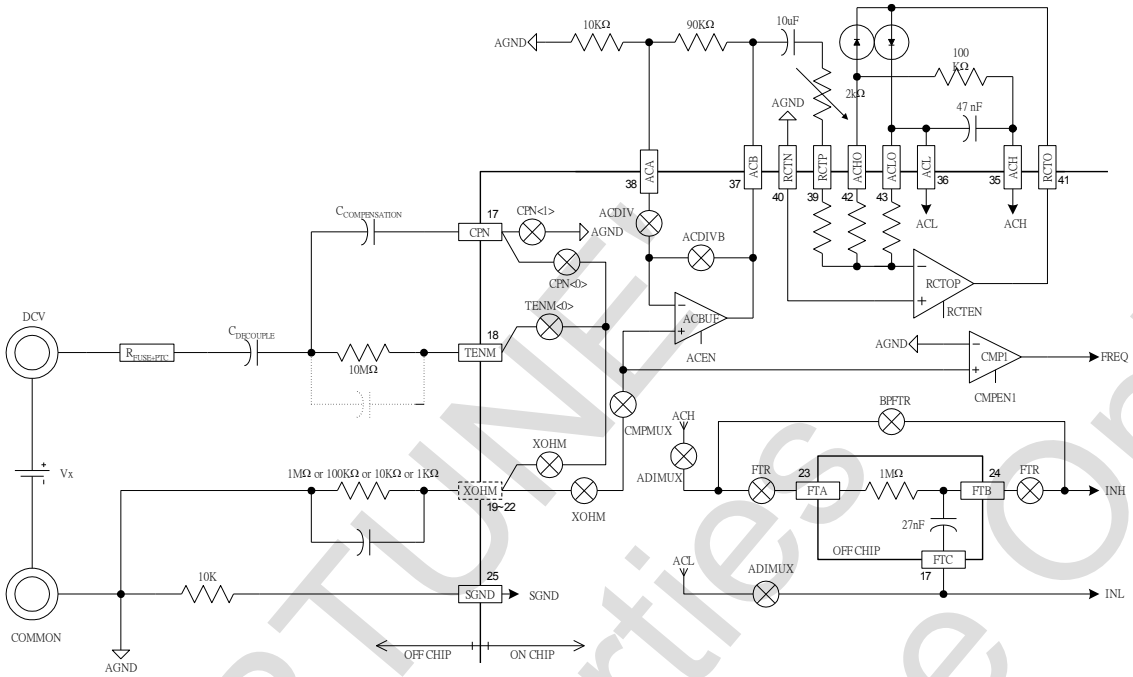
Address	Register	0.5V~5V	50V	500V	1000V
00	RGD<7:0>	10h	20h	40h	80h

Chart 25. Voltage range setup

The voltage signal will decay to be lower than 0.5V by a suitable multiple of decay network. It will go through a pre-filter, and then into ADC. Only the signal of 0.5V, decayed 10-times, will amplify 10-times before flow into ADC.

FORTUNE Properties For Reference Only

AC Voltage (ACV)



Graph 20. Function network diagram of AC voltage.

Address	00	01	02	03	04	05	06	07	08
Register	RDG	SIN	SRF	SCP	AFT	ADG	SETADC	MISC1	MISC2
0.5V	10h	5Bh	00h	10h	F0h	93	9F	00	00
5V~100V	x0h	5Bh	00h	10h	D0h	93h	9Fh	00h	00h

Chart 26. AC voltage register setup.

Whereas, the value of RGD<7:4> is determined by the function, as show in Chart .

The voltage signal of 5V~1000V will decay to be lower than 0.5V by a suitable multiple of decay network. It will go through a AC buffer with gain value of 1, and then into a AC/DC converter or true mean square converter. It then goes through a pre-filter, and into ADC. Under 0.5V, setting ACDIV=1 will allow the 10-times decay signal to be 10-times amplified by AC buffer, reversing it back within the dynamic range of 0.5V before feeding it into AC/DC converter or true mean square converter.

DC Current (DCA)

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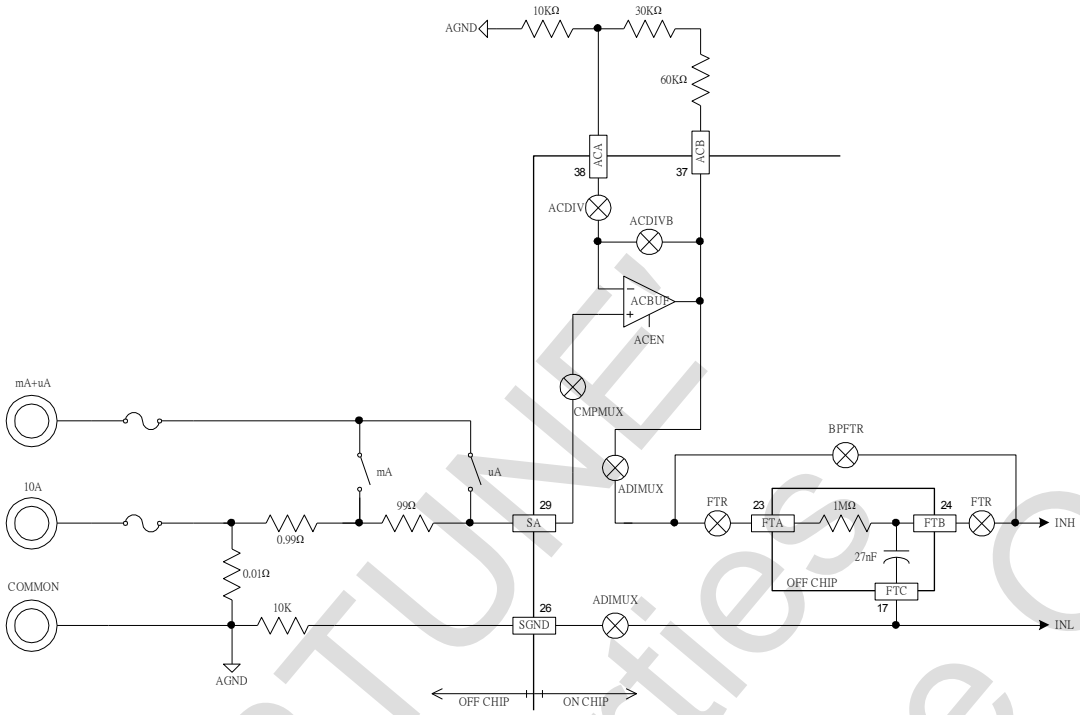

Graph 21.

Function network diagram of DC current.

Address	00	01	02	03	04	05	06	07	08
Register	RDG	SIN	SRF	SCP	AFT	ADG	SETADC	MISC1	MISC2
5000uA, 500mA, 10A	00h	80h	08h	20h	10h	93h	9Fh	00h	80h
500uA, 5mA, 5A	00h	80h	08h	20h	30h	93h	9Fh	00h	80h

Chart 27. DC current register setup.

AS shown in Graph , and assuming the transferring resistor to be approx. 100Ω, the transferring voltage will be 0.5V under 5.0000 mA. It will then flow into ADC through the ACBUF buffer of 1 (ACDIV=AFT<5>=0). Under 50.000 mA, when using the transferring resistor of 100Ω, the transferring voltage of 5V will be too high. If using 1Ω, the transferring voltage will be 50mV, and the gain of ACBUF will be 10 (ACDIV=AFT<5>=1). Amplify the signal 10-times before feeding it into ADC.

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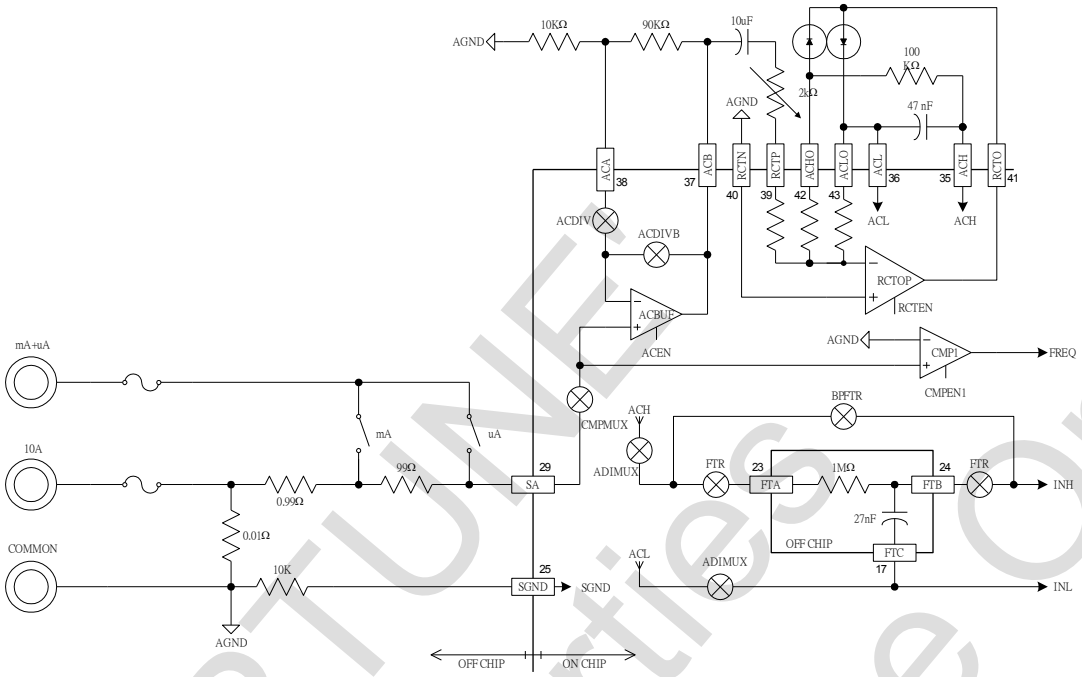
AC Current (ACA)



Graph 22. Function network diagram of AC current.

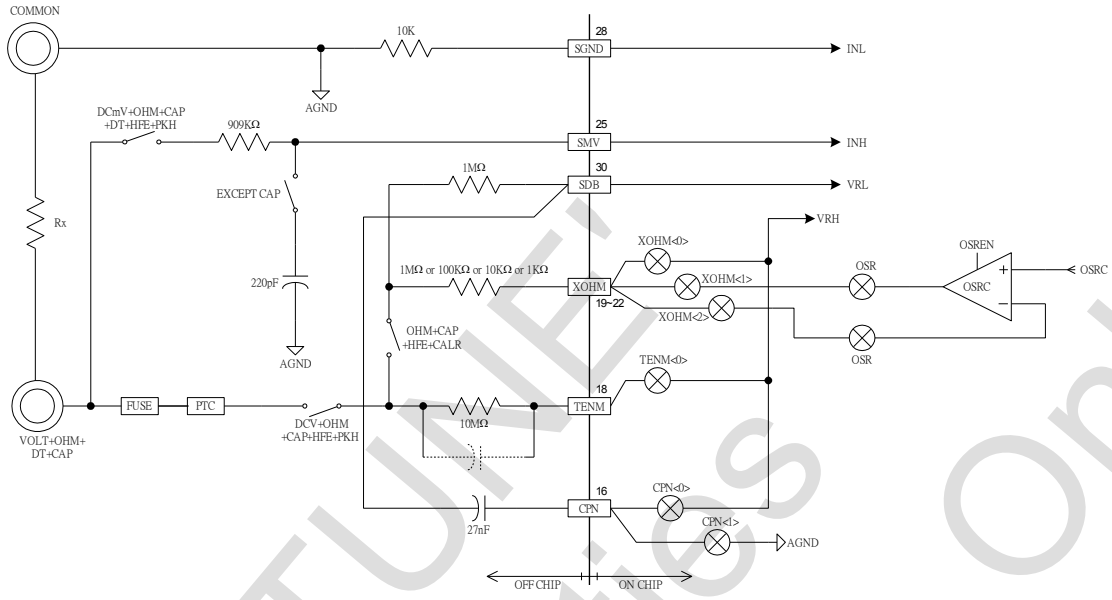
Address	00	01	02	03	04	05	06	07	08
Register	RDG	SIN	SRF	SCP	AFT	ADG	SETADC	MISC1	MISC2
5000uA, 500mA, 10A	00h	5Bh	08h	20h	D0h	93h	9Fh	00h	00h
500uA, 5mA, 5A	00h	5Bh	08h	20h	F0h	93h	9Fh	00h	00h

Chart 28. AC current register setup.

As shown in Graph, the measuring path of AC current, up to the output of AC buffer, is the same as DC current. After going through AC buffer, the signal will flow through AC/DC converter or true mean square converter to convert AC signal into DC signal before flow into ADC.

FORTUNE Properties For Reference Only

Resistor (Ω)



Graph 23. Function network diagram of resistor.

Address	00	01	02	03	04	05	06	07	08
Register	RDG	SIN	SRF	SCP	AFT	ADG	SETADC	MISC1	MISC2
Value	89h	00h	Dah	00h	00h	93h	1Fh	00h	00h

Chart 29. Resistor register setup.

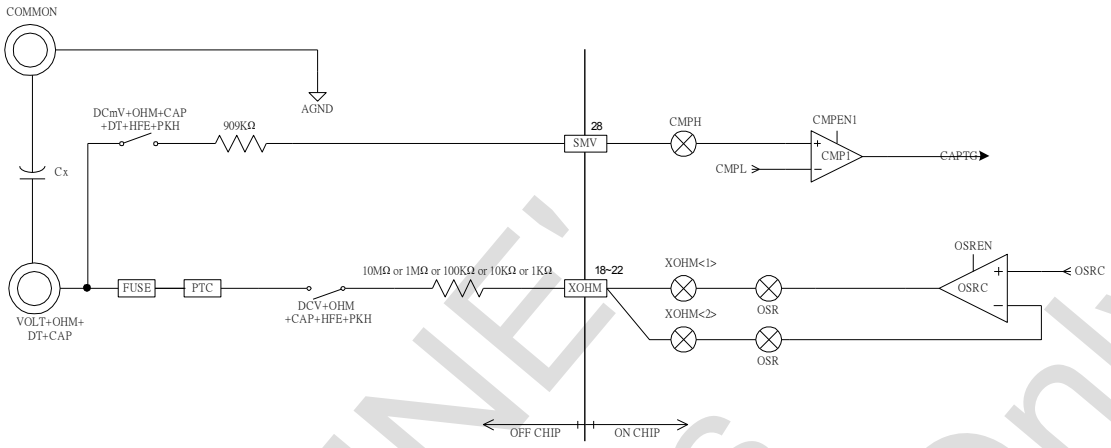
The setup of RGD<7:4>, SRF<7:0>, ADG<7:0>, and MISC1<7:0> varies with different functions. See below for details.

Address	Register	500Ω	5KΩ	50KΩ	500KΩ	5MΩ	40MΩ
00	RGD<7:0>	89h	49h	29h	19h	09h	09h
02	SRF<7:0>	Dah	4Ah	4Ah	4Ah	4Ah	4Ah
05	ADG<7:0>	93h	93h	93h	93h	93h	98H
07	MISC1<7:0>	00h	00h	00h	00h	40h	40h

Chart 30. Resistor range setup.

FORTUNE Properties For Reference Only

Capacitor



Graph 24. Function network diagram of capacitor.

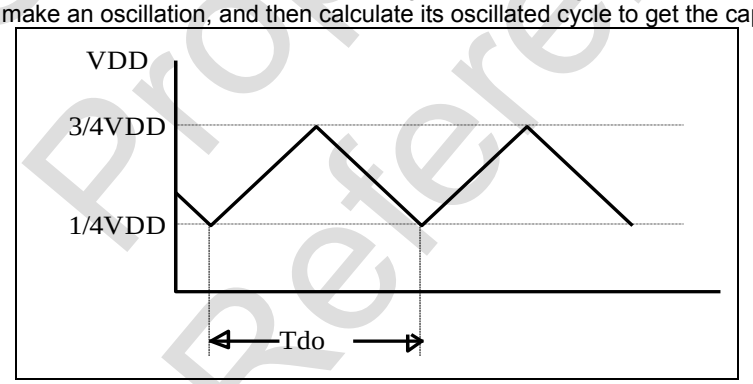
Address	00	01	02	03	04	05	06	07	08
Register	RDG	SIN	SRF	SCP	AFT	ADG	SETADC	MISC1	MISC2
Value	1Bh	00h	00h	01h	00h	00h	00h	00h	00h

Chart 31. Capacitor register setup.

Address	Register	500nF	5uF	50uF	500uF
00	RGD<7:0>	1Bh	2Bh	4Bh	8Bh
04	AFT<7:0>	00h	00h	00h	04h
07	MISC1<7:0>	00h	00h	00h	20h

Chart 32. Capacitor range setup.

- Measuring capacitor value of FS9704B is to charge and discharge the resistor reference added by XOHM Pin to make an oscillation, and then calculate its oscillated cycle to get the capacitor value.



Capacitor Measurement

- To calculate the cycle, we send the square wave that out from CAPTG to the frequency counter. When operating the frequency measurement, the necessary timer reference signal is FTB. For the measuring frequency, it can be gained through the following formula. In this formula, Ksg is the signal counter and Ktb is the value of the time-base counter.

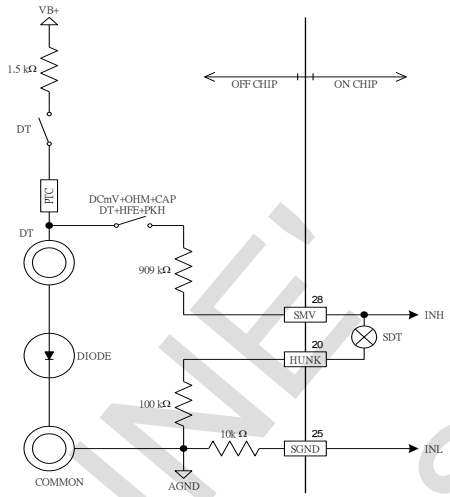
Fin = (Ksg / Ktb) * FTB

- The revise of the calculated Fin is the cycle.

1 / Fin = { 1 / [(Ksg / Ktb) * FTB] }

FORTUNE Properties For Reference Only

Diode



Graph 25. Function network of diode measurement.

Address	00	01	02	03	04	05	06	07	08
Register	RDG	SIN	SRF	SCP	AFT	ADG	SETADC	MISC1	MISC2
Setup value	01h	00h	08h	00h	00h	93h	1Fh	00h	00h

Chart 33. Diode register setup.

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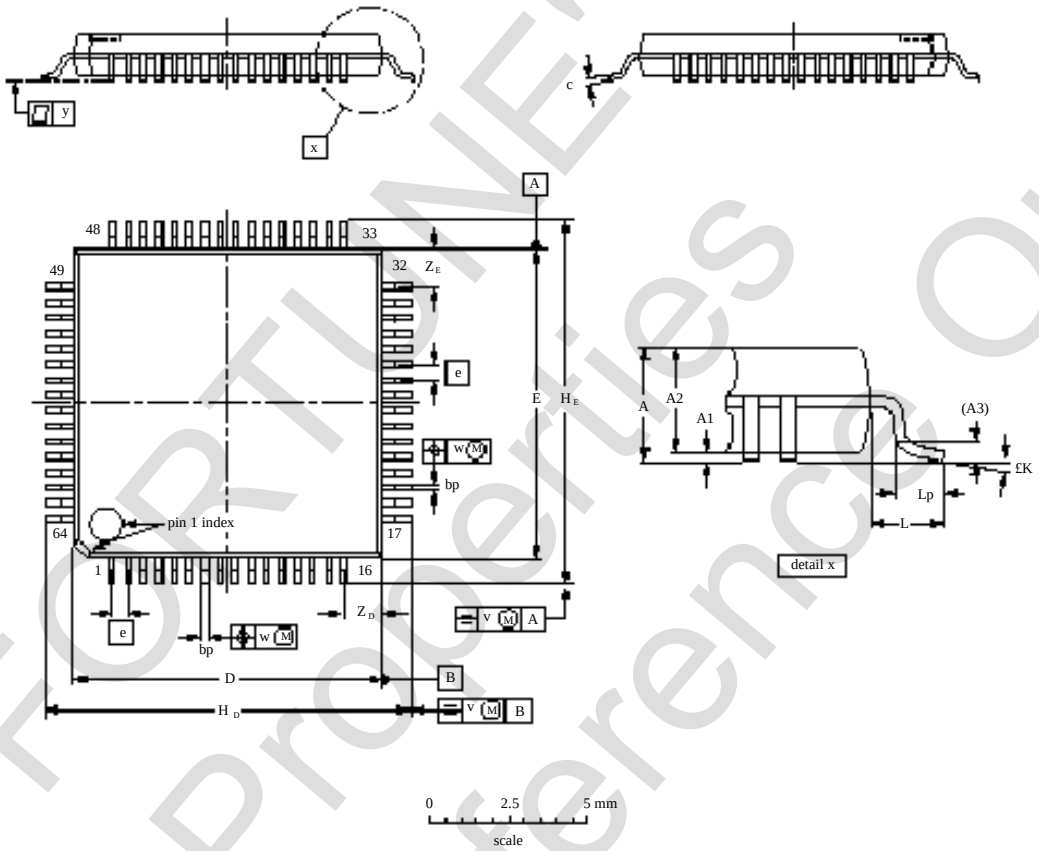
15. Package Outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x1.4 mm



DIMENSIONS (mm are the origlinal dimensions)

UNIT	A max.	A1	A2	A3	bp	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	Lp	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	£K
mm	1.60	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.2	0.12	0.075	1.45 1.05	1.45 1.05	7 ¢X 0 ¢X

Note: 1.Plastic or metal protrusions of 0.25 mm maximum per side are not included.

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16. Attachment (1) OP-AMP Specifications

(VDD = 6V, VSS = 0V, T_A=+25℃, unless otherwise indicated)

Instrumentation Amplifier @ Gain = 30, Vref=0.5V, T_A=25℃					
PARAMETER	**TEST CONTITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Offset Voltage without AZ	Rs<100		20		V
Input Offset Voltage with AZ	Rs<100		0	3	V
Input Offset Drift without AZ	-20℃<T_A<+50℃		200		nV/℃
Input Offset Drift with AZ	-20℃<T_A<+50℃		20		nV/℃
Input Referred Noise	Rs=100 , 0.1Hz~1Hz		0.3	0.6	Vpp
Input Bias Current	[2]		100	300	pA
Current Consumption			180	220	A

[1] These parameters are guaranteed by design and are tested only by sampling while mass production.
[2] While a voltage source with large output impedance is measured by an instrument-ation amplifier having input bias current, an additional input offset voltage will introduced. However, this offset voltage could be cancelled by mirrored offset cancellation technique.

17. Revision History

Ver.	Date	Page	Description
3.9	2004/01/28	12	Revise typical application circuit
4.0	2004/04/23	5	1. Revise datasheet format 2. Add ordering information
4.1	2006/12/21	All 17	1. Revise datasheet format 2. Add revision history
4.2	2007/02/28	6	Add Pb free ordering information
4.3	2010/02/23	6	Revise Green ordering information
4.4	2014/05/22	2	Revised company address

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