

UM11144

FRDM-HB2002ESEVM evaluation board

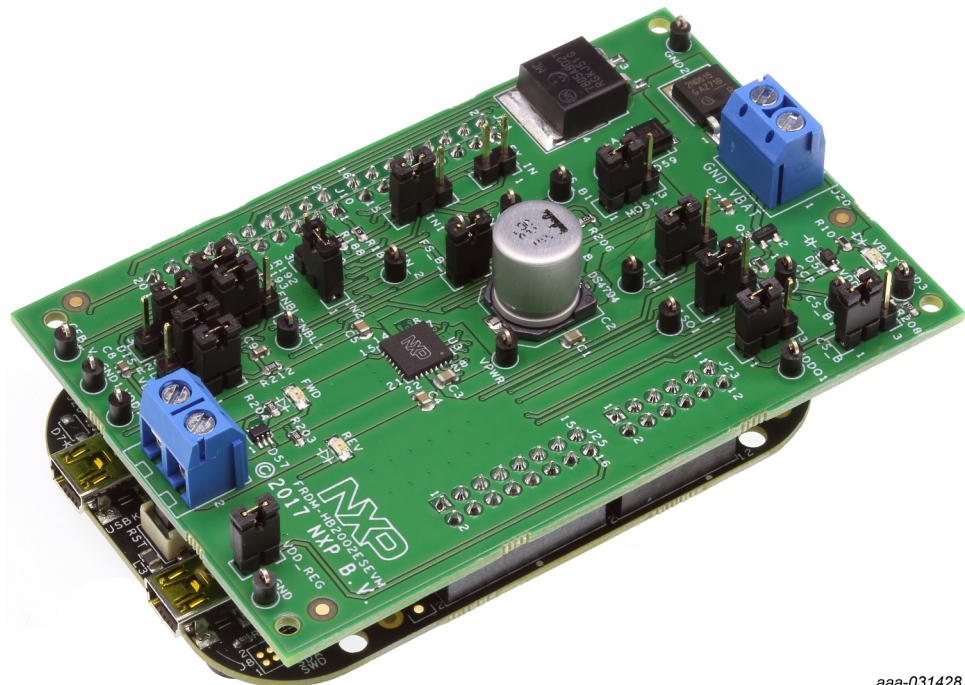
Rev. 1.0 — 13 September 2018

User guide

FRDM-HB2002ESEVM

The FRDM-HB2002ESEVM evaluation kit exercises all the functions of the MC33HB2002 H-bridge device. Lab equipment or any MCU with GPIOs can control the parallel inputs to provide PWM control to the inputs.

The board can be used with a FRDM-KL25Z board connected to a USB port of a PC. Configure, control, and monitor the status of MC33HB2002 by using the SPI communication capabilities of the board.



aaa-031428



1 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on <http://www.nxp.com>.

The information page for FRDM-HB2002ESEVM evaluation board is at <http://www.nxp.com/FRDM-HB2002ESEVM>. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the FRDM-HB2002ESEVM evaluation board, including the downloadable assets referenced in this document.

1.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at <http://community.nxp.com>.

2 Getting ready

Working with the FRDM-HB2002ESEVM requires the kit contents, additional hardware and a Windows PC workstation with installed software.

2.1 Kit contents

- Assembled and tested FRDM-HB2002ESEVM and preprogrammed FRDM-KL25Z microcontroller board in an anti-static bag
- Quick Start Guide

2.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

- DC power supply: 5.0 V to 40 V with up to 20 A current handling capability, depending on motor requirements
- USB standard A (male) to mini-B (male) cable
- 3/16-inch blade screwdriver for connecting the cables
- Typical loads (brushed DC motor, power resistors, or inductive load with up to 5.0 A and 28 V operation)
- Function generator (optional)

2.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- USB-enabled computer with Windows 7, Windows 8, or Windows 10

2.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation board's information page at <http://www.nxp.com/FRDM-HB2002ESEVM>.

- SPI Generator (SPIGen) software, version 7.1.8 or later, a Graphical User Interface (GUI)

Note: Software must be installed in a specific order. See [Configuring the hardware](#).

3 Getting to know the hardware

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost and improved performance in powering state-of-the-art systems.

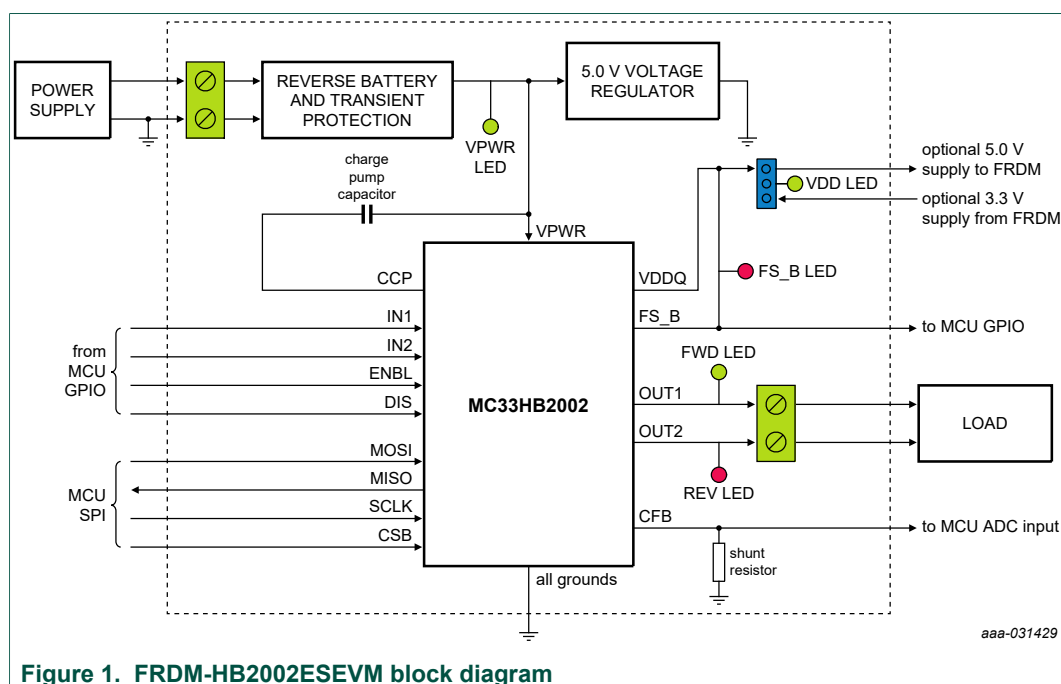
3.1 Kit overview

3.1.1 FRDM-HB2002ESEVM features

The FRDM-HB2002ESEVM board evaluates the NXP part MC33HB2002, including all functions. The board features the following:

- Built-in reverse battery protection
- Test points that allow signal probing
- Built-in voltage regulator to supply logic level circuitry
- Current feedback network for real-time load current monitoring by MCU ADC
- LEDs to indicate the supply status and the direction of the motor
- Low ESR capacitor to reduce ripple in the power supply
- TVS protection diode to handle system level transients

3.1.2 FRDM-HB2002ESEVM block diagram



3.1.3 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the FRDM-HB2002ESEVM are available at <http://www.nxp.com/FRDM-HB2002ESEVM>.

3.2 Featured components

[Figure 2](#) identifies important components on the FRDM-HB2002ESEVM board and [Table 1](#) provides additional details on these components.

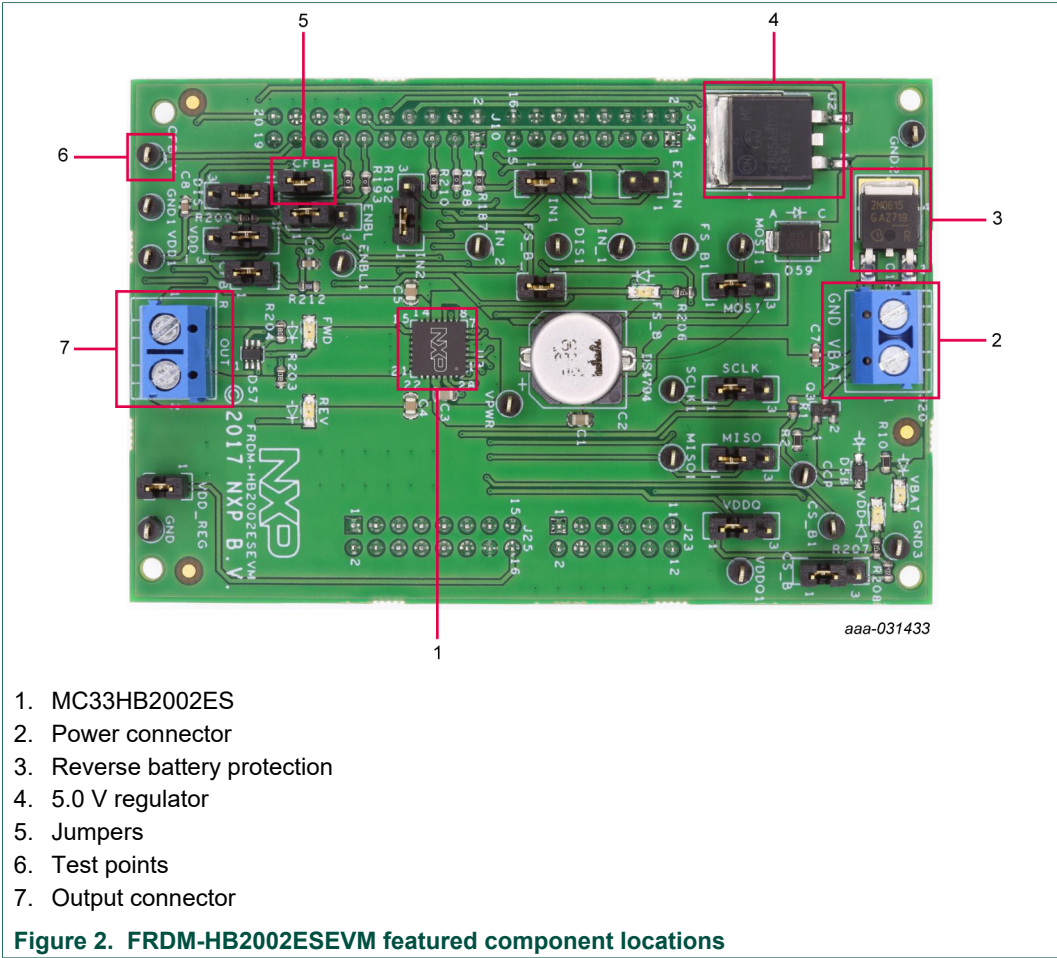


Table 1. FRDM-HB2002ESEVM board component descriptions	
Name	Description
MC33HB2002ES	monolithic H-bridge motor driver IC in a robust, thermally enhanced 28-pin HVQFN (6 × 6 mm) package
Power and ground inputs	power supply terminal to connect the battery/power supply with the board
Reverse battery protection	MOSFET for protecting MC33HB2002 in reverse battery condition
5.0 V regulator	5.0 V regulator for VDD and supply
Jumpers	jumpers for configuring the board for different modes of operation
Test points	test points to probe different signals
Output terminal	output connector to connect a load to the MC33HB2002 output

3.2.1 MC33HB2002: 10 A H-bridge, SPI programmable brushed DC motor driver

3.2.1.1 General description

The MC33HB2002 is a SMARTMOS monolithic H-bridge power IC, enhanced with SPI configurability and diagnostic capabilities. It is designed primarily for DC motor or

servo motor control applications within the specified current (average load is 3.0 A, peak current is 10 A) and voltage limits.

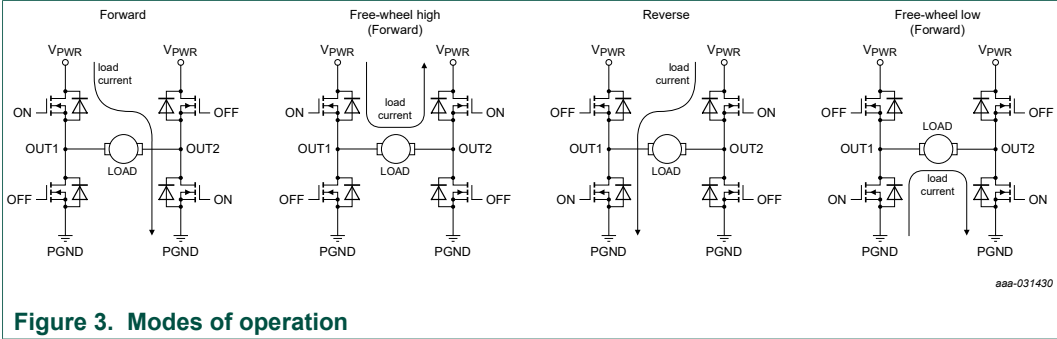
The MC33HB2002 is similar to the MC33HB2000 device with higher overtemperature setting and the use of current foldback for current limiting to extend fault operation range.

This part is designed to specifically address the ISO 26262 safety requirements. It meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 1 qualified.

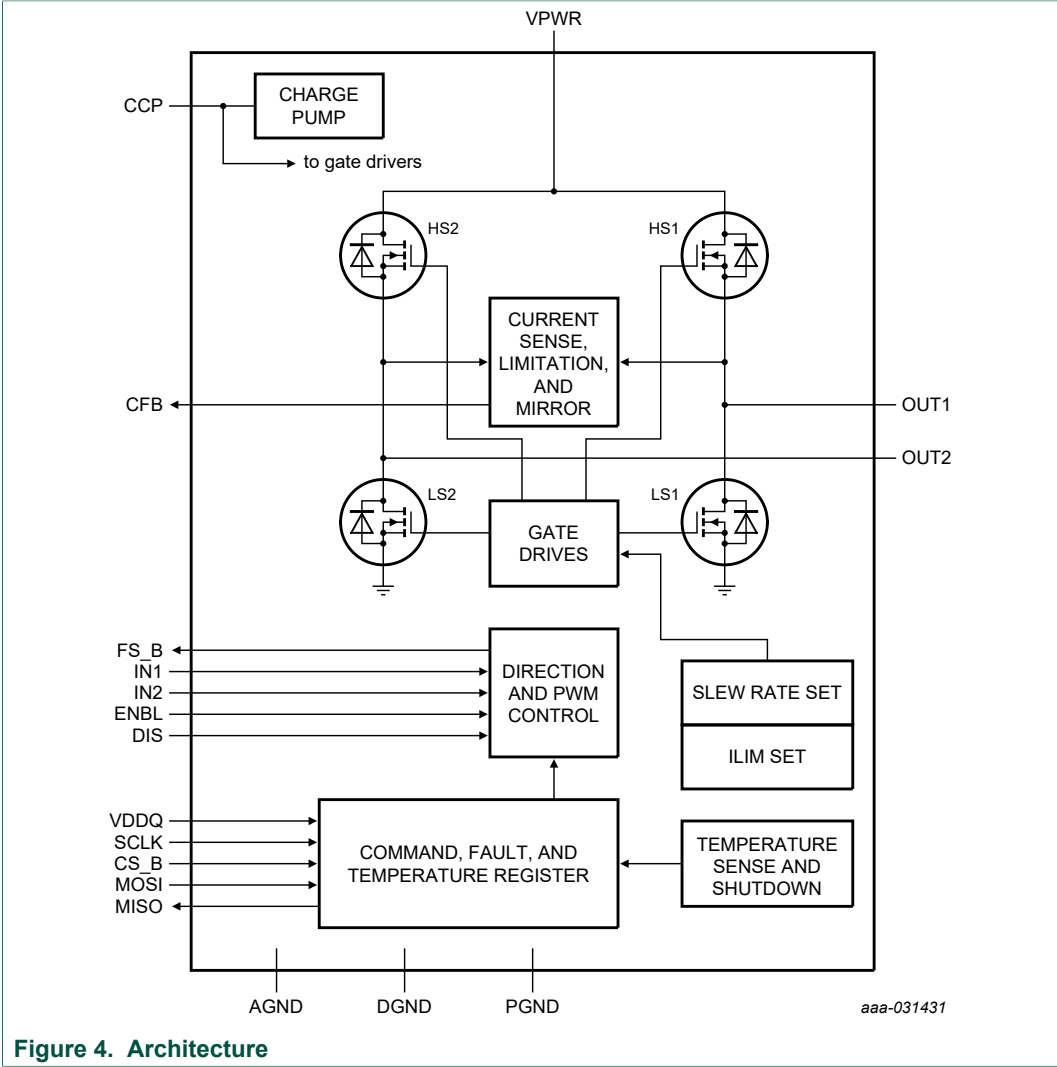
3.2.1.2 Features

- Advanced diagnostic reporting via a serial peripheral interface (SPI): charge pump undervoltage, overvoltage, and undervoltage on VPWR, short to ground and short to VPWR for each output, open load, temperature warning and overtemperature shutdown
- Thermal management: Excellent thermal resistance of $<1.0\text{ }^{\circ}\text{C/W}$ between junction and case (exposed pad)
- Eight selectable slew rates via the SPI: $0.25\text{ V}/\mu\text{s}$ to more than $16\text{ V}/\mu\text{s}$ for EMI and thermal performance optimization
- Four selectable current limits via the SPI: $5.4/7.0/8.8/10.7\text{ A}$ covering a wide range of applications
- Extended high temperature operating range with current foldback while limiting the current
- Three package sizes available in SOIC, PQFN and HVQFN to meet footprint and application requirement
- Can be operated without SPI with default slew rate of $2.0\text{ V}/\mu\text{s}$ and a 7.0 A current limit threshold
- Highly accurate real-time current feedback through a current mirror output signal with less than $5.0\text{ }\%$ error
- Drives inductive loads in a full H-bridge or half-bridge configuration
- Overvoltage protection places the load in high-side recirculation (braking) mode with notification in H-bridge mode
- Wide operating range: 5.0 V to 28 V operation
- Low $R_{\text{DS(on)}}$ integrated MOSFETs: maximum of $235\text{ m}\Omega$ ($T_J = 150\text{ }^{\circ}\text{C}$) for each MOSFET
- Internal protection for overtemperature, undervoltage, and short-circuit by signaling the error condition and disabling the outputs
- I/O pins can withstand up to 36 V
- AEC-Q100 grade 1 qualified

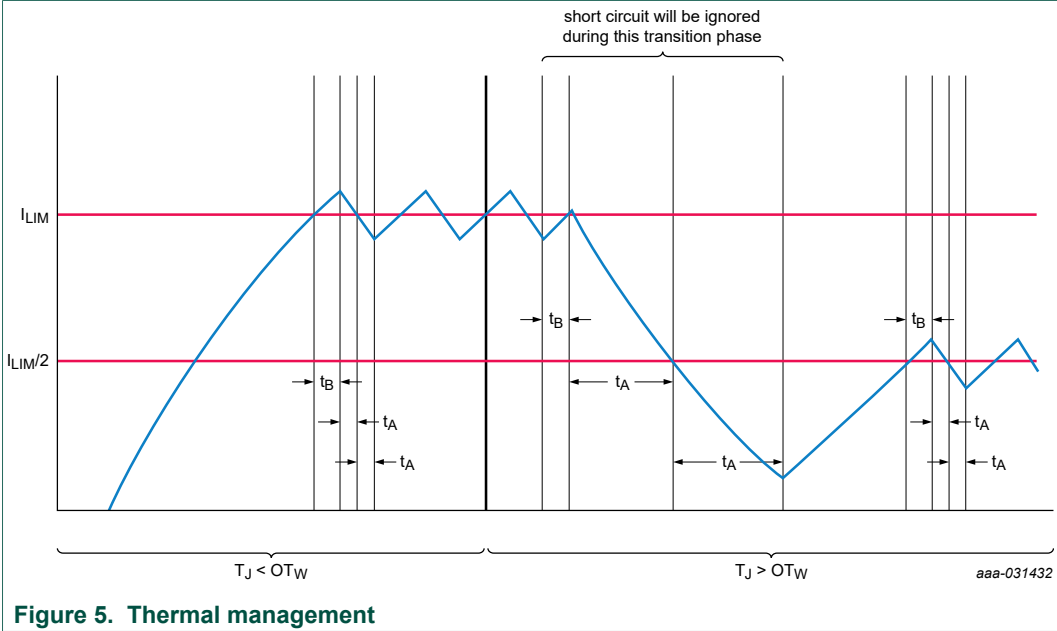
3.2.1.3 Modes of operation



3.2.1.4 Architecture



3.2.1.5 Thermal management



3.3 Indicators

The following LEDs are provided as visual output devices for the evaluation board:

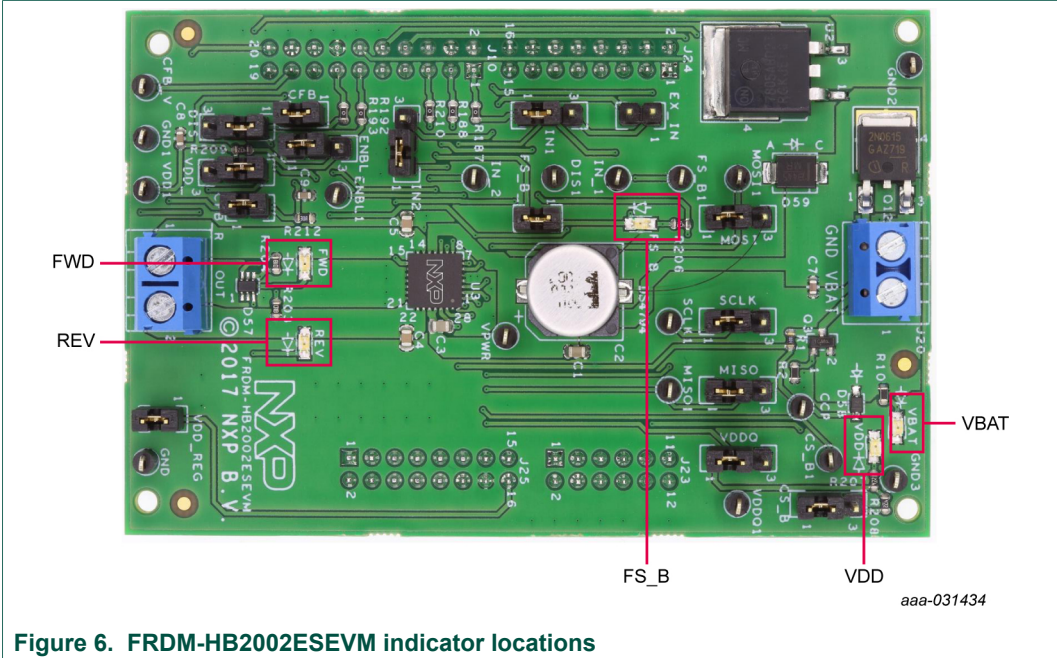


Table 2. FRDM-HB2002ESEVM indicator descriptions

Label	Description
VBAT	green LED, indicates when main/battery supply is connected
VDD	green LED, indicates when +5.0 V supply is connected

Label	Description
FS_B	red LED, illuminates when the H-bridge detects a fault
FWD	green LED, indicates output current in forward direction ($V_{OUT1} > V_{OUT2}$)
REV	red LED, indicates output current in reverse direction ($V_{OUT2} > V_{OUT1}$)

3.4 Jumpers

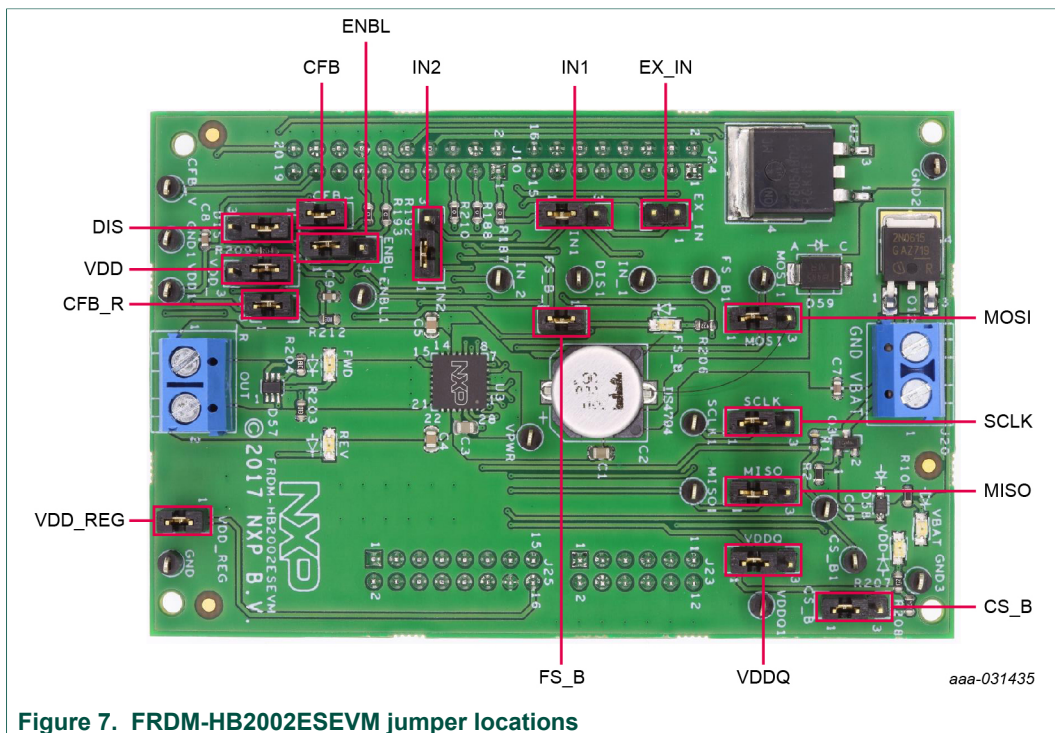


Figure 7. FRDM-HB2002ESEVM jumper locations

Table 3. Jumper descriptions

Name	Signal	Jumper position	Connection
J1	IN1	1–2	IN1 control through MCU parallel output on J10 pin 1 (DATA0)
		2–3	IN1 control through external input on EX_IN pin 1
J2	DIS	1–2	DIS control through MCU parallel output on J10 pin 13 (CTRL1)
		2–3	DIS connected to GND to keep the outputs enabled
J3	IN2	1–2	IN2 control through MCU parallel output on J10 pin 3 (DATA1)
		2–3	IN2 control through external input on EX_IN pin 2
J4	CS_B	1–2	CS_B control through MCU SPI output J10 pin 6 (SPI_CS_B)
		2–3	CS_B pulled up to VDD for operation without SPI
J5	ENBL	1–2	ENBL control through MCU parallel output J10 pin 11 (CTRL0)
		2–3	ENBL pulled up to VDD to keep the outputs enabled
J6	SCLK	1–2	SPI clock SCLK from MCU J10 pin 12 (SPI_SCLK)
		2–3	SCLK connected to GND for operation without SPI

Name	Signal	Jumper position	Connection
J7	MOSI	1–2	MOSI control through MCU SPI output J10 pin 8 (SPI_MOSI)
		2–3	MOSI connected to GND for operation without SPI
J8	MISO	1–2	MISO control through MCU SPI output J10 pin 10 (SPI_MISO)
		2–3	MISO not connected (open) for operation without SPI
J11	CFB	1–2	CFB connected to 200 Ω , 0.047 μ F sense network (on-board)
J14	VDDQ	1–2	Selected VDD connected to VDDQ pin
		2–3	VDDQ pin not connected to on-board VDD supply
J17	VDD	1–2	On-board 5.0 V regulator supplies VDD rail
		2–3	FRDM board 3.3 V regulator supplies VDD rail
J18	CFB_R	1–2	CFB sense network connected to MCU ADC input J10 pin 17 (CFB_READ)
J19	FS_B	1–2	FS_B pin connected to the LED, pull-up resistor, and MCU input through J10 pin 5 (FS_B)
J26	VDD_REG	1–2	On-board 5.0 V regulator powers FRDM board
J15	EX_IN	open	IN1 and IN2 external inputs

The FRDM-HB2002ESEVM, with a FRDM-KL25Z board (shipped with the kit), can evaluate the design with a GUI, any MCU with GPIO or with simple lab equipment. A FRDM-KL25Z compatible GUI and MCU program are available online at the following link: <http://www.nxp.com/FRDM-HB2002ESEVM>.

The FRDM-HB2002ESEVM is compatible with any Arduino platform board. However, if a board other than the FRDM-KL25Z is used, MCU code must be written to work with the board.

3.5 Input signal definitions

The following input signals control the outputs or functions inside the circuit.

Table 4. Input signal definitions

Input name	Description
DIS	enable/disable signal to activate/3-state the outputs
ENBL	enable/disable signal to activate/3-state the outputs and put the device to Sleep mode
IN1	logic input to control OUT1
IN2	logic input to control OUT2
MOSI	master output slave input for the SPI
CS_B	chip select bar input for the SPI
SCLK	clock for the SPI

3.6 Output signal definitions

The FRDM-HB2002ESEVM generates the following output signals to drive a load (such as a brushed DC motor), report fault conditions, and communicate back to the master over SPI. The board provides an analog output for real-time load current monitoring. This signal allows closed-loop control of the load.

Table 5. Output signal definitions

Output name	Description
OUT1	output 1 of H-bridge
OUT2	output 2 of H-bridge
FS_B	open-drain active LOW status flag output to indicate fault
CFB	current mirror output for real-time load current monitoring
MISO	master input slave output for SPI

3.7 Test points

The following test points provide access to various signals to and from the board.

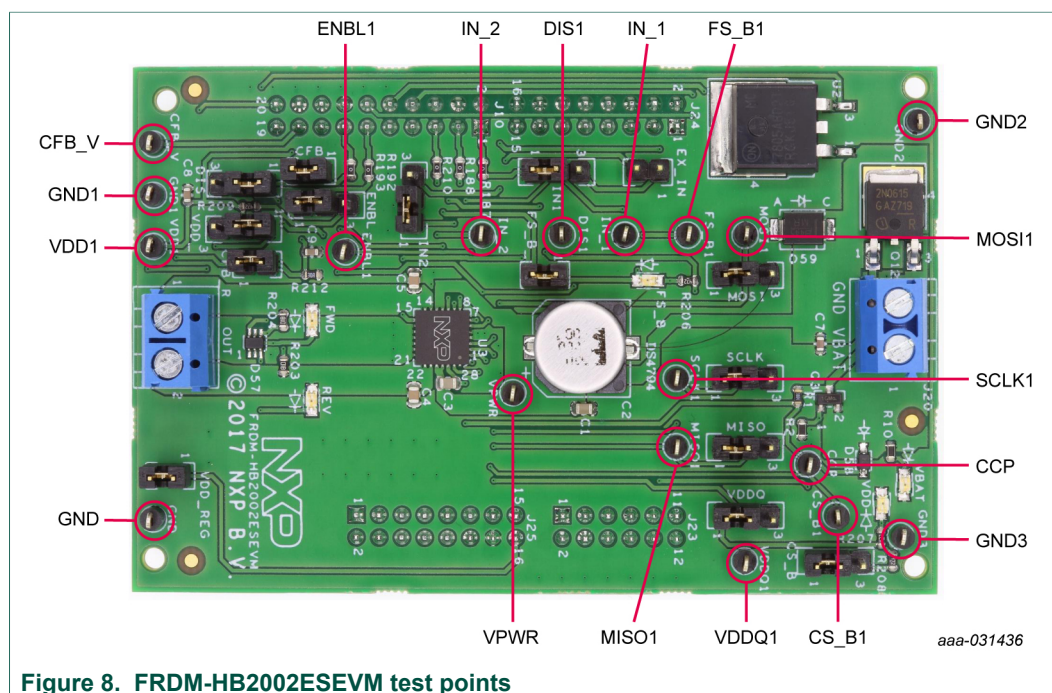


Figure 8. FRDM-HB2002ESEVM test points

Table 6. FRDM-HB2002ESEVM test point descriptions

Test point name	Signal name	Description
CFB_V	CFB_READ	CFB pin voltage going to ADC
CCP	CCP	charge pump voltage
ENBL1	ENBL	enable/disable signal to activate/3-state the outputs and put the device to Sleep mode
DIS1	DIS	enable/disable signal to activate/3-state the outputs

Test point name	Signal name	Description
IN_1	IN1	direction control in H-bridge mode and OUT1 control in Half-bridge mode
IN_2	IN2	PWM control in H-bridge mode and OUT2 control in Half-bridge mode
VPWR	VPWR	system voltage
VDDQ1	VDDQ	VDDQ digital output supply voltage
FS_B1	FSB	fault status monitoring pin
VDD1	VDD	V _{DD} supply for the part
CS_B1	CS_B	chip select bar
SCLK1	SCLK	clock for SPI
MOSI1	MOSI	master output slave input signal
MISO1	MISO	master input slave output signal
GND	GND	ground signal
GND1	GND	ground signal
GND2	GND	ground signal
GND3	GND	ground signal

3.8 Screw terminal connections

The board has the following screw terminal connections to connect the power supply and the load.

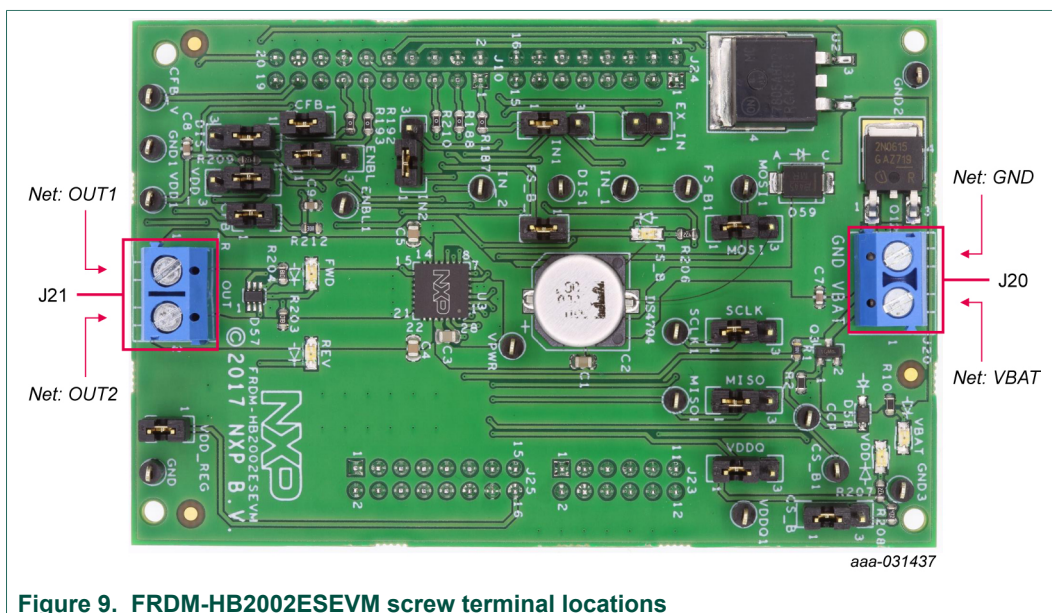


Figure 9. FRDM-HB2002ESEVM screw terminal locations

Table 7. Screw terminal connections

Screw terminal name	Description
J20	power supply connector for the MC33HB2002
J21	output connector to connect load

4 FRDM-HB2002ESEVM to FRDM-KL25Z connection information

The FRDM-KL25Z evaluation board was chosen specifically to work with the FRDM-HB2002ESEVM kit because of its low cost and features. The FRDM-KL25Z board uses the USB, built-in LEDs, and I/O ports available with NXP's Kinetis KL2x family of microcontrollers.

The FRDM-KL25Z connects to a PC through a USB port, which permits the user to interact with the motor driver per the evaluation board inputs. The FRDM-KL25Z also monitors the SPI registers, by that facilitating the use of safety and advanced diagnostic functions.

The FRDM-HB2002ESEVM connects to the FRDM-KL25Z using the four dual row Arduino R3 connectors on the bottom of the board (see [Table 8](#) and [Figure 10](#)). The board contains GPIO and SPI pin inputs to control and operate a brushed DC motor.

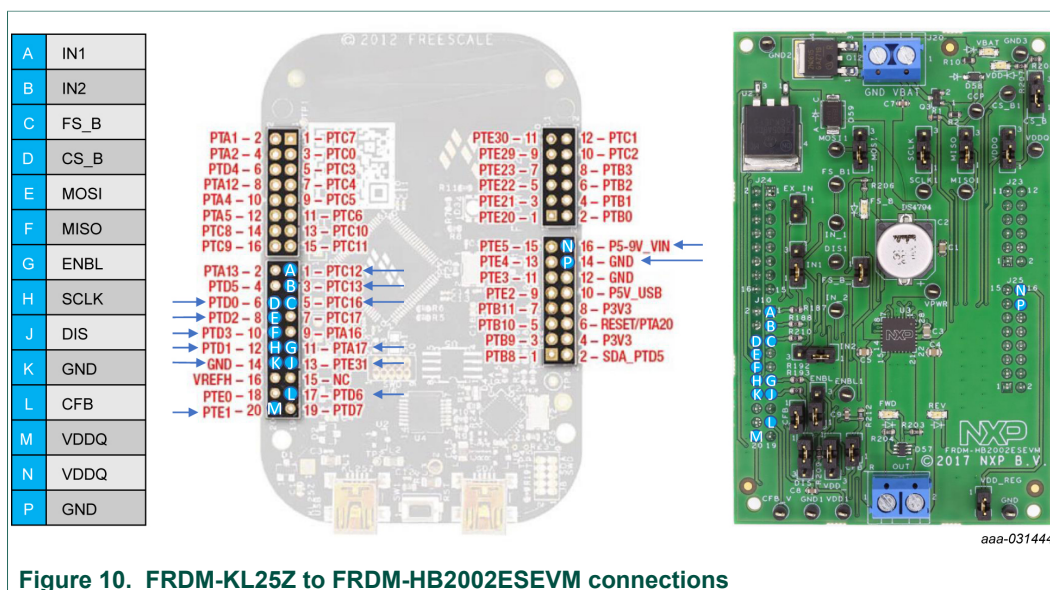


Table 8. FRDM-HB2002ESEVM to FRDM-KL25Z connections

FRDM-KL25Z			FRDM-HB2002ESEVM			MC33HB2002ES		Description
Header	Pin	Name	Header	Pin	Name	Pin	Name	
J1	1	PTC7	J24	1	n.c.	—	n.c.	not connected
J1	2	PTA1	J24	2	n.c.	—	n.c.	not connected
J1	3	PTC0	J24	3	n.c.	—	n.c.	not connected
J1	4	PTA2	J24	4	n.c.	—	n.c.	not connected
J1	5	PTC3	J24	5	n.c.	—	n.c.	not connected
J1	6	PTD4	J24	6	n.c.	—	n.c.	not connected
J1	7	PTC4	J24	7	n.c.	—	n.c.	not connected
J1	8	PTA12	J24	8	n.c.	—	n.c.	not connected
J1	9	PTC5	J24	9	n.c.	—	n.c.	not connected

FRDM-KL25Z			FRDM-HB2002ESEVM			MC33HB2002ES		Description
Header	Pin	Name	Header	Pin	Name	Pin	Name	
J1	10	PTA4	J24	10	n.c.	—	n.c.	not connected
J1	11	PTC6	J24	11	n.c.	—	n.c.	not connected
J1	12	PTA5	J24	12	n.c.	—	n.c.	not connected
J1	13	PTC10	J24	13	n.c.	—	n.c.	not connected
J1	14	PTC8	J24	14	n.c.	—	n.c.	not connected
J1	15	PTC11	J24	15	n.c.	—	n.c.	not connected
J1	16	PTC9	J24	16	n.c.	—	n.c.	not connected
J2	1	PTC12	J10	1	DATA0	9	IN1	IN1 input signal for the H-bridge
J2	2	PTA13	J10	2	n.c.	—	n.c.	not connected
J2	3	PTC13	J10	3	DATA1	8	IN2	IN2 input signal for the H-bridge
J2	4	PTD5	J10	4	n.c.	—	n.c.	not connected
J2	5	PTC16	J10	5	FS_B	15	FS_B	fault status pin (active low) reporting faults
J2	6	PTD0	J10	6	SPI_CS_B	27	CS_B	SPI chip select (active low)
J2	7	PTC17	J10	7	n.c.	—	n.c.	not connected
J2	8	PTD2	J10	8	SPI_MOSI	3	MOSI	SPI master-out, slave-in
J2	9	PTA16	J10	9	n.c.	—	n.c.	not connected
J2	10	PTD3	J10	10	SPI_MISO	1	MISO	SPI master-in, slave-out
J2	11	PTA17	J10	11	CTRL0	6	ENBL	enable signal (active high) to put the part in sleep mode and 3-state the outputs
J2	12	PTD1	J10	12	SPI_SCLK	2	SCLK	SPI clock signal
J2	13	PTE31	J10	13	CTRL1	7	DIS	disable signal (active high) to 3-state the outputs
J2	14	GND	J10	14	GND	4-5, 16-21	GND	ground
J2	15	NC	J10	15	n.c.	—	n.c.	not connected
J2	16	VREFH	J10	16	n.c.	—	n.c.	not connected
J2	17	PTD6	J10	17	CFB_READ	10	CFB	Current feedback output to ADC, sense network on-board
J2	18	PTE0	J10	18	n.c.	—	n.c.	not connected
J2	19	PTD7	J10	19	n.c.	—	n.c.	not connected
J2	20	PTE1	J10	20	FRDM_VDD	28	VDDQ	3.3 V logic supply available from KL25Z, routable to VDDQ
J10	1	PTE20	J23	1	n.c.	—	n.c.	not connected
J10	2	PTB0	J23	2	n.c.	—	n.c.	not connected
J10	3	PTE21	J23	3	n.c.	—	n.c.	not connected
J10	4	PTB1	J23	4	n.c.	—	n.c.	not connected
J10	5	PTE22	J23	5	n.c.	—	n.c.	not connected
J10	6	PTB2	J23	6	n.c.	—	n.c.	not connected
J10	7	PTE23	J23	7	n.c.	—	n.c.	not connected
J10	8	PTB3	J23	8	n.c.	—	n.c.	not connected
J10	9	PTE29	J23	9	n.c.	—	n.c.	not connected
J10	10	PTC2	J23	10	n.c.	—	n.c.	not connected
J10	11	PTE30	J23	11	n.c.	—	n.c.	not connected
J10	12	PTC1	J23	12	n.c.	—	n.c.	not connected
J9	1	PTB8	J25	1	n.c.	—	n.c.	not connected
J9	2	SDA_PTD5	J25	2	n.c.	—	n.c.	not connected
J9	3	PTB9	J25	3	n.c.	—	n.c.	not connected
J9	4	P3V3	J25	4	n.c.	—	n.c.	not connected
J9	5	PTB10	J25	5	n.c.	—	n.c.	not connected
J9	6	RESET/PTA20	J25	6	n.c.	—	n.c.	not connected
J9	7	PTB11	J25	7	n.c.	—	n.c.	not connected
J9	8	P3V3	J25	8	n.c.	—	n.c.	not connected
J9	9	PTE2	J25	9	n.c.	—	n.c.	not connected

FRDM-KL25Z			FRDM-HB2002ESEVM			MC33HB2002ES		Description
Header	Pin	Name	Header	Pin	Name	Pin	Name	
J9	10	P5V_USB	J25	10	n.c.	—	n.c.	not connected
J9	11	PTE3	J25	11	n.c.	—	n.c.	not connected
J9	12	GND	J25	12	n.c.	—	n.c.	not connected
J9	13	PTE4	J25	13	n.c.	—	n.c.	not connected
J9	14	GND	J25	14	GND	4-5, 16-21	GND	ground
J9	15	PTE5	J25	15	n.c.	—	n.c.	not connected
J9	16	P5-9V_VIN	J25	16	VDD_REG	28	VDDQ	5.0 V logic supply from on-board regulator, routable to VDDQ

5 Configuring the hardware

The FRDM-HB2002ESEVM consists of an H-bridge, a parallel and SPI interface, power conditioning circuitry and a FRDM-KL25Z board. The board can be configured for use with a FRDM-KL25Z board or a function generator.

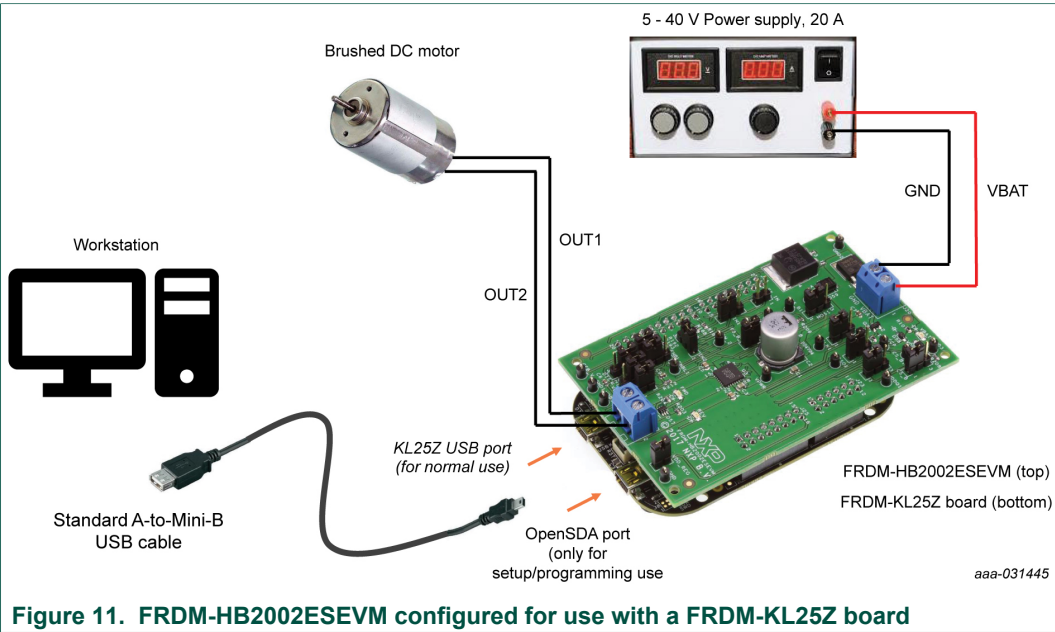


Caution

When using the FRDM-HB2002ESEVM, make sure that the maximum motor supply voltage (VPWR) stays within the 5.0 V to 40 V range. Operating outside this range may cause damage to the board.

5.1 Configuring the hardware for use with a FRDM-KL25Z

Figure 11 illustrates the typical hardware configuration using a FRDM-KL25Z.



- To configure the FRDM-HB2002ESEVM for use with the FRDM-KL25Z do the following:
1. Connect the FRDM-HB2002ESEVM to the FRDM-KL25Z using the Arduino connectors on each board.
 2. Connect the USB cable (not supplied with the kit) between the PC and the KL25Z USB port on the FRDM-KL25Z board.

3. With the power switched off, attach the DC power supply to the VBAT and GND screw connector terminal (J20) on the evaluation board.
4. Connect the load to the screw terminal (J21).

5.2 Configuring the hardware for use with a function generator

Figure 12 illustrates the typical hardware configuration using a function generator.

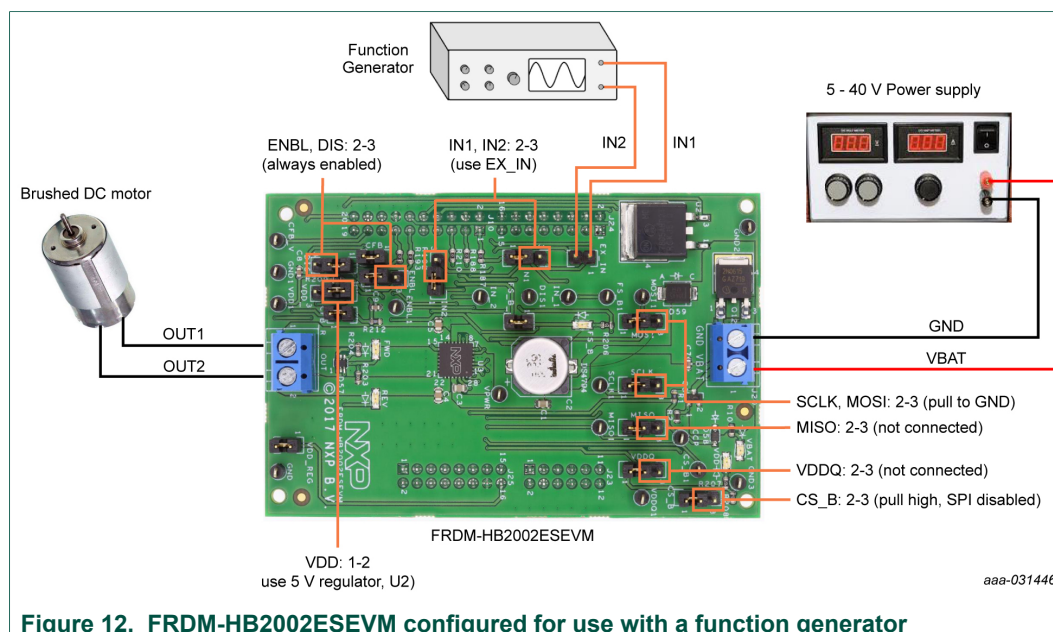


Figure 12. FRDM-HB2002ESEVM configured for use with a function generator

This section describes how to configure the FRDM-HB2002ESEVM for use with a function generator. The same connections apply if the board is connected to a microcontroller instead of a function generator. To configure the board for use in a specific environment, see [Section 3.2](#), [Section 3.4](#), and the MC33HB2002 data sheet.

1. Connect the function generator to the EX_IN jumper, with one channel attached to each pin.
2. Change the board jumper connections, as shown in [Figure 12](#).
3. With the power switched off, attach the DC power supply to the VBAT and GND screw connector terminal (J20) on the evaluation board.
4. Connect the load to the screw terminal (J21).

6 Installing and configuring software and tools

6.1 Configuring the FRDM-KL25Z microcode

By default, the FRDM-KL25Z with this kit has the required firmware to interface with the FRDM-HB2002ESEVB. In the event of a loss of functionality following a reset, reprogramming, or corrupted data issue, the microcode may be rewritten per the following steps:

1. To clear the memory and place the board in bootloader mode, hold down the reset button while plugging a USB cable into the **OpenSDA** USB port.
2. Verify the board appears as a "BOOTLOADER" device and continue to step 3. If the board appears as "KL25Z," you may skip to step 6.

3. Download the **Firmware Apps** .zip archive from the PEmicro OpenSDA web page (<http://www.pemicro.com/opensda/>). Validate your email address to access the files.
4. Find the most recent MDS-DEBUG-FRDM-KL25Z_Pemicro_v***.SDA and copy/drag-and-drop into the **BOOTLOADER** device.
5. Reboot the board by unplugging and re-plugging the connection to the **OpenSDA** port. Verify now the device appears as a “KL25Z” device to continue.
6. Download the product-specific firmware “UsbSPIDongleKL25Z_HB2000_HB2001_v512.srec” for HB2002 from the following link: <http://www.nxp.com/Usb-Spi-Dongle-firmware-KL25Z-HB2000-1>
 - a. The .srec file is a product/family-specific configuration file for FRDM-KL25Z containing the pin definitions, SPI/PWM generation code, and pin mapping assignments necessary to interface with the FRDM-HB2002ESEVB.
7. With the KL25Z still plugged through the **OpenSDA** port, copy/drag-and-drop the .srec file into the KL25Z device memory. Once done, disconnect the USB and plug into the other USB port, labeled **KL25Z**.
 - a. The device may not appear as a distinct device to the computer while connected through the KL25Z USB port, this is normal.
8. The FRDM-KL25Z board is now fully set up to work with FRDM-HB2002ESEVB and the SPIGen GUI.
 - a. There is also no firmware stored on the FRDM-HB2002ESEVB board itself, only on the MCU FRDM-KL25Z.

All uploaded firmware is stored in non-volatile memory until the reset button is hit on the FRDM-KL25Z. There is no need to repeat this process upon every power up, and there is no loss of data associated with a single unplug event.

6.2 Installing SPIGen on your computer

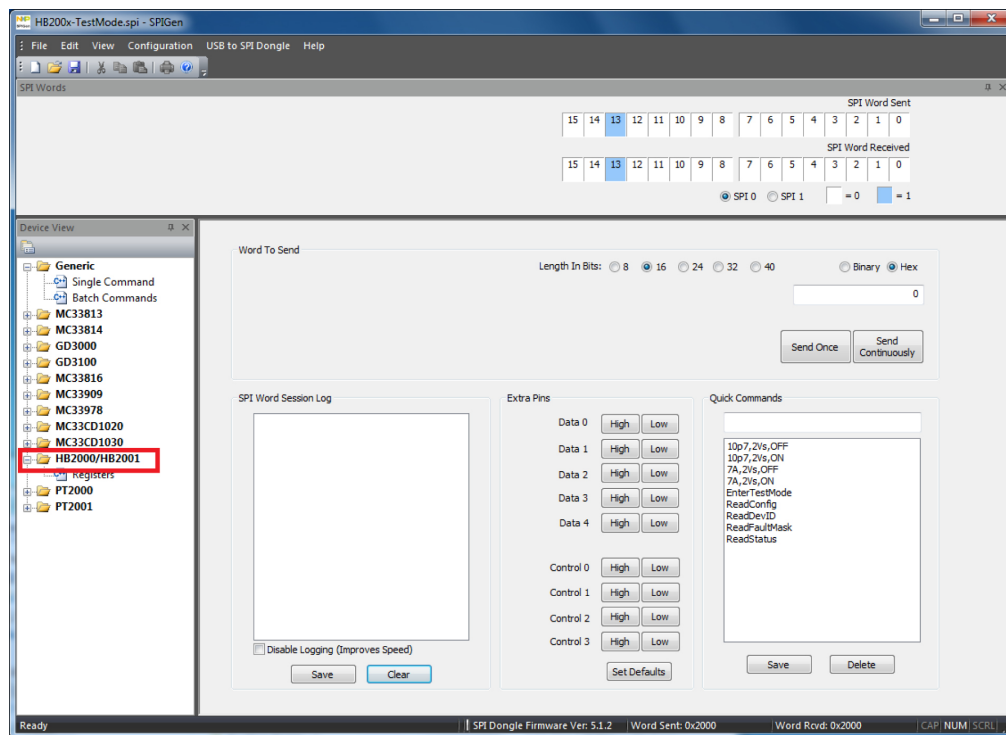
The latest version of SPIGen supports the MC33HB2002 and is designed to run on any Windows 10, Windows 8, or Windows 7-based operating system. To install the software, do the following:

1. Go to www.nxp.com/SPIGen and click **Download**.
2. When the SPIGEN: SPI Generator (SPIGen) software page appears, go to the **Lab and Test Software** section and click **Download** associated with the description of the selected environment. A wizard guides the user through the process.
3. If instructed for the SPIGen wizard to create a shortcut, a SPIGen icon appears on the desktop. By default, the SPIGen executable file is installed at **C:\Program Files (x86)\SPIGen**.

Installing the device drivers overwrites any previous SPIGen installation and replaces it with a current version containing the MC33HB2002 drivers. However, configuration files (.spi) from the previous version remain intact.

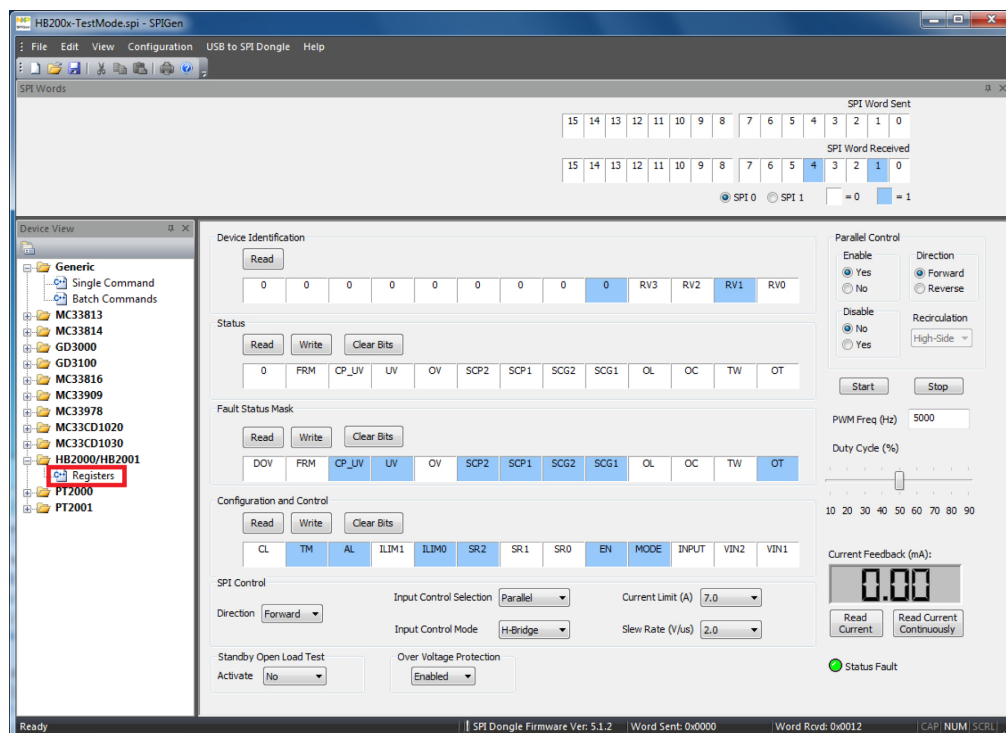
6.3 Using SPIGen graphical user interface

1. Launch SPIGen. The HB2000/HB2001 device appears in the **Device View** panel.



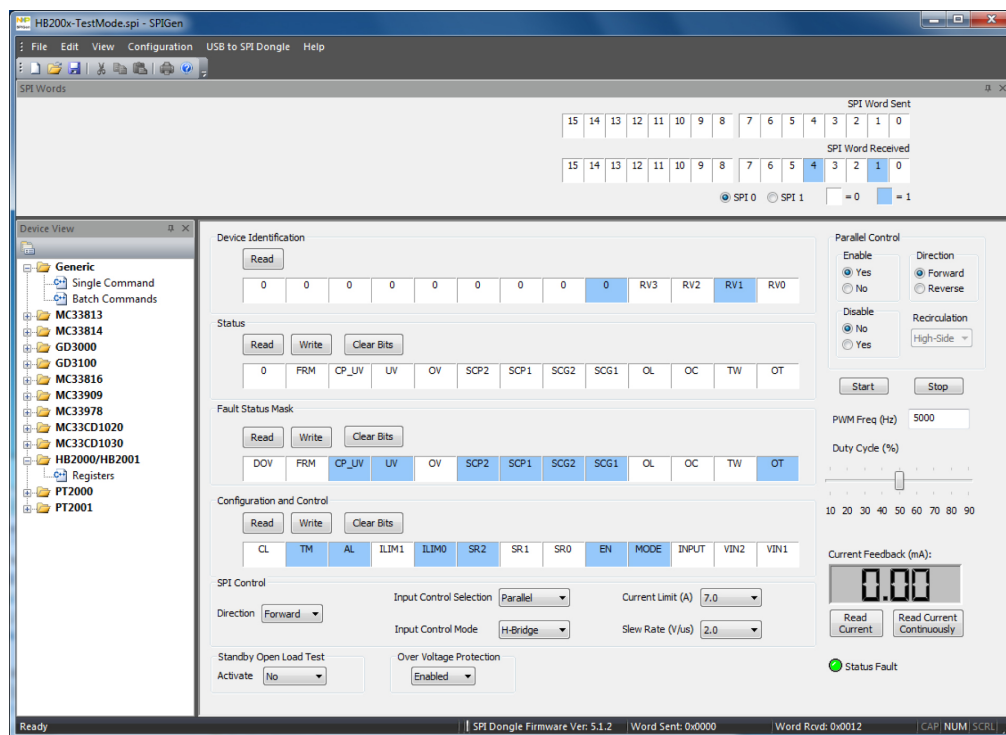
aaa-031439

- To access the HB2000/HB2001 tab in the SPIGen window, expand the HB2000/HB2001 folder in the Device View. Then click **Registers** icon.



aaa-031440

3. Reading all the SPI registers displays the following default status. At this point the system is ready to drive a motor and/or report application faults.



aaa-031441

6.3.1 SPI control

Device Identification

Read

0 0 0 0 0 0 0 0 0 RV3 RV2 RV1 RV0

Status

Read Write Clear Bits

0 FRM CP_UV UV OV SCP2 SCP1 SCG2 SCG1 OL OC TW OT

Fault Status Mask

Read Write Clear Bits

DOV FRM CP_UV UV OV SCP2 SCP1 SCG2 SCG1 OL OC TW OT

Configuration and Control

Read Write Clear Bits

CL TM AL ILIM1 ILIM0 SR2 SR1 SR0 EN MODE INPUT VIN2 VIN1

SPI Control

Direction Forward

Input Control Selection Parallel

Current Limit (A) 7.0

Input Control Mode H-Bridge

Slew Rate (V/us) 2.0

Standby Open Load Test Activate No

Over Voltage Protection Enabled

aaa-031442

Figure 13. SPI control description

Read	To read the content of each register, click the read button on top of each register.
Write	Click individual bits of any register and then press the corresponding write button to write into the register.
Clear Bits	Clears GUI readout only of register bits. To clear or reset register values to default, write back the existing data to the register.
Direction	Select output direction through the use of SPI control bits VIN1 and VIN2. • Forward (default) is defined as $VOUT1 > VOUT2$ • Reverse is defined as $VOUT2 > VOUT1$ This selection, and VIN1 and VIN2 bits, are ignored when operating in parallel mode.
Input Control Selection	Select device input control method with INPUT bit. Write the device configuration register upon edit. • Parallel sets INPUT = 0, using I/O pins (IN1, IN2) for device control • SPI sets INPUT = 1, using SPI bits (VIN1, VIN2) for device control

Input Control Mode	Select mode of operation (full-bridge or half-bridge) with MODE bit. Write the device configuration register upon edit to correctly interpret input signals. • H-Bridge (default) operates the device in full-bridge mode • Half-Bridge operates the device in half-bridge mode This dropdown selection affects the PWM waveforms generated by the microcontroller.
Current Limit (A)	Select from four current limit options using the ILIM0 and ILIM1 bits. Write the device configuration register upon edit.
Slew Rate (V/μs)	Select from eight slew rate settings using the SR0, SR1, and SR2 bits. Write the device configuration register upon edit.
Standby Open Load Test	Enable openload test in Standby mode, using CL bit. Write the device configuration register upon edit. • No (default) sets CL = 0 and disables the test • Yes sets CL = 1 and executes openload test on next Standby state Openload standby test is available in full-bridge mode only.
Over Voltage Protection	Configure response to overvoltage condition using DOV bit. Write the fault status mask register upon edit. • Enabled (default) sets DOV = 0; during overvoltage, the OV warning bit is set and the outputs are in high-side recirculation to protect the system. • Disabled sets DOV = 1; during overvoltage only the OV warning bit is set. Overvoltage protection is available in full-bridge mode only.

Additional functionality is available by setting configuration and status registers over SPI. For a full description of this functionality, see MC33HB2002 data sheet.

6.3.2 Parallel control

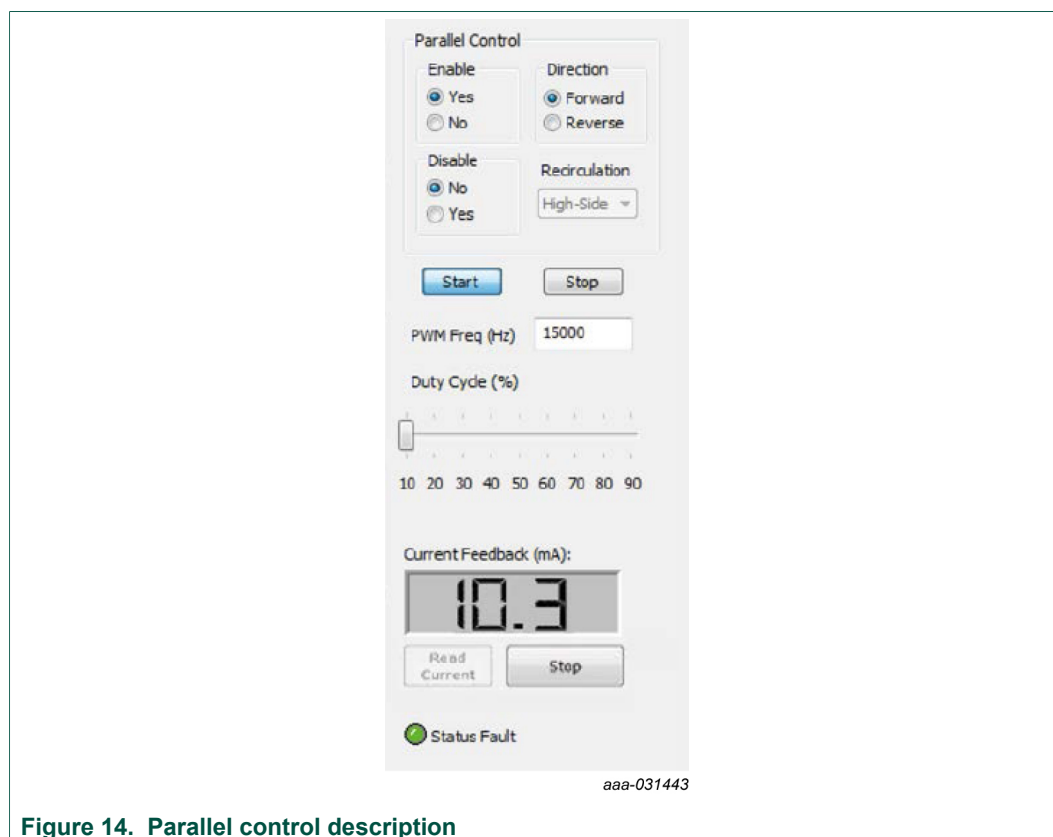


Figure 14. Parallel control description

Direction	• Forward: Current flowing through OUT1 to OUT2 • Reverse: Current flowing through OUT2 to OUT1
Recirculation	• High-side: Freewheel-High (both high-side FETs turned on) during PWMing • Low-side: Freewheel-Low (both low-side FETs turned on) during PWMing (only available for Half-bridge mode)
Enable (ENBL pin)	• Yes: ENBL is logic HIGH, the H-bridge is operational • No: ENBL is logic LOW, the H-bridge outputs are 3-stated and placed in Sleep mode
Disable (DIS pin)	• Yes: DIS is logic HIGH, both OUT1 and OUT2 are 3-stated • No: DIS is logic LOW, both OUT1 and OUT2 are enabled
PWM Freq (Hz)	Enter PWM frequency up to 20000 Hz
Duty Cycle (%)	Select PWM duty cycle from 10 % to 90 %
Start	After selection of parallel control configuration, press Start to activate the outputs
Stop	Press Stop to deactivate the outputs
Current Feedback (mA)	Shows current through the high-side FETs using the current recopy feature exercised over the on-board sense network, then interpreted by the KL25Z microcontrollers ADC
Status Fault	• Reports system fault status in real time, per mask register (all masked AND detected faults are OR-ed together) • Status fault also goes low in response to DIS high or open

Table 9. Logic behind direction control with high-side versus low-side recirculation

Direction	Recirculation	Input signal (INx) generated
Half-bridge mode (MODE = 0)		
Forward	high-side recirculation	IN1 = 1
		IN2 = PWM signal with selected duty cycle and frequency
Reverse	high-side recirculation	IN1 = PWM signal with selected duty cycle and frequency
		IN2 = 1
Forward	low-side recirculation	IN1 = PWM signal with selected duty cycle and frequency
		IN2 = 0
Reverse	low-side recirculation	IN1 = 0
		IN2 = PWM signal with selected duty cycle and frequency
Full H-bridge mode (MODE = 1)		
Forward	high-side recirculation	IN1 = 1
		IN2 = PWM signal with selected duty cycle and frequency
Reverse	high-side recirculation	IN1 = 0
		IN2 = PWM signal with selected duty cycle and frequency

7 References

- [1] **FRDM-HB2002ESEVM** — detailed information on this board, including documentation, downloads, and software and tools
<http://www.nxp.com/FRDM-HB2002ESEVM>
- [2] **H-bridge motor driver** — product information on H-bridge motor driver, MC33HB2002
<http://www.nxp.com/MC33HB2002>
- [3] **FRDM-KL25Z** — Freedom Development Platform for Kinetis® KL14, KL15, KL24, KL25 MCUs
<http://www.nxp.com/FRDM-KL25Z>
- [4] **SPIGen** — SPI generator software
<http://www.nxp.com/SPIGEN>

8 Revision history

Revision history

Rev	Date	Description
v.1	20180913	Initial version

9 Important notice

NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

Should this evaluation kit not meet the specifications indicated in the kit, it may be returned within 30 days from the date of delivery and will be replaced by a new kit.

NXP reserves the right to make changes without further notice to any products herein. NXP makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Typical parameters can and do vary in different applications and actual performance may vary over time. All operating parameters, including Typical, must be validated for each customer application by customer's technical experts.

NXP does not convey any license under its patent rights nor the rights of others. NXP products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the NXP product could create a situation where personal injury or death may occur.

Should the Buyer purchase or use NXP products for any such unintended or unauthorized application, the Buyer shall indemnify and hold NXP and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges NXP was negligent regarding the design or manufacture of the part.

10 Legal information

10.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

10.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive

applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out of the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US\$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Safety of high-voltage evaluation products — The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire. This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel that is qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. The product does not comply with IEC 60950 based national or regional safety standards. NXP Semiconductors does not accept any liability for damages incurred due to inappropriate use of this product or related to non-insulated high voltages. Any use of this product is at customer's own risk and liability. The customer shall fully indemnify and hold harmless NXP Semiconductors from any liability, damages and claims resulting from the use of the product.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

10.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Tables

Tab. 1.	FRDM-HB2002ESEVM board component descriptions	5	Tab. 6.	FRDM-HB2002ESEVM test point descriptions	11
Tab. 2.	FRDM-HB2002ESEVM indicator descriptions	8	Tab. 7.	Screw terminal connections	13
Tab. 3.	Jumper descriptions	9	Tab. 8.	FRDM-HB2002ESEVM to FRDM-KL25Z connections	13
Tab. 4.	Input signal definitions	10	Tab. 9.	Logic behind direction control with high-side versus low-side recirculation	23
Tab. 5.	Output signal definitions	11			

Figures

Fig. 1.	FRDM-HB2002ESEVM block diagram	4	Fig. 9.	FRDM-HB2002ESEVM screw terminal locations	12
Fig. 2.	FRDM-HB2002ESEVM featured component locations	5	Fig. 10.	FRDM-KL25Z to FRDM-HB2002ESEVM connections	13
Fig. 3.	Modes of operation	7	Fig. 11.	FRDM-HB2002ESEVM configured for use with a FRDM-KL25Z board	15
Fig. 4.	Architecture	7	Fig. 12.	FRDM-HB2002ESEVM configured for use with a function generator	16
Fig. 5.	Thermal management	8	Fig. 13.	SPI control description	20
Fig. 6.	FRDM-HB2002ESEVM indicator locations	8	Fig. 14.	Parallel control description	22
Fig. 7.	FRDM-HB2002ESEVM jumper locations	9			
Fig. 8.	FRDM-HB2002ESEVM test points	11			

Contents

1	Finding kit resources and information on the NXP web site	2
1.1	Collaborate in the NXP community	2
2	Getting ready	2
2.1	Kit contents	2
2.2	Additional hardware	2
2.3	Windows PC workstation	2
2.4	Software	3
3	Getting to know the hardware	3
3.1	Kit overview	3
3.1.1	FRDM-HB2002ESEVM features	3
3.1.2	FRDM-HB2002ESEVM block diagram	4
3.1.3	Schematic, board layout and bill of materials	4
3.2	Featured components	4
3.2.1	MC33HB2002: 10 A H-bridge, SPI programmable brushed DC motor driver	5
3.2.1.1	General description	5
3.2.1.2	Features	6
3.2.1.3	Modes of operation	7
3.2.1.4	Architecture	7
3.2.1.5	Thermal management	8
3.3	Indicators	8
3.4	Jumpers	9
3.5	Input signal definitions	10
3.6	Output signal definitions	11
3.7	Test points	11
3.8	Screw terminal connections	12
4	FRDM-HB2002ESEVM to FRDM-KL25Z connection information	13
5	Configuring the hardware	15
5.1	Configuring the hardware for use with a FRDM-KL25Z	15
5.2	Configuring the hardware for use with a function generator	16
6	Installing and configuring software and tools	16
6.1	Configuring the FRDM-KL25Z microcode	16
6.2	Installing SPIGen on your computer	17
6.3	Using SPIGen graphical user interface	17
6.3.1	SPI control	20
6.3.2	Parallel control	22
7	References	24
8	Revision history	24
9	Important notice	24
10	Legal information	25

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2018.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 13 September 2018
Document identifier: UM11144